MAXIM

1998 NEW RELEASES DATA BOOK

Volume VII

Featuring

- *Product Selection Tables and Trees*
- *Data Sheets*
- *Free Sample Request Cards*

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- *1994 to 1997 New Releases Data Books*
- *Notebook Computer Applications Data Book*
- *High-Frequency ASIC Development Handbook*
- *Full-Line Data Catalog on CD-ROM*

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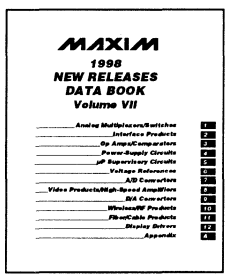
HOW TO USE THE 1998 NEW RELEASES DATA BOOK

Maxim's 1998 *New Releases Data Book* (Vol. VII) brings together over 350 new devices from 13 product families in a single, easy-to-use "Design Guide" format. Each section contains: (1) data sheets for all new products in that family of parts, (2) product-family selection tables and trees.

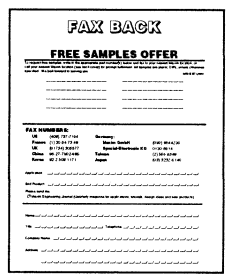
If you need samples for further evaluation, simply fill out one of the sample request cards and fax it to the nearest Maxim office, or call the nearest Maxim office (see back cover) for prompt fulfillment.

We've provided a variety of reference guides to help you locate a specific product or product family:

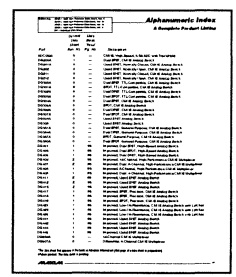
1	Analog Multiplexers/Switches
2	Interface Products
3	Op Amps/Comparators
4	Power-Supply Circuits
5	µP Supervisory Circuits
6	Voltage References
7	A/D Converters
8	Video Products/ High-Speed Amplifiers
9	D/A Converters
10	Wireless/RF Products
11	Fiber/Cable Products
12	Display Drivers



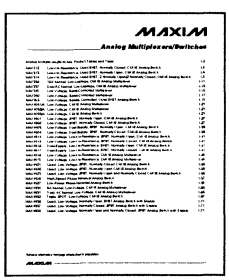
PRODUCT-FAMILY SECTIONS, INDICATED BY TAB NUMBER



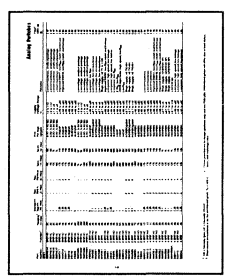
FREE SAMPLE REQUEST CARDS



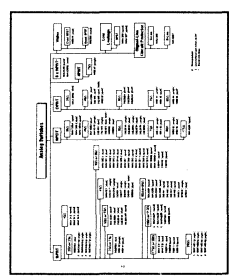
COMPLETE ALPHANUMERIC INDEX OF PART NUMBERS, CROSS REFERENCED TO OTHER MAXIM DATA BOOKS



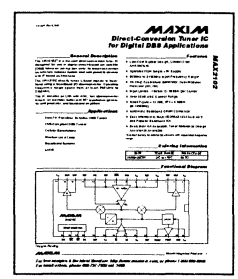
SECTION TABLES OF CONTENTS, SORTED BY PRODUCT FAMILY



PRODUCT-FAMILY SELECTION TABLES WITH SPECIFICATIONS, FEATURES, AND PRICING



PRODUCT-FAMILY SELECTION TREES



DATA SHEETS

VISIT MAXIM'S SITE ON THE WORLD WIDE WEB: http://www.maxim-ic.com

MAXIM

1998 NEW RELEASES DATA BOOK Volume VII

Analog Multiplexers/Switches 1
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Introduction

Maxim Integrated Products designs, develops, manufactures, and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify, and convert real-world signals—such as temperature, pressure, or sound—into digital signals a computer can process. Over the past 14 years, Maxim has introduced over 1300 analog ICs—more than any other company in our industry.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. Our product lines include the following: microprocessor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-management products, timers and counters, display circuits, multiplexers, switches, voltage detectors, fiber optic transceivers, wireless products, and analog filters.

Recognizing the growing demand for BiCMOS technology, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, and are available in several different packages and temperature ranges to meet varying customer requirements.

World Wide Web

Visit our WWW site at http://www.maxim-ic.com to access our latest data sheets and free samples. Data sheets can be downloaded instantaneously, and samples that are in stock will be shipped within 24 hours.

Customer Service

If you don't have access to the WWW, call or fax your nearest Maxim location for free samples and literature. Evaluation kits or a small quantity of parts can be ordered using VISA or MasterCard by calling U.S. Headquarters at (800) 998-8800 extension 3468 (U.S. only) or (408) 737-7600 extension 3468. Outside the U.S., call your nearest Maxim location.

Customer service representatives are available during normal business hours to provide information on orders placed directly with the factory. Please see the back cover for a list of domestic and international distributors.

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Maxim has a large, highly qualified group of senior applications engineers available to provide full technical support. Simply call U.S. headquarters at (408) 737-7600 extension 4000 between 8:00 a.m. and 5:00 p.m. Pacific Standard Time, or fax your questions to (408) 732-8159.

Maxim also offers a wide variety of technical publications, including the *Product Selector Guide*, a *Full-Line Data Catalog* on CD-ROM, the *Engineering Journal* (a quarterly magazine explaining the application of our new products), a *Notebook Computer Applications Data Book*, Design Guides for each product family, and the *High-Frequency ASIC Development Handbook*. Call your nearest Maxim location for any literature you may need.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve your design problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

ISO 9001/9002 Certification

In November 1993, the wafer fab at Maxim's Sunnyvale headquarters received formal ISO 9001 certification, validating that our quality system meets the worldwide standard. The wafer fab at our Beaverton, Oregon facility was also 9001 certified, as of July 1994. ISO 9001 is the most stringent of the 9000 series of specifications, because it includes review of design, test, manufacturing, and shipment processes.

In May 1995, ISO 9002 certification was granted to Maxim UK.

Information furnished by Maxim Integrated Products is believed to be accurate and reliable. However, the company cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product; nor for any infringements of patents or other rights of third parties that may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Maxim Integrated Products. Maxim reserves the right to change the circuitry and specifications without notice.

Life Support Policy: Maxim does not authorize any Maxim product for use in life support devices and/or systems without the express written approval of an officer of Maxim Integrated Products, Inc. Life support devices or systems are devices or systems which, (i) are intended for surgical implant into the body or (ii) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

Products in this book may be covered by one or more of the patents listed below. Additional patents are pending.

4,217,599, 4,228,447, 4,229,756, 4,260,425, 4,261,761, 4,435,655, 4,622,736, 4,628,406, 4,636,930, 4,679,134, 4,700,286, 4,701,694, 4,714,872, 4,732,865, 4,733,218, 4,752,700, 4,767,946, 4,769,619, 4,774,478, 4,774,497, 4,777,577, 4,777,580, 4,786,856, 4,797,569, 4,797,899, 4,801,888, 4,806,875, 4,809,152, 4,812,891, 4,819,049, 4,819,147, 4,823,028, 4,847,522, 4,857,778, 4,859,963, 4,862,096, 4,866,314, 4,876,214, 4,897,774, 4,902,640, 4,994,400, 4,994,694, 4,999,761, 5,017,814, 5,027,165, 5,055,796, 5,142,242, 5,151,775, 5,209,117, 5,247,468, 5,268,315, 5,414,314, 5,446,414, 5,498,984, 5,508,650, 5,528,132, 5,532,577, 5,539,603, 5,552,741, 5,563,549, 5,565,715, 5,574,403, 5,594,381, 5,617,051, 5,619,163, 5,629,612, 5,649,210.

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Alphanumeric Index

A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
ADC0820	1	—	CMOS, High-Speed, 8-Bit ADC with Track/Hold
DG200A	1	—	Dual SPST, CMOS Analog Switch
DG201A	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
DG202	0	—	Quad SPST, Normally Open, CMOS Analog Switch
DG211	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
DG212	0	—	Quad SPST, Normally Open, CMOS Analog Switch
DG300A	0	—	Dual SPST, TTL-Compatible, CMOS Analog Switch
DG301A	0	—	SPDT, TTL-Compatible, CMOS Analog Switch
DG302A	0	—	Dual DPST, TTL-Compatible, CMOS Analog Switch
DG303A	0	—	Dual SPDT, TTL-Compatible, CMOS Analog Switch
DG304A	0	—	Dual SPST, CMOS Analog Switch
DG305A	0	—	SPDT, CMOS Analog Switch
DG306A	0	—	Dual DPST, CMOS Analog Switch
DG307A	0	—	Dual SPDT, CMOS Analog Switch
DG308A	0	—	Quad SPST Analog Switch
DG309	0	—	Quad SPST Analog Switch
DG381A	0	—	Dual SPST, General-Purpose, CMOS Analog Switch
DG384A	0	—	Dual DPST, General-Purpose, CMOS Analog Switch
DG387A	0	—	SPDT, General-Purpose, CMOS Analog Switch
DG390A	0	—	Dual SPDT, General-Purpose, CMOS Analog Switch
DG401	1	95	Improved, Dual SPST, High-Speed Analog Switch
DG403	1	95	Improved, Dual SPDT, High-Speed Analog Switch
DG405	1	95	Improved, Dual DPST, High-Speed Analog Switch
DG406	2	95	Improved, 16-Channel, High-Performance CMOS Multiplexer
DG407	2	95	Improved, Dual, 8-Channel, High-Performance CMOS Multiplexer
DG408	1	93	Improved, 8-Channel, High-Performance CMOS Multiplexer
DG409	1	93	Improved, Dual, 4-Channel, High-Performance CMOS Multiplexer
DG411	2	95	Improved, Quad SPST Analog Switch
DG412	2	95	Improved, Quad SPST Analog Switch
DG413	2	95	Improved, Quad SPST Analog Switch
DG417	2	95	Improved, SPST, Precision, CMOS Analog Switch
DG418	2	95	Improved, SPST, Precision, CMOS Analog Switch
DG419	2	95	Improved, SPDT, Precision, CMOS Analog Switch
DG421	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG423	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG425	1	95	Improved, Low-On-Resistance, CMOS Analog Switch with Latches
DG441	2	95	Improved, Quad SPST Analog Switch
DG442	2	95	Improved, Quad SPST Analog Switch
DG444	1	95	Improved, Quad SPST Analog Switch
DG445	1	95	Improved, Quad SPST Analog Switch
DG506A	0	—	16-Channel CMOS Multiplexer
DG507A	0	—	Differential, 8-Channel CMOS Multiplexer

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year/98 Book Page No.	Description
DG508A	2	—	8-Channel CMOS Multiplexer
DG509A	2	—	Differential, 4-Channel CMOS Multiplexer
DG528	0	—	8-Channel, Latchable Multiplexer
DG529	0	—	Differential, 4-Channel, Latchable Multiplexer
HI-201	0	—	Quad SPST, CMOS Analog Switch
HI-201HS	1	—	High-Speed, Quad SPST, CMOS Analog Switch
HI-508A	0	92	Fault-Protected, 8-Channel Multiplexer
HI-509A	0	92	Fault-Protected, Differential 4-Channel Multiplexer
ICL7106	0	—	3 1/2-Digit ADC with LCD Drivers
ICL7107	0	—	3 1/2-Digit ADC with LED Drivers
ICL7109	0	—	12-Bit ADC with Three-State Binary Outputs
ICL7116	0	—	3 1/2-Digit ADC with LCD Drivers and Display Hold
ICL7117	0	—	3 1/2-Digit ADC with LED Drivers and Display Hold
ICL7126	0	—	Low-Power, 3 1/2-Digit ADC with LCD Drivers
ICL7129A	0	—	Low-Noise, 4 1/2-Digit, Single-Chip ADC with Multiplexed LCD Drivers
ICL7135	0	—	4 1/2-Digit ADC with Multiplexed BCD Outputs
ICL7136	1	—	Low-Power, 3 1/2-Digit ADC with LCD Drivers
ICL7137	0	—	Low-Power, 3 1/2-Digit ADC with LED Drivers
ICL7611	0	—	Low-Power, Industry-Standard Op Amp
ICL7612	0	—	Low-Power, Industry-Standard Op Amp
ICL7614	0	—	Low-Power, Industry-Standard Op Amp
ICL7616	0	—	Low-Power Op Amp
ICL7621	0	—	Dual, Low-Power, Industry-Standard Op Amp
ICL7622	0	—	Dual, Low-Power, Industry-Standard Op Amp
ICL7631	0	—	Triple, Low-Power, Industry-Standard Op Amp
ICL7632	0	—	Triple, Low-Power, Industry-Standard Op Amp
ICL7641	0	—	Quad, Low-Power, Industry-Standard Op Amp
ICL7642	0	—	Quad, Low-Power, Industry-Standard Op Amp
ICL7650/B	1	—	Chopper-Stabilized Op Amp
ICL7652/B	0	—	Chopper-Stabilized Op Amp
ICL7660	1	93	10mA Charge-Pump Voltage Converter
ICL7662	1	—	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
ICL7663A	1	—	Low-Power, Adjustable-Output, Positive-Voltage Linear Regulator
ICL7664	2	—	Low-Power, Adjustable-Output, Negative-Voltage Linear Regulator
ICL7665	2	—	µP Voltage Monitor with Dual Over/Undervoltage Detection
ICL7667	0	—	Dual-Power MOSFET Driver (Inverting)
ICL8069	0	—	1.2V Voltage Reference
ICM7211	1	—	4-Digit, LCD Decoder/Driver
ICM7212	1	—	4-Digit, LED Decoder/Driver
ICM7217	0	—	4-Digit, Presettable, LED Up/Down Counter
ICM7218	0	—	8-Digit, Multiplexed, LED Decoder/Driver
ICM7224	0	—	4 1/2-Digit, LCD, High-Speed Counter/Decoder/Driver

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
ICM7225	0	—	4 1/2-Digit, LED, High-Speed Counter/Decoder/Driver
ICM7228	0	—	8-Digit, LED Display Driver
ICM7240	0	—	8-Bit Binary, Programmable, RC Timer/Counter
ICM7242	0	—	7-Bit Binary, Fixed, RC Timer/Counter
ICM7250	0	—	Two-Digit BCD, Programmable, RC Timer/Counter
ICM7260	0	—	Module-60, Programmable, RC Timer/Counter
ICM7555	2	—	Low-Power, General-Purpose Timer
ICM7556	2	—	Low-Power, General-Purpose Dual Timer
IH5040	1	—	SPST, Normally Open, CMOS Analog Switch
IH5041	1	—	Dual SPST, Normally Open, CMOS Analog Switch
IH5042	1	—	SPDT, CMOS Analog Switch
IH5043	1	—	Dual SPDT, CMOS Analog Switch
IH5044	1	—	DPST, Normally Open, CMOS Analog Switch
IH5045	1	—	Dual DPST, Normally Open, CMOS Analog Switch
IH5047	1	—	4PST, Normally Open, CMOS Analog Switch
IH5048	1	—	Dual SPST, 75Ω Analog Switch
IH5048A	1	—	Dual SPST, Low-On-Resistance, 25Ω Analog Switch
IH5049	1	—	Dual DPST, Low-Charge-Injection Analog Switch
IH5050	1	—	SPDT, Low-Charge-Injection Analog Switch
IH5051	1	—	Dual SPDT, Low-Charge-Injection Analog Switch
IH5108	0	92	See MAX358
IH5140	0	—	Low-Power, SPST, Fast, CMOS Analog Switch
IH5141	0	—	Dual SPST, Low-Power, Fast, CMOS Analog Switch
IH5142	0	—	SPDT, Low-Power, Fast, CMOS Analog Switch
IH5143	0	—	Dual SPDT, Low-Power, Fast, CMOS Analog Switch
IH5144	0	—	DPST, Low-Power, Fast, CMOS Analog Switch
IH5145	0	—	Dual DPST, Low-Power, Fast, CMOS Analog Switch
IH5208	0	92	See MAX359
IH5341	1	—	Dual SPST, RF/Video Switch
IH5352	1	—	Quad SPST, RF/Video Switch
IH6108	0	—	See DG508A
IH6116	0	—	See DG506A
IH6208	0	—	See DG509A
IH6216	0	—	See DG507A
MAX038	2	95	High-Frequency Waveform Generator
MAX038EVKIT	2	—	Evaluation Kit for the MAX038
MAX100	0	96	250Msps, 8-Bit ADC with Track/Hold
MAX100EVKIT	0	—	Evaluation Kit for the MAX100
MAX101A	0	96	500Msps, 8-Bit ADC with Track/Hold
MAX101AEVKIT	1	—	Evaluation Kit for the MAX101A
MAX104	—	**7-9***	**1Gsps, 8-Bit ADC with Track/Hold**
MAX104EVKIT	†	—	Evaluation Kit for the MAX104

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX110	3	96	±5V, Low-Cost, 2-Channel, Serial ±14-Bit ADC
MAX110EVKIT	1	—	Evaluation Kit for the MAX110/MAX111
MAX111	3	96	5V, Low-Cost, 2-Channel, Serial ±14-Bit ADC
MAX113	1	97	3V, 8-Bit, 4-Channel, Parallel Interface Low-Power ADC
MAX114	1	97	5V, 8-Bit, 4-Channel, Parallel Interface Low-Power ADC
MAX115	—	**7-11***	**±5V Input, 2x4-Channel, Simultaneous-Sampling 12-Bit DAS**
MAX116	—	**7-11***	**±2.5V Input, 2x4-Channel, Simultaneous-Sampling 12-Bit DAS**
MAX117	1	97	3V, 8-Bit, 8-Channel, Parallel Interface Low-Power ADC
MAX117EVKIT	0	—	Evaluation Kit for MAX117/MAX118
MAX118	1	97	5V, 8-Bit, 8-Channel, Parallel Interface Low-Power ADC
MAX120	0	95	500ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX120EVKIT	0	—	Evaluation Kit for the MAX120/MAX122
MAX121	1	—	308ksps, Sampling, 14-Bit ADC with Track/Hold and Reference
MAX121EVKIT	0	—	Evaluation Kit for the MAX121
MAX122	0	95	333ksps, Sampling, 12-Bit ADC with Track/Hold and Reference
MAX125	—	**7-13***	**2x4 Channel, 14-Bit, Simultaneous-Sampling ADC with ±5V Input Range**
MAX125EVKIT	†	—	Evaluation Kit for the MAX125
MAX126	—	**7-13***	**2x4 Channel, 14-Bit, Simultaneous-Sampling ADC with ±2.5V Input Range**
MAX130	0	—	3 1/2-Digit ADC with Bandgap Reference
MAX131	0	—	3 1/2-Digit ADC with Bandgap Reference
MAX132	2	93	±18-Bit, Low-Power ADC with Serial Interface
MAX132EVKIT	2	—	Evaluation Kit for the MAX132
MAX133	0	—	9V, 3 3/4-Digit DMM Circuit
MAX134	0	—	±5V, 3 3/4-Digit DMM Circuit
MAX134EVBRD	0	—	PC-Based Evaluation System for the MAX133/MAX134
MAX135	0	93	±15-Bit, Low-Power ADC with Parallel Interface
MAX136	0	—	Low-Power, 3 1/2-Digit ADC with Display Hold and LCD Drivers
MAX138	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and LCD Drivers
MAX139	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and LED Drivers
MAX140	2	—	3 1/2-Digit ADC with Reference, Charge-Pump and Low-Current LED Drivers
MAX146	**1**	**7-15**	**2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC with Internal Reference**
MAX146EVKIT	†	—	Evaluation Kit for the MAX146
MAX147	**1**	**7-15**	**2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC**
MAX147EVKIT	1	—	Evaluation Kit for the MAX147
MAX148	**1**	**7-39**	**2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC**
MAX149	**1**	**7-39**	**2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC with Internal Reference**
MAX150	1	—	CMOS, 1.3µs, 8-Bit ADC with Voltage Reference and Track/Hold
MAX151	0	92	300kHz, 10-Bit ADC with Reference and Track/Hold
MAX152	1	—	3V, 8-Bit ADC with 1µA Power-Down

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX152EVKIT	1	—	Evaluation Kit for the MAX152/MAX153
MAX153	1	—	1Msps, µP-Compatible, 8-Bit ADC with 1µA Power-Down
MAX154	3	—	CMOS, High-Speed, 4-Channel, 8-Bit ADC with Reference
MAX155	1	93	High-Speed, 8-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX155EVKIT	0	—	Evaluation Kit for the MAX155
MAX156	1	93	High-Speed, 4-Channel, 8-Bit ADC with Simultaneous Track/Holds and Reference
MAX158	3	—	CMOS, High-Speed, 8-Channel, 8-Bit ADC with Reference
MAX160	0	—	CMOS, µP-Compatible, 4µs, 8-Bit ADC
MAX161	1	—	CMOS, 20µs, 8-Bit, 8-Channel Data-Acquisition System
MAX162	0	92	CMOS, 3µs, 12-Bit ADC with Reference
MAX163	1	92	CMOS, 5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX164	0	92	CMOS, ±5V-Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX165	1	93	5µs, 8-Bit ADC with Track/Hold and Reference
MAX166	1	93	Differential Input, 5µs, 8-Bit ADC with Track/Hold and Reference
MAX167	0	92	CMOS, ±2.5V Input, 100ksps, 12-Bit ADC with Track/Hold and Reference
MAX170	0	—	Serial-Output, 5.6µs, 12-Bit ADC with Reference
MAX172	0	92	CMOS, 10µs, 12-Bit ADC with Reference
MAX173	0	—	CMOS, 5µs, 10-Bit ADC with Reference
MAX174	2	—	Industry-Standard, 12-Bit ADC with Reference
MAX176	1	94	250ksps, Serial, 12-Bit ADC with Track/Hold and Reference
MAX176EVKIT	1	—	Evaluation Kit for the MAX176
MAX177	0	—	CMOS, 12-Bit ADC with Track/Hold and Reference
MAX178	0	92	Calibrated, 12-Bit ADC with Track/Hold and Reference
MAX180	0	92	Complete, 100ksps, 8-Channel, 12-Bit Data-Acquisition System
MAX180EVKIT	0	—	Evaluation Kit for the MAX180/MAX181
MAX181	0	92	Complete, 100ksps, 6-Channel, 12-Bit Data-Acquisition System
MAX182	0	92	Calibrated, 4-Channel, 12-Bit ADC with Track/Hold and Reference
MAX183	0	92	3µs, 12-Bit ADC
MAX184	0	92	5µs, 12-Bit ADC
MAX185	0	92	10µs, 12-Bit ADC
MAX186	4	—	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold and Reference
MAX186EVKIT	1	—	Evaluation Kit for the MAX186/MAX188
MAX187	0	95	Low-Power, Serial 12-Bit ADC with Track/Hold and Reference (8-Pin)
MAX187EVKIT	0	—	Evaluation Kit for the MAX187/MAX189
MAX188	4	—	Low-Power, 8-Channel, 133ksps, Serial 12-Bit ADC with Track/Hold
MAX189	0	95	Low-Power, Serial 12-Bit ADC with Track/Hold (8-Pin)
MAX190	2	—	75ksps, 5V, 12-Bit ADC with Track/Hold and Reference
MAX191	3	94	Low-Power, Sampling, 12-Bit ADC with Reference and Power-Down
MAX191EVKIT	3	—	Evaluation Kit for the MAX191

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX192	0	95	Low-Power, 8-Channel, Serial 10-Bit ADC
MAX194	3	96	85ksps, Serial 14-Bit ADC with 10µA Shutdown
MAX194EVKIT	1	—	Evaluation Kit for the MAX194
MAX195	0	96	16-Bit, 85ksps ADC with 10µA Shutdown
MAX195EVKIT	1	—	Evaluation Kit for the MAX195
MAX196	0	97	6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection
MAX196EVKIT	0	—	Evaluation Kit for the MAX196/MAX198
MAX197	1	97	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection
MAX197EVKIT	1	—	Evaluation Kit for the MAX197/MAX199
MAX198	0	97	6-Channel, Multi-Range, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection
MAX199	0	96	8-Channel, Multi-Range, 5V, 12-Bit DAS with 8+4 Bus Interface and Fault Protection
MAX200	5	95	5V, 5-Channel RS-232 Transmitter with 0.1µF External Capacitors
MAX201	5	95	5V/9V to 13.2V, Dual RS-232 Transceiver with 0.1µF External Capacitors
MAX202	5	95	5V, Dual RS-232 Transceiver with 0.1µF External Capacitors
MAX202E	3	97	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX203	5	95	Complete, 5V, Dual RS-232 Transceiver
MAX203E	3	97	±15kV ESD-Protected, Complete, 5V, Dual RS-232 Transceiver
MAX204	5	95	5V, Quad RS-232 Transmitter with 0.1µF External Capacitors
MAX205	5	95	Complete, 5V, 5-Channel RS-232 Transceiver
MAX205E	3	97	±15kV ESD-Protected, 5-Driver/5-Receiver, +5V, RS-232 Transceiver with Shutdown
MAX206	5	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX206E	3	97	±15kV ESD-Protected, 4-Driver/3-Receiver, +5V, RS-232 Transceiver with Shutdown
MAX207	5	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX207E	3	97	±15kV ESD-Protected, 5-Driver/3-Receiver, +5V, RS-232 Transceiver
MAX208	5	95	5V, Quad RS-232 Transceiver with 0.1µF External Capacitors
MAX208E	3	—	±15kV ESD-Protected, 4-Driver/4-Receiver, +5V, RS-232 Transceiver
MAX209	5	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX211	5	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX211E	3	97	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX212	2	95	3V, 3-Driver/5-Receiver, True RS-232 Serial Port
MAX212EVKIT	—	—	Evaluation Kit for the MAX212
MAX213	5	95	5V RS-232 Transceiver with 0.1µF External Capacitors
MAX213E	3	97	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX214	1	95	5V, Programmable, DTE/DCE RS-232 Transceiver
MAX216	0	94	Low-Power, AppleTalk Interface Transceiver

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX218	1	95	1.8V to 4.25V, Dual RS-232 Transceiver
MAX220	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX222	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX223	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX225	6	—	5V, Multi-Channel RS-232 Driver/Receiver
MAX230	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX231	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232A	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX232E	3	97	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX233	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX233A	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX234	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX235	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX236	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX237	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX238	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX239	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX240	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX241	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX241E	3	97	±15kV ESD-Protected, 5V RS-232 Transceiver
MAX242	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX243	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX244	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX245	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX246	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX247	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX248	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX249	6	95	5V, Multi-Channel RS-232 Driver/Receiver
MAX250	0	92	5V, Isolated, RS-232 Driver/Receiver
MAX251	0	92	5V, Isolated, RS-232 Driver/Receiver
MAX252A/B	2	92	Complete, 5V, Isolated, Dual RS-232 Transceiver Module
MAX253	0	95	Isolated RS-485 Power Driver
MAX260	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX260SOFT	—	—	Filter Design Software for the MAX260
MAX261	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX262	0	92	µP-Programmable, Universal Switched-Capacitor Filter
MAX263	2	92	Pin-Programmable, Universal Switched-Capacitor Filter
MAX264	2	92	Pin-Programmable, Universal Switched-Capacitor Filter
MAX265	0	—	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX266	0	—	Resistor/Pin-Programmable, Universal Switched-Capacitor Filter
MAX267	2	92	Pin-Programmable, Bandpass Switched-Capacitor Filter

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX268	2	92	Pin-Programmable, Bandpass Switched-Capacitor Filter
MAX270	1	92	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter
MAX271	1	92	Digitally Programmable, Dual, 2nd-Order, Continuous Lowpass Filter with Track/Hold
MAX274	3	93	8th-Order, Continuous Analog Filter
MAX274SOFT	3	—	Filter Design Software for the MAX274/MAX275
MAX274EVKIT	2	—	Evaluation Kit for the MAX274
MAX275	3	93	4th-Order, Continuous Analog Filter
MAX280	3	—	5th-Order, Zero DC Error, Butterworth, Switched-Capacitor Lowpass Filter
MAX281	0	92	5th-Order, Zero DC Error, Bessel, Switched-Capacitor Lowpass Filter
MAX291	3	93	8th-Order, Butterworth, Clock-Tunable, 100:1 Lowpass Filter
MAX292	3	93	8th-Order, Bessel, Clock-Tunable, 100:1 Lowpass Filter
MAX293	0	93	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX294	0	93	8th-Order, Elliptic, 1.2 Transition Ratio, Clock-Tunable, 100:1 Lowpass Filter
MAX295	3	93	8th-Order, Butterworth, Clock-Tunable, 50:1 Lowpass Filter
MAX296	3	93	8th-Order, Bessel, Clock-Tunable, 50:1 Lowpass Filter
MAX297	0	93	8th-Order, Elliptic, 1.5 Transition Ratio, Clock-Tunable, 50:1 Lowpass Filter
MAX301	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX303	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX305	0	95	Low-On-Resistance, Precision, Dual, SPST, High-Speed Analog Switch
MAX306	0	95	Precision, 16-Channel, High-Performance, CMOS Analog Multiplexer
MAX307	0	95	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX308	0	95	Precision, 8-Channel, High-Performance, CMOS Analog Multiplexer
MAX309	0	95	Precision, Dual 4-Channel, High-Performance, CMOS Analog Multiplexer
MAX310	0	92	8-Channel, CMOS RF/Video Multiplexer
MAX311	0	92	Differential 4-Channel, CMOS RF/Video Multiplexer
MAX312	0	97	Low-On-Resistance, Quad SPST, Normally Closed, CMOS Analog Switch
MAX313	0	97	Low-On-Resistance, Quad SPST, Normally Open, CMOS Analog Switch
MAX314	0	97	Low-On-Resistance, Quad SPST, 2 Normally Open/2 Normally Closed, CMOS Analog Switch
MAX317	1	95	Precision, SPST, CMOS Analog Switch
MAX318	1	95	Precision, SPST, CMOS Analog Switch
MAX319	1	95	Precision, SPST, CMOS Analog Switch
MAX320	0	96	Precision, Dual-Supply, Dual SPST, Normally Open, CMOS Analog Switch
MAX321	0	96	Precision, Dual-Supply, Dual SPST, Normally Closed, CMOS Analog Switch
MAX322	0	96	Precision, Dual-Supply, Dual SPST, CMOS Analog Switch
MAX323	0	96	Precision, Single-Supply, SPST, Normally Open Analog Switch
MAX324	0	96	Precision, Single-Supply, SPST, Normally Closed Analog Switch
MAX325	0	96	Precision, Single-Supply, SPST Analog Switch
MAX326	2	92	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX327	2	92	Quad SPST, Ultra-Low-Leakage, CMOS Analog Switch
MAX328	1	92	Ultra-Low-Leakage, Single-Ended, Monolithic, CMOS Analog Multiplexer

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX329	1	92	Ultra-Low-Leakage, Differential, Monolithic, CMOS Analog Multiplexer
MAX331	0	—	Quad SPST, Normally Closed, CMOS Analog Switch
MAX332	0	—	Quad SPST, Normally Open, CMOS Analog Switch
MAX333	0	—	Quad SPDT, CMOS Analog Switch
MAX333A	0	95	Improved, Low-On-Resistance, Quad SPDT, CMOS Analog Switch
MAX334	0	—	Quad SPST, High-Speed, Break-Before-Make Analog Switch
MAX335	2	95	Serial-Controlled, Octal SPST Analog Switch
MAX336	**0**	**1-9**	**16-Channel, Low-Leakage, CMOS Analog Multiplexer**
MAX337	**0**	**1-9**	**Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexer**
MAX338	0	95	8-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX339	0	95	Dual 4-Channel, Low-Leakage, CMOS Analog Multiplexer
MAX349	0	97	Low-Voltage, Serial-Controlled Multiplexer
MAX350	0	97	Low-Voltage, Serial-Controlled Multiplexer
MAX351	1	95	Precision, Quad SPST Analog Switch
MAX352	1	95	Precision, Quad SPST Analog Switch
MAX353	1	95	Precision, Quad SPST, Normally Closed Analog Switch
MAX354	2	96	Single, 8-Channel, Fault-Protected CMOS Multiplexer—Improved MAX358
MAX355	2	96	Dual, 4-Channel, Fault-Protected CMOS Multiplexer
MAX358	0	92	8-Channel, Fault-Protected Multiplexer
MAX359	0	92	Differential 4-Channel, Fault-Protected Multiplexer
MAX361	0	95	Precision, Quad SPST Analog Switch
MAX362	0	95	Precision, Quad SPST Analog Switch
MAX364	0	95	Precision, Quad SPST Analog Switch
MAX365	0	95	Precision, Quad SPST Analog Switch
MAX366	0	96	Signal-Line Circuit Protector with Three Independent Protectors
MAX367	0	96	Signal-Line Circuit Protector with Eight Independent Protectors
MAX368	1	92	8-Channel, Fault-Protected, Latched Multiplexer
MAX369	1	92	Differential 4-Channel, Fault-Protected, Latched Multiplexer
MAX378	1	92	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX379	1	92	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX381	0	96	Precision, Dual, Low-Voltage, SPST CMOS Analog Switch
MAX382	0	96	Low-Voltage, 1-of-8 CMOS Multiplexer with Latchable Inputs
MAX383	0	96	Precision, Dual, Low-Voltage, SPDT CMOS Analog Switch
MAX384	0	96	Low-Voltage, Dual, 4-Channel CMOS Multiplexer with Latchable Inputs
MAX385	0	96	Precision, Dual, Low-Voltage, DPST CMOS Analog Switch
MAX388	2	93	8-Channel, High-Voltage, Fault-Protected Multiplexer
MAX389	2	93	Differential 4-Channel, High-Voltage, Fault-Protected Multiplexer
MAX391	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX392	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX393	0	95	Low-Voltage, 5V/±5V Quad, CMOS Analog Switch
MAX394	0	96	Low-Voltage, Quad SPDT, CMOS Analog Switch—Replaces MAX333A
MAX395	0	97	Low-Voltage, Serially Controlled, Octal SPST Analog Switch

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX396	1	96	Precision, 16-Channel, Low-Voltage, CMOS Analog Multiplexer—DG406 Pinout
MAX397	1	96	Precision, Dual, 8-Channel, Low-Voltage, CMOS Analog Multiplexer—DG407 Pinout
MAX398	2	96	Precision, 8-Channel, Low-Voltage, CMOS Analog Multiplexer—DG408 Pinout
MAX399	2	96	Precision, Dual, 4-Channel, Low-Voltage, CMOS Analog Multiplexer
MAX400	0	—	Ultra-Low-Offset Op Amp
MAX402	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX403	2	94	High-Speed, Low-Voltage, Micropower Op Amp
MAX404	0	92	Video Op Amp
MAX405	1	92	Precision Video Buffer Amplifier
MAX406	2	94	Single, 1.2µA Max, Single-Supply Op Amp
MAX407	2	94	Dual, 1.2µA Max, Single-Supply Op Amp
MAX408	0	—	High-Speed, High Output Current Op Amp
MAX409	2	94	Single, 1.2µA Max, 150kHz, Single-Supply Op Amp
MAX410	2	94	Single, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX412	2	94	Dual, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX414	2	94	Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amp
MAX417	2	94	Dual, 1.2µA Max, Single-Supply Op Amp
MAX418	2	94	Quad, 1.2µA Max, Single-Supply Op Amp
MAX419	2	94	Quad, 1.2µA Max, Single-Supply Op Amp
MAX420	1	—	±15V Chopper-Stabilized Op Amp
MAX421	1	—	±15V Chopper-Stabilized Op Amp
MAX422	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX423	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX427	0	94	Low-Noise, High-Precision Op Amp
MAX428	0	—	Dual, High-Speed, High-Output-Current Op Amp
MAX430	1	—	±15V Chopper-Stabilized Op Amp
MAX432	1	—	Low-Power, ±15V Chopper-Stabilized Op Amp
MAX435	1	94	275MHz Wideband Transconductance Amplifier with Differential Output
MAX436	1	94	200MHz Wideband Transconductance Amplifier with Single-Ended Output
MAX437	0	94	Low-Noise, High-Precision Op Amp
MAX440	1	93	8-Channel, High-Speed, Video Multiplexer/Amplifier
MAX441	1	93	4-Channel, High-Speed, Video Multiplexer/Amplifier
MAX442	1	93	2-Channel, 140MHz, Video Multiplexer/Amplifier
MAX445	0	95*	High-Voltage, 200MHz Video CRT Driver
MAX448	0	—	Quad, High-Speed, High-Output-Current Op Amp
MAX451	0	—	Low-Bias-Current, 10MHz Video Amplifier
MAX452	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX453	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX454	0	92	50MHz Video Amplifier and Multiplexer/Amplifier

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).

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MAX455	0	92	50MHz Video Amplifier and Multiplexer/Amplifier
MAX456	2	—	8x8 Crosspoint Video Switch
MAX457	0	92	Dual, 70MHz Video Amplifier
MAX458	2	95	8x4 Video Crosspoint Switches with Buffers
MAX459	2	95	8x4 Video Crosspoint Switches with Buffers
MAX459EVKIT	2	—	Evaluation Kit for the MAX458/MAX459
MAX460	0	—	High-Accuracy Fast Buffer
MAX463	2	95	100MHz, Triple RGB Video Switch with Gain of +1 Buffer
MAX464	2	95	100MHz, Quad RGB Video Switch with Gain of +1 Buffer
MAX465	2	95	90MHz, Triple RGB Video Switch with Gain of +2 Buffer
MAX466	2	95	90MHz, Quad RGB Video Switch with Gain of +2 Buffer
MAX466EVKIT	2	—	Evaluation Kit for the MAX464/MAX466
MAX467	2	95	100MHz, Triple RGB Video Gain of +1 Buffer
MAX468	2	95	100MHz, Quad Gain of +1 Video Buffer
MAX469	2	95	90MHz, Triple RGB Video Gain of +2 Buffer
MAX470	2	95	90MHz, Quad Gain of +2 Video Buffer
MAX471	2	96	Precision, High-Side Current-Sense Amplifier
MAX472	2	96	Precision, High-Side Current-Sense Amplifier
MAX473	1	96	Single, 10MHz, 15V/µs, Single-Supply Op Amp
MAX474	1	96	Dual, 10MHz, 15V/µs, Single-Supply Op Amp
MAX475	1	96	Quad, 10MHz, 15V/µs, Single-Supply Op Amp
MAX477	2	97	300MHz High-Speed Amplifier
MAX477EVKIT	2	—	Evaluation Kit for the MAX477
MAX478	0	94	Dual, 17µA Max, Single-Supply, Precision Op Amp
MAX479	0	94	Quad, 17µA Max, Single-Supply, Precision Op Amp
MAX480	2	92	High-Precision, Low-Voltage, Micropower Op Amp
MAX481	5	95	500µA RS-485 Transceiver with Low-Power Shutdown
MAX481E	3	97	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX483	5	95	Slew-Rate-Limited, 350µA RS-485 Transceiver with Low-Power Shutdown
MAX483E	3	97	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with Shutdown
MAX485	5	95	500µA, RS-485 Transceiver—Direct LTC485 Replacement
MAX485E	3	97	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX487	5	95	Slew-Rated-Limited, 350µA RS-485 Transceiver with 1/4-Unit Load
MAX487E	3	97	250kbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver with 1/4-Unit Load
MAX488	5	95	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX488E	3	97	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver
MAX489	5	95	Slew-Rated-Limited, 350µA, Full-Duplex RS-485 Transceiver
MAX489E	3	97	250kbps, ±15kV ESD-Protected, Low-Power, Full-Duplex RS-485/RS-422 Transceiver

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MAX490	5	95	500µA, Full-Duplex RS-485 Transceiver
MAX490E	3	97	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX491	5	95	500µA, Full-Duplex RS-485 Transceiver
MAX491E	3	97	2.5Mbps, ±15kV ESD-Protected, Low-Power RS-485/RS-422 Transceiver
MAX492	2	96	Dual, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX494	2	96	Quad, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX495	2	96	Single, Micropower, Single-Supply, Rail-to-Rail, I/O Op Amp
MAX496	0	97	375MHz, Quad, Gain of +1 Video Buffer
MAX497	0	97	275MHz, Quad, Gain of +2 Video Buffer
MAX497EVKIT	0	—	Evaluation Kit for the MAX496/MAX497
MAX498	0	97	310MHz, RGB Video Multiplexer with High-Speed Amplifier
MAX498EVKIT	0	—	Evaluation Kit for the MAX498
MAX499	0	97	310MHz, RGB Video Multiplexer with High-Speed Amplifier
MAX500	2	—	CMOS, Quad, Serial 8-Bit DAC
MAX501	1	93	Voltage-Output, Multiplying, 12-Bit DAC with 8+4 Interface
MAX502	1	93	Voltage-Output, Multiplying, 12-Bit DAC with 12-Bit Interface
MAX503	0	96	5V, Low-Power, Parallel-Input, Voltage-Output, 10-Bit DAC
MAX504	1	96	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC with Internal Reference
MAX505	2	—	Quad, 8-Bit DAC with Rail-to-Rail Outputs
MAX506	2	—	Quad, 8-Bit DAC with Rail-to-Rail Outputs
MAX507	A	93	Voltage-Output, 12-Bit DAC with Internal Reference and 12-Bit Interface
MAX508	A	93	Voltage-Output, 12-Bit DAC with Internal Reference and 8+4 Interface
MAX509	2	—	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX510	2	—	Quad, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX512	2	95	5V, Triple, Voltage-Output, Serial, 8-Bit DAC
MAX513	2	95	3V, Triple, Voltage-Output, Serial, 8-Bit DAC
MAX514	0	93	Quad, CMOS, Serial, Multiplying, 12-Bit DAC
MAX515	1	96	5V, Low-Power, Voltage-Output, Serial, 10-Bit DAC
MAX516	1	92	Quad, DAC-Programmed, CMOS Comparator
MAX517	0	96	Single, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX518	0	96	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs in 8-Pin Package
MAX519	0	96	Dual, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX520A/B	3	97	Quad, 2-Wire, Serial, 8-Bit DAC with Unbuffered Outputs
MAX521	3	97	Octal, 2-Wire, Serial, 8-Bit DAC with Rail-to-Rail Outputs
MAX522	0	96	Dual, Voltage-Output, Serial, 8-Bit DAC in 8-Pin Package
MAX525	1	97	Lowest Power, +5V, Serial, Quad 12-Bit DAC
MAX526	3	93	Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX527	3	93	±5V, Calibrated, Quad, Voltage-Output, 12-Bit DAC
MAX528	2	93	Octal, Serial, 8-Bit DAC with Output Buffers
MAX529	2	93	±5V, Octal, Serial, 8-Bit DAC with Output Buffers
MAX530	3	95	5V, Low-Power, Voltage-Output, Parallel, 12-Bit DAC with Reference
MAX531	6	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC with Reference

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX532	1	95	Dual, Serial-Input, Voltage-Output, Multiplying, 12-Bit DAC
MAX533	0	97	+3V, Serial, Quad 8-Bit DAC in QSOP Package
MAX534	0	97	+5V, Serial, Quad 8-Bit DAC in QSOP Package
MAX535	**1**	**9-7**	**+5V, 13-Bit, Serial, Voltage-Output DAC in 8-Pin µMAX Package**
MAX536	2	95	Quad, Serial, Voltage-Output, 12-Bit DAC
MAX537	2	95	Quad, Serial, Voltage-Output, ±5V, 12-Bit DAC
MAX538	6	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 2.6V Output
MAX539	6	95	5V, Low-Power, Voltage-Output, Serial, 12-Bit DAC, 0V to 4.5V Output
MAX541	1	97	+5V, 16-Bit, Serial, Voltage-Output DAC in 8-Pin Package
MAX542	1	97	+5V, 16-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration
MAX543	1	—	Serial, CMOS, Multiplying, 12-Bit DAC in 8-Pin Package
MAX544	2	97	+5V, 14-Bit, Serial, Voltage-Output DAC in 8-Pin Package
MAX545	2	97	+5V, 14-Bit, Serial, Voltage-Output DAC with Bipolar Output Configuration
MAX547	3	95	Octal, Voltage-Output, 13-Bit DAC with Parallel Interface
MAX548A	**0**	**9-23**	**2.7V to 5.5V, 8-Bit, Dual, Voltage-Output DAC in µMAX-8 Package**
MAX549A	**0**	**9-23**	**2.7V to 5.5V, 8-Bit, Dual, Voltage-Output DAC in µMAX-8 Package**
MAX550A	**0**	**9-23**	**2.7V to 5.5V, 8-Bit, Single, Serial, Voltage-Output DAC in µMAX-8 Package**
MAX551	**0**	**9-37**	**+5V, 12-Bit, Current-Output Multiplying DAC in µMAX-10 Package**
MAX552	**0**	**9-37**	**+3V, 12-Bit, Current-Output Multiplying DAC in µMAX-10 Package**
MAX555	1	96	300Msps, 12-Bit DAC with Complementary Voltage Outputs
MAX555EVKIT	1	—	Evaluation Kit for the MAX555
MAX560	0	93	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX561	0	93	3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown
MAX562	0	95	2.7V to 5.25V, High-Speed RS-232 Serial Port
MAX563	0	95	3.3V, Dual EIA/TIA-562 Transceiver
MAX603	0	96	5V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulator
MAX604	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 500mA Linear Regulator
MAX606	0	97	Low-Profile, 0.8MHz, Step-Up DC-DC Converter for Type 1 Flash Memory/PCMCIA Cards
MAX606EVKIT	0	—	Evaluation Kit for the MAX606/MAX607
MAX607	0	97	Low-Profile, 0.4MHz, Step-Up DC-DC Converter for Type 2 and 3 Flash Memory/PCMCIA Cards
MAX608	0	97	Low-Input-Voltage, High-Efficiency, Step-Up DC-DC Controller
MAX608EVKIT	0	—	Evaluation Kit for the MAX608
MAX613	0	95	Dual-Slot, PCMCIA Analog Power Controller
MAX614	0	95	Single-Slot, PCMCIA Analog Power Controller
MAX619	2	95	Regulated 5V Charge-Pump DC-DC Converter
MAX619EVKIT	1	—	Evaluation Kit for the MAX619
MAX620	2	—	Quad, High-Side MOSFET Driver
MAX621	2	—	Quad, High-Side MOSFET Driver
MAX622	0	92	High-Side Power Supply

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX623	0	92	High-Side Power Supply
MAX624	1	96	Dual-Output, 1MHz, DC-DC Boost Converter for PCMCIA Applications
MAX626	1	—	Dual-Power MOSFET Driver (Inverting)
MAX627	1	—	Dual-Power MOSFET Driver (Noninverting)
MAX628	1	—	Dual-Power MOSFET Driver (Inverting & Noninverting)
MAX629	**1**	**4-13**	**28V, Low-Power, High-Voltage Boost or Inverting DC-DC Converter**
MAX629EVKIT	1	—	Evaluation Kit for the MAX629
MAX630	0	92	CMOS, Micropower, Step-Up Switching Regulator
MAX631	0	92	5V/Adjustable, Step-Up Switching Regulator
MAX632	0	92	12V/Adjustable, CMOS, Step-Up Switching Regulator
MAX633	0	92	15V/Adjustable, CMOS, Step-Up Switching Regulator
MAX634	0	92	CMOS, Micropower, Inverting Switching Regulator
MAX635	0	92	-5V/Adjustable, CMOS, Inverting Switching Regulator
MAX636	0	92	-12V/Adjustable, CMOS, Inverting Switching Regulator
MAX637	0	92	-15V/Adjustable, CMOS, Inverting Switching Regulator
MAX638	0	92	5V/Adjustable, CMOS, Step-Down Switching Regulator
MAX639	2	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX639EVKIT	0	—	Evaluation Kit for the MAX639/MAX640/MAX653
MAX640	2	95	3.3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX641	0	92	5V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX642	0	92	12V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX643	0	92	15V/Adjustable, 10W, CMOS, Step-Up, Switching Regulator Controller
MAX649	2	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX651	2	95	3.3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX652	2	95	3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Controller
MAX653	2	95	3V/Adjustable, High-Efficiency, Low I_Q, Step-Down DC-DC Converter
MAX660	2	92	100mA, Charge-Pump Voltage Converter
MAX662A	1	95	12V, 30mA Flash Memory Programming Supply
MAX662EVKIT	1	—	Evaluation Kit for the MAX662A
MAX663	1	92	CMOS, 5V/Adjustable, Micropower, Positive Linear Regulator
MAX664	1	92	CMOS, -5V/Adjustable, Micropower, Negative Linear Regulator
MAX665	0	93	100mA, 1.5V to 8V, CMOS, Switched-Capacitor Voltage Converter
MAX666	1	92	5V/Adjustable, Micropower, Positive Linear Regulator with Low-Battery Detector
MAX667	3	95	5V/Programmable, Low-Dropout Voltage Regulator
MAX674	0	92	Precision, 10V Voltage Reference
MAX675	0	92	Precision, 5V Voltage Reference
MAX678	1	95*	Calibrated, 1ppm/°C, Low-Drift, 10V Precision Voltage Reference
MAX679	**0**	**4-23**	**Regulated 3.3V Charge Pump**
MAX679EVKIT	0	—	Evaluation Kit for the MAX679
MAX680	1	92	5V to ±10V, Switched-Capacitor Voltage Converter
MAX681	1	92	5V to ±10V, Switched-Capacitor Voltage Converter

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).

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MAX682	—	**4-29***	**Regulated 5V Charge Pump with 250mA Output**
MAX682EVKIT	†	—	Evaluation Kit for the MAX682
MAX683	—	**4-29***	**Regulated 5V Charge Pump with 100mA Output**
MAX684	—	**4-29***	**Regulated 5V Charge Pump with 50mA Output**
MAX684EVKIT	†	—	Evaluation Kit for the MAX683/MAX684
MAX685	—	**4-31***	**Dual-Output, Positive and Negative, CCD and LCD Power Supply**
MAX685EVKIT	†	—	Evaluation Kit for the MAX685
MAX686	—	**4-33***	**28V DC-DC Converter with Internal Switch and DAC Output Control**
MAX686EVKIT	†	—	Evaluation Kit for the MAX686
MAX687	0	96	3.3V, Low-Noise, Linear Regulator Controller with Automatic Shutdown
MAX687EVKIT	0	—	Evaluation Kit for the MAX687
MAX688	0	96	3.3V, Low-Noise, Linear Regulator Controller
MAX688EVKIT	0	—	Evaluation Kit for the MAX688/MAX689
MAX689	0	96	3V, Low-Noise, Linear Regulator Controller
MAX690	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX690A	3	95	µP Reset IC with Watchdog and Battery Switchover
MAX690R/S/T	1	95	µP Reset IC with Watchdog and Battery Switchover
MAX691	2	—	µP Reset IC with Watchdog, Chip Enable, and Battery Switchover
MAX691A	7a	95	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX692	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX692A	3	95	µP Reset IC with Watchdog and Battery Switchover
MAX693	2	—	µP Reset IC with Watchdog, Chip Enable, and Battery Switchover
MAX693A	7a	—	µP Reset IC with Watchdog, Chip Enable, and Battery Backup
MAX694	2	—	µP Reset IC with Watchdog and Battery Switchover
MAX695	2	—	µP Reset IC with Watchdog, Chip Enable, and Battery Switchover
MAX696	0	92	µP Supervisor with Battery Switchover and Programmable Reset
MAX697	0	92	µP Supervisor with Programmable Reset
MAX698	0	92	Low-Cost Power-On Reset IC
MAX699	0	92	Low-Cost Power-On Reset IC with Watchdog Controller
MAX700	0	92	Adjustable-Threshold Power-Supply Monitor with Reset
MAX701	0	92	Power-Supply Monitor with Reset
MAX702	0	92	Power-Supply Monitor with Reset
MAX703	1	94	µP Reset IC with Battery Backup
MAX704	1	94	µP Reset IC with Battery Backup
MAX704R/S/T	0	95	3V µP Reset IC with Battery Backup
MAX705	5	95	µP Reset IC with Watchdog
MAX706	5	95	µP Reset IC with Watchdog
MAX706P/R/S/T	2	95	3V µP Reset IC with Watchdog
MAX707	5	95	µP Reset IC with Power-Fail Warning
MAX708	5	95	µP Reset IC with Power-Fail Warning
MAX708R/S/T	2	95	3V µP Reset IC with Power-Fail Warning
MAX709L/M/R/S/T	1	94	Power-Supply Monitor with Reset

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).
†Future product. The data sheet is pending.

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX710	**0**	**4-35**	**250mA Step-Up/Down DC-DC Converter**
MAX710EVKIT	0	—	Evaluation Kit for the MAX710/MAX711
MAX711	**0**	**4-35**	**250mA Step-Up/Down DC-DC Converter**
MAX712	3	94	Battery Fast-Charge Controller (NiMH)
MAX712EVKIT	3	—	Linear-Mode Evaluation Kit for the MAX712/MAX713
MAX713	3	94	Battery Fast-Charge Controller (NiCd)
MAX713SWEVKIT	3	—	Switch-Mode Evaluation Kit for the MAX712/MAX713
MAX714	2	93	3-Output, Battery-Powered Supply System
MAX715	2	93	6-Output, Battery-Powered Supply System
MAX716	2	93	7-Output, Battery-Powered Supply System
MAX716EVKIT	1	—	Evaluation Kit for the MAX716
MAX717	0	94	3.3V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718	0	94	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX718EVKIT	0	—	Evaluation Kit for the MAX717/MAX718/MAX719
MAX719	0	94	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX720	0	94	3.3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX721	0	94	3V/5V Palmtop Computer and Flash Memory Power-Supply Regulator
MAX722	0	93	3.3V/5V Palmtop Computer and LCD Power-Supply Regulator
MAX722EVKIT	0	—	Evaluation Kit for the MAX722/MAX723
MAX723	0	93	3V Palmtop Computer and LCD Power-Supply Regulator
MAX724	3	94	5A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX726	3	94	2A, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX727	2	94	2A, 5V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX728	2	94	2A, 3.3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX729	2	94	2A, 3V, Step-Down, PWM, Switch-Mode DC-DC Converter
MAX730A	2	95	5V, Step-Down, Current-Mode, PWM DC-DC Converter
MAX731	2	—	5V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX731EVKIT	0	—	Evaluation Kit for the MAX731
MAX732	2	93	12V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX732EVKIT	2	—	Evaluation Kit for the MAX732
MAX733	2	93	15V, Step-Up, Current-Mode, PWM DC-DC Converter
MAX734	2	94	12V, 120mA Flash Memory Programming Supply
MAX734EVKIT	2	—	Evaluation Kit for the MAX734
MAX735	1	94	-5V, Inverting, PWM DC-DC Converter
MAX736	3	—	-12V, Inverting, PWM, Current-Mode DC-DC Converter
MAX737	3	—	-15V, Inverting, PWM, Current-Mode DC-DC Converter
MAX738EVKIT	N/A	—	Evaluation Kit for the MAX730A/38A/44A/48A/63A
MAX738A	2	95	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX739	3	93	-5V, Inverting, PWM, Current-Mode DC-DC Converter
MAX739EVKIT	3	—	Evaluation Kit for the MAX736/MAX737/MAX739/MAX759
MAX741	1	94	Pin-Programmed, Low-Voltage, PWM Current-Mode Controller
MAX741EVKIT	1	—	Evaluation Kit for the MAX741

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX742	2	92	Switch-Mode Regulator with 5V to ±1V or ±15V Dual Output
MAX742EVKIT	2	—	Evaluation Kit for the MAX742
MAX743	0	92	Dual-Output, PWM Switch-Mode Regulator (5V to ±15V or ±12V)
MAX743EVKIT	0	—	Evaluation Kit for the MAX743
MAX744A	2	95	5V, Step-Down, PWM, Current-Mode DC-DC Converter
MAX745	1	—	High-Efficiency, 4A Lithium-Ion Battery Charger
MAX745EVKIT	1	—	Evaluation Kit for the MAX745
MAX746	1	—	High-Efficiency, PWM, Step-Down, N-Channel DC-DC Controller
MAX747	1	94	High-Efficiency, PWM, Step-Down Controller (External P-Channel Driver)
MAX747EVKIT	0	—	Evaluation Kit for the MAX747
MAX748A	0	95	3.3V, PWM, Step-Down DC-DC Converter
MAX749	1	94	Digitally Adjustable LCD Bias Supply
MAX749EVKIT	1	—	Evaluation Kit for the MAX749
MAX750A	0	95	Adjustable, PWM, Step-Down Regulator
MAX751	1	94	5V, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752	2	93	Adjustable, Step-Up, PWM, Current-Mode DC-DC Converter
MAX752EVKIT	0	—	Evaluation Kit for the MAX732/MAX733/MAX752
MAX753	1	—	CCFT Backlight and LCD Negative Contrast Controller
MAX754	1	—	CCFT Backlight and LCD Positive Contrast Controller
MAX755	1	94	Adjustable, PWM, Inverting DC-DC Converter
MAX756	2	—	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX756EVKIT	2	—	Evaluation Kit for the MAX756/MAX757
MAX757	2	—	3.3V/5V, High-Efficiency, Step-Up DC-DC Converter
MAX758A	0	95	Adjustable, PWM, Step-Down DC-DC Converter
MAX758EVKIT	N/A	—	Evaluation Kit for the MAX750A/MAX758A
MAX759	3	—	Adjustable, Inverting, PWM, Current-Mode DC-DC Converter
MAX759LCDKIT	3	—	Evaluation Kit for the MAX759
MAX761	0	95	12V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converter
MAX761EVKIT	0	—	Evaluation Kit for the MAX761/MAX762
MAX762	0	95	15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Converter
MAX763A	0	95	3.3V, PWM, Step-Down DC-DC Converter
MAX764	0	95	-5V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter
MAX764EVKIT	0	—	Evaluation Kit for the MAX764/MAX765/MAX766
MAX765	0	95	-12V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter
MAX766	0	95	-15V/Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Converter
MAX767	2	95	5V Supply to 3.3V Output, Synchronous, Step-Down Power-Supply Controller
MAX767EVKIT	1	—	Evaluation Kit for the MAX767
MAX768	0	—	Low-Noise, Dual-Output, Regulated Charge Pump for GaAsFET, LCD, and VCO Supplies
MAX770	2	95	5V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX770EVKIT	2	—	Evaluation Kit for the MAX770/MAX771/MAX772
MAX771	2	95	12V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX772	2	95	15V/Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX773	2	95	5V/12V/15V/Adjustable, High-Voltage, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX774	1	95	-5V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX774EVKIT	0	—	Evaluation Kit for the MAX774/MAX775/MAX776
MAX775	1	95	-12V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX776	1	95	-15V or Adjustable, High-Efficiency, Low I_Q, Inverting DC-DC Controller
MAX777L	2	—	1V-Input, 5V-Output, Step-Up DC-DC Converter
MAX778L	2	—	1V-Input, 3V/3.3V-Output, Step-Up DC-DC Converter
MAX778LEVKIT	2	—	Evaluation Kit for the MAX777L/MAX778L/MAX779L
MAX779L	2	—	1V-Input, Adjustable-Output, Step-Up DC-DC Converter
MAX780	1	—	Dual-Slot, PCMCIA Analog Power Controller
MAX781	0	—	PDA/Hand-Held Computer Power Controller
MAX782	2	—	Triple-Output Power-Supply Controller for Notebook Computers
MAX782EVKIT	2	—	Evaluation Kit for the MAX782
MAX783	1	—	3.3V/5V Notebook Computer Power Supply, Dual PCMCIA VPP Outputs (6-Cell Input)
MAX783EVKIT	1	—	Evaluation Kit for the MAX783
MAX786	1	95	3.3V/5V Notebook Computer Power Supply with 25µA Shutdown
MAX786EVKIT	1	—	Evaluation Kit for the MAX786
MAX787	3	95	5V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX788	3	95	3.3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX789	3	95	3V, 5A Step-Down, PWM, Switch-Mode DC-DC Regulator
MAX791	5	—	µP Supervisory Circuit
MAX792L/M/R/S/T	1	—	µP and Non-Volatile Memory Supervisory Circuit
MAX793R/S/T	1	96	3V/3.3V µP Supervisory Circuit
MAX794	1	96	3V/3.3V Adjustable, µP Supervisory Circuit
MAX795R/S/T	1	96	3V/3.3V µP Supervisory Circuit
MAX796	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Positive Secondary
MAX796EVKIT	2	—	Evaluation Kit for the MAX796/MAX799
MAX797	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power
MAX797EVKIT	2	—	Evaluation Kit for the MAX797
MAX797H	0	—	High-Voltage, Step-Down Controller with Synchronous Rectifier for CPU Power
MAX798	**0**	**4-45**	**Step-Down, PWM Controller with Synchronous Rectifier for CPU Power, Adjustable from 5.5V to 1.6V**
MAX799	2	96	Step-Down, PWM Controller with Synchronous Rectifier for CPU Power with Negative Secondary
MAX800L/M	7	—	µP Reset IC with Watchdog, Battery Switchover, and ±2% Power-Fail Accuracy
MAX801L/M/N	0	97	8-Pin µP Supervisory Circuit with ±1.5% Accuracy and Watchdog Timer

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX802L/M	3	95	High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX802R/S/T	0	95	3V, High-Accuracy µP Reset IC with Watchdog and Battery Backup
MAX804R/S/T	0	95	3V, High-Accuracy µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805L	3	95	µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX805R/S/T	0	95	3V µP Reset IC (asserted high) with Watchdog and Battery Backup
MAX806R/S/T	0	95	3V, High-Accuracy µP Reset IC with Battery Backup
MAX807L/M/N	0	96*	µP Supervisory Circuit with ±1.5% Reset Accuracy
MAX808L/M/N	0	97	8-Pin µP Supervisory Circuit with ±1.5% Reset Accuracy and On-Board Gating of Chip Enable
MAX809L/M/R/S/T	2	96*	3-Pin µP Reset Circuit
MAX810L/M/R/S/T	2	96*	3-Pin µP Reset Circuit
MAX811L/M/R/S/T	1a	96	4-Pin µP Voltage Monitor with Manual $\overline{\text{RESET}}$ Output
MAX812L/M/R/S/T	1a	96*	4-Pin µP Voltage Monitor with Manual RESET Output
MAX813L	5	95	µP Reset IC (asserted high) with Watchdog
MAX814K/L/N/T	0	96	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX815K/L/N/T	0	96	High-Accuracy, 1%, Low-Power, 3V and 5V µP Supervisory Circuit
MAX816	0	96	High-Accuracy, 1%, Low-Power, Adjustable µP Supervisory Circuit
MAX817L/M	1	97	5V µP Supervisory Circuit
MAX818L/M	1	97	5V Microprocessor Supervisory Circuit in a µMax Package
MAX819L/M	1	97	5V µP Supervisory Circuit with Manual Reset Input
MAX820L/M/R/S/T	1	—	µP and Non-Volatile Memory Supervisory Circuit
MAX821L/M/R/S/T	0	97	4-Pin µP Supervisory Circuit with Active-Low Reset
MAX822L/M/R/S/T	0	97	4-Pin µP Supervisory Circuit with Active-High Reset
MAX823L/M/R/S/T	0	97	5-Pin µP Supervisory Circuit with Watchdog Input and Manual-Reset Input
MAX824L/M/R/S/T	0	97	5-Pin µP Supervisory Circuit with Watchdog Input and Active-High Reset
MAX825L/M/R/S/T	0	97	5-Pin µP Supervisory Circuit with Manual-Reset Input and Active-High Reset
MAX828	2	97	Ultra-Small, 25mA Inverting Charge Pump in SOT23
MAX829	2	97	Ultra-Small, 25mA Inverting Charge Pump in SOT23
MAX830	2	96	1A, Adjustable V_{OUT}, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX831	2	96	1A, 5V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX831EVKIT	2	—	Evaluation Kit for the MAX830–MAX833
MAX832	2	96*	1A, 3.3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX833	2	96*	1A, 3V, Step-Down, PWM DC-DC Converter—Surface Mountable
MAX834	0	97*	Micropower, Latching Voltage Monitor in SOT23 with Open-Drain Output
MAX835	0	97*	Micropower, Latching Voltage Monitor in SOT23 with Push/Pull Output
MAX836	0	97	4-Pin Micropower Voltage Monitor with Open-Drain Output
MAX837	0	97	4-Pin Micropower Voltage Monitor with Push/Pull Output
MAX840	1	96	Low-Noise, Regulated, -2V GaAsFET Bias
MAX840EVKIT	1	—	Evaluation Kit for the MAX840/MAX843/MAX844

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX843	1	96	Low-Noise, Regulated, -2V GaAsFET Bias with Adjustable Reference
MAX844	1	96	Low-Noise, Regulated, -2V GaAsFET Bias with LCD Output
MAX845	3	96	750mW Isolated Transformer Driver for PCMCIA Applications
MAX845EVKIT	3	—	Evaluation Kit for the MAX845
MAX846A	0	97	Cost-Saving, Chemistry-Independent Battery-Charger System
MAX846AEVKIT	0	—	Evaluation Kit for the MAX846A
MAX847	—	**4-55***	**1-Cell, Step-Up, Two-Way Pager System IC**
MAX848	1	97	1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converter with 0.5A MOSFET Power Switch
MAX848EVKIT	†	—	Evaluation Kit for the MAX848/MAX849
MAX849	1	97	1-Cell to 3-Cell, High-Power, Low-Noise, Step-Up DC-DC Converter with 1A MOSFET Power Switch
MAX850	2	95	-4.1V/Adjustable, GaAsFET Bias Supply
MAX850EVKIT	2	—	Evaluation Kit for the MAX850–MAX853
MAX851	2	95	-4.1V/Adjustable, GaAsFET Bias Supply
MAX852	2	95	-4.1V/Adjustable, GaAsFET Bias Supply with Adjustable Oscillator
MAX853	2	95	Adjustable-Output GaAsFET Bias Supply with Adjustable Reference Level
MAX856	4	95	3.3V/5V, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX856EVKIT	4	—	Evaluation Kit for the MAX856–MAX859
MAX857	4	95	Adjustable-Output, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX858	4	95	3.3V/5V, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX859	4	95	Adjustable-Output, High-Efficiency, Low I_Q, DC-DC Step-Up Converter
MAX860	1	95	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX861	1	95	50mA, Frequency-Selectable, Switched-Capacitor Voltage Converter
MAX863	**1**	**4-57**	**Dual-Output, High-Efficiency, PFM, Step-Up DC-DC Controller**
MAX863EVKIT	0	—	Evaluation Kit for the MAX863
MAX864	0	97	Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter with Shutdown
MAX865	0	97	Dual-Output, Doubling/Inverting Charge-Pump Voltage Converter in µMAX
MAX866	1	96	3.3V/5V-Output, Single-Cell DC-DC Converter for Pagers
MAX866EVKIT	0	—	Evaluation Kit for the MAX866/MAX867
MAX867	1	96	Adjustable-Output, Single-Cell DC-DC Converter for Pagers
MAX868	—	**4-73***	**Regulating -2x Charge Pump with 10mA Output**
MAX869L	**0**	**4-75***	**2A, Current-Limited Power Switch with Accurate Adjustable Limit**
MAX870	**0**	**4-77**	**Ultra-Small Inverting Charge Pump in SOT23 (125kHz)**
MAX871	**0**	**4-77**	**Ultra-Small Inverting Charge Pump in SOT23 (500kHz)**
MAX872	1	94	10µA, Low-Dropout, 2.5V Precision Voltage Reference
MAX873	1	94	Low-Power, Low-Drift, 2.5V Precision Voltage Reference
MAX874	1	94	10µA, Low-Dropout, 4.096V Precision Voltage Reference
MAX875	1	94	Low-Power, Low-Drift, 5V Precision Voltage Reference
MAX876	1	94	Low-Power, Low-Drift, 10V Precision Voltage Reference
MAX881R	—	**4-85***	**Low-Noise Bias Supply for GaAsFET PA with Power-OK in µMAX**

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†Future product. The data sheet is pending.

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MAX882	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Standby Mode
MAX883	0	96	5V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Shutdown Mode
MAX884	0	96	3.3V or Adjustable, Low-Dropout, Low I_Q, 200mA Linear Regulator with Shutdown Mode
MAX887	0	97	Low-Noise, Adjustable-Output, Step-Down DC-DC Converter with Synching Capability
MAX887EVKIT	0	—	Evaluation Kit for the MAX887
MAX890L	0	97	90mΩ, 1A, Current-Limited Power Switch
MAX891L	**0**	**4-87**	**150mΩ, 0.5A, Current-Limited Power Switch**
MAX892L	**0**	**4-87**	**300mΩ, 0.25A, Current-Limited Power Switch**
MAX894L	0	97	150mΩ, 0.5A, Dual Current-Limited Power Switch
MAX895L	0	97	300mΩ, 0.25A, Dual Current-Limited Power Switch
MAX900	3	92	Quad, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX901	3	92	Quad, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX902	3	92	Dual, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX903	3	92	Single, High-Speed, Low-Power, Single-Supply Voltage Comparator
MAX905	0	93	High-Speed, Clocked, Master/Slave, ECL Voltage Comparator
MAX906	0	93	Dual, High-Speed, Clocked, Master/Slave, ECL Voltage Comparator
MAX907	3	94	Dual, High-Speed, Low-Power, Single 5V TTL Comparator
MAX908	3	94	Quad, High-Speed, Low-Power, Single 5V TTL Comparator
MAX909	3	94	Single, High-Speed, Low-Power, Single 5V TTL Comparator
MAX910	1	93	High-Speed, Threshold-Programmable Voltage Comparator
MAX912	1	95	Dual, Ultra-Fast, Low-Power, Single-Supply, TTL Comparator
MAX913	1	95	Single, Ultra-Fast, Low-Power, Single-Supply, TTL Comparator
MAX915	0	—	Single, Ultra-High-Speed, Master/Slave TTL Comparator
MAX921	3	94	Single, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Reference
MAX922	3	94	Dual, Ultra-Low-Power, Single-Supply Comparator
MAX923	3	94	Dual, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Ref.
MAX924	3	94	Quad, Ultra-Low-Power, Single-Supply Comparator with 1% Precision Ref.
MAX931	1	95	Single, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX932	1	95	Dual, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX933	1	95	Dual, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX934	1	95	Quad, Ultra-Low-Power, Low-Cost, Single-Supply Comparator with 2%-Accurate Reference
MAX941	3	95	Single, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator
MAX942	3	95	Dual, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator

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MAX944	3	95	Quad, 3V and 5V, Single-Supply, 75ns, Rail-to-Rail Input Comparator
MAX951	1	97	7µA, Single-Supply Op Amp + Comparator + Reference
MAX952	1	97	7µA, Single-Supply Op Amp + Comparator + Reference
MAX953	1	97	5µA, Single-Supply Op Amp + Comparator
MAX954	1	97	5µA, Single-Supply Op Amp + Comparator
MAX961	**2**	**3-11**	**Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX962	**2**	**3-11**	**Dual, Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX963	**2**	**3-11**	**Dual, Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX964	**2**	**3-11**	**Quad, Single-Supply, Operation Down to 2.7V, 4.5ns Comparator**
MAX965	**0**	**3-21**	**Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference**
MAX966	**0**	**3-21**	**Dual, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator**
MAX967	**0**	**3-21**	**Dual, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference**
MAX968	**0**	**3-21**	**Dual, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference**
MAX969	**0**	**3-21**	**Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference**
MAX970	**0**	**3-21**	**Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator**
MAX971	0	97	Single, Ultra-Low-Power, Open-Drain-Output Comparator with 1%-Accurate Reference
MAX972	0	97	Dual, Ultra-Low-Power, Open-Drain-Output Comparator
MAX973	0	97	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 1%-Accurate Reference
MAX974	0	97	Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 1%-Accurate Reference
MAX975	0	97	+3V/+5V Dual-Speed Comparator with Auto-Standby
MAX976	—	**3-33***	**Dual, 20ns, Low-Power, +3V/+5V Comparator**
MAX977	0	97	Dual, +3V/+5V Dual-Speed Comparator with Auto-Standby
MAX978	—	**3-33***	**Quad, 20ns, Low-Power, +3V/+5V Comparator**
MAX981	0	97	Single, Ultra-Low-Power, Open-Drain-Output Comparator with 2%-Accurate Reference
MAX982	0	97	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2%-Accurate Reference
MAX983	0	97	Dual, Ultra-Low-Power, Open-Drain-Output Comparator with 2%-Accurate Reference
MAX984	0	97	Quad, Ultra-Low-Power, Open-Drain-Output Comparator with 2%-Accurate Reference
MAX985	**1**	**3-35**	**SOT23, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX986	**1**	**3-35**	**SOT23, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output**

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MAX987	**0a**	**3-45**	**SOT23, Micropower, 120ns, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX988	**0a**	**3-45**	**SOT23, Micropower, 120ns, Rail-to-Rail I/O Comparator with Open-Drain Output**
MAX989	**1**	**3-35**	**Dual, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX990	**1**	**3-35**	**Dual, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output**
MAX991	**0a**	**3-45**	**Dual, Micropower, 120ns, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX992	**0a**	**3-45**	**Dual, Micropower, 120ns, Rail-to-Rail I/O Comparator with Open-Drain Output**
MAX993	**1**	**3-35**	**Quad, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX994	**1**	**3-35**	**Quad, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output**
MAX995	**0a**	**3-45**	**Quad, Micropower, 120ns, Rail-to-Rail I/O Comparator with Push/Pull Output**
MAX996	**0a**	**3-45**	**Quad, Micropower, 120ns, Rail-to-Rail I/O Comparator with Open-Drain Output**
MAX997	**—**	**3-57***	**+3V/+5V, High-Speed, Rail-to-Rail, 6-Pin SOT23 Comparator with Shutdown**
MAX998	**—**	**3-33***	**+3V/+5V, High-Speed, Rail-to-Rail, 6-Pin SOT23 Comparator with Shutdown**
MAX999	**—**	**3-57***	**+3V/+5V, High-Speed, Rail-to-Rail Comparator in SOT23-5**
MAX1002	**0**	**7-61**	**Dual, 6-Bit, 60Msps ADC**
MAX1002EVKIT	0	—	Evaluation Kit for the MAX1002/MAX1003
MAX1003	**0**	**7-73**	**Dual, 6-Bit, 90Msps ADC**
MAX1005	**—**	**7-85***	**Intermediate Frequency Undersampler (CODEC)**
MAX1007	**—**	**7-87***	**Mobile-Radio Analog Controller**
MAX1044	1	93	10µA Charge-Pump Voltage Converter
MAX1101	**0**	**7-89**	**Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA**
MAX1110	**1**	**7-101**	**+2.7V, Low-Power, 8-Channel, Serial ADC with Reference**
MAX1110EVKIT	0	—	Evaluation Kit for the MAX1110/MAX1112
MAX1111	**1**	**7-101**	**+2.7V, Low-Power, 4-Channel, Serial 8-Bit ADC with Reference**
MAX1112	**0**	**7-121**	**+5V, Low-Power, 8-Channel, Serial 8-Bit ADC with Reference**
MAX1113	**0**	**7-121**	**+5V, Low-Power, 4-Channel, Serial 8-Bit ADC with Reference**
MAX1114	0	97*	8-Bit, 150Msps ADC
MAX1114EVKIT	0	—	Evaluation Kit for the MAX1114
MAX1125	0	97	8-Bit, 300Msps ADC
MAX1125EVKIT	0	—	Evaluation Kit for the MAX1125
MAX1150	0	97	8-Bit, 500Msps ADC

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MAX1151	0	97	8-Bit, 750Msps ADC
MAX1150EVKIT	0	—	Evaluation Kit for the MAX1150/MAX1151
MAX1160	**0**	**7-141**	**10-Bit, 20Msps ADC**
MAX1160EVKIT	0	—	Evaluation Kit for the MAX1160/MAX1161
MAX1161	**0**	**7-149**	**10-Bit, 40Msps ADC**
MAX1170	0	97	12-Bit, 10Msps ADC
MAX1170EVKIT	0	—	Evaluation Kit for MAX1170/MAX1171/MAX1172
MAX1171	0	97	12-Bit, 20Msps ADC
MAX1172	0	97	12-Bit, 30Msps ADC
MAX1202	**1**	**7-157**	**+5V, 8-Channel, Serial, 12-Bit ADC with 3V Digital Interface**
MAX1202EVKIT	†	—	Evaluation Kit for the MAX1202/MAX1203
MAX1203	**1**	**7-157**	**+5V, 8-Channel, Serial, 12-Bit ADC with 3V Digital Interface**
MAX1204	**0**	**7-181**	**+5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface and Reference**
MAX1232	1	92	µP Monitor
MAX1240	**1**	**7-203**	**+2.7V, 12-Bit Serial ADC with Internal Reference in 8-Pin Package**
MAX1241	**1**	**7-203**	**+2.7V, Serial 12-Bit ADC**
MAX1241EVKIT	0	—	Evaluation Kit for the MAX1241
MAX1242	**1**	**7-217**	**+2.7V, 10-Bit Serial ADC with Internal Reference in 8-Pin Package**
MAX1243	**1**	**7-217**	**+2.7V, Serial 10-Bit ADC**
MAX1245	0	97	+2.375V, 8-Channel, Serial 12-Bit ADC
MAX1246	**0**	**7-229**	**+2.7V, Low-Power, 4-Channel Serial 12-Bit ADC with Internal Reference in QSOP-16 Package**
MAX1246EVKIT	1	—	Evaluation Kit for the MAX1246
MAX1247	**0**	**7-229**	**+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADC**
MAX1247EVKIT	1	—	Evaluation Kit for the MAX1247
MAX1248	**1**	**7-251**	**+2.7V, 4-Channel, Serial 10-Bit ADC with Internal Reference in QSOP-16 Package**
MAX1249	**1**	**7-251**	**+2.7V, Low-Power, 4-Channel, Serial 10-Bit ADC**
MAX1259	1	92	Battery Manager
MAX1406	0	97	±15kV ESD-Protected, EMC-Compliant, 230kbps, 3-Tx/3-Rx RS-232 IC
MAX1480A/B	1	97	Complete, Isolated RS-485/RS-422 Data Interface
MAX1482	0	96	20µA, 1/8-Unit-Load, Slew-Rate-Limited, Full-Duplex RS-485 Transceiver
MAX1483	0	96	20µA, 1/8-Unit-Load, Slew-Rate-Limited, Half-Duplex RS-485 Transceiver
MAX1487	5	—	1/4-Unit Load, Half-Duplex RS-485/RS-422 Transceiver
MAX1487E	3	97	2.5Mbps, ±15kV ESD-Protected, Low-Power, RS-485/RS-422 Transceiver
MAX1488E	0	97	±15kV ESD-Protected, Quad, Low-Power RS-232 Line Driver
MAX1489E	0	97	±15kV ESD-Protected, Quad, Low-Power RS-232 Line Receiver
MAX1490A/B	1	97	Complete, Isolated, Full-Duplex RS-485/RS-422 Data Interface ICs
MAX1600	2	97	Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network
MAX1601	1	97	Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface

†Future product. The data sheet is pending.

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MAX1602	0	97	Single-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network
MAX1603	2	97	Dual-Channel CardBus and PCMCIA VCC/VPP Power-Switching Network
MAX1604	1	97	Dual-Channel CardBus and PCMCIA Power-Switch with SMBus Serial Interface
MAX1610	0	97	Digitally Controlled CCFL Backlight Power Supply
MAX1611	0	97	Digitally Controlled CCFL Backlight Power Supply with SMBus Interface
MAX1611EVKIT	0	—	Evaluation Kit for the MAX1610/MAX1611
MAX1615	**1**	**4-95**	**High-Voltage, Low-Power Linear Regulator for Notebook Computers**
MAX1620	**0**	**4-101**	**Digitally Adjustable LCD Bias Supply**
MAX1620EVKIT	0	—	Evaluation Kit for the MAX1620/MAX1621
MAX1621	**0**	**4-101**	**Digitally Adjustable LCD Bias Supply with SMBus Interface**
MAX1624	**0**	**4-119**	**High-Speed Step-Down Controller with Synchronous Rectification for CPU Power**
MAX1624EVKIT	0	—	Evaluation Kit for the MAX1624
MAX1625	**0**	**4-119**	**High-Speed Step-Down Controller with Synchronous Rectification for CPU Power**
MAX1625EVKIT	0	—	Evaluation Kit for the MAX1625
MAX1626	0	97	100% Duty Cycle, PFM, 5V or 3.3V, Pin-Selectable, Step-Down DC-DC Controller
MAX1626EVKIT	0	—	Evaluation Kit for the MAX1626/MAX1627
MAX1627	0	97	100% Duty Cycle, PFM, 1.3V to Input Adjustable, Step-Down DC-DC Controller
MAX1630	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1630EVKIT	0	—	Evaluation Kit for the MAX1630/MAX1633
MAX1631	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1631EVKIT	0	—	Evaluation Kit for the MAX1631/MAX1634
MAX1632	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1632EVKIT	0	—	Evaluation Kit for the MAX1632/MAX1635
MAX1633	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1634	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1635	2	97	High-Efficiency, 3.3V/5V (or adj.), 12V-Output Controller for Notebooks
MAX1636	**0**	**4-143**	**Low-Voltage, Precision Step-Down Controller for Portable CPU Power**
MAX1636EVKIT	0	—	Evaluation Kit for the MAX1636
MAX1637*	—	**4-165***	**Low-Voltage, Precision, Step-Down Controller for Portable CPU Power in a QSOP**
MAX1638	—	**4-167***	**Pentium Pro/Pentium II Supply, Compatible with Intel VRM/VID Code**
MAX1638EVKIT	†	—	Evaluation Kit for the MAX1638
MAX1639	—	**4-167***	**High-Speed, Step-Down Controller with Synchronous Rectification for CPU Power**
MAX1640	**0**	**4-169**	**PWM Current Source with High-Side Sense**
MAX1640EVKIT	0	—	Evaluation Kit for the MAX1640/MAX1641

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†Future product. The data sheet is pending.

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MAX1641	**0**	**4-169**	**PWM Current Source with Low-Side Sense**
MAX1642	**0**	**4-181**	**1-Cell, High-Efficiency, Step-Up DC-DC Converter with Shutdown**
MAX1642EVKIT	0	—	Evaluation Kit for the MAX1642/MAX1643
MAX1643	**0**	**4-181**	**1-Cell, High-Efficiency, Step-Up DC-DC Converter with 2 LBI/LBOs**
MAX1647	**0**	**4-191**	**Chemistry-Independent Battery Charger with SmBus Interface**
MAX1648	**0**	**4-191**	**Chemistry-Independent Battery Charger**
MAX1649	2	96	5V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX1649EVKIT	†	—	Evaluation Kit for the MAX1649/MAX1651
MAX1651	2	96	3.3V or Adjustable, High-Efficiency, Low-Dropout, Step-Down DC-DC Controller
MAX1652	—	**4-215***	**Compact, High-Efficiency, Step-Down PWM Controller with Secondary Boost**
MAX1653	—	**4-215***	**Compact, High-Efficiency, Step-Down PWM Controller with Low-Noise Option**
MAX1653EVKIT	†	—	Evaluation Kit for the MAX1652–MAX1655
MAX1654	—	**4-215***	**Compact, High-Efficiency, Step-Down PWM Controller with Secondary Inverter**
MAX1655	—	**4-215***	**Compact, High-Efficiency, Step-Down PWM Controller with Low Output Voltage**
MAX1658	**0**	**4-217**	**350mA, Low-Dropout Linear Regulator (3.3V/Adj. Output)**
MAX1659	**0**	**4-217**	**350mA, Low-Dropout Linear Regulator (5V/Adj. Output)**
MAX1660	—	**4-227***	**Digitally Controlled Fuel-Gauge Interface**
MAX1661	—	**4-229***	**Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for N-Channel MOSFETs**
MAX1662	—	**4-229***	**Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for P-Channel MOSFETs**
MAX1663	—	**4-229***	**Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for P-Channel MOSFETs**
MAX1672	—	**4-231***	**150mA, Step-Up/Step-Down DC-DC Converter**
MAX1672EVKIT	†	—	Evaluation Kit for the MAX1672/MAX1673
MAX1673	—	**4-233***	**100mA, 350kHz, Regulated Charge-Pump DC-DC Converter**
MAX1680	**0**	**4-235**	**125mA, 250kHz, Charge-Pump DC-DC Converter**
MAX1681	**0**	**4-235**	**125mA, 1MHz Charge-Pump DC-DC Converter**
MAX1691	2	96	Integrated µP Supervisory Module with Lithium Backup Battery
MAX1700	—	**4-245***	**1-Cell to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converter with 1A Switch**
MAX1700EVKIT	†	—	Evaluation Kit for the MAX1700
MAX1701	—	**4-245***	**1-Cell to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converter with 1A Switch and Battery Monitors**
MAX1703	—	**4-247***	**1-Cell to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converter with 2A Switch**

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MAX1703EVKIT	†	—	Evaluation Kit for the MAX1703
MAX1705	**0**	**4-249**	**1-Cell to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converter with Linear Regulator and 1A Switch**
MAX1705EVKIT	0	—	Evaluation Kit for the MAX1705/MAX1706
MAX1706	**0**	**4-249**	**1-Cell to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converter with Linear Regulator and 0.5A Switch**
MAX1732	—	94	12V, 120mA Flash Memory Programmer Module
MAX1771	1	95	12V or Adjustable, High-Efficiency, Low I_Q, Step-Up DC-DC Controller
MAX1771EVKIT	1	—	Evaluation Kit for the MAX1771
MAX2003	2	96	NiCd/NiMH Battery Fast-Charge Controller
MAX2003A	2	96	NiCd/NiMH Battery Fast-Charge Controller with Pulse Trickle
MAX2003AEVKIT	2	—	Evaluation Kit for the MAX2003/MAX2003A
MAX2100 Cells	0	96	Quadrature Digitizer Circuits
MAX2101	4	96	6-Bit Quadrature Digitizer
MAX2101EVKIT	1	—	Evaluation Kit for the MAX2101
MAX2102	**0**	**10-7**	**Zero-IF Broadband I/Q Downconverter**
MAX2102EVKIT	0	—	Evaluation Kit for the MAX2102
MAX2402	1	96	800MHz to 1000MHz Spread-Spectrum Transmitter
MAX2402EVKIT	1	—	Evaluation Kit for the MAX2402
MAX2406	—	**10-21***	**Low-Cost Downconverter with Low-Noise Amplifier**
MAX2410	—	**10-23***	**Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver**
MAX2411A	—	**10-25***	**Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver**
MAX2420	—	**10-27***	**900MHz Image-Reject Transceiver with 10.7MHz IF and High-Side LO**
MAX2420EVKIT	†	—	Evaluation Kit for the MAX2420
MAX2421	—	**10-27***	**900MHz Image-Reject Transceiver with 46MHz IF and High-Side LO**
MAX2421EVKIT	†	—	Evaluation Kit for the MAX2421
MAX2422	—	**10-27***	**900MHz Image-Reject Transceiver with 70MHz IF and High-Side LO**
MAX2422EVKIT	†	—	Evaluation Kit for the MAX2422
MAX2426	—	**10-29***	**900MHz Image-Reject Transceiver with 70MHz IF and Balanced Transmit Mixer**
MAX2426EVKIT	†	—	Evaluation Kit for the MAX2426
MAX2430	0	97	900MHz, 100mW Power Amplifier/Predriver
MAX2430EVKIT	0	—	Evaluation Kit for the MAX2430
MAX2450	0	97	70MHz Quadrature Modulator/Demodulator
MAX2450EVKIT	1a	—	Evaluation Kit for the MAX2450/MAX2451/MAX2452
MAX2451	0	97	70MHz Quadrature Demodulator
MAX2452	1	97	70MHz Quadrature Modulator
MAX2452EVKIT	0	—	Evaluation Kit for the MAX2452
MAX2460	†	**10-27***	**900MHz Image-Reject Transceiver with 110MHz IF and Low-Side LO**

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MAX2460EVKIT	†	—	Evaluation Kit for the MAX2460
MAX2463	—	**10-27***	**900MHz Image-Reject Transceiver with 110MHz IF and Low-Side LO**
MAX2510	—	**10-31***	**Low-Voltage IF Transceiver with Limiter, RSSI, and Quadrature Modulator**
MAX2510EVKIT	†	—	Evaluation Kit for the MAX2510
MAX2511	**0**	**10-33**	**Low-Voltage IF Transceiver with Limiter and RSSI**
MAX2511EVKIT	0	—	Evaluation Kit for the MAX2511
MAX2601	**2**	**10-49**	**3.6V, 1W RF Power Transistor for 900MHz Applications**
MAX2602	**2**	**10-49**	**3.6V, 1W RF Power Transistor with Matched Diode for 900MHz Applications**
MAX2602EVKIT	2	—	Evaluation Kit for the MAX2601/MAX2602
MAX2611	0	97	DC-to-Microwave General-Purpose Amplifier
MAX2611PCB	1	—	Circuit Board to Evaluate MAX2611
MAX2620	**0**	**10-55**	**Low-Phase-Noise, Low-Power, 3V RF Oscillator**
MAX2620EVKIT	0	—	Evaluation Kit for the MAX2620
MAX2630	**1**	**10-63**	**VHF-to-Microwave, 3V, General-Purpose Amplifier**
MAX2631	**1**	**10-63**	**VHF-to-Microwave, 3V, General-Purpose Amplifier with Shutdown**
MAX2632	**1**	**10-63**	**VHF-to-Microwave, 3V, General-Purpose Amplifier with Bias Control**
MAX2633	**1**	**10-63**	**VHF-to-Microwave, 3V, General-Purpose Amplifier with Shutdown and Bias Control**
MAX2633PCB	†	—	Circuit Board to Evaluate MAX2630–MAX2633
MAX2650	0	97	5V, 1GHz,General-Purpose Amplifier
MAX2650PCB	†	—	Circuit Board to Evaluate MAX2650
MAX2662	—	**10-73***	**Low-Noise, Low-Voltage Upconverter**
MAX2662EVKIT	†	—	Evaluation Kit for the MAX2662
MAX2690	—	**10-75***	**High-Linearity, 400MHz to 2.5GHz, Low-Noise Downconverter Mixer**
MAX2690EVKIT	†	—	Evaluation Kit for the MAX2690
MAX3080	0	97	Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver
MAX3081	0	97	Fail-Safe, 115kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver
MAX3082	0	97	Fail-Safe, 115kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver
MAX3083	0	97	Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver
MAX3084	0	97	Fail-Safe, 500kbps, Slew-Rate-Limited, Full-Duplex RS-485/RS-422 Transceiver
MAX3085	0	97	Fail-Safe, 500kbps, Slew-Rate-Limited, Half-Duplex RS-485/RS-422 Transceiver
MAX3086	0	97	Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver
MAX3087	0	97	Fail-Safe, 10Mbps, Full-Duplex RS-485/RS-422 Transceiver

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†Future product. The data sheet is pending.

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX3088	0	97	Fail-Safe, 10Mbps, Half-Duplex RS-485/RS-422 Transceiver
MAX3089	0	97	Fail-Safe, 115kbps/500kbps/10Mbps, Half- or Full-Duplex RS-485/RS-422 Transceiver
MAX3100	**0**	**2-9**	**SPI/Microwire-Compatible UART in QSOP-16**
MAX3185	0	97	±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Motherboards/Desktop PCs
MAX3186	0	97	±15kV ESD-Protected, EMC-Compliant, 230kbps, RS-232 Serial Port for Modems
MAX3187	**0**	**2-33**	**±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktop PCs**
MAX3212	0	96	1µA, 2.7V to 3.6V, 3-Driver/5-Receiver, True RS-232 Transceiver
MAX3218	0	96	1µA, 1.8V to 4.25V RS-232 Transceiver with AutoShutdown
MAX3221	5	97	True 3V to 5.5V, RS-232 Transceiver with AutoShutdown Draws 1µA
MAX3222	4	97	300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors
MAX3223	5	97	1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown
MAX3232	4	97	300µA, 2-Driver/2-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors
MAX3237	4	97	500µA, 5-Driver/3-Receiver, True RS-232 Transceiver with 1Mbps Data Rate, Using Four 0.1µF Capacitors
MAX3238	0	97	Low-Power, 250kbps, True RS-232 Transceiver with AutoShutdown Plus
MAX3241	4	97	300µA, 3-Driver/5-Receiver, True RS-232 Transceiver Using Four 0.1µF Capacitors
MAX3243	5	97	1µA, 3V to 5.5V, True RS-232 Transceiver with AutoShutdown
MAX3243E	**1**	**2-41**	**±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown**
MAX3244	**0**	**2-59**	**1µA Supply Current, 3.0V to 5.5V, 250kbps RS-232 Transceiver with AutoShutdown Plus**
MAX3244E	**1**	**2-41**	**±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus**
MAX3245	**0**	**2-59**	**1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus**
MAX3245E	**1**	**2-41**	**±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus and 24V/µs Slew Rate**
MAX3260	0	96	1GHz Transimpedance Preamplifier with 25dB Dynamic Range
MAX3261	3	96	Single 5V, Fully Integrated, 1.2Gbps Laser Diode Driver
MAX3261EVKIT	†	—	Evaluation Kit for the MAX3261
MAX3262	1	96	1Gbps, High-Speed Limiting Amplifier with Chatter-Free Loss-of-Signal Detection
MAX3263	0	97	Single 5V, Fully Integrated, 155Mbps Laser Diode Driver
MAX3270	0	96	155Mbps/622Mbps Clock Recovery and Data Retiming IC with Fully Integrated Phase/Frequency Detector

†Future product. The data sheet is pending.

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX3320A/B/L/T	**0**	**2-41**	**3V to 5.5V, 250kbps, True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset**
MAX3480A/B	0	97	Complete, Isolated, 3.3V RS-485/RS-422 Data Interface ICs
MAX3483	0	96	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3485	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3486	0	96	3.3V, 2.5Mbps, True RS-485/RS-422 Transceiver
MAX3488	0	96	3.3V, Slew-Rate-Limited, True RS-485/RS-422 Transceiver
MAX3490	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3491	0	96	3.3V, 10Mbps, True RS-485/RS-422 Transceiver
MAX3664	0	97	622Mbps, Ultra-Low-Power, 3.3V Transimpedance Preamp for SDH/SONET
MAX3664EVKIT	0	—	Evaluation Kit for the MAX3664
MAX3675	**0a**	**11-5**	**622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier**
MAX3675EVKIT	0a	—	Evaluation Kit for the MAX3675
MAX3680	**0**	**11-19**	**+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs**
MAX3680EVKIT	0	—	Evaluation Kit for the MAX3680
MAX3681	0	97	+3.3V, 622Mbps, SDH/SONET 1:4 Deserializer with LVDS Outputs
MAX3681EVKIT	0	—	Evaluation Kit for the MAX3681
MAX3691	**0**	**11-27**	**+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs**
MAX3691EVKIT	†	—	Evaluation Kit for the MAX3691
MAX3761	1	97	Low-Power, 622Mbps Limiting Amplifier with TTL Interface and Chatter-Free Power Detect for LANs
MAX3761EVKIT	0	—	Evaluation Kit for the MAX3761
MAX3762	1	97	Low-Power, 622Mbps Limiting Amplifier with TTL Interface and Chatter-Free Power Detect for LANs
MAX3762EVKIT	0	—	Evaluation Kit for the MAX3762
MAX4005	0	96	950MHz FET-Input Buffer with 75Ω Output
MAX4012	**0**	**8-9**	**Low-Cost, SOT23, 200MHz, Single-Supply, Rail-to-Rail Op Amp**
MAX4014	**—**	**8-25***	**Low-Cost, SOT23, 200MHz, Single-Supply, Rail-to-Rail Buffer (A_V = +2V/V)**
MAX4016	**0**	**8-9**	**Low-Cost, Dual, 150MHz, Single-Supply, Rail-to-Rail Op Amp**
MAX4017	**—**	**8-25***	**Low-Cost, Dual, 150MHz, Single-Supply, Rail-to-Rail Buffer (A_V = +2V/V)**
MAX4018	**0**	**8-9**	**Low-Cost, Triple, 150MHz, Single-Supply, Rail-to-Rail Op Amp with Enable**
MAX4019	**—**	**8-25***	**Low-Cost, Triple, 150MHz, Single-Supply, Rail-to-Rail Buffer (A_V = +2V/V) with Enable**
MAX4020	**0**	**8-9**	**Low-Cost, Quad, 150MHz, Single-Supply, Rail-to-Rail Op Amp**
MAX4022	**—**	**8-25***	**Low-Cost, Quad, 150MHz, Single-Supply, Rail-to-Rail Buffer (A_V = +2V/V)**
MAX4051/A	0	97	Low-Voltage, CMOS Analog Multiplexer

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MAX4052/A	0	97	Low-Voltage, CMOS Analog Multiplexer
MAX4053/A	0	97	Low-Voltage, CMOS Analog Switch
MAX4066/A	1	—	Low-Cost, Low-Voltage, Quad SPST, CMOS Analog Switch
MAX4100	1	97	500MHz, High-Speed, Low-Power Op Amp
MAX4100EVKIT	0	—	Evaluation Kit for the MAX4100/MAX4101
MAX4101	1	97	200MHz, A_{VCL} = +2V/V, High-Speed, Low-Power Op Amp
MAX4102	0	97	250MHz, High-Speed, Low-Power, Video Op Amp
MAX4103	0	97	180MHz, A_{VCL} = +2V/V, High-Speed, Low-Power Op Amp
MAX4103EVKIT	0	—	Evaluation Kit for the MAX4102/MAX4103
MAX4106	1	97	350MHz, A_{VCL} = +5V/V, High-Speed, Ultra-Low-Noise Op Amp
MAX4106EVKIT	0	—	Evaluation Kit for the MAX4106/MAX4107
MAX4107	1	97	300MHz, A_{VCL} = +10V/V, High-Speed, Ultra-Low-Noise Op Amp
MAX4108	**2**	**8-117**	**400MHz, High-Speed, Ultra-Low-Distortion Op Amp**
MAX4108EVKIT	0	—	Evaluation Kit for the MAX4108/MAX4109
MAX4109	**2**	**8-117**	**225MHz, A_{VCL} = +2V/V, High-Speed, Ultra-Low-Distortion Op Amp**
MAX4111	0	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4112	2	97	500MHz, High-Speed, Current-Mode Feedback Op Amp
MAX4112EVKIT	1	—	Evaluation Kit for the MAX4112/MAX4113
MAX4113	2	97	275MHz, A_{VCL} = +8V/V, High-Speed, Current-Mode Feedback Op Amp
MAX4117	2	97	500MHz, A_{VCL} = +2V/V, High-Speed, Current-Mode Feedback Op Amp
MAX4117EVKIT	0	—	Evaluation Kit for the MAX4117/MAX4118
MAX4118	2	97	275MHz, A_{VCL} = +8V/V, High-Speed, Current-Mode Feedback Op Amp
MAX4119	0	97*	Quad, 270MHz, Low-Power, Current-Mode Feedback Amplifier
MAX4120	0	97*	Quad, 300MHz, Low-Power, Current-Mode Feedback Amplifier
MAX4121	0	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4121EVKIT	0	—	Evaluation Kit for the MAX4111/MAX4121
MAX4122	0	97	Single, 5MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4123	0	97	Single, 5MHz, Rail-to-Rail I/O, Single-Supply Op Amp with Shutdown
MAX4124	0	97	Single, 25MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4125	0	97	Single, 25MHz, Rail-to-Rail I/O, Single-Supply Op Amp with Shutdown
MAX4126	0	97	Dual, 5MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4127	0	97	Dual, 5MHz, Rail-to-Rail I/O, Single-Supply Op Amp with Shutdown
MAX4128	0	97	Dual, 25MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4129	0	97	Quad, 5MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4130	2	97	Single, 10MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4131	2	97	Single, 10MHz, Rail-to-Rail I/O, Single-Supply Op Amp with Shutdown
MAX4132	2	97	Dual, 10MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4133	2	97	Dual, 10MHz, Rail-to-Rail I/O, Single-Supply Op Amp with Shutdown
MAX4134	2	97	Quad, 10MHz, Rail-to-Rail I/O, Single-Supply Op Amp
MAX4135	0	97	1-Input/6-Output Video Distribution Amplifier
MAX4135EVKIT	0	—	Evaluation Kit for the MAX4135–MAX4138
MAX4136	0	97	1-Input/6-Output Video Distribution Amplifier

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MAX4137	0	97	1-Input/4-Output Video Distribution Amplifier
MAX4138	0	97	1-Input/4-Output Video Distribution Amplifier
MAX4141	0	96	330MHz, 4x1, Multiplexer/Crosspoint Building Block IC
MAX4141EVKIT	0	—	Evaluation Kit for the MAX4141
MAX4142	—	**8-27***	**High-Speed, Differential Line Driver**
MAX4144	—	**8-29***	**High-Speed Instrumentation Amplifier**
MAX4144EVKIT	1	—	Evaluation Kit for the MAX4144
MAX4145	—	**8-29***	**High-Speed, Differential Line Receiver**
MAX4146	—	**8-29***	**High-Speed Instrumentation Amplifier**
MAX4146EVKIT	†	—	Evaluation Kit for the MAX4146
MAX4147	0	97	350MHz, Low Power, High-Output-Current, Differential Line Driver
MAX4147EVKIT	0	—	Evaluation Kit for the MAX4147
MAX4158	**1**	**8-31**	**350MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4159	**1**	**8-31**	**350MHz, 2-Channel, High-Speed, Video Multiplexer/Amplifier**
MAX4159EVKIT	1	—	Evaluation Kit for the MAX4159/MAX4259
MAX4160	—	**8-47***	**350MHz, 4-Channel Video Multiplexer-Amplifier (A_V > +1V/V)**
MAX4161	—	**8-47***	**350MHz, 8-Channel Video Multiplexer-Amplifier (A_V > +1V/V)**
MAX4162	**0**	**3-59**	**SOT23, 200kHz, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4163	**0**	**3-59**	**Dual, 200kHz, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4164	**0**	**3-59**	**Quad, 200kHz, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4165	**0**	**3-71**	**SOT23, High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4166	**0**	**3-71**	**High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4167	**0**	**3-71**	**Dual, High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4168	**0**	**3-71**	**Dual, High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4169	**0**	**3-71**	**Quad, High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4172	**0**	**3-87**	**Low-Cost, Precision, High-Side Current-Sense Amplifier**
MAX4178	1	97	330MHz, Precision, Closed-Loop, Fixed Gain of +1 Buffer
MAX4178EVKIT	1	—	Evaluation Kit for the MAX4178/MAX4278
MAX4180	**1**	**8-49**	**High-Speed, 1mA, SOT23 Current-Feedback Amplifier (A_V > +2V/V)**
MAX4180EVKIT	0	—	Evaluation Kit for the MAX4180/MAX4181
MAX4181	**1**	**8-49**	**High-Speed, 1mA, SOT23 Current-Feedback Amplifier with Shutdown**
MAX4182	**1**	**8-49**	**Dual, High-Speed, 1mA, SOT23 Current-Feedback Amplifier (A_V > +2V/V)**
MAX4183	**1**	**8-49**	**Dual, High-Speed, 1mA, SOT23 Current-Feedback Amplifier with Shutdown (A_V > +2V/V)**
MAX4184	**1**	**8-49**	**Dual, High-Speed, 1mA Current-Feedback Amplifier**
MAX4185	**1**	**8-49**	**Dual, High-Speed, 1mA Current-Feedback Amplifier with Shutdown**

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX4186	1	8-49	**Quad, High-Speed, 1mA Current-Feedback Amplifier (AV > +2V/V)**
MAX4187	1	8-49	**Quad, High-Speed, 1mA Current-Feedback Amplifier with Shutdown**
MAX4188	—	8-73*	**Triple, Ultra-Low-Power Current-Feedback Amplifier with Disable (AV > +2V/V)**
MAX4189	—	8-73*	**Triple, Ultra-Low-Power Current-Feedback Amplifier with Disable (AV > +1V/V)**
MAX4189EVKIT	†	—	Evaluation Kit for the MAX4189
MAX4190	—	8-73*	**Ultra-Low-Power Current-Feedback Amplifier with Disable (AV > +2V/V)**
MAX4191	—	8-73*	**Ultra-Low-Power Current-Feedback Amplifier with Disable (AV > +1V/V)**
MAX4193	0	92	CMOS, Micropower, Step-Up Switching Regulator
MAX4200	—	8-75*	**High-Speed, 1A, Open-Loop Buffer in 5-Pin SOT23**
MAX4201	—	8-75*	**High-Speed, 1A, Open-Loop Buffer with 50Ω Output Termination**
MAX4202	—	8-75*	**High-Speed, 1A, Open-Loop Buffer with 75Ω Output Termination**
MAX4203	—	8-75*	**High-Speed, 2A, Open-Loop Buffer in 8-Pin µMAX**
MAX4204	—	8-75*	**High-Speed, 2A, Open-Loop Buffer with 50Ω Output Termination**
MAX4205	—	8-75*	**High-Speed, 2A, Open-Loop Buffer with 75Ω Output Termination**
MAX4206	—	8-77*	**High-Speed, Low-Power, Open-Loop Buffer in 5-Pin SOT23**
MAX4207	—	8-77*	**High-Speed, Low-Power, Open-Loop Buffer with 50Ω Output Termination**
MAX4208	—	8-77*	**High-Speed, Low-Power, Open-Loop Buffer with 75Ω Output Termination**
MAX4209	—	8-77*	**High-Speed, Low-Power, Open-Loop Buffer in 8-Pin µMAX**
MAX4210	—	8-77*	**Dual, High-Speed, Low-Power, Open-Loop Buffer with 50Ω Output Termination**
MAX4211	—	8-77*	**Dual, High-Speed, Low-Power, Open-Loop Buffer with 75Ω Output Termination**
MAX4212	0	8-79	**SOT23, 300MHz, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4213	0	8-79	**300MHz, Single-Supply, Rail-to-Rail I/O Op Amp with Enable**
MAX4213EVKIT	0	—	Evaluation Kit for the MAX4213
MAX4214	—	8-95*	**SOT23, 300MHz, Single-Supply, Rail-to-Rail Buffer (AV = +2V/V)**
MAX4215	—	8-95*	**SOT23, 300MHz, Single-Supply, Rail-to-Rail Buffer (AV = +2V/V) with Enable**
MAX4216	0	8-79	**Dual, 200MHz, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4217	—	8-95*	**Dual, 200MHz, Single-Supply, Rail-to-Rail Buffer (AV = +2V/V)**
MAX4218	0	8-79	**Miniature, 200MHz, Single-Supply, Rail-to-Rail Op Amp with Enable**
MAX4219	—	8-95*	**Miniature, 200MHz, Rail-to-Rail Triple Op Amp with Enable**
MAX4220	0	8-79	**Quad, 200MHz, Single-Supply, Rail-to-Rail I/O Amp**
MAX4221	2	96	330MHz Multiplexer/Crosspoint Building Block IC
MAX4221EVKIT	2	—	Evaluation Kit for the MAX4221
MAX4222	—	8-95*	**Quad, 200MHz, Single-Supply, Rail-to-Rail Buffer (AV = +2V/V)**
MAX4223	2	8-97	**1GHz, Low-Power, SOT23 Current-Feedback Amplifier with Shutdown (A_{VCL} = +1V/V)**

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX4223EVKIT	0	—	Evaluation Kit for the MAX4223/MAX4224
MAX4224	**2**	**8-97**	**600MHz, Low-Power, SOT23 Current-Feedback Amplifier with Shutdown (A_{VCL} = +2V/V)**
MAX4225	**2**	**8-97**	**Dual, 1GHz, Low-Power Current-Feedback Amplifier (A_{VCL} = +1V/V)**
MAX4226	**2**	**8-97**	**Dual, 1GHz, Low-Power Current-Feedback Amplifier with Enable (A_{VCL} = +1V/V)**
MAX4227	**2**	**8-97**	**Dual, 600MHz, Low-Power Current-Feedback Amplifier (A_{VCL} = +2V/V)**
MAX4228	**2**	**8-97**	**Dual, 600MHz, Low-Power Current-Feedback Amplifier with Enable (A_{VCL} = +2V/V)**
MAX4230	**—**	**3-95***	**SOT23, Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp**
MAX4231	**—**	**3-95***	**Dual, Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp in 8-Pin µMAX**
MAX4232	**—**	**3-95***	**Quad, Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp**
MAX4233	**—**	**3-95***	**Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp in 5-Pin SOT23**
MAX4234	**—**	**3-95***	**Dual, Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp in 8-Pin µMAX**
MAX4235	**—**	**3-95***	**Quad, Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp**
MAX4240	**—**	**3-97***	**SOT23, 1.8V, Micropower, Rail-to-Rail I/O Op Amp**
MAX4241	**—**	**3-97***	**1.8V, Micropower, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4242	**—**	**3-97***	**Dual, 1.8V, Micropower, Rail-to-Rail I/O Op Amp**
MAX4243	**—**	**3-97***	**Dual, 1.8V, Micropower, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4244	**—**	**3-97***	**Quad, 1.8V, Micropower, Rail-to-Rail I/O Op Amp**
MAX4249	**—**	**3-99***	**Dual, Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)**
MAX4250	**—**	**3-99***	**Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp**
MAX4251	**—**	**3-99***	**Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp**
MAX4252	**—**	**3-99***	**Dual, Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp**
MAX4253	**—**	**3-99***	**Dual, Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp with Shutdown**
MAX4254	**—**	**3-99***	**Quad, Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp**
MAX4255	**—**	**3-99***	**Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)**
MAX4256	**—**	**3-99***	**Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp with Shutdown (A_V > +10V/V)**
MAX4257	**—**	**3-99***	**Dual, Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)**
MAX4258	**1**	**8-31**	**250MHz, A_{VCL} = +2V/V, 2-Channel, High-Speed, Video Mux/Amp**
MAX4259	**1**	**8-31**	**250MHz, A_{VCL} = +2V/V, 2-Channel, High-Speed, Video Mux/Amp**
MAX4260	**—**	**8-47***	**250MHz, 4-Channel Video Multiplexer/Amplifier (A_V > +2V/V)**
MAX4261	**—**	**8-47***	**250MHz, 8-Channel Video Multiplexer/Amplifier (A_V > +2V/V)**
MAX4278	1	97	310MHz, Precision, Closed-Loop, Fixed Gain of +2 Buffer
MAX4278EVKIT	1	—	Evaluation Kit for the MAX4178/MAX4278

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MAX4308	**2**	**8-117**	**220MHz, Ultra-Low-Distortion Op Amp**
MAX4309	**2**	**8-117**	**200MHz, Ultra-Low-Distortion Op Amp**
MAX4310	—	**8-129***	**2-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +1V/V)**
MAX4311	—	**8-129***	**4-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +1V/V)**
MAX4312	—	**8-129***	**8-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +1V/V)**
MAX4313	—	**8-129***	**2-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +2V/V)**
MAX4314	—	**8-129***	**4-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +2V/V)**
MAX4315	—	**8-129***	**8-Channel, Single-Supply Video Multiplexer/Amplifier (A_V > +2V/V)**
MAX4330	**2**	**3-101**	**3MHz, SOT23, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4331	**2**	**3-101**	**3MHz, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4332	**2**	**3-101**	**Dual, 3MHz, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4333	**2**	**3-101**	**Dual, 3MHz, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown**
MAX4334	**2**	**3-101**	**Quad, 3MHz, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp**
MAX4391	0	92	CMOS, Micropower, Inverting Switching Regulator
MAX4420	0	94	High-Speed, 6A MOSFET Driver (Noninverting)
MAX4426	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Inverting)
MAX4427	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Noninverting)
MAX4428	0	—	Dual, High-Speed, 1.5A MOSFET Driver (Inverting & Noninverting)
MAX4429	0	94	High-Speed, 6A MOSFET Driver (Inverting)
MAX4501	0	97	Low-Voltage, SPST, Normally Open, CMOS Analog Switch
MAX4502	0	97	Low-Voltage, SPST, Normally Closed, CMOS Analog Switch
MAX4503	0	97	Low-Voltage, Dual-Supply, SPST, Normally Open, CMOS Analog Switch
MAX4504	0	97	Low-Voltage, Dual-Supply, SPST, Normally Closed, CMOS Analog Switch
MAX4514	0	97	Low-Voltage, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch
MAX4515	0	97	Low-Voltage, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch
MAX4516	0	97	Dual-Supply, Low-On-Resistance, SPST, Normally Open, CMOS Analog Switch
MAX4517	0	97	Dual-Supply, Low-On-Resistance, SPST, Normally Closed, CMOS Analog Switch
MAX4518	0	97	Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer
MAX4519	0	97	Low-Voltage, Low-On-Resistance, CMOS Analog Multiplexer
MAX4521	1	97	Quad, Low-Voltage, SPST, Normally Closed CMOS Analog Switch
MAX4522	1	97	Quad, Low-Voltage, SPST, Normally Open CMOS Analog Switch
MAX4523	1	97	Quad, Low-Voltage, SPST, Normally Open and Normally Closed CMOS Analog Switch
MAX4526	**0**	**1-21**	**Phase-Reversal Analog Switch**
MAX4527	**0**	**1-21**	**Phase-Reversal Analog Switch**
MAX4528	—	**1-33***	**Low-Voltage, Phase-Reversal Switch**

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX4530	0	1-35	Low-Voltage, 8-Channel Analog Multiplexer with Enable Inputs and Address Latching
MAX4531	0	1-35	Low-Voltage, Dual 4-Channel, Analog Multiplexer with Enable Inputs and Address Latching
MAX4532	0	1-35	Low-Voltage, Triple SPDT, Analog Switch
MAX4536	0	1-51	Quad, Low-Voltage, SPST, Normally Open Analog Switch with Enable
MAX4537	0	1-51	Quad, Low-Voltage, SPST, Normally Closed Analog Switch with Enable
MAX4538	0	1-51	Quad, Low-Voltage, SPST, Normally Open and Normally Closed Analog Switch with Enable
MAX4541	0	1-63	Low-Voltage, Single-Supply, Dual, Normally Open SPST Analog Switch
MAX4542	0	1-63	Low-Voltage, Single-Supply, Dual, Normally Closed SPST Analog Switch
MAX4543	0	1-63	Low-Voltage, Single-Supply, Dual, Normally Open and Normally Closed SPST Analog Switch
MAX4544	0	1-63	Low-Voltage, Single-Supply, SPDT Analog Switch
MAX4545	0	1-75	Quad, Low-Voltage, SPST, Normally Open, Bidirectional RF/Video Switch
MAX4546	0	1-75	Quad, Low-Voltage, SPST, Normally Open and Normally Closed, Bidirectional RF/Video Switch
MAX4547	0	1-75	Dual, Low-Voltage, SPDT, Bidirectional RF/Video Switch
MAX4554	—	1-91*	3PST Force-Sense Switch
MAX4555	—	1-91*	4SPST Force-Sense Switch
MAX4556	—	1-91*	3SPDT Force-Sense Switch
MAX4565	0	1-93	Quad, Low-Voltage, SPST, Normally Open, Bidirectional RF/Video Switch
MAX4566	0	1-93	Quad, Low-Voltage, SPST, Normally Open and Normally Closed, Bidirectional RF/Video Switch
MAX4567	0	1-93	Dual, Low-Voltage, SPDT, Bidirectional RF/Video Switch
MAX5012	0	9-49	12-Bit, 100Msps ECL DAC
MAX5013	0	9-55	12-Bit, 100Msps TTL DAC
MAX5018	0	9-61	165/275Msps Video DAC with Controls
MAX5140	1	9-73	400Msps High-Resolution Video DAC with Controls
MAX5150	0	9-85	+5V, 13-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package
MAX5151	0	9-85	+3V, 13-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package
MAX5152	—	9-101*	+5V, 13-Bit, Serial, Voltage-Output (Force/Sense) Dual DAC in QSOP-16 Package
MAX5153	—	9-101*	+3V, 13-Bit, Serial, Voltage-Output (Force/Sense) Dual DAC in QSOP-16 Package
MAX5154	—	9-103*	+5V, 12-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package
MAX5155	—	9-103*	+3V, 12-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package
MAX5156	—	9-105*	+5V, 12-Bit, Serial, Voltage-Output (Force/Sense) Dual DAC in QSOP-16 Package

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX5157	—	**9-105***	**+3V, 12-Bit, Serial, Voltage-Output (Force/Sense) Dual DAC in QSOP-16 Package**
MAX5158	—	**9-107***	**+5V, 10-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package**
MAX5159	—	**9-107***	**+3V, 10-Bit, Serial, Voltage-Output Dual DAC in QSOP-16 Package**
MAX5250	**0**	**9-109**	**Low-Power, Quad, 10-Bit, Voltage-Output DAC with Serial Interface**
MAX5251	**0**	**9-125**	**+3V, Quad, 10-Bit, Voltage-Output DAC with Serial Interface**
MAX5253	0	97	3V, Quad, 12-Bit, Voltage-Output DAC with Serial Interface
MAX5351	**1**	**9-7**	**+3.3V, Single-Supply, 13-Bit, Voltage-Output DAC with Serial Interface**
MAX5352	**0**	**9-141**	**+5V, Single-Supply, 12-Bit, Voltage-Output DAC with Serial Interface**
MAX5353	**0**	**9-141**	**+3.3V, Single-Supply, 12-Bit, Voltage-Output DAC with Serial Interface**
MAX5354	**1**	**9-157**	**+5V, Single-Supply, 10-Bit, Voltage-Output DAC**
MAX5355	**1**	**9-157**	**+3.3V, Single-Supply, 10-Bit, Voltage-Output DAC**
MAX6120	1	97	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference
MAX6125	**0**	**6-5**	**2.5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23**
MAX6141	**0**	**6-5**	**4.096V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23**
MAX6145	**0**	**6-5**	**4.5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23**
MAX6150	**0**	**6-5**	**5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23**
MAX6160	**0**	**6-5**	**Adjustable-Output, Low-Dropout, Micropower, 3-Terminal Voltage Reference**
MAX6225	2a	97	Low-Drift, Low-Noise, 2.5V Precision Voltage Reference
MAX6241	2a	97	Low-Drift, Low-Noise, 4.096V Precision Voltage Reference
MAX6250	2a	97	Low-Drift, Low-Noise, 5.0V Precision Voltage Reference
MAX6301	0	97	5V, Low-Power µP Supervisory IC with Active-Low, Adjustable Reset
MAX6302	0	97	5V, Low-Power µP Supervisory IC with Active-High, Adjustable Reset
MAX6303	0	97	5V, Low-Power µP Supervisory IC with Push-Pull Reset
MAX6304	0	97	5V, Low-Power µP Supervisory IC with Active-High, Push-Pull Reset
MAX6305	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Open-Drain $\overline{\text{RESET}}$ Output
MAX6306	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Manual-Reset Input
MAX6307	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Overvoltage Protection
MAX6308	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull $\overline{\text{RESET}}$ Output
MAX6309	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull $\overline{\text{RESET}}$ Output and Manual-Reset Input
MAX6310	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull $\overline{\text{RESET}}$ Output and Overvoltage Protection

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX6311	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull RESET Output
MAX6312	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull RESET Output and Manual-Reset Input
MAX6313	0	97	5-Pin, Multiple-Input, Programmable Reset IC with Push/Pull RESET Output and Overvoltage Protection
MAX6314	0	97	68HC11/Bidirectional-Compatible µP Reset Circuit
MAX6315	0	97	Open-Drain SOT µP Reset Circuit
MAX6316	—	**5-7***	**5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$ and Push/Pull $\overline{\text{RESET}}$ Output or Bidirectional $\overline{\text{RESET}}$ Output**
MAX6317	—	**5-7***	**5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$ and Push/Pull RESET Output**
MAX6318	—	**5-7***	**5-Pin µP Supervisory Circuit with Watchdog, Push/Pull RESET and Push/Pull $\overline{\text{RESET}}$ Output or Bidirectional $\overline{\text{RESET}}$ Output**
MAX6319	—	**5-7***	**5-Pin µP Supervisory Circuit with Manual $\overline{\text{RESET}}$, Push/Pull RESET and Push/Pull $\overline{\text{RESET}}$ Output or Bidirectional $\overline{\text{RESET}}$ Output**
MAX6320	—	**5-7***	**5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$, and Open-Drain $\overline{\text{RESET}}$ Output**
MAX6321	—	**5-7***	**5-Pin µP Supervisory Circuit with Watchdog, Open-Drain $\overline{\text{RESET}}$, and Push/Pull RESET Output**
MAX6322	—	**5-7***	**5-Pin µP Supervisory Circuit with Manual $\overline{\text{RESET}}$, Open-Drain $\overline{\text{RESET}}$, and Push/Pull RESET Output**
MAX6325	**0**	**6-13**	**1ppm/°C, Low-Noise, +2.5V Voltage Reference**
MAX6326	—	**5-9***	**3-Pin, Ultra-Low-Power µP Reset Circuit with Push/Pull $\overline{\text{RESET}}$ Output**
MAX6327	—	**5-9***	**3-Pin, Ultra-Low-Power µP Reset Circuit with Push/Pull RESET Output**
MAX6328	—	**5-9***	**3-Pin, Ultra-Low-Power µP Reset Circuit with Open-Drain $\overline{\text{RESET}}$ Output**
MAX6330L/S/T	—	**5-11***	**µP Reset Circuit with Shunt Regulator in 3-Pin SOT23 with $\overline{\text{RESET}}$ Output**
MAX6331L/S/T	—	**5-11***	**µP Reset Circuit with Shunt Regulator in 3-Pin SOT23 with RESET Output**
MAX6341	**0**	**6-13**	**1ppm/°C, Low-Noise, +4.096V Voltage Reference**
MAX6350	**0**	**6-13**	**1ppm/°C, Low-Noise, +5V Voltage Reference**
MAX6501	**0**	**5-13***	**Low-Cost, +2.7V to +5.5V, Micropower SOT Temperature-Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Hot Temp. Threshold**
MAX6502	**0**	**5-13***	**Low-Cost, +2.7V to +5.5V, Micropower SOT Temperature-Reset IC with Push/Pull RESET Output and Hot Temp. Threshold**
MAX6503	**0**	**5-13***	**Low-Cost, +2.7V to +5.5V, Micropower SOT Temperature-Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Cold Temp. Threshold**
MAX6504	**0**	**5-13***	**Low-Cost, +2.7V to +5.5V, Micropower SOT Temperature-Reset IC with Push/Pull RESET Output and Cold Temp. Threshold**

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX6520	0	97	Low-Cost, Micropower, Precision 3-Terminal, 1.2V Voltage Reference
MAX7219	**3**	**12-5**	**Serially Interfaced, 8-Digit, LED Display Driver**
MAX7221	**3**	**12-5**	**Serially Interfaced, 8-Digit, LED Display Driver with Slew-Rate-Limited Segment Drivers**
MAX7231	0	—	8-Digit, Triplexed LCD Decoder/Driver
MAX7232	0	—	10-Digit, Triplexed LCD Decoder/Driver
MAX7233	0	—	4-Character, Triplexed LCD Decoder/Driver
MAX7234	0	—	5-Character, Triplexed LCD Decoder/Driver
MAX7624	1	—	Improved MX7524
MAX7645	1	—	Improved MX7545
MAX7705	0	—	µP Power-Supply Monitor with Reset
MAX8211	3	—	µP Voltage Monitor with Programmable Voltage Detection
MAX8212	3	—	µP Voltage Monitor with Programmable Voltage Detection
MAX8213	1	—	Five Universal Voltage Monitors, Complete µP Voltage Monitoring
MAX8214	1	—	Five Universal Voltage Monitors with Active Pull-Ups
MAX8215	0	—	±5V, ±12V Dedicated µP Voltage Monitor
MAX8216	0	—	±5V, ±12V Dedicated µP Voltage Monitor
MAX8862	0	97	Low-Cost, Low-Dropout, Dual Linear Regulator (250mA/100mA)
MAX8863	0	97	120mA LDO Linear Regulator in SOT23
MAX8864	0	97	120mA LDO Linear Regulator in SOT23 with C_{OUT} Discharge
MAX8865	0	97	Dual, Low-Dropout, 100mA Linear Regulator
MAX8866	0	97	Dual, Low-Dropout, 100mA Linear Regulator with Auto-Discharge
MAX8867	—	**4-267***	**Low-Noise, Low-Dropout, 160mA Linear Regulator in SOT23**
MAX8868	—	**4-267***	**Low-Noise, Low-Dropout, 160mA Linear Regulator in SOT23 with C_{OUT} Discharge**
MAX8873	**0**	**4-269**	**Low-Dropout, 120mA Linear Regulator in SOT23 with LP2980 Pinout**
MAX8874	**0**	**4-269**	**Low-Dropout, 120mA Linear Regulator in SOT23 with LP2980 Pinout and C_{OUT} Discharge**
MAX8877	—	**4-277***	**Low-Noise, Low-Dropout, 160mA Linear Regulator in SOT23 with LP2982 Pinout**
MAX8878	—	**4-277***	**Low-Noise, Low-Dropout, 160mA Linear Regulator in SOT23 with LP2982 Pinout and C_{OUT} Discharge**
MAX9000	—	**3-117***	**Low-Power, 1MHz Op Amp + Comparator + Reference**
MAX9001	—	**3-117***	**Low-Power, 1MHz Op Amp + Comparator + Reference, with Shutdown**
MAX9002	—	**3-117***	**Low-Power, 8MHz Op Amp (A_V = +10V/V) + Comparator + Reference**
MAX9003	—	**3-117***	**Low-Power, 8MHz Op Amp (A_V = +10V/V) + Comparator + Reference, with Shutdown**
MAX9004	—	**3-117***	**Low-Power, 1MHz Op Amp + Comparator + Reference**
MAX9005	—	**3-117***	**Low-Power, 8MHz Op Amp (A_V = +10V/V) + Comparator + Reference**
MAX9685	1	—	Ultra-Fast ECL-Output Comparator with Latch Enable
MAX9686	0	—	Single, Very-Fast TTL-Latched Output Comparator
MAX9687	1	—	Dual, Ultra-Fast ECL-Output Comparator

*The data sheet that appears in this book is Advance Information (first page of a data sheet in preparation).

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A Complete Product Listing

Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MAX9690	2	—	Ultra-Fast ECL-Output Comparator
MAX9698	0	—	Dual, Very-Fast, TTL-Latched Output Comparator
MAXC001	0	—	150µF, Low-ESR Aluminum Electrolytic Capacitor
MAXL001	0	92	100µH Toroid Inductor
MF10	1	—	Dual, Second-Order, Universal Switched-Capacitor Filter
MX536A	1	—	True RMS-to-DC Converter
MX565A	0	—	High-Speed, 12-Bit, Monolithic DAC with Voltage Reference
MX566A	0	—	High-Speed, 12-Bit, Monolithic DAC
MX574A	2	—	Industry-Standard, Complete 12-Bit ADC
MX580	1	—	Precision 2.5V Voltage Reference
MX581	1	—	Precision 10V Voltage Reference
MX584	1	—	Pin-Programmable 10V, 7.5V, 5V, 2.5V, Precision Voltage Reference
MX636	1	—	True RMS-to-DC Converter
MX674A	2	—	Industry-Standard, Complete, 12-Bit ADC
MX7224	2	—	CMOS, Double-Buffered, 8-Bit Voltage-Output DAC
MX7225	1	—	CMOS, Quad, 8-Bit DAC with Voltage Outputs
MX7226	1	—	CMOS, Quad, 8-Bit DAC with Voltage Outputs
MX7228	0	—	CMOS, Octal, 8-Bit DAC
MX7245	0	—	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7248	0	—	Complete, 12-Bit, Voltage-Output Multiplying DAC
MX7501	0	—	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7502	0	—	Differential, 4-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7503	0	—	8-Channel, Low-Power, Monolithic, CMOS Multiplexer
MX7506	0	—	Monolithic CMOS Multiplexer
MX7507	0	—	Monolithic CMOS Multiplexer
MX7520	1	—	CMOS, 10-Bit Multiplying DAC
MX7521	1	—	CMOS, 12-Bit Multiplying DAC
MX7523	0	—	CMOS, 8-Bit Multiplying DAC
MX7524	1	—	CMOS, Buffered, 8-Bit Multiplying DAC
MX7528	3	—	CMOS, Dual, Buffered, 8-Bit Multiplying DAC
MX7530	1	—	CMOS, 10-Bit Multiplying DAC
MX7531	1	—	CMOS, 12-Bit Multiplying DAC
MX7533	1	—	CMOS, Low-Cost, 10-Bit Multiplying DAC
MX7534	1	—	µP-Compatible, 14-Bit DAC
MX7535	1	—	µP-Compatible, 14-Bit DAC
MX7536	0	—	µP-Compatible, 14-Bit DAC
MX7537	1	—	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7538	1	—	CMOS, µP-Compatible, 14-Bit DAC
MX7541/A	2	—	CMOS, 12-Bit Multiplying DAC
MX7542	1	—	CMOS, 12-Bit, µP-Compatible DAC
MX7543	2	—	CMOS, 12-Bit, Serial-Input DAC
MX7545/A	1	—	CMOS, Buffered, 12-Bit Multiplying DAC

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Part	Current DS Rev. No.	Data Book Year / 98 Book Page No.	Description
MX7547	1	—	CMOS, Parallel-Loading, Dual, 12-Bit Multiplying DAC
MX7548	0	—	CMOS, Parallel-Interface, 12-Bit DAC
MX7549	1	—	CMOS, Dual, Double-Buffered, 12-Bit, µP-Compatible DAC
MX7572	0	92	CMOS, Complete, High-Speed, 12-Bit ADC
MX7574/A	0	—	CMOS, µP-Compatible, 8-Bit ADC
MX7575	1	—	CMOS, µP-Compatible, 5µs, 8-Bit ADC
MX7576	1	—	CMOS, µP-Compatible, 10µs, 8-Bit ADC
MX7578	0	—	Calibrated, 12-Bit ADC
MX7581	1	—	CMOS, 8-Bit, 8-Channel Data-Acquisition System
MX7582	1	—	Calibrated, 4-Channel, 12-Bit ADC
MX7628	3	—	CMOS, Dual, Buffered, 8-Bit, Multiplying DAC
MX7672	0	—	High-Speed 12-Bit ADC with External Reference Input
MX7820	1	—	CMOS, 1.3µs, 8-Bit ADC with Track/Hold
MX7821	1	92	µP-Compatible, 660ns, 8-Bit ADC with Track/Hold
MX7824	2	—	CMOS, High-Speed, 8-Bit ADC with 4-Channel Multiplexer
MX7828	2	—	CMOS, High-Speed, 8-Bit ADC with 8-Channel Multiplexer
MX7837	0	—	Complete, Dual, 12-Bit Multiplying DAC with 8-Bit Bus Interface
MX7845	0	—	Complete, 12-Bit Multiplying DAC
MX7847	0	—	Complete, Dual, 12-Bit Multiplying DAC with 12-Bit Bus Interface
MXD1210	1	—	Nonvolatile RAM Controller
MXL1001	1	—	Low-Offset, Precision Op Amp
MXL1007	1	—	Low-Noise, Precision Op Amp
MXL1013	2	—	Dual, Precision Op Amp
MXL1014	2	—	Quad, Precision Op Amp
MXL1016	2	—	Ultra-Fast, Precision TTL Comparator
MXL1028	1	—	Ultra-Low-Noise, High-Speed Precision Op Amp
MXL1062	3	—	5th-Order, Zero-Error, Butterworth, Switched-Capacitor Lowpass Filter
MXL1074	3	—	5A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1076	3	—	2A, Step-Down, PWM, Switch-Mode DC-DC Regulator
MXL1116	2	—	Ultra-Fast, Single-Supply, Precision TTL Comparator
MXL1178	1	—	Dual, Single-Supply, Micropower, Precision Op Amp
MXL1179	1	—	Quad, Single-Supply, Micropower, Precision Op Amp
MXT429	0	—	High-Speed, 6A MOSFET Driver (Inverting)
OP07	1	—	Precision Op Amp
OP27	0	—	Low-Noise, Precision Op Amp
OP37	0	—	Low-Noise, Precision Op Amp
OP90	0	—	Precision, Low-Voltage, Micropower Op Amp
REF01	0	—	Precision, 10V Voltage Reference
REF02	0	—	Precision, 5V Voltage Reference
Si7661	1	—	CMOS, Switched-Capacitor Voltage Converter (Up to 20V Input)
TSC426	1	—	Dual-Power MOSFET Driver (Inverting)
TSC427	1	—	Dual-Power MOSFET Driver (Noninverting)
TSC428	1	—	Dual-Power MOSFET Driver (Inverting and Noninverting)

MAXIM

Analog Multiplexers/Switches

Analog Multiplexers/Switches, Product Tables and Trees 1-2

MAX336	16-Channel, Low-Leakage, CMOS Analog Multiplexer	1-9
MAX337	Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexer	1-9
MAX4526	Phase-Reversal Analog Switch	1-21
MAX4527	Phase-Reversal Analog Switch	1-21
MAX4528	Low-Voltage, Phase-Reversal Switch	1-33*
MAX4530	Low-Voltage, 8-Channel, CMOS Analog Mux with Enable Inputs and Address Latching	1-35
MAX4531	Low-Voltage, Dual 4-Channel, CMOS Analog Mux with Enable Inputs and Address Latching	1-35
MAX4532	Low-Voltage, CMOS Analog SPDT Switch with Enable Inputs and Address Latching	1-35
MAX4536	Quad, Low-Voltage, SPST, Normally Open Analog Switch with Enable	1-51
MAX4537	Quad, Low-Voltage, SPST, Normally Closed Analog Switch with Enable	1-51
MAX4538	Quad, Low-Voltage, SPST Analog Switch	1-51
MAX4541	Low-Voltage, Single-Supply, Dual SPST, Normally Open Analog Switch	1-63
MAX4542	Low-Voltage, Single-Supply, Dual SPST, Normally Closed Analog Switch	1-63
MAX4543	Low-Voltage, Single-Supply, Dual SPST Analog Switch	1-63
MAX4544	Low-Voltage, Single-Supply, Dual SPDT Analog Switch	1-63
MAX4545	Quad, Low Voltage, SPST, Normally Open, Bidirectional RF/Video Switch	1-75
MAX4546	Quad, Low-Voltage, SPST, Normally Open and Normally Closed, Bidirectonal RF/Video Switch	1-75
MAX4547	Dual, Low-Voltage, SPDT, Bidirectional RF/Video Switch	1-75
MAX4554	3PST Force-Sense Switch	1-91*
MAX4555	4SPST Force-Sense Switch	1-91*
MAX4556	3SPDT Force-Sense Switch	1-91*
MAX4565	Quad, SPST, NO, Low-Voltage, Bidirectional RF/Video Switch	1-93
MAX4566	Quad, SPST, NO/NC, Low-Voltage, Bidirectional RF/Video Switch	1-93
MAX4567	Dual, SPDT, Low-Voltage, Bidirectional RF Video Switch	1-93

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*Advance Information–first page of a data sheet in preparation.

Analog Switches

SPST

6Ω & 30Ω
† MAX4555

10Ω
MAX312 (quad)
MAX313 (quad)
MAX314 (quad)

20Ω or 25Ω
MAX4514‡ (single)
MAX4515‡ (single)
MAX4516‡ (single)
MAX4517‡ (single)
IH5048A (dual)

30Ω or 35Ω
MAX320‡ (dual)
MAX321‡ (dual)
MAX322‡ (dual)
MAX323‡ (dual)
MAX324‡ (dual)
MAX325‡ (dual)
MAX351 (quad)
MAX352 (quad)
MAX353 (quad)
MAX381‡ (dual)
MAX391‡ (quad)
MAX392‡ (quad)
MAX393‡ (quad)
MAX4066‡ (quad)
MAX4066A‡ (quad)
★ MAX4541‡ (dual)
★ MAX4542‡ (dual)
★ MAX4543‡ (dual)
DG411 (quad)
DG412 (quad)
DG413 (quad)

45Ω
MAX301 (dual)
MAX317 (single)
MAX318 (single)
DG401 (dual)
DG417 (single)
DG418 (single)
DG421 (dual, latch)
IH5048 (dual)

50Ω or 55Ω
MAX334 (quad)
DG300A (dual)
DG304A (dual)
DG381A (dual)
HI-201HS (quad)

70Ω or 75Ω
DG200A (dual)
IH5140 (single)
IH5141 (dual)

80Ω to 90Ω
MAX361 (quad)
MAX362 (quad)
MAX364 (quad)
MAX365 (quad)
† MAX4529
DG441 (quad)
DG442 (quad)
DG444 (quad)
DG445 (quad)
HI-201 (quad)
IH5040 (single)
IH5041 (dual)

100Ω or 110Ω
MAX4521‡ (quad)
MAX4522‡ (quad)
MAX4523‡ (quad)
★ MAX4536‡ (quad)
★ MAX4537‡ (quad)
DG308A (quad)
DG309 (quad)

175Ω or 200Ω
DG201A (quad)
DG202 (quad)
DG211 (quad)
DG212 (quad)

250Ω
MAX4501‡ (single)
MAX4502‡ (single)
MAX4503‡ (single)
MAX4504‡ (single)

SPDT

6Ω & 60Ω
† MAX4554
† MAX4556

35Ω
MAX333A (quad)
MAX383‡ (dual)
MAX394‡ (quad)
★ MAX4544‡

45Ω
MAX303 (dual)
MAX319 (single)
DG403 (dual)
DG419 (single)
DG423 (dual, latch)
IH5050 (single)
IH5051 (dual)

50Ω
DG301A (single)
DG303A (dual)
DG305A (single)
DG307A (dual)
DG387A (single)
DG390A (dual)

75Ω
★ MAX4532 (triple)
★ MAX4538‡ (triple)
IH5142 (single)
IH5143 (dual)

80Ω/100Ω
MAX4053/A (triple)
IH5042 (single)
IH5043 (dual)

175Ω
MAX333 (quad)

DPST

35Ω
MAX385‡ (dual)

45Ω
MAX305 (dual)
DG405 (dual)
DG425 (dual, latch)
IH5049 (dual)

50Ω
DG302A (dual)
DG306A (dual)
DG384A (dual)

75Ω
IH5144 (single)
IH5145 (dual)

80Ω
IH5044 (single)
IH5045 (dual)

8 x SPST*
MAX335 (octal)
MAX395‡ (octal)

4PST

75Ω
IH5047 (single)

Video/RF

SPST
† MAX4529

Dual SPST
IH5341 (dual)

Quad SPST
★ MAX4545
★ MAX4565
IH5352

Dual SPDT
★ MAX4546
★ MAX4547
★ MAX4566
★ MAX4567

Low Leakage

SPST
MAX326 (quad)
MAX327 (quad)

Signal-Line Circuit Protector

3-Line
MAX366

8-Line
MAX367

Phase-Reversal Switches
★ MAX4526
★ MAX4527
† MAX4528

Force-Sense Switches
† MAX4554
† MAX4555
† MAX4556

★ New product
† Future product
‡ Guaranteed operation at 2.7V

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$/ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	t_{ON} (ns max)	t_{OFF} (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
SPST											
MAX4514/15	SPST NO/NC	20	1	–	–	150	100	8-SO, 5-SOT23	+2 to +12	Low on-resistance, smallest package	0.47
MAX4516/17	SPST NO/NC	20	1	–	–	100	75	8-SO, 5-SOT23	±1 to ±6	Low on-resistance, smallest package	0.47
MAX317/18	SPST NC/NO	45	0.25	–	3	175	145	8-DIP/SO	±4.5 to ±20	Improved DG417, low R_{ON} match and flatness	0.96
DG417/18	SPST NC/NO	45	0.25	–	4	175	145	8-DIP/SO	±4.5 to ±20		0.96
IH5140	SPST NO	75	1	–	–	150	125	16-DIP/SO	±4.5 to ±20		2.89
IH5040	SPST NO	80	5	–	–	400	200	16-DIP/SO	±4.5 to ±20		2.06
MAX4501/2	SPST NO/NC	250	1	–	–	75	50	8-SO, 5-SOT23	+2 to +12	Low voltage, smallest package	0.42
MAX4503/4	SPST NO/NC	250	1	–	–	150	100	8-SO, 5-SOT23	±1 to ±6	Low voltage, smallest package	0.42
MAX4555	2 SPST	6	0.25	1	1.5	225	185	16-DIP/SO/SSOP	±15 to ±20	Low R_{ON} (force)	††
	2 SPST	30	0.25	4.5	6.0	225	185	16-DIP/SO/SSOP	±15 to ±20	Medium R_{ON} (sense)	
IH5048A	2 SPST NO	25	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20	Low power, low R_{ON}	4.49
MAX320/1	2 SPST NO/NC	35	0.1	2	4	150	100	8-DIP/SO/µMAX	±2.7 to ±8	Low voltage, low on-resistance	0.89
MAX322	2 SPST NO, NC	35	0.1	2	4	150	100	8-DIP/SO/µMAX	±2.7 to ±8	Low voltage, low on-resistance	0.89
MAX381	2 SPST NO	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply, +2.7V to +16V	1.23
MAX301	2 SPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG401, low R_{ON} match and flatness	1.23
DG401	2 SPST NO	45	0.5	2	3	150	100	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.23
DG421	2 SPST NO	45	0.25	3	4	250	200	16-DIP/SO	±4.5 to ±20	Low power, high speed, has latches	1.59
IH5048	2 SPST NO	45	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20	Low power, low R_{ON}	4.49
DG300A	2 SPST NC	50	1	–	–	300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	1.94
DG304A	2 SPST NC	50	1	–	–	250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.18
DG381A	2 SPST NO	50	1	–	–	300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.08
MAX323/4	2 SPST NO/NC	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2.7 to +16	Single supply, +2.7V/+5V	0.89
MAX325	2 SPST NO, NC	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2.7 to +16	Single supply, +2.7V/+5V	0.89
MAX4541/2	2 SPST NO/NC	60	0.1	2	6	150	75	8-DIP/SO/µMAX	+2 to +12	Low-cost MAX323/MAX324	0.41
MAX4543	2 SPST NO, NC	60	0.1	2	6	150	100	8-DIP/SO/µMAX	+2 to +12	Low-cost MAX325	0.41
DG200A	2 SPST NC	70	2	–	–	1000	500	14-DIP/SO	±4.5 to ±20		0.93
IH5141	2 SPST NO	75	1	–	–	150	125	16-DIP/SO	±4.5 to ±20		3.23
IH5041	2 SPST NC	80	1	–	–	400	200	16-DIP/SO	±4.5 to ±20		1.84
MAX312/13	4 SPST NC/NO	10	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low on-resistance	2.49
MAX314	4 SPST NO, NC	10	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low on-resistance	2.49
MAX351/2	4 SPST NC/NO	35	0.25	2	3	175	145	16-DIP/SO	±4.5 to ±20	Improved DG411/DG412, low R_{ON} match and flatness	1.76
MAX353	4 SPST NO, NC	35	0.25	2	3	175	145	16-DIP/SO	±4.5 to ±20	Improved DG413, low R_{ON} match and flatness	1.76
MAX391/2	4 SPST NC/NO	35	0.1	2	4	130	75	16-DIP/SO	±2.7 to ±8	Single supply, +3V/+5V/+12V	1.87
MAX393	4 SPST NO, NC	35	0.1	2	4	130	75	16-DIP/SO	±2.7 to ±8	Single supply, +3V/+5V/+12V	1.87
MAX4066A	4 SPST NO	35	0.1	2	4	130	75	14-DIP/SO	+2.7 to +16	Low leakage	1.87
DG411/12	4 SPST NC/NO	35	0.25	2	4	175	145	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.85
DG413	4 SPST NO, NC	35	0.25	3	4	175	145	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	1.85
MAX4066	4 SPST	45	1	4	6	130	75	14-DIP/SO, 16-QSOP	+2.7 to +16	Low voltage, 74HC4066 upgrade	0.99
MAX334	4 SPST NC	50	1	–	–	100	50	16-DIP/SO	±4.5 to ±20	High speed, low on-resistance	2.88
HI-201HS	4 SPST NC	50	1	–	–	50	50	16-DIP/SO	±4.5 to ±20	Low R_{ON}, high speed	2.64
HI-201	4 SPST NC	80	5	–	–	400	300	16-DIP/SO	±4.5 to ±20	Low R_{ON}	2.00
MAX361/2	4 SPST NC/NO	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG441/DG442, low R_{ON} match and flatness	1.29
MAX364/5	4 SPST NC/NO	85	0.5	2	5	250	120	16-DIP/SO	±4.5 to ±20	Improved DG444/DG445, low R_{ON} match and flatness	1.03
DG441/2	4 SPST NC/NO	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.29
DG444/5	4 SPST NC/NO	85	0.5	4	9	250	120	16-DIP/SO	±4.5 to ±20		1.03
MAX4521/2	4 SPST NC/NO	100	1	4	12	80	30	16-DIP/SO/QSOP	+2 to +12	Improved, low-voltage DG211/DG212 replacement	0.69
MAX4523	4 SPST	100	1	4	12	80	30	16-DIP/SO/QSOP	+2 to +12	Improved, low-voltage DG213 replacement	0.69
MAX4536/7	4 SPST NO/NC	100	1	4	10	100	50	16-DIP/SO/QSOP	+2 to +12	Improved 74HC4316 with enable	0.98
MAX4538	4 SPST NO, NC	100	1	4	10	100	50	16-DIP/SO/QSOP	+2 to +12	Improved 74HC4316 with enable	0.98

[1] NO = Normally Open, NC = Normally Closed

[2] Drain-source on-resistance is for the commercial grade, T_A = +25°C.

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$/ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	t_{ON} (ns max)	t_{OFF} (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
DG211/12	4 SPST NC/NO	175	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20	No V_{LOGIC} supply	0.91
DG201A/2	4 SPST NC/NO	200	1	–	–	600	450	16-DIP/SO	±4.5 to ±20	Low power, no V_{LOGIC} supply	0.95
MAX326/7	4 SPST NC/NO	3500	0.01	–	–	1000	500	16-DIP/SO	±4.5 to ±20	Ultra-low leakage, low charge injection	2.78
MAX395	8 SPST	100	1	4	–	400	400	24-DIP/SO/SSOP	±2.7 to ±8	Low voltage, serial interface	2.98
MAX335	8 SPST	175	1	–	–	400	400	24-DIP/SO	±4.5 to ±20	Serial interface with break-before-make	2.84
SPDT											
MAX319	SPDT	45	0.25	2	3	175	145	8-DIP/SO	±4.5 to ±20	Improved DG419, low R_{ON} match and flatness	1.19
DG419	SPDT	45	0.25	3	4	175	145	8-DIP/SO	±4.5 to ±20		1.19
IH5050	SPDT	45	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20		3.94
DG301A	SPDT	50	1	–	–	300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	1.94
DG305A	SPDT	50	1	–	–	250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.55
DG387A	SPDT	50	1	–	–	300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.08
MAX4544	SPDT	60	0.1	2	6	150	100	8-DIP/SO, 6-SOT23	+2 to +12	Low-cost SOT23-6	0.41
IH5142	SPDT	75	1	–	–	200	125	16-DIP/SO	±4.5 to ±20		3.23
IH5042	SPDT	80	5	–	–	400	200	16-DIP/SO	±4.5 to ±20		1.84
MAX383	2 SPDT	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply (+2.7V to +16V)	2.57
MAX303	2 SPDT	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG403, low R_{ON} match and flatness	2.57
DG403	2 SPDT	45	0.5	2	3	150	100	16-DIP/SO	±4.5 to ±20	Low power, high speed, low leakage	2.57
DG423	2 SPDT	45	0.25	3	4	250	200	16-DIP/SO	±4.5 to ±20	Low power, high speed, has latches	3.30
IH5051	2 SPDT	45	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20	Low power, low R_{ON}	4.73
DG303A	2 SPDT	50	1	–	–	300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	2.36
DG307A	2 SPDT	50	1	–	–	250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.36
DG390A	2 SPDT	50	1	–	–	300	250	14-DIP	±4.5 to ±20	Low R_{ON}	2.60
IH5143	2 SPDT	75	1	–	–	200	125	16-DIP/SO	±4.5 to ±20		3.49
IH5043	2 SPDT	80	1	–	–	400	200	16-DIP/SO	±4.5 to ±20		2.36
MAX4554	3 PST	6	0.25	1	1.5	300	250	16-DIP/SO/SSOP	±20, -10	Low R_{ON} (force switch)	††
	3 PST	60	0.25	9	12	300	250	16-DIP/SO/SSOP	±20, -10	Medium R_{ON} (sense switch)	
MAX4556	SPDT	6	0.25	1	1.5	225	185	16-DIP/SO/SSOP	±15 to ±20	Low R_{ON} (force switch)	††
	2 SPDT	60	0.25	9	12	225	185	16-DIP/SO/SSOP	±15 to ±20	Medium R_{ON} (sense switch)	
MAX4532	3 SPDT	100	1	10	2	175	150	16 DIP/SO/QSOP	±2.7 to ±5	Low-voltage, improved 74HC4353	1.12
MAX4053	3 SPDT	125	1	6	10	175	150	16 DIP/SO/QSOP	±2.7 to ±8	Improved 744HC4053	1.46
MAX4053A	3 SPDT	125	0.1	6	10	175	150	16 DIP/SO/QSOP	±2.7 to ±8	Improved 744HC4053	1.87
MAX333A	4 SPDT	35	0.25	2	3	175	145	18-DIP/SO	±4.5 to ±20	Improved MAX333, low R_{ON}	3.60
MAX394	4 SPDT	35	0.25	2	3	175	145	18-SO, 20-SSOP	±2.7 to ±8	MAX333A replacement, low voltage (+2.7V to +16V)	3.19
MAX333	4 SPDT	175	5	–	–	1000	500	18-DIP/SO	±4.5 to ±20		2.87
DPST											
IH5144	DPST NO	75	1	–	–	200	125	16-DIP/SO	±4.5 to ±20		3.23
IH5044	DPST NO	80	5	–	–	400	200	16-DIP/SO	±4.5 to ±20		2.29
MAX385	2 DPST	35	0.1	2	4	175	100	16-DIP/SO	±2.7 to ±8	Single supply, +2.7V to +16V	2.57
MAX305	2 DPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	Improved DG405, low R_{ON} match and flatness	2.57
DG405	2 DPST NO	45	0.25	2	3	150	100	16-DIP/SO	±4.5 to ±20	High speed, low leakage	2.57
DG425	2 DPST	45	0.25	2	3	250	200	16-DIP/SO	±4.5 to ±20	High speed, has latches	3.30
IH5049	2 DPST NO	45	5	–	–	1000	500	16-DIP/SO	±4.5 to ±20	Low R_{ON}	5.35
DG302A	2 DPST NC	50	1	–	–	300	250	14-DIP	±4.5 to ±20	2.4V_{IH}, low R_{ON}	2.50
DG306A	2 DPST NC	50	1	–	–	250	150	14-DIP	±4.5 to ±20	CMOS logic levels, high speed, low R_{ON}	2.53
DG384A	2 DPST NC	50	1	–	–	300	250	14-DIP	±4.5 to ±20		2.92
IH5145	2 DPST NC	75	1	–	–	200	125	16-DIP/SO	±4.5 to ±20		3.82
IH5045	2 DPST NC	80	1	–	–	400	200	16-DIP/SO	±4.5 to ±20		2.44
IH5047	4PST NC	75	1	–	–	400	200	16-DIP/SO	±4.5 to ±20		2.44
PHASE-REVERSAL SWITCHES											
MAX4526	Dual SPDT	175	0.5	–	–	0.1	0.1	8-DIP/SO/µMAX	±4.5 to ±20	High speed	2.17
MAX4527	Dual SPDT	175	0.5	–	–	0.2	0.2	8-DIP/SO/µMAX	±4.5 to ±20	Low power	2.17
MAX4528	Dual SPDT	175	0.5	–	–	0.2	0.2	8-DIP/SO/µMAX	±2.7 to ±5	Low voltage	††

[1] NO = Normally Open, NC = Normally Closed
[2] Drain-source on-resistance is for the commercial grade, T_A = + 25°C.

Video Switches

Part Number	Function[1]	$R_{DS(ON)}$[2] (Ω max)	$I_{COM(OFF)}$/ $I_{D(OFF)}$ (nA max)	R_{ON} Match (Ω max)	R_{ON} Flatness (Ω max)	t_{ON} (ns max)	t_{OFF} (ns max)	Pins-Package Options	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX4529	SPST	90	0.5	–	10	75	75	6 SOT23, 8-µMAX	+2.7 to +12, ±2.7 to ±6	80dB isolation at 10MHz	††
MAX4545	4 SPST	20	1	1	0.5	200	150	20-SO/SSOP	±2.7 to ±5.5	70dB isolation at 10MHz	1.80
MAX4546	2 SPDT	20	1	1	0.5	200	150	16-SO/QSOP	±2.7 to ±5.5	70dB isolation at 10MHz	1.62
MAX4547	2 SPDT	20	1	1	0.5	200	150	16-SO/QSOP	±2.7 to ±5.5	80dB isolation at 10MHz	1.62
MAX4565	4 SPST	60	1	2	1	200	150	20-SO/SSOP	±2.7 to ±5.5	70dB isolation at 10MHz	1.55
MAX4566	2 SPDT	60	1	2	1	200	150	16-SO/QSOP	±2.7 to ±5.5	70dB isolation at 10MHz	1.35
MAX4567	2 SPDT	60	1	2	1	200	150	16-SO/QSOP	±2.7 to ±5.5	80dB isolation at 10MHz	1.35
IH5341	2 SPST NO	75	1	5	–	300	150	14-DIP/SO	±5 to ±18	70dB isolation at 10MHz	2.48
IH5352	4 SPST NO	75	1	5	–	300	150	16-DIP/SO	±5 to ±18	70dB isolation at 10MHz	4.50

Signal-Line Circuit Protectors

Part Number	Function	$R_{DS(ON)}$[2] (Ω max)	$I_{D(OFF)}$ (nA max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX366‡	3-line	100	1	-12.5 to +13.5	±35V overvoltage protected	1.42
MAX367‡	8-line	100	1	-12.5 to +13.5	±35V overvoltage protected	2.43

1 NO = Normally Open, NC = Normally Closed
2 Drain-source on-resistance is for the commercial grade, T_A = + 25°C.
‡ No control required. Switches are always on when power is on.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Analog Multiplexers

Fault Protected

8-Channel

MAX354* (±35V)
MAX355* (diff ±35V)
MAX358* (±35V)
MAX359* (diff ±35V)
MAX368* (latch ±35V)
MAX369* (latch, diff ±35V)
MAX378* (±75V)
MAX379* (diff ±75V)
MAX388* (latch ±100V)
MAX389* (latch, diff ±100V)
HI-508A* (±35V)
HI-509A* (diff ±35V)

Standard

4-Channel

MAX4518‡
MAX4519‡ (dual 2:1)

8-Channel

MAX308
MAX309 (diff)
MAX349‡
MAX350‡ (diff)
MAX382‡ (latch)
MAX384‡ (latch, diff)
MAX398‡
MAX399‡ (diff)
MAX4051‡
MAX4051A‡
MAX4052‡
MAX4052A‡ (diff)
★ MAX4530‡
★ MAX4531‡ (diff)
DG408
DG409 (diff)
DG508A
DG509A (diff)
DG528 (latch)
DG529 (latch, diff)
MX7501
MX7502 (diff)
MX7503

16-Channel

MAX306
MAX307 (diff)
MAX396‡
MAX397‡ (diff)
DG406
DG407 (diff)
DG506A
DG507A (diff)
MX7506
MX7507 (diff)

Video

8-Channel

MAX310 (70dB at 10MHz)
MAX311 (diff 70dB at 10MHz)

Mux/Amplifier

MAX440
MAX441
MAX442
MAX453 (1 of 2, drives 75Ω)
MAX454 (1 of 4, drives 75Ω)
MAX455 (1 of 8, drives 75Ω)

Crosspoint

MAX456 (8x8)
MAX458 (8x4)
MAX459 (8x4)
MAX4111 (1x1)
MAX4121 (2x1)
MAX4221 (dual 2x1)
MAX4141 (4x1)

Low Leakage

8-Channel

MAX328 (10pA)
MAX329 (diff, 10pA)
MAX338 (20pA)
MAX339 (diff, 10pA)

16-Channel

★ MAX336 (20pA)
★ MAX337 (diff, 10pA)

★ New product
† Future product
* Withstands quoted input or output voltage indefinitely with/without supply voltage present
‡ Guaranteed 3V operation

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}/I_{COM(OFF)}$ (nA max)	R_{ON} Match (Ω max)	t_{ON}/t_{OFF} (µs max)	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX4053A	1-of-2	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
MAX4518	1-of-4	100	0.2	4	0.15/0.15	±2.7 to ±8	Low voltage, guaranteed R_{ON} match	1.15
MAX308	1-of-8	100	0.75	5	0.225/0.150	±4.5 to ±20	Improved DG408, guaranteed R_{ON} match and flatness	2.59
MAX349	1-of-8	100	0.1	5	0.275/0.150	+3, +5, ±5	Serial interface	2.98
MAX382	1-of-8	100	0.2	4	0.15/0.15	+3, +5, ±5	Low-voltage, latchable address inputs	3.00
MAX398	1-of-8	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG408 pinout	2.59
MAX4051A	1-of-8	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
MAX4530	1-of-8	100	1	10	–	+2 to +12	Improved 74HC4351	1.12
DG408	1-of-8	100	1	–	0.225/0.150	±4.5 to ±20	Industry standard	2.59
MAX4051	1-of-8	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4051 upgrade, ±2.7V to ±8V	1.46
MAX4053	1-of-2	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4053 upgrade	1.46
MAX354	1-of-8	350	0.5	12	0.25/0.20	±4.5 to ±20	Improved MAX358, improved R_{ON}, ±35V fault protection	2.45
DG508A	1-of-8	350	2	–	1.0/1.7	±15	Industry standard	2.39
MX7501	1-of-8	350	5	–	1.5/1.0	±15	Industry standard	5.58
MX7503	1-of-8	350	5	–	1.5/1.0	±15	Industry standard	5.58
MAX338	1-of-8	400	0.02	10	0.50/0.50	±4.5 to ±20	Improved DG508A, low-leakage upgrade, QSOP	2.39
DG528	1-of-8	450	10	–	1.5	±15	Industry standard with latches	2.28
MAX358	1-of-8	1800	1	–	0.5	±15	Fault protected to ±35V	2.45
MAX368	1-of-8	1800	2	–	1.5/1.0	±15	Fault protected with latches to ±35V	3.50
HI-508A	1-of-8	1800	2	–	0.5	±15	Fault protected to ±35V	2.75
MAX388	1-of-8	3000	1	–	1	±15	Fault protected with latches to ±100V	4.50
MAX378	1-of-8	3500	1	–	0.75/0.5	±15	Fault protected to ±75V	3.50
MAX328	1-of-8	5000	0.02	–	1	±15	Ultra-low leakage	3.61
MAX306	1-of-16	100	2	5	0.2/0.15	±4.5 to ±20	Improved DG406, guaranteed R_{ON} match and flatness	3.87
MAX396	1-of-16	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG406 pinout	4.04
MAX397	1-of-16	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG407 pinout	4.04
DG406	1-of-16	100	2	–	0.2/0.15	±4.5 to ±20	Industry standard	4.53
MAX336	1-of-16	400	0.02	10	0.5/0.5	±4.5 to ±20	Improved DG506A, low leakage, SSOP	3.69
MX7506	1-of-16	450	5	–	15/1.0	±15	Insustry standard	10.25
DG506A	1-of-16	450	5	–	1.0/0.4(typ)	±15	Industry standard	3.68
IH5108	Use MAX358 (pin-for-pin compatible upgrade)							–
IH6108	Use DG508A (pin-for-pin compatible upgrade)							–
MAX4519	2-of-4	100	0.1	4	0.15/0.15	±2.7 to ±8	Low-voltage, guaranteed R_{ON} match	1.15
MAX309	2-of-8	100	1	5	0.225/0.150	±4.5 to ±20	Improved DG409, guaranteed R_{ON} match and flatness	2.59
MAX384	2-of-8	100	0.2	4	0.15/0.15	+3, +5, ±5	Low-voltage, latchable address inputs	3.00
MAX399	2-of-8	100	0.1	4	0.15/0.15	+3, +5, ±5	Low-voltage, DG409 pinout	2.59
MAX4052A	2-of-8	100	0.1	4	0.15/0.15	+2.7 to +16	Improved 74HC4051, low voltage, improved R_{ON}	1.87
MAX4531	2-of-8	100	1	10	–	+2 to +12	Improved 74HC4352	1.12
DG409	2-of-8	100	1	–	0.225/0.150	±4.5 to ±20	Industry standard	2.59
MAX350	2-of-8	125	1	10	0.275/0.150	+3, +5, ±5	Low-voltage, serial interface	2.98
MAX4052	2-of-8	125	1	10	0.15/0.15	+2.7 to +16	Low-voltage, 74HC4052 upgrade, ±2.7V to ±8V	1.46
MAX355	2-of-8	350	0.5	12	0.25/0.20	±4.5 to ±20	Improved MAX359, improved R_{ON}, ±35V fault protection	2.45
DG509A	2-of-8	350	2	–	1.0/1.7	±15	Industry standard	2.39
MX7502	2-of-8	350	3	–	1.5/1.0	±15	Industry standard	5.58
MAX339	2-of-8	400	0.02	10	0.50/0.50	±4.5 to ±20	Improved DG509A, low-leakage upgrade, QSOP	2.39
DG529	2-of-8	450	10	–	1.5	±15	Industry standard with latches	2.28
MAX359	2-of-8	1800	1	–	0.5	±15	Fault protected to ±35V	2.45
MAX369	2-of-8	1800	1	–	1.5/1.0	±15	Fault protected with latches to ±35V	3.50
HI-509A	2-of-8	1800	2	–	0.5	±15	Fault protected to ±35V	2.75
MAX389	2-of-8	3000	1	–	1	±15	Fault protected with latches to ±100V	4.50
IH5208	Use MAX359 (pin-for-pin compatible upgrade)							–
IH6208	Use DG509A (pin-for-pin compatible upgrade)							–

* Drain-source on-resistance is for the commercial grade, T_A = + 25°C.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Analog Multiplexers (continued)

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}/I_{COM(OFF)}$ (nA max)	R_{ON} Match (Ω max)	t_{ON}/t_{OFF} (µs max)	Supply Voltage Range (V)	Features	Price† 1000-up ($)
MAX379	2-of-8	3500	1	–	0.75/0.5	±15	Fault protected to ±75V	3.50
MAX329	2-of-8	5000	0.02	–	1	±15	Ultra-low leakage	3.61
MAX307	2-of-16	100	2	5	0.2/0.15	±4.5 to ±20	Improved DG407, guaranteed R_{ON} match and flatness	3.87
DG407	2-of-16	100	2	–	0.2/0.15	±15	Industry standard	4.53
MAX337	2-of-16	400	0.02	10	0.5/0.5	±4.5 to ±20	Improved DG507A, low leakage, SSOP	3.69
MX7507	2-of-16	450	5	–	1.5/1.0	±15	Industry standard	10.25
DG507A	2-of-16	450	5	–	1.0/0.4(typ)	±15	Industry standard	3.68
IH6116	Use MAX506A (pin-for-pin compatible upgrade)							–
IH6216	Use DG507A (pin-for-pin compatible upgrade)							–

Video Multiplexers

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	DP/DG (degrees/%)	Output Current (mA max)	Supply Voltage (V)	Supply Current (mA)	Features	Price† 1000-up ($)
MAX440	160 110 ($A_V \geq 2$)	370	0.03/0.04	35	±5	40	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain error, 15ns switch time, high-Z output state	8.95
MAX441	160 110 ($A_V \geq 2$)	370	0.03/0.04	35	±5	40	Video amp with 4-channel mux 0.03°/0.04% diff phase/gain error, 15ns switch time	5.90
MAX442	140	250	0.03/0.04	35	±5	40	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45

Part Number	Function	$R_{DS(ON)}$* (Ω max)	$I_{D(OFF)}$ (nA max)	t_{ON} (µs max)	V_{IL}/V_{IH} (V)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX453	1-of-2 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	3.94
MAX454	1-of-4 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	5.25
MAX310	1-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	5.18
MAX455	1-of-8 mux	Buffered output	10	0.12	0.8/2.4	±2	On-chip output amp	8.75
MAX311	2-of-8 mux	250	10	1.5	0.8/2.4	-12.5 to +13.5	70dB isolation at 10MHz	7.20

Video Crosspoint Switches

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	DP/DG (degrees/%)	Off Isolation (dB typ)	Crosstalk (dB typ)	EV Kit	Features	Price† 1000-up ($)
MAX456	35	250	1/0.5	80 (5MHz)	70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z cutput capability	19.98
MAX458/459	100/90	300	0.05/0.01	60 (10MHz)	55 (10MHz)	Yes	8x4 crosspoint switch array with four 75Ω cable drivers, high-Z output capability	21.85
MAX4111	330	700	0.01/0.01	74 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	700	0.01/0.01	74 (30MHz)	66	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4221	330	700	0.01/0.01	74 (30MHz)	66	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50
MAX4141	330	700	0.01/0.01	74 (30MHz)	66	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	4.50

* Drain-source on-resistance is for the commercial grade, T_A = + 25°C.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-1193; Rev 0; 4/97

MAXIM

16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

General Description

The MAX336/MAX337 are monolithic, CMOS analog multiplexers (muxes). The 16-channel MAX336 is designed to connect one of 16 inputs to a common output by control of a 4-bit binary address. The dual, 8-channel MAX337 is designed to connect one of eight inputs to a common output by control of a 3-bit binary address. Both devices can be used as either a mux or a demux. On-resistance is 400Ω (max), and the devices conduct current equally well in both directions.

These muxes feature extremely low off leakages (less than 20pA at +25°C) and on-channel leakages (less than 50pA at +25°C). The new design offers guaranteed low charge injection (3.5pC typical) and electrostatic discharge (ESD) protection greater than 2000V, per method 3015.7. These improved muxes are pin-compatible upgrades for the industry-standard DG506 and DG507.

The MAX336/MAX337 operate from a single +4.5V to +30V supply or from dual ±4.5V to ±20V supplies. All control inputs (whether address or enable) are TTL compatible (0.8V to 2.4V) over the full specified temperature range and over the ±4.5V to ±18V supply range.

Applications

Precision Data Acquisition

Precision Signal Routing

Test Equipment

Features

- ♦ **<400Ω (max) On-Resistance**
- ♦ **<500ns Transition Time**
- ♦ **<10Ω On-Resistance Match**
- ♦ **<20pA NO-Off Leakage Current at +25°C**
- ♦ **3.5pC Charge Injection**
- ♦ **+4.5V to +30V Single Supply**
  ±4.5V to ±20V Dual Supplies
- ♦ **Plug-In Upgrade for Industry-Standard DG506/DG507**
- ♦ **Bidirectional Rail-to-Rail® Signal Handling**
- ♦ **TTL/CMOS-Logic Compatible**
- ♦ **>2000V ESD Protection, per Method 3015.7**

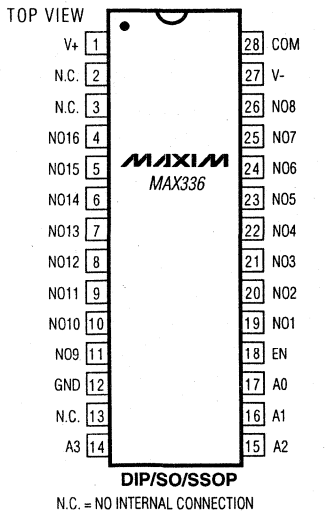
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX336CPI	0°C to +70°C	28 Plastic DIP
MAX336CWI	0°C to +70°C	28 Wide SO
MAX336CAI	0°C to +70°C	28 SSOP
MAX336C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

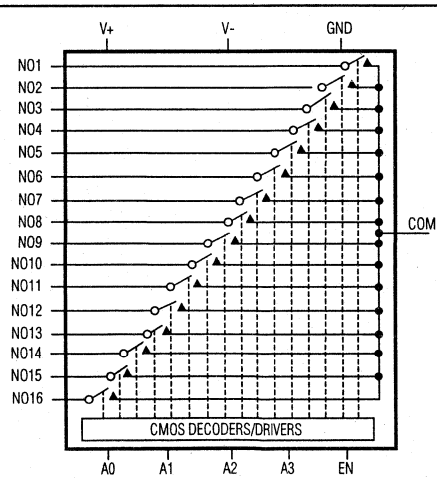
* *Contact factory for dice specifications.*

Pin Configurations/Functional Diagrams/Truth Tables



DIP/SO/SSOP

N.C. = NO INTERNAL CONNECTION



MAX336 16-CHANNEL SINGLE-ENDED MULTIPLEXER

MAX336					
A3	**A2**	**A1**	**A0**	**EN**	**ON SWITCH**
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

Continued at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ .....-0.3V, 44V
GND .....-0.3V, 25V
Digital Inputs, A_, EN_, NO, COM
(Note 1).....(V- - 0.3V) to (V+ + 0.3V)
or 30mA (whichever occurs first)
Continuous Current (any terminal).....30mA
Peak Current, NO or COM
(pulsed at 1ms, 10% duty cycle max) 100mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 14.29mW/°C above +70°C) 1.14W
Wide SO (derate 12.50mW/°C above +70°C).....1.00W
SSOP (derate 9.52mW/°C above +70°C) 762mW
CERDIP (derate 16.67mW/°C above +70°C).....1.33W
Operating Temperature Ranges
MAX336C_I/MAX337C_I .....0°C to +70°C
MAX336E_I/MAX337E_I.....-40°C to +85°C
MAX336MJI/MAX337MJI .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Note 1: Signals on any terminal exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)				-15		15	V
On-Resistance	R_{ON}	I_{NO} = 0.2mA, V_{COM} = ±10V		T_A = +25°C			220	400	Ω
				T_A = T_{MIN} to T_{MAX}				500	
On-Resistance Matching Between Channels	ΔR_{ON}	I_{NO} = 0.2mA, V_{COM} = ±10V (Note 4)		T_A = +25°C			5	10	Ω
				T_A = T_{MIN} to T_{MAX}				15	
NO-Off Leakage Current (Note 5)	$I_{NO(OFF)}$	V_{COM} = ∓10V, V_{NO} = ±10V, V_{EN} = 0V		T_A = +25°C		-0.02	0.001	0.02	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-1.25		1.25	
					M	-20		20	
COM-Off Leakage Current (Note 5)	$I_{COM(OFF)}$	V_{NO} = ±10V, V_{COM} = ∓10V, V_{EN} = 0V	MAX336	T_A = +25°C		-0.05		0.05	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-6.5		6.5	
					M	-80		80	
		V_{NO} = ∓10V, V_{COM} = ±10V, V_{EN} = 0V	MAX337	T_A = +25°C		-0.05		0.05	
				T_A = T_{MIN} to T_{MAX}	C, E	-3.25		3.25	
					M	-40		40	
COM-On Leakage Current (Note 5)	$I_{COM(ON)}$	V_{COM} = ±10V, V_{NO} = ±10V, sequence each switch on	MAX336	T_A = +25°C		-0.05		0.05	nA
				T_A = T_{MIN} to T_{MAX}	C, E	-6.5		6.5	
					M	-80		80	
			MAX337	T_A = +25°C		-0.05		0.05	
				T_A = T_{MIN} to T_{MAX}	C, E	-3.25		3.25	
					M	-40		40	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V or 15V		-1.0	0.001	1.0	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V or 2.4V, V_A = 0V		-1.0		1.0	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V	T_A = +25°C	-1	0.01	1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
		V_{EN} = 2.4V, $V_{A(ALL)}$ = 2.4V	T_A = +25°C		400	700	
			T_A = T_{MIN} to T_{MAX}			1100	
Negative Supply Current	I-	V_{EN} = 0V or 2.4V; $V_{A(ALL)}$ = 0V, 2.4V, or 5V	T_A = +25°C	-1		1	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 2, T_A = +25°C			200	500	ns
Break-Before-Make Interval	t_{OPEN}	Figure 4, T_A = +25°C		10	50		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3	T_A = +25°C		250	500	ns
			T_A = T_{MIN} to T_{MAX}			750	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3	T_A = +25°C		100	500	ns
			T_A = T_{MIN} to T_{MAX}			750	
Charge Injection (Note 3)	Q	C_L = 100pF, V_{NO} = 0V, R_S = 0Ω, Figure 6, T_A = +25°C			3.5	10	pC
Off Isolation (Note 6)	V_{ISO}	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz, T_A = +25°C			-82		dB
Crosstalk Between Channels	V_{CT}	V_{EN} = 2.4V, f = 100kHz, V_{GEN} = 1Vp-p, R_L = 1kΩ, Figure 7, T_A = +25°C			-86		dB
Logic Input Capacitance	C_{IN}	f = 1MHz, T_A = +25°C			2		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_{NO} = 0V, Figure 8, T_A = +25°C			2		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, V_{EN} = 0.8V, V_{COM} = 0V, Figure 8, T_A = +25°C	MAX336		20		pF
			MAX337		10		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, V_{EN} = 2.4V, V_{COM} = 0V, Figure 8, T_A = +25°C	MAX336		22		pF
			MAX337		12		

16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

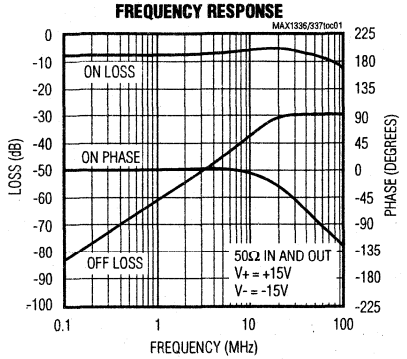
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	V_{NO}, V_{COM}	(Note 3)	0		12	V
On-Resistance	R_{ON}	I_{NO} = 0.2mA, V_{COM} = 3V or 10V, T_A = +25°C		460	700	Ω
DYNAMIC						
Transition Time (Note 3)	t_{TRANS}	$V_{NO_}$ = ±5V, V_{IN} = 2.4V, Figure 1, T_A = +25°C		350	600	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3, T_A = +25°C		350	600	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 5V, Figure 3, T_A = +25°C		110	500	ns
Charge Injection (Note 3)	Q	C_L = 100pF, V_{NO} = 0V, R_S = 0Ω, T_A = +25°C		5.0	10	pC

Note 2: The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$.
Note 5: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = 20log V_{COM}/V_{NO}, where V_{COM} = output and V_{NO} = input to off switch.

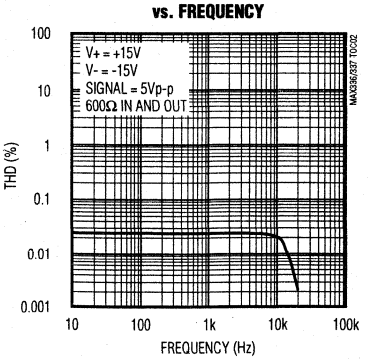
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

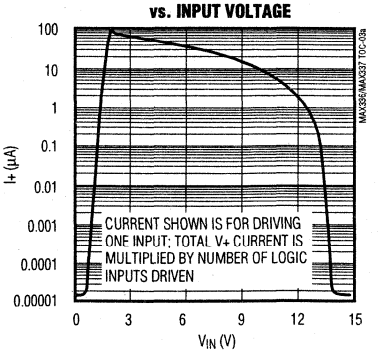
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



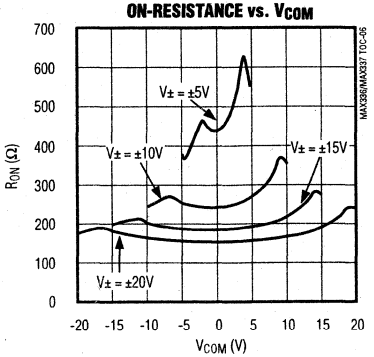
SUPPLY CURRENT vs. INPUT VOLTAGE



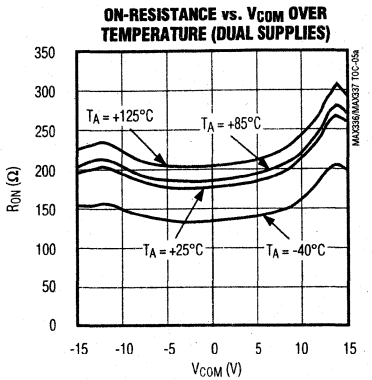
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

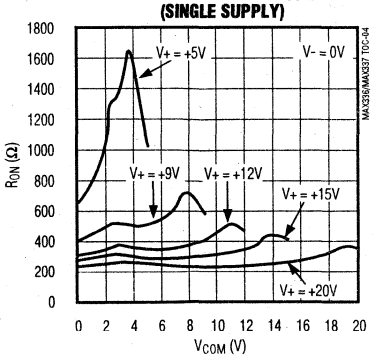
ON-RESISTANCE vs. V_{COM}



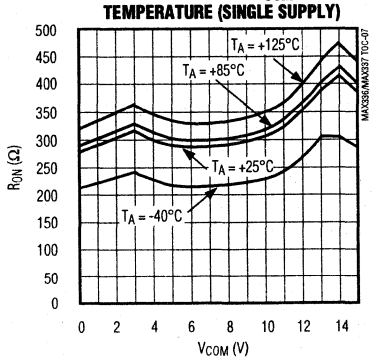
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (DUAL SUPPLIES)



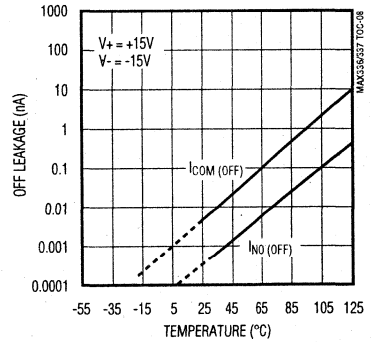
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



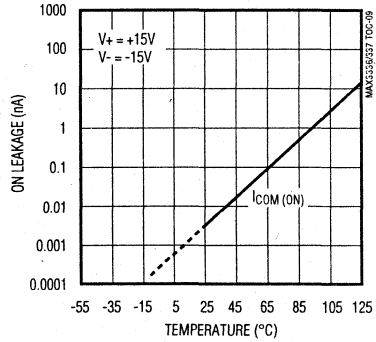
ON-RESISTANCE vs. V_{COM} OVER TEMPERATURE (SINGLE SUPPLY)



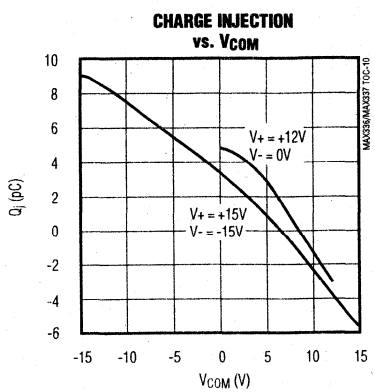
OFF LEAKAGE vs. TEMPERATURE



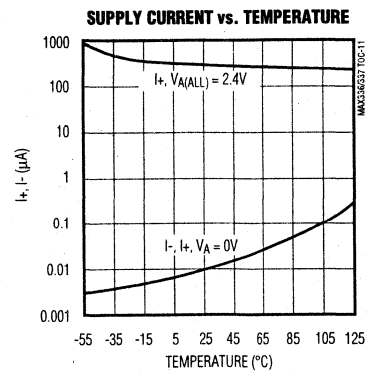
ON LEAKAGE vs. TEMPERATURE



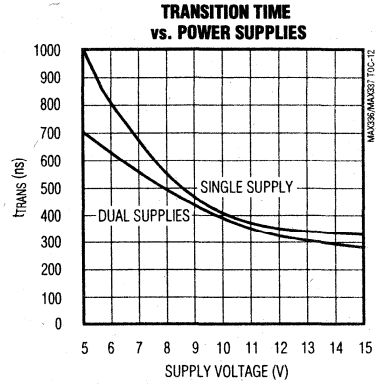
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



TRANSITION TIME vs. POWER SUPPLIES



16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Description

PIN		NAME	FUNCTION
MAX336	MAX337		
1	1	V+	Positive Supply-Voltage Input
2, 3, 13	3, 13, 14	N.C.	No Internal Connection
—	2	COMB	Analog Signal B Output* (bidirectional)
4–11	—	NO16-NO9	Analog Signal Inputs* (bidirectional)
—	4–11	NO8B–NO1B	Analog Signal B Inputs* (bidirectional)
12	12	GND	Logic Ground
14–17	—	A3–A0	Logic Address Inputs
—	15, 16, 17	A2, A1, A0	Logic Address Inputs
18	18	EN	Logic Enable Input
19–26	—	NO1–NO8	Analog Signal Inputs* (bidirectional)
—	19–26	NO1A–NO8A	Analog Signal A Inputs* (bidirectional)
27	27	V-	Negative Supply-Voltage Input. Connect to GND for single-supply operation.
28	—	COM	Analog Signal Output* (bidirectional)
—	28	COMA	Analog Signal A Output* (bidirectional)

** Analog signal inputs and outputs are names of convenience only; they are identical and interchangeable.*

Applications Information

Operation with Supply Voltages Other than 15V

Using supply voltages less than ±15V will reduce the analog signal range. The MAX336/MAX337 switches operate with ±4.5V to ±20V bipolar supplies or with a +4.5V to +30V single supply. Connect V- to GND when operating with a single supply. Both device types can also operate with unbalanced supplies such as +24V and -5V. The *Typical Operating Characteristics* graphs show typical on-resistance with 20V, 15V, 10V, and 5V supplies. (Switching times increase by a factor of two or more for operation at 5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, then V-, followed by the logic inputs NO and COM. If power-supply sequencing is not possible, add two small signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, but does not significantly affect the devices' low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed 44V.

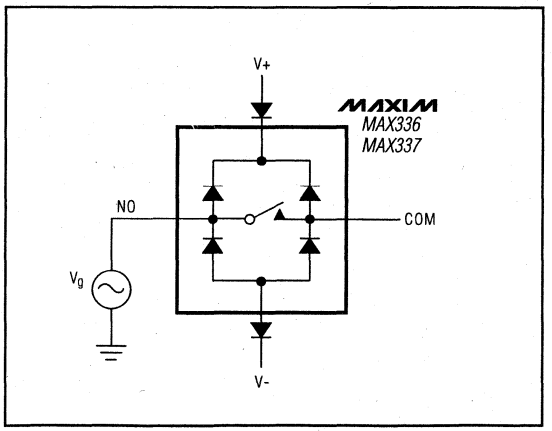


Figure 1. Overvoltage Protection Using External Blocking Diodes

Test Circuits/Timing Diagrams

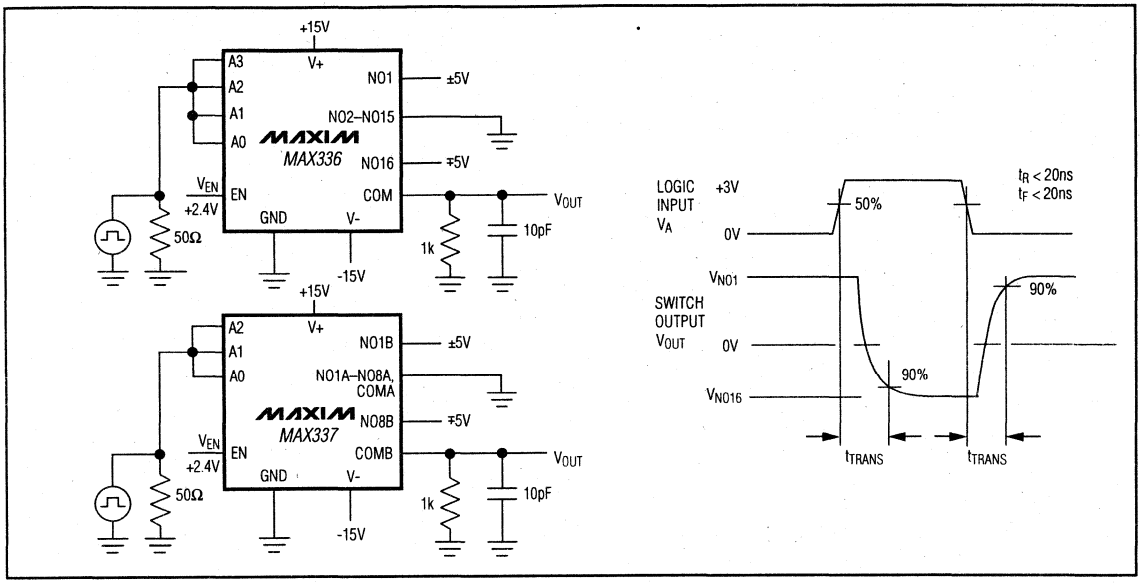


Figure 2. Transition Time

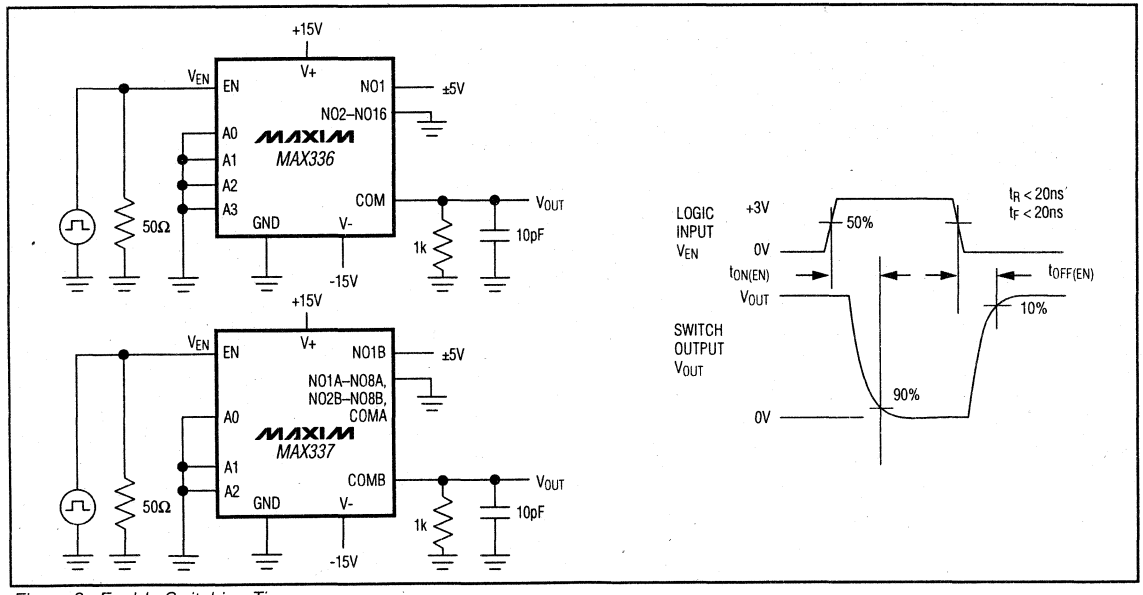


Figure 3. Enable Switching Time

16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

Test Circuits/Timing Diagrams (continued)

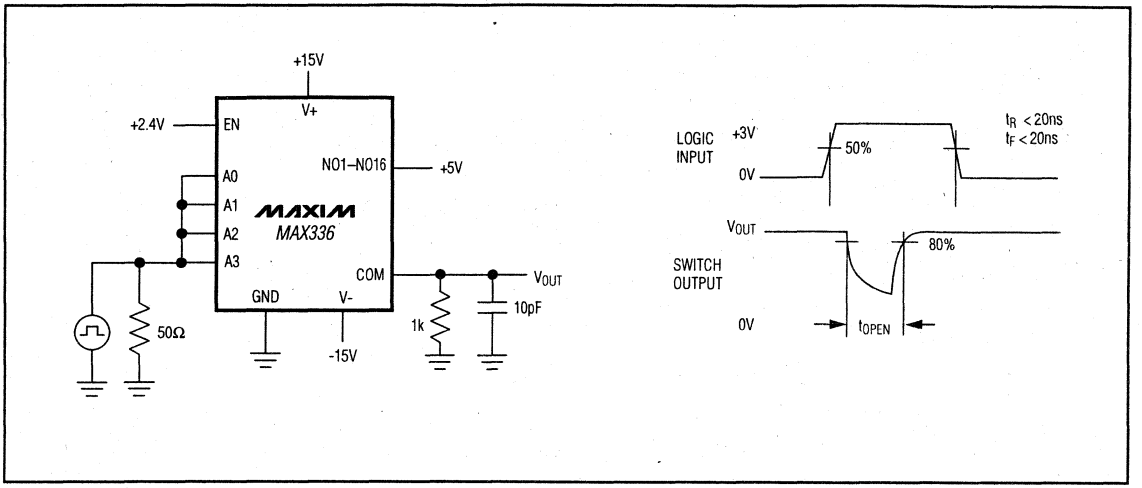


Figure 4. Break-Before-Make Interval

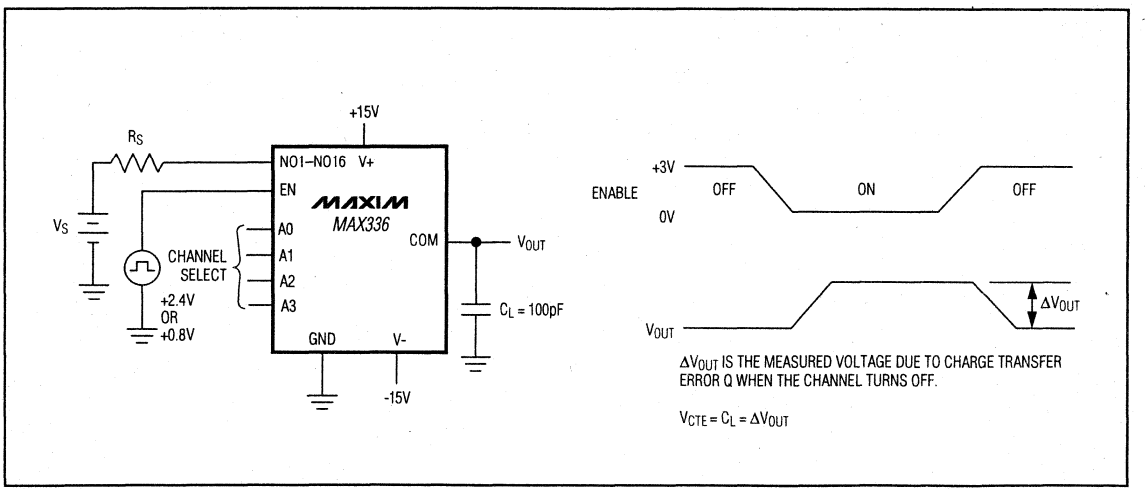


Figure 5. Charge Injection (V_{CTE})

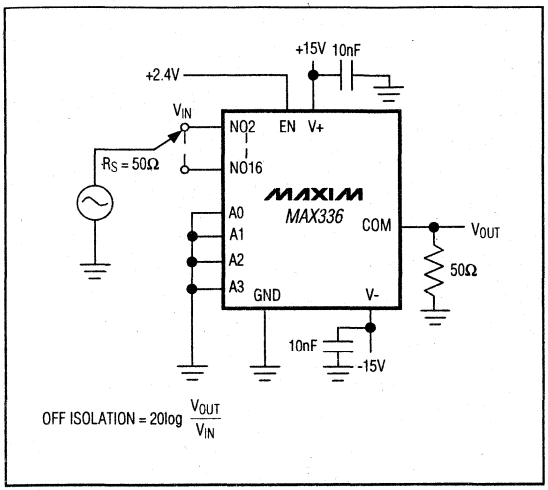


Figure 6. Off Isolation

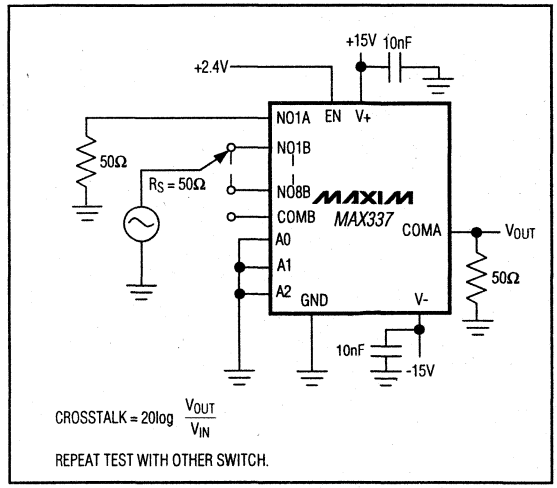


Figure 7. Crosstalk

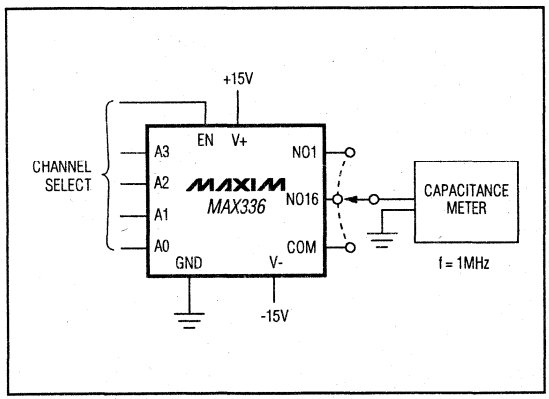
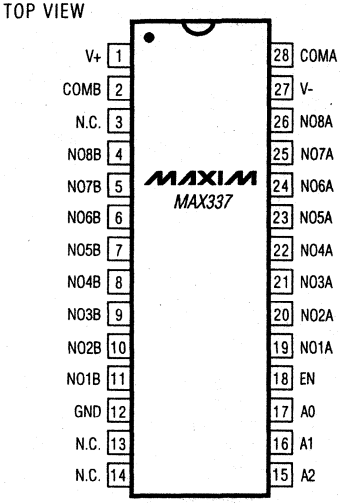


Figure 8. NO/COM Capacitance

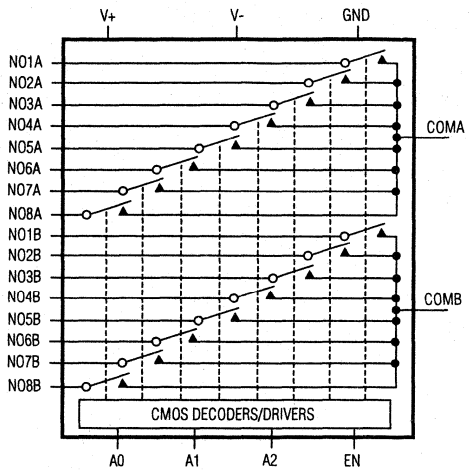
16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW



DIP/SO/SSOP



MAX337 8-CHANNEL DIFFERENTIAL MULTIPLEXER

MAX337				
A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "0" = $V_{AL} \leq 0.8V$, LOGIC "1" = $V_{AH} \geq 2.4V$

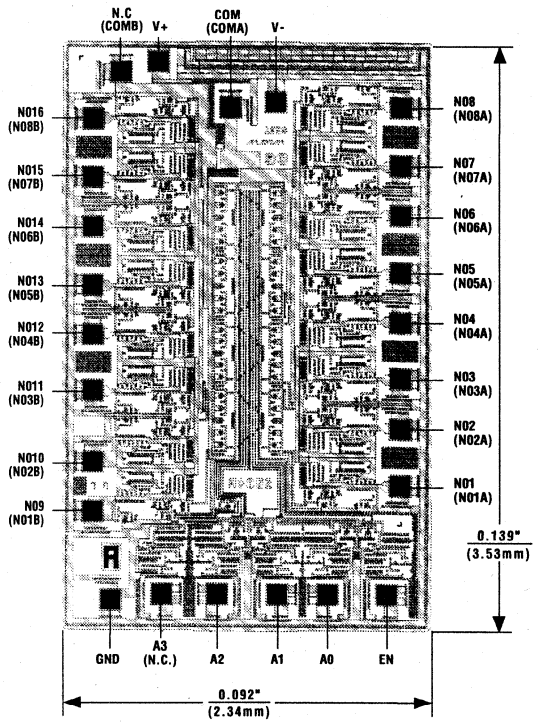
16-Channel/Dual 8-Channel, Low-Leakage, CMOS Analog Multiplexers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX336EPI	-40°C to +85°C	28 Plastic DIP
MAX336EWI	-40°C to +85°C	28 Wide SO
MAX336EAI	-40°C to +85°C	28 SSOP
MAX336EJI	-40°C to +85°C	28 CERDIP**
MAX336MJI	-55°C to +125°C	28 CERDIP**
MAX337CPI	0°C to +70°C	28 Plastic DIP
MAX337CWI	0°C to +70°C	28 Wide SO
MAX337CAI	0°C to +70°C	28 SSOP
MAX337C/D	0°C to +70°C	Dice*
MAX337EPI	-40°C to +85°C	28 Plastic DIP
MAX337EWI	-40°C to +85°C	28 Wide SO
MAX337EAI	-40°C to +85°C	28 SSOP
MAX337EJI	-40°C to +85°C	28 CERDIP**
MAX337MJI	-55°C to +125°C	28 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability.*

Chip Topography



( ) ARE FOR MAX337

TRANSISTOR COUNT: 466
BACKSIDE IS V+
SUBSTRATE CONNECTED TO V+

19-1165; Rev 0; 12/96

MAXIM

Phase-Reversal Analog Switches

General Description

The MAX4526/MAX4527 are CMOS analog ICs configured as phase-reversal switches. The MAX4526 is optimized for high-speed applications, such as chopper amplifiers, while the MAX4527 is optimized for low-power applications.

The MAX4526/MAX4527 operate from a +4.5V to +36V single supply or ±4.5V to ±18V dual supplies. On-resistance (175Ω max) is matched between switches to 8Ω maximum. Each switch can handle rail-to-rail analog signals. Maximum leakage current is only 0.5nA at +25°C and 10nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility.

Features

- **10pC (max) Charge Injection**
- **2pC (max) Charge-Injection Match**
- **175Ω Signal Paths with ±15V Supplies**
- **Guaranteed Break-Before-Make**
- **Rail-to-Rail Signal Handling**
- **Transition Time < 100ns with ±15V Supplies**
- **1µA Current Consumption (MAX4527)**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Available in Small, 8-Pin µMAX Package**

Applications

Chopper-Stabilized Amplifiers

Balanced Modulators/Demodulators

Data Acquisition

Test Equipment

Audio-Signal Routing

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4526CPA	0°C to +70°C	8 Plastic DIP
MAX4526CSA	0°C to +70°C	8 SO
MAX4526CUA	0°C to +70°C	8 µMAX
MAX4526C/D	0°C to +70°C	Dice*
MAX4526EPA	-40°C to +85°C	8 Plastic DIP
MAX4526ESA	-40°C to +85°C	8 SO
MAX4526EUA	-40°C to +85°C	8 µMAX

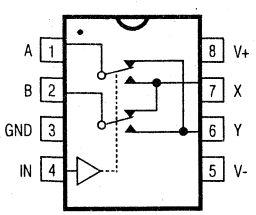
Ordering Information continued at end of data sheet.

**Contact factory for availability.*

Pin Configuration/Functional Diagram/Truth Table

TOP VIEW

MAXIM
MAX4526
MAX4527



DIP/SO/µMAX

TRUTH TABLE		
IN	A	B
0	Y	X
1	X	Y

SWITCH POSITIONS SHOWN WITH IN = LOW

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Phase-Reversal Analog Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)

V+ .....-0.3V to +44V
V- .....-25V to +0.3V
V+ to V-.....-0.3V to +44V
All Other Pins (Note 1).....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal.....±20mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle).....±30mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Ranges
MAX452_C_A.....0°C to +70°C
MAX452_E_A.....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on IN, A, B, X, or Y exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±15V Supplies

(V+ = +15V, V- = -15V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog-Signal Range	V_A, V_B, V_X, V_Y	(Note 3)	C, E	-V		V+	V
A-X, A-Y, B-X, B-Y On-Resistance	R_{ON}	V_A = V_B = ±10V, I_A = I_B = 1mA	+25°C		105	175	Ω
			C, E			200	
A-X, A-Y, B-X, B-Y On-Resistance Match (Note 4)	ΔR_{ON}	V_A = V_B = ±10V, I_A = I_B = 1mA	+25°C		0.5	8	Ω
			C, E			10	
A-X, A-Y, B-X, B-Y On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V_A = V_B = -5V, 0V, +5V; I_A = I_B = 1mA	+25°C		12	18	Ω
			C, E			30	
A, B, X, Y Leakage Current (Note 6)	$I_{A(OFF)}$, $I_{B(OFF)}$, $I_{X(OFF)}$, $I_{Y(OFF)}$	V+ = 16.5V, V- = -16.5V; V_{IN} = 0V, 3V; V_A = ±15.5V, V_B = ±15.5V	+25°C	-0.5	0.01	0.5	nA
			C, E	-10		10	
LOGIC INPUT							
IN Input Logic Threshold High	V_{INH}		C, E		1.6	2.4	V
IN Input Logic Threshold Low	V_{INL}		C, E	0.8	1.6		V
IN Input Current Logic High or Low	I_{INH}, I_{INL}	$V_{IN_}$ = 0.8V or 2.4V	C, E	1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—±15V Supplies (continued)

(V+ = +15V, V- = -15V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Transition Time	t_{TRANS}	$V_A = V_B = \pm10V$, V+ = 15V, V- = -15V, Figure 3	MAX4526	+25°C		65	100	ns
				C, E			125	
			MAX4527	+25°C		95	200	
				C, E			250	
Break-Before-Make Time Delay	t_{BBM}	$V_A = V_B = \pm10V$, V+ = 15V, V- = -15V, Figure 4		+25°C	1	5		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_A or V_B = 0V, R_S = 0Ω, Figure 5		+25°C		1	10	pC
A-X, A-Y, B-X, B-Y Capacitance	C_{OFF}	$V_A = V_B$ = GND, f = 1MHz, Figure 6		+25°C		13		pF
A-X, A-Y, B-X, B-Y Isolation (Note 7)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_A = V_B = 1V_{RMS}$, f = 1MHz, Figure 7		+25°C		-65		dB
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E	±4.5		±20	V
V+ Supply Current	I+	V+ = 16.5V, V_{IN} = 0V or V+	MAX4526	+25°C		0.7	1	mA
				C, E			1.5	
			MAX4527	+25°C		0.05	1	µA
				C, E			10	
V- Supply Current	I-	V- = -16.5V	MAX4526	+25°C	-400			µA
				C, E	-500			
			MAX4527	+25°C	-1	0.05		
				C, E	-1			

Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.

Note 5: Resistance flatness is defined as the difference between the maximum and minimum values of on-resistance as measured over the specified analog-signal range.

Note 6: Leakage current is 100% tested at maximum rated hot temperature, and is guaranteed by correlation at T_A = +25°C and minimum rated cold temperature.

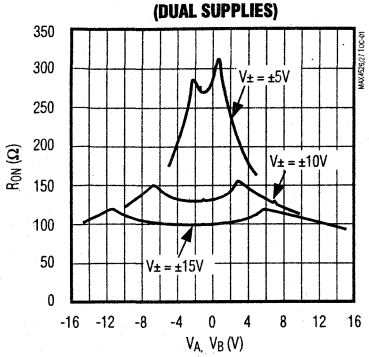
Note 7: Off-isolation = 20log10 [(V_X or V_Y) / (V_A or V_B)], V_X or V_Y = output, V_A or V_B = input to off switch.

Phase-Reversal Analog Switches

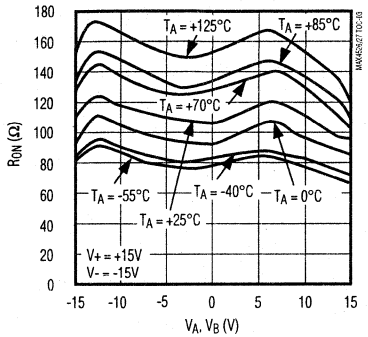
Typical Operating Characteristics

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

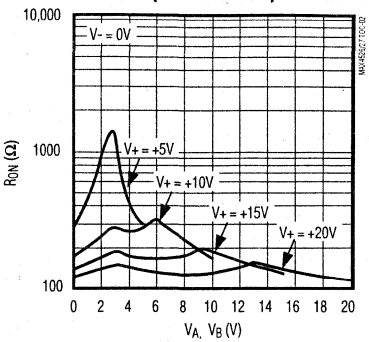
ON-RESISTANCE vs. V_A, V_B (DUAL SUPPLIES)



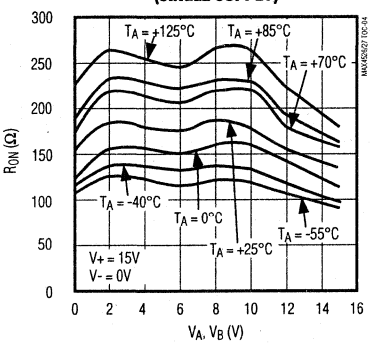
ON-RESISTANCE vs. V_A, V_B, AND TEMPERATURE (DUAL SUPPLIES)



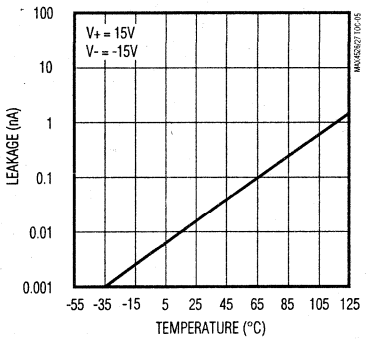
ON-RESISTANCE vs. V_A, V_B (SINGLE SUPPLY)



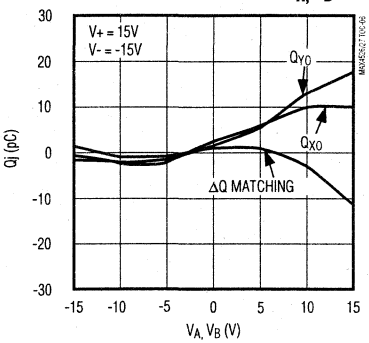
ON-RESISTANCE vs. V_A, V_B, AND TEMPERATURE (SINGLE SUPPLY)



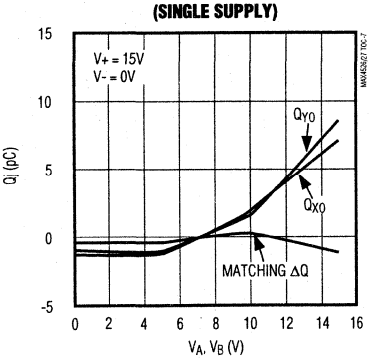
LEAKAGE vs. TEMPERATURE



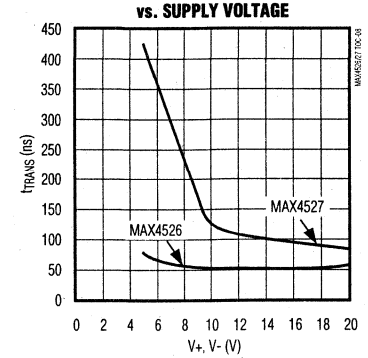
CHARGE INJECTION, CHARGE-INJECTION MATCHING vs. V_A, V_B



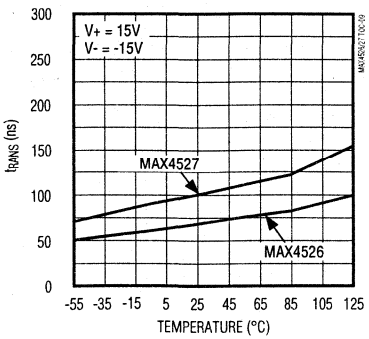
CHARGE INJECTION, CHARGE-INJECTION MATCHING vs. V_A, V_B (SINGLE SUPPLY)



TRANSITION TIME vs. SUPPLY VOLTAGE



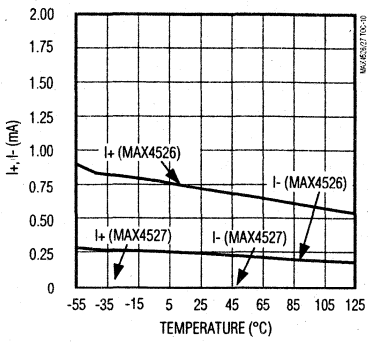
TRANSITION TIME vs. TEMPERATURE



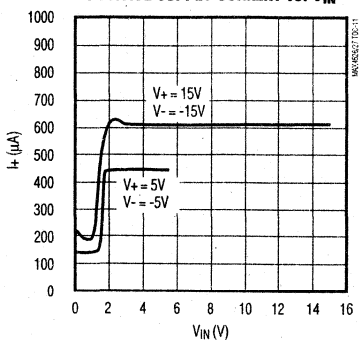
Typical Operating Characteristics (continued)

(V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C, unless otherwise noted.)

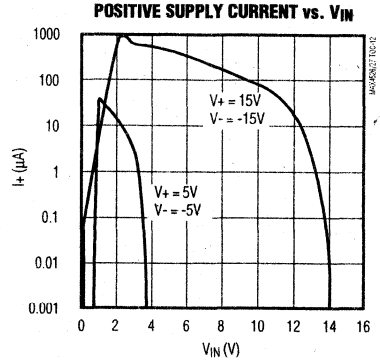
SUPPLY CURRENT vs. TEMPERATURE



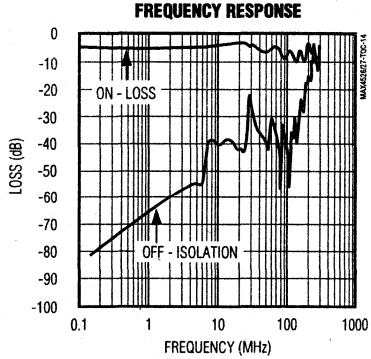
MAX4526
POSITIVE SUPPLY CURRENT vs. V_{IN}



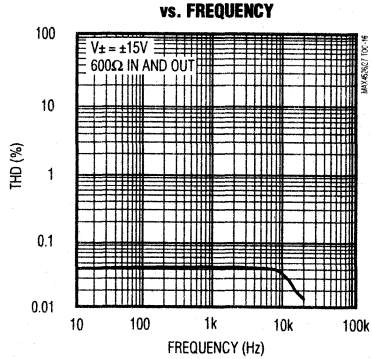
MAX4527
POSITIVE SUPPLY CURRENT vs. V_{IN}



MAX4526
FREQUENCY RESPONSE



TOTAL HARMONIC DISTORTION
vs. FREQUENCY



Phase-Reversal Analog Switches

Pin Configuration

PIN	NAME	FUNCTION
1	A	Analog-Switch Input Terminal A. Connected to Y when IN is low; connected to X when IN is high.
2	B	Analog-Switch Input Terminal B. Connected to X when IN is low; connected to Y when IN is high.
3	GND	Ground. Connect GND to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
4	IN	Logic-Level Control Inputs (see *Truth Table*).
5	V-	Negative Analog Supply-Voltage Input. Connect V- to GND for single-supply operation.
6	Y	Analog-Switch Output Terminal Y.
7	X	Analog-Switch Output Terminal X.
8	V+	Positive Analog/Digital Supply-Voltage Input. Internally connected to substrate.

Note: A, B, X and Y pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction. However, AC symmetry is best when A and B are the input, and X and Y are the output. Reduce AC balance in critical applications by using A and X or A and Y as the input, and B and Y or B and X as the output.

Detailed Description

The MAX4526/MAX4527 are phase-reversal analog switches, consisting of two normally open and two normally closed CMOS analog switches arranged in a bridge configuration. Analog signals are put into two input pins and taken out of two output pins. A logic-level signal controls whether the input signal is routed through normally or inverted. A low-resistance DC path goes from inputs to outputs at all times, yet isolation between the two signal paths is excellent. Analog signals range from V- to V+.

These parts are characterized and optimized with ±15V supplies, and they can operate from a single supply. The MAX4526 is optimized for high-frequency operation, and has a higher-speed logic-level translator and switch driver. The MAX4527 has identical analog switch characteristics, but has a slower logic-level translator and switch driver for lower current consumption.

The MAX4526/MAX4527 are designed for DC and low-frequency-signal phase-reversal applications, such as chopper amplifiers, modulator/demodulators, and self-zeroing or self-calibrating circuits. Unlike conventional CMOS switches externally wired in a bridge configuration, both DC and AC symmetry are optimized with a small 8-pin configuration that allows simple board layout and isolation of logic signals from analog signals.

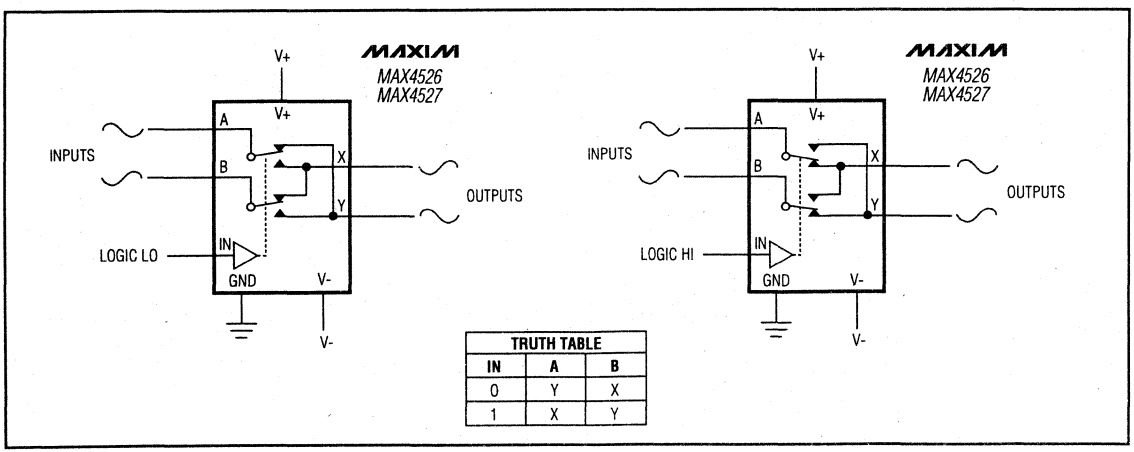


Figure 1. Typical Application Circuits

Power-Supply Considerations

Overview

The MAX4526/MAX4527 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the analog-voltage limits on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin, and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-.

Virtually all of the analog leakage current is through the ESD diodes to V+ or V-. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out-of-phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translator and set the input logic threshold. The logic-level translator converts the logic levels to switched V+ and V- signals to drive the analog switches' gates. This drive signal is the only connection between GND and the analog supplies. V+ and V- have ESD-protection diodes to GND. The logic-level input has ESD protection to V+ and to V- but not to GND, so the logic signal can go below GND (as low as V-) when bipolar supplies are used.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the internal P-channel switches, reducing the overall switch on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level input pin, IN, has ESD-protection diodes to V+ and V- but not to GND, so it can be safely driven to V+ and V-. The logic-level threshold, V_{IN}, is CMOS/TTL compatible when V+ is between 4.5V and 36V (see *Typical Operating Characteristics*).

Bipolar Supplies

The MAX4526/MAX4527 operate with bipolar supplies between ±4.5V and ±18V. However, since all factory characterization is done with ±15V supplies, specifications at other supplies are not guaranteed. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 44V (see *Absolute Maximum Ratings*).

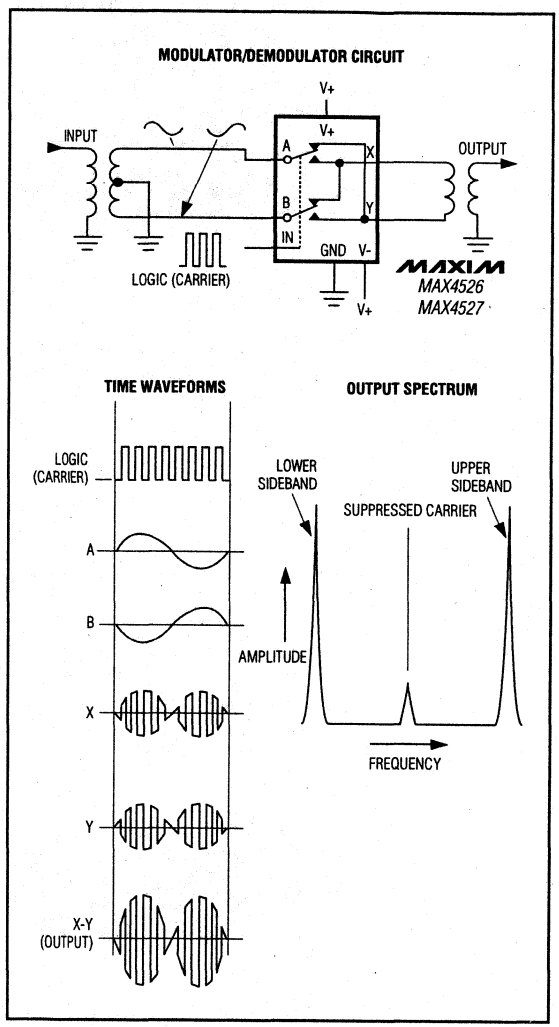


Figure 2. Balanced Modulator/Demodulator

Phase-Reversal Analog Switches

Single Supply

The MAX4526/MAX4527 operate from a single supply between +4.5V and +36V when V- is connected to GND. Observe all of the bipolar precautions when operating from a single supply.

Applications Information

The MAX4526/MAX4527 are designed for DC and low-frequency-signal phase-reversal applications. Both DC and AC symmetry are optimized for use with ±15V supplies.

Signal Phase/Polarity Reversal

The MAX4526/MAX4527 can reverse the phase or polarity of a pair of signals that are out-of-phase and balanced to ground. This is done by routing signals through the MAX4526/MAX4527 and under control of the IN pin, reversing the two signals paths inside the switch before sending out to a balanced output. Figure 1 shows a typical example. **The MAX4526/MAX4527 cannot reverse the phase or polarity of a single-grounded signal, as can be done with an inverting op amp or transformer.**

Balanced Modulators/Demodulators

The MAX4526/MAX4527 can be used as a balanced modulator/demodulator at carrier frequencies up to 100kHz (Figure 2). Higher frequencies are possible, but as frequency increases, small imbalances in the MAX4526/MAX4527's internal capacitance and resistance gradually impair performance. Similarly, imbalances in external circuit capacitance and resistance to GND reduce overall carrier suppression.

The carrier is applied as a logic-level square wave to IN. (Note that this voltage can go as negative as V-.) For best carrier suppression, the power-supply voltages should be equal, the square wave should have a precise 50% duty cycle, and both the input and output signals should be symmetrical about ground. Bypass V+ and V- to GND with 0.1µF ceramic capacitors, as close to the IC pins as possible. Since the logic-level translator/driver in the MAX4526 is faster than the one in the MAX4527, it gives better results at higher frequencies. In critical applications, carrier suppression can be optimized by trimming duty cycle, DC bias around GND, or external source and load capacitance.

In signal lines, balancing both capacitance and resistance to GND produces the best carrier suppression.

Transformer coupling of input and output signals provides the best isolation and carrier suppression. Transformers can also provide signal filtering, impedance matching, or low-noise voltage gain. Use a center-tapped transformer or high-resistance voltage divider to provide a DC path to GND on either the input signal or output signal. This ensures a DC path to GND and symmetrical operation of the internal switches.

Test Circuits/Timing Diagrams

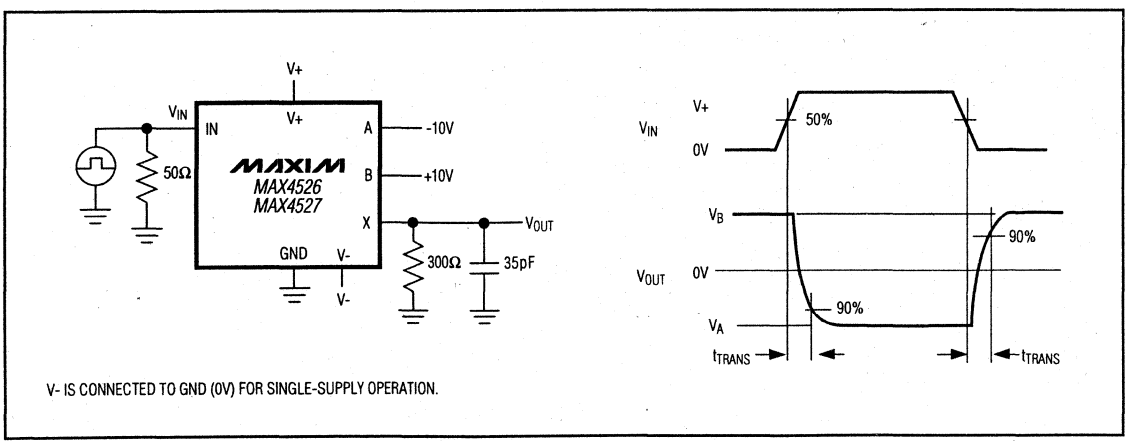


Figure 3. Address Transition Time

Test Circuits/Timing Diagrams (continued)

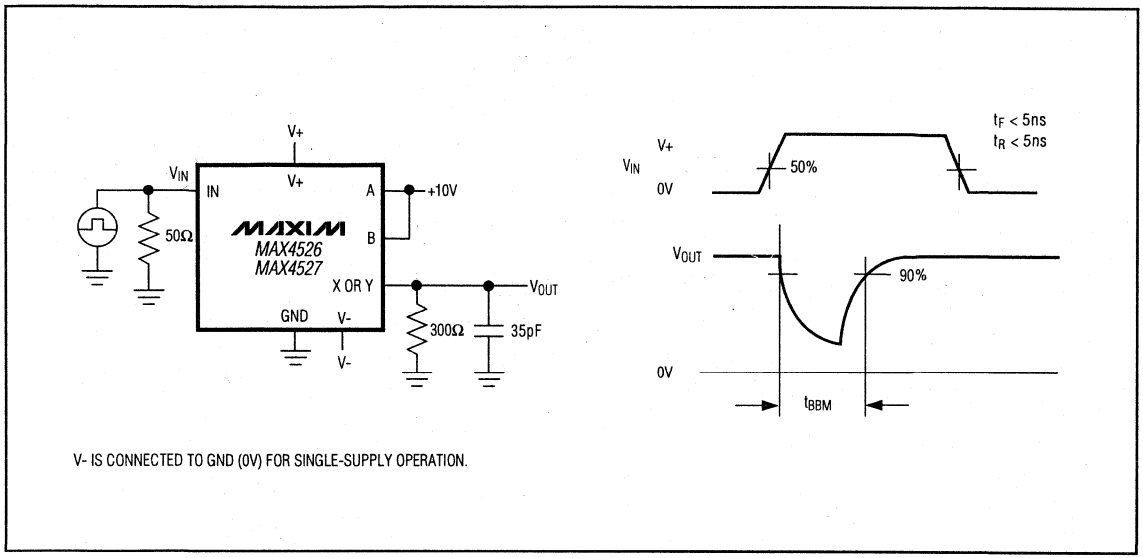


Figure 4. Break-Before-Make Interval

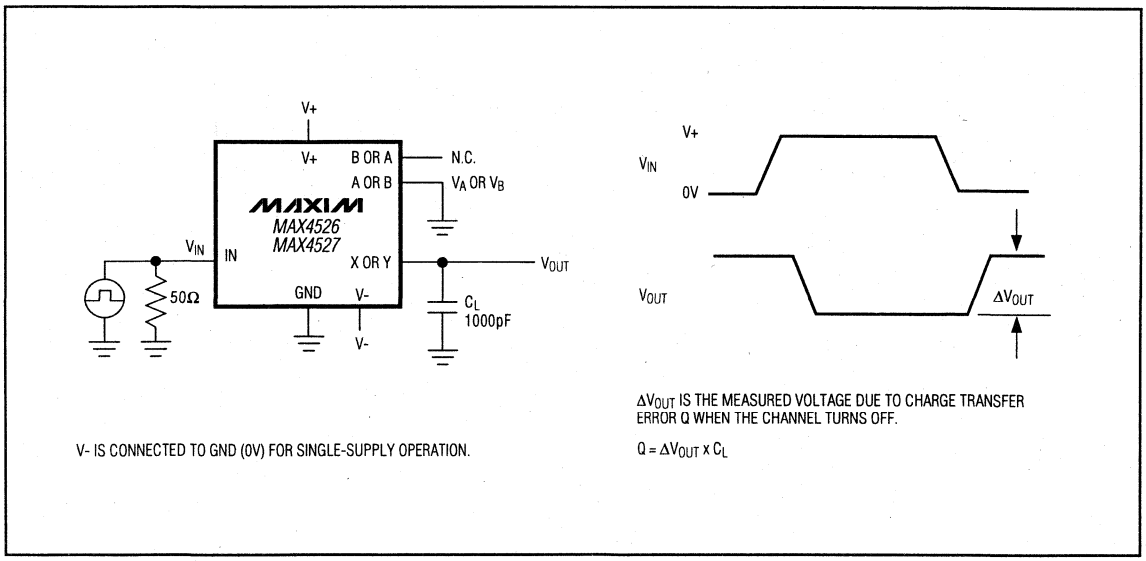


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

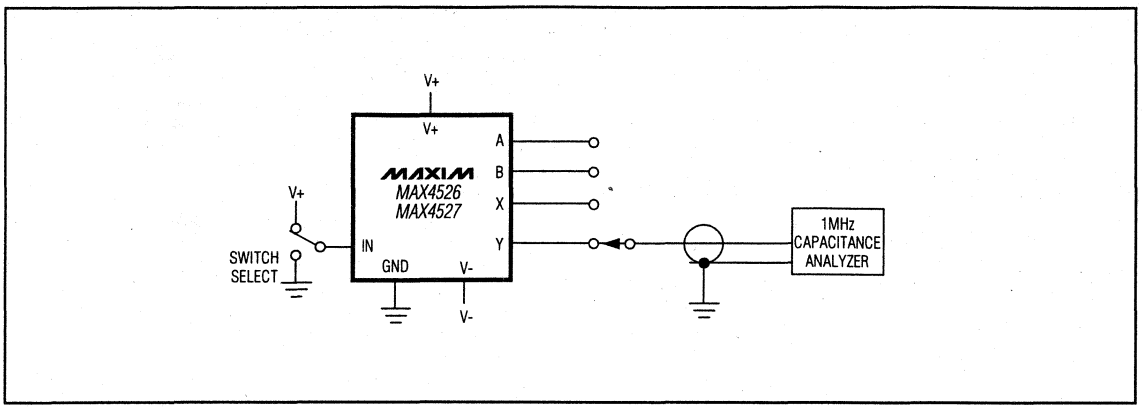


Figure 6. A, B, X, Y Capacitance

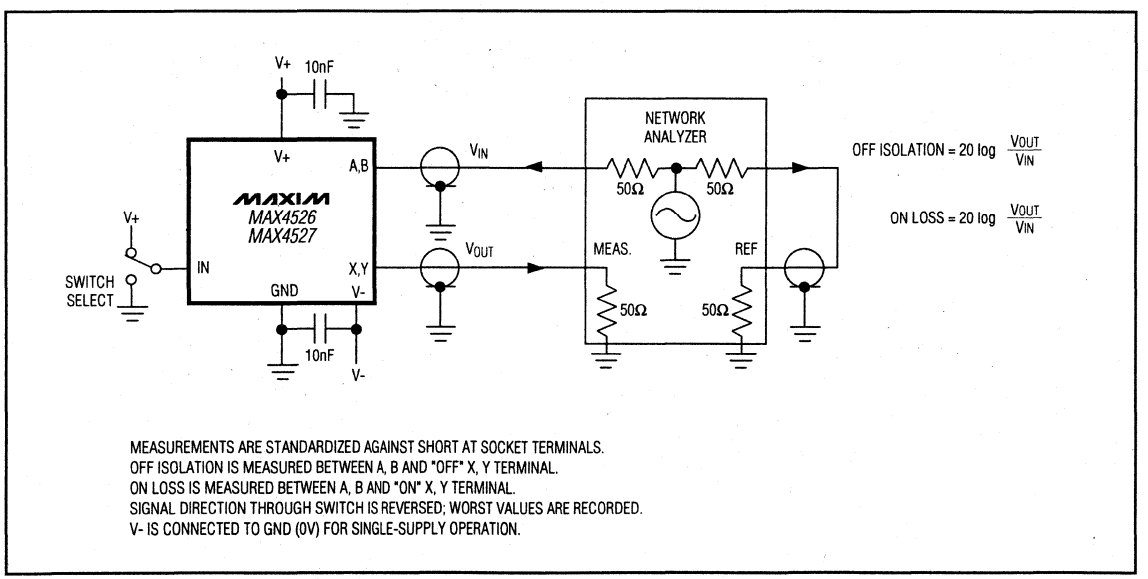


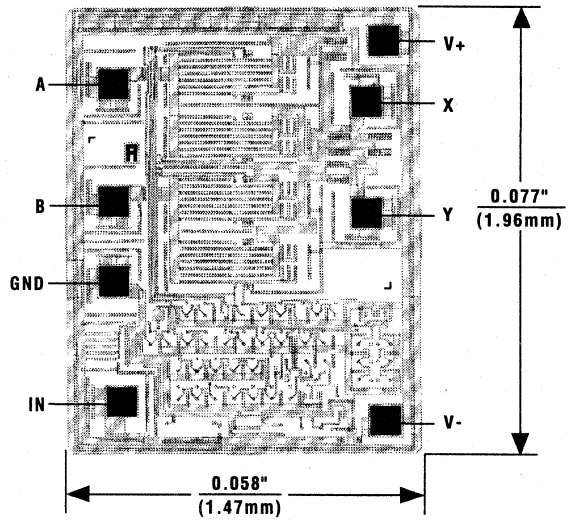
Figure 7. Off Isolation and On Loss

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4527CPA	0°C to +70°C	8 Plastic DIP
MAX4527CSA	0°C to +70°C	8 SO
MAX4527CUA	0°C to +70°C	8 µMAX
MAX4527C/D	0°C to +70°C	Dice*
MAX4527EPA	-40°C to +85°C	8 Plastic DIP
MAX4527ESA	-40°C to +85°C	8 SO
MAX4527EUA	-40°C to +85°C	8 µMAX

Contact factory for availability.

Chip Topography



TRANSISTOR COUNT: 50

SUBSTRATE IS INTERNALLY CONNECTED TO V+

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Low-Voltage, Phase-Reversal Analog Switch

General Description

The MAX4528 is a low-voltage, CMOS analog IC configured as a phase-reversal switch and optimized for high-speed applications such as chopper amplifiers.

The MAX4528 operates from a +2.7V to +12V single supply or from ±2.7V to ±6V dual supplies. On-resistance (120Ω max) is matched between switches to 4Ω (max). Each switch can handle Rail-to-Rail® analog signals. Off-leakage current is only 0.5nA at +25°C and 40nA at +85°C.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility.

Features

- ♦ **Low Charge Injection, 5pC (max)**
- ♦ **120Ω Signal Paths with ±5V Supplies**
- ♦ **Rail-to-Rail Signal Handling**
- ♦ **t_{ON}/t_{OFF} = 150ns/100ns at a ±5V Supply**
- ♦ **10µA (max) Power Consumption**
- ♦ **>2kV ESD Protection per Method 3015.7**
- ♦ **TTL/CMOS-Compatible Inputs**
- ♦ **Small Packages: 8-Pin DIP/SO**

Applications

Chopper-Stabilized Amplifiers

Balanced Modulators/Demodulators

Data Acquisition

Test Equipment

Audio-Signal Routing

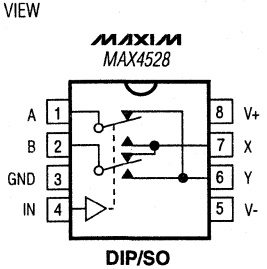
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4528CPA	0°C to +70°C	8 Plastic DIP
MAX4528CSA	0°C to +70°C	8 SO
MAX4528CUA	0°C to +70°C	8 µMAX
MAX4528C/D	0°C to +70°C	Dice*
MAX4528EPA	-40°C to +85°C	8 Plastic DIP
MAX4528ESA	-40°C to +85°C	8 SO
MAX4528EUA	-40°C to +85°C	8 µMAX

**Contact factory for dice specifications.*

Pin Configuration/ Functional Diagram/Truth Table

TOP VIEW



DIP/SO

TRUTH TABLE		
IN	A	B
0	Y	X
1	X	Y

NOTE: SWITCH POSITIONS SHOWN WITH IN = LOW

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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19-1162; Rev 0; 12/96

MAXIM

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

General Description

The MAX4530/MAX4531/MAX4532 are low-voltage, CMOS analog ICs configured as an 8-channel multiplexer (mux) (MAX4530), two 4-channel muxes (MAX4531), and three single-pole/double-throw switches (MAX4532). These devices are pin compatible with the industry-standard 74HC4351/74HC4352/74HC4353. All devices have two complementary switch-enable inputs and address latching.

The MAX4530/MAX4531/MAX4532 operate from a single supply of +2V to +12V, or from dual supplies of ±2V to ±6V. On-resistance (150Ω max) is matched between switches to 8Ω max. Each switch can handle rail-to-rail analog signals. Off-leakage current is only 1nA at T_A = +25°C and 50nA at T_A = +85°C.

All digital inputs have 0.8V and 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

Battery-Operated Equipment
Data Acquisition
Test Equipment
Avionics
Networking
ATE Equipment
Audio-Signal Routing

Features

- **Pin Compatible with 74HC4351/74HC4352/74HC4353**
- **±2.0V to ±6V Dual Supplies +2.0V to +12V Single Supply**
- **75Ω Signal Paths with ±5V Supplies 150Ω Signal Paths with +5V Supply**
- **Rail-to-Rail Signal Handling**
- **t_{ON} and t_{OFF} = 150ns and 120ns at ±4.5V**
- **<1µW Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Small, 20-Pin SSOP/SO/DIP Packages**

Ordering Information

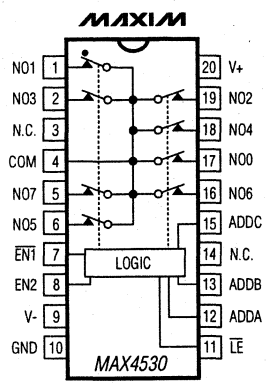
PART	TEMP. RANGE	PIN-PACKAGE
MAX4530CPP	0°C to +70°C	20 Plastic DIP
MAX4530CWP	0°C to +70°C	20 SO
MAX4530CAP	0°C to +70°C	20 SSOP
MAX4530C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

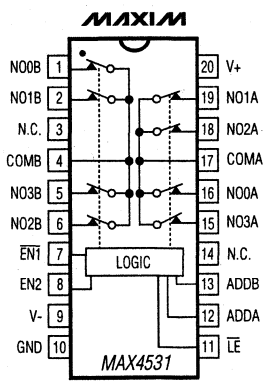
**Contact factory for availability.*

Pin Configurations

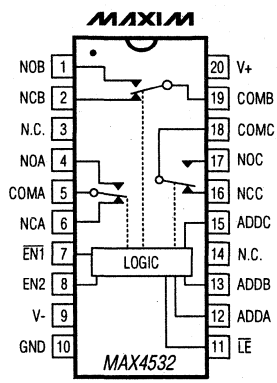
TOP VIEW



NARROW DIP/WIDE SO



NARROW DIP/WIDE SO



NARROW DIP/WIDE SO

N.C. = NOT CONNECTED

Truth Table appears at end of data sheet.

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For small orders, phone 408-737-7600 ext. 3468.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-
V+ ..... -0.3 to +13V
Voltage into Any Terminal (Note 1)
or ±20mA (whichever occurs first) ..... -0.3 to (V+ + 0.3V)
Continuous Current into Any Terminal ..... ±20mA
Peak Current, NO, NC, or COM_
(pulsed at 1ms, 10% duty cycle) ..... ±40mA
ESD per Method 3015.7 ..... >2000V

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX453_C_P ..... 0°C to +70°C
MAX453_E_P ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Voltages exceeding V+ or V- on any signal terminal are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, $V_{ADD_H} = V_{EN_H} = V_{\overline{LE}}$ = 2.4V, $V_{ADD_L} = V_{EN_L}$ = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog-Signal Range	V_{COM}, V_{NO}, $V_{NC_}$	(Note 3)			V-		V+	V
Channel On-Resistance	R_{ON}	I_{NO} = 2mA, V_{COM} = ±3.5V, V+ = +4.5V, V- = -4.5V		T_A = +25°C		45	75	Ω
				$T_A = T_{MIN}$ to T_{MAX}			100	
On-Resistance Matching Between Channels (Note 4)	ΔR_{ON}	I_{NO} = 2mA, V_{COM} = ±4.5V, V+ = +4.5V, V- = -4.5V		T_A = +25°C		1	8	Ω
				$T_A = T_{MIN}$ to T_{MAX}			12	
On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	I_{NO} = 2mA; V_{COM} = -3V, 0V, +3V; V+ = 5V; V- = -5V		T_A = +25°C		4	10	Ω
				$T_A = T_{MIN}$ to T_{MAX}			13	
NO-Off Leakage Current (Note 6)	$I_{NO(OFF)}$	V_{NO} = ±4.5V, V_{COM} = ∓4.5V, V+ = 5.5V, V- = -5.5V		T_A = +25°C	-1	0.01	1	nA
				$T_A = T_{MIN}$ to T_{MAX}	-10		10	
COM-Off Leakage Current (Note 6)	$I_{COM(OFF)}$	V_{COM} = ±4.5V, V_{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4530	T_A = +25°C	-2	0.01	2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
		V_{COM} = ±4.5V, V_{NO} = ∓4.5V, V+ = 5.5V, V- = -5.5V	MAX4531/ MAX4532	T_A = +25°C	-1	0.01	1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	
COM-On Leakage Current (Note 6)	$I_{COM(ON)}$	V_{COM} = ±4.5V, V+ = 5.5V, V- = -5.5V	MAX4530	T_A = +25°C	-2	0.01	2	nA
				$T_A = T_{MIN}$ to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1	0.01	1	
				$T_A = T_{MIN}$ to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, $V_{ADD_H} = V_{EN_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD_L} = V_{EN_L} = 0.8V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Logic High Threshold	V_{ADD_H}, V_{EN_H}, $V_{\overline{LE}}$		$T_A = T_{MIN}$ to T_{MAX}		1.5	2.4	V
Logic Low Threshold	V_{ADD_L}, V_{EN_L}, $V_{\overline{LE}}$		$T_A = T_{MIN}$ to T_{MAX}	0.8	1.5		V
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, $I_{\overline{LE}}$	$V_{ADD_H} = 2.4V$, $V_{ADD_L} = 0.8V$		-0.1	0.01	0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, $I_{\overline{LE}}$	$V_{ADD_H} = 2.4V$, $V_{ADD_L} = 0.8V$		-0.1		0.1	µA
SUPPLY							
Power-Supply Range	V+, V-			±2.0		±6	V
Positive Supply Current	I+	$V_{EN_} = V_{ADD_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	$T_A = +25°C$	-1	0.001	1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
Negative Supply Current	I-	$V_{EN_} = V_{ADD_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	$T_A = +25°C$	-1	0.001	1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
I_{GND} Supply Current	I_{GND}	$V_{EN_} = V_{ADD_} = V_{\overline{LE}} = 0V/V+$, V+ = 5.5V, V- = -5.5V	$T_A = +25°C$	-1		1	µA
			$T_A = T_{MIN}$ to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 1	$T_A = +25°C$		60	150	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3	$T_A = +25°C$	4	10		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 2	$T_A = +25°C$		10	150	ns
			$T_A = T_{MIN}$ to T_{MAX}			250	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 2	$T_A = +25°C$		40	100	ns
			$T_A = T_{MIN}$ to T_{MAX}			150	
Setup Time, Channel Select to Latch Enable	t_S	Figure 4	$T_A = +25°C$	50			ns
			$T_A = T_{MIN}$ to T_{MAX}	60			
Hold Time, Latch Enable to Channel Select	t_H	Figure 6	$T_A = +25°C$	0			ns
			$T_A = T_{MIN}$ to T_{MAX}	0			
Pulse Width, Latch Enable	t_{MPW}	Figure 5	$T_A = +25°C$	60			ns
			$T_A = T_{MIN}$ to T_{MAX}	70			
Charge Injection (Note 3)	Q	$C_L = 1nF$, $V_{NO} = 0V$, Figure 6	$T_A = +25°C$		1.5	5	pC
Off Isolation (Note 7)	V_{ISO}	$V_{EN2} = 0V$, $R_L = 1k\Omega$, f = 1MHz	$T_A = +25°C$		-65		dB
Crosstalk Between Channels	V_{CT}	$V_{\overline{EN1}} = 0V$, $V_{EN2} = 2.4V$, f = 1MHz, $V_{GEN} = 1V_{p-p}$, $R_L = 1k\Omega$	$T_A = +25°C$		-92		dB

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +5V ±10%, V- = -5V ±10%, GND = 0V, V_{ADD_H} = V_{EN_H} = $V_{\overline{LE}}$ = 2.4V, V_{ADD_L} = V_{EN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
Distortion, THD				T_A = +25°C		0.025		
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		3		pF
NO-Off Capacitance	$C_{NO(OFF)}$	f = 1MHz, V_{EN} = V_{COM} = 0V		T_A = +25°C		3		pF
COM-Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, V_{EN2} = V_{COM} = 0V	MAX4530	T_A = +25°C		15		pF
			MAX4531			9		
			MAX4532			6		
COM-On Capacitance	$C_{COM(ON)}$	f = 1MHz, V_{EN1} = V_{COM} = 0V, V_{EN2} = 2.4V	MAX4530	T_A = +25°C		26		pF
			MAX4531			20		
			MAX4532			17		

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{ADD_H} = V_{EN_H} = $V_{\overline{LE}}$ = 2.4V, V_{ADD_L} = V_{EN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{COM}, V_{NO}	(Note 3)			0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		80	150	Ω
				T_A = T_{MIN} to T_{MAX}			200	
On-Resistance Matching Between Channels (Notes 3, 4)	ΔR_{ON}	I_{NO} = 1mA, V_{COM} = 3.5V, V+ = 4.5V		T_A = +25°C		2	15	Ω
				T_A = T_{MIN} to T_{MAX}			20	
On-Resistance Flatness	R_{FLAT}	I_{NO} = 1mA; V_{COM} = 3V, 2V, 1V; V+ = 5V		T_A = +25°C		10		Ω
NO-Off Leakage Current (Note 8)	$I_{NO(OFF)}$	V_{NO} = 4.5V; V_{COM} = 4.5V, 1V; V+ = 5.5V		T_A = +25°C	-1		1	nA
				T_A = T_{MIN} to T_{MAX}	-10		10	
COM-Off Leakage Current (Note 8)	$I_{COM(OFF)}$	V_{COM} = 4.5V, 1V; V_{NO} = 1V, 4.5V; V+ = 5.5V	MAX4530	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	
COM-On Leakage Current (Note 8)	$I_{COM(ON)}$		MAX4530	T_A = +25°C	-2		2	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
			MAX4531/ MAX4532	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = +5V ±10%, V- = 0V, GND = 0V, V_{ADD_H} = V_{EN_H} = $V_{\overline{LE}}$ = 2.4V, V_{ADD_L} = V_{EN_L} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DIGITAL LOGIC INPUT							
Logic-High Threshold	V_{ADD_H}, V_{EN_H}, $V_{\overline{LE}}$		T_A = T_{MIN} to T_{MAX}		1.5	2.4	V
Logic-Low Threshold	V_{ADD_L}, V_{EN_L}, $V_{\overline{LE}}$		T_A = T_{MIN} to T_{MAX}	0.8	1.5		V
Input Current with Input Voltage High	I_{ADD_H}, I_{EN_H}, $I_{\overline{LE}}$	V_H = 2.4V, V_L = 0.8V		-0.1		0.1	µA
Input Current with Input Voltage Low	I_{ADD_L}, I_{EN_L}, $I_{\overline{LE}}$	V_H = 2.4V, V_L = 0.8V		-0.1		0.1	µA
SUPPLY							
Power-Supply Range				2.0		12	V
Positive Supply Current	I+	$V_{EN_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
Negative Supply Current	I-	$V_{EN_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
I_{GND} Supply Current	I_{GND}	$V_{EN_}$ = V_{ADD} = $V_{\overline{LE}}$ = 0V, V+; V+ = 5.5V; V- = 0V	T_A = +25°C	-1.0		1.0	µA
			T_A = T_{MIN} to T_{MAX}	-10		10	
DYNAMIC							
Transition Time	t_{TRANS}	Figure 1, V_{NO} = 3V	T_A = +25°C		90	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_{BBM}	Figure 3 (Note 3)	T_A = +25°C	10	20		ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	Figure 2	T_A = +25°C		100	200	ns
			T_A = T_{MIN} to T_{MAX}			250	
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	Figure 3	T_A = +25°C		40	100	ns
			T_A = T_{MIN} to T_{MAX}			125	
Set-Up Time, Channel Select to Latch Enable	t_S	Figure 7	T_A = +25°C	50			ns
			T_A = T_{MIN} to T_{MAX}	60			
Hold Time, Latch Enable to Channel Select	t_H	Figure 7	T_A = +25°C	0			ns
			T_A = T_{MIN} to T_{MAX}	0			
Pulse Width, Latch Enable	t_{MPW}	Figure 7	T_A = +25°C	60			ns
			T_A = T_{MIN} to T_{MAX}	70			
Charge Injection (Note 3)	Q	Figure 7, C_L = 1nF, V_{NO} = 0V	T_A = +25°C		1.5	5	pC

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to 3.6V, V- = 0V, GND = 0V, $V_{ADD_H} = V_{EN_H} = V_{\overline{LE}} = 2.4V$, $V_{ADD_L} = V_{EN_L} = 0.5V$, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		V+	V
On-Resistance	R_{ON}	I_{NO} = 1mA, V_{COM} = 1.5V, V+ = 2.7V	T_A = +25°C		220	500	Ω
			$T_A = T_{MIN}$ to T_{MAX}			600	
DYNAMIC							
Transition Time (Note 3)	t_{TRANS}	Figure 1, V_{IN} = 2.4V, V_{NO1} = 1.5V, V_{NO8} = 0V	T_A = +25°C		150	350	ns
Enable Turn-On Time (Note 3)	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		150	350	ns
Enable Turn-Off Time (Note 3)	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{NO1} = 1.5V	T_A = +25°C		60	150	ns
Set-Up Time, Channel Select to Latch Enable)	t_S	Note 3	T_A = +25°C	100			ns
Hold Time, Latch Enable to Channel Select	t_H	Note 3	T_A = +25°C	0			ns
Pulse Width, Latch Enable	t_{MPW}	Note 3	T_A = +25°C	120			ns

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = R_{ON}(max) - R_{ON}(min)$.

Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges, i.e., V_{NO} = 3V to 0V and 0V to -3V.

Note 6: Leakage parameters are 100% tested at maximum rated hot operating temperature, and guaranteed by correlation at T_A = +25°C.

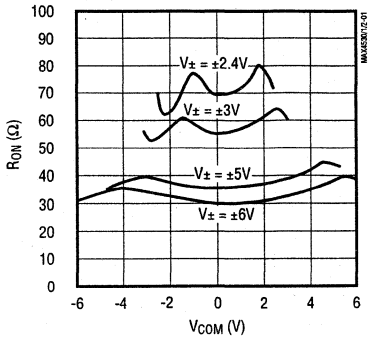
Note 7: Worst-case isolation is on channel 4 because of its proximity to the COM pin. Off isolation = 20log V_{COM} / V_{NO}, V_{COM} = output, V_{NO} = input to off switch.

Note 8: Leakage testing at single supply is guaranteed by correlation testing with dual supplies.

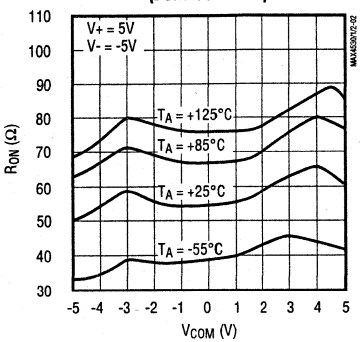
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

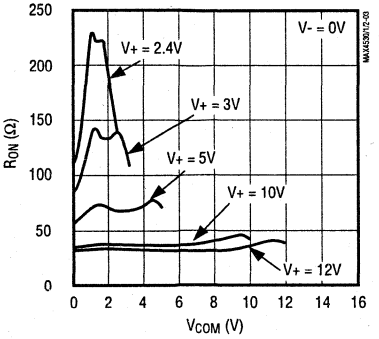
ON-RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



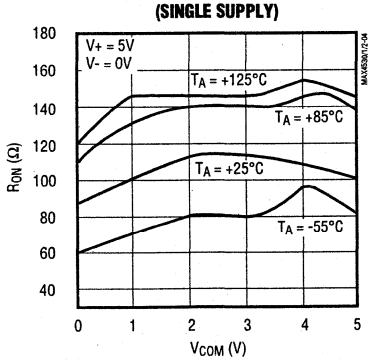
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



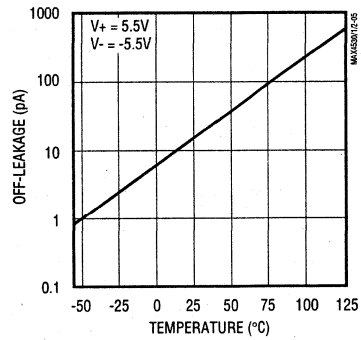
ON-RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



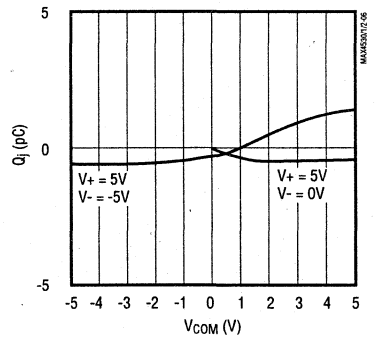
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



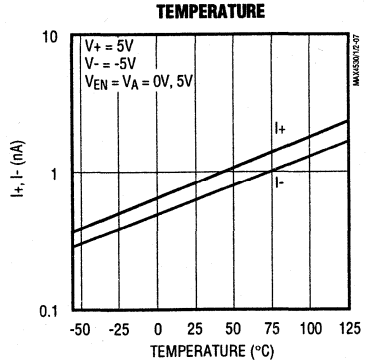
OFF-LEAKAGE vs. TEMPERATURE



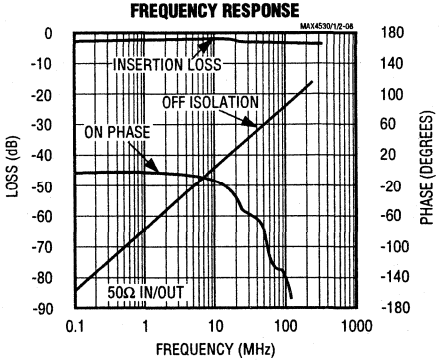
CHARGE INJECTION vs. V_{COM}



SUPPLY CURRENT vs. TEMPERATURE



FREQUENCY RESPONSE



Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Pin Description

PIN			NAME	FUNCTION
MAX4530	MAX4531	MAX4532		
17, 1, 19, 2, 18, 6, 16, 5	—	—	NO0–NO7	Analog Switch Inputs 0–7
—	1, 2, 6, 5	—	NO0B–NO3B	Analog Switch "B" Inputs 0–3
—	—	1	NOB	Analog Switch "B" Normally Open Input
—	—	2	NCB	Analog Switch "B" Normally Closed Input
3, 14	3, 14	3, 14	N.C.	Not Internally Connected
4	—	—	COM	Analog Switch Common
—	4	19	COMB	Analog Switch "B" Common
—	—	4	NOA	Analog Switch "A" Normally Open Input
—	17	5	COMA	Analog Switch "A" Common
—	—	6	NCA	Analog Switch "A" Normally Closed Input
7	7	7	EN1	Enable Logic Input #1 (see *Truth Table*).
8	8	8	EN2	Enable Logic Input #2 (see *Truth Table*).
9	9	9	V-	Negative Analog Supply Voltage Input. Connect to GND for single supply operation.
10	10	10	GND	Negative Digital Supply Voltage Input. Connect to digital ground. (Analog signals have no ground
11	11	11	LE	Address Latch Logic Input (see *Truth Table*).
12	12	12	ADDA	Address "A" Logic Input (see *Truth Table*).
13	13	13	ADDB	Address "B" Logic Input (see *Truth Table*).
15	—	15	ADDC	Address "C" Logic Input (see *Truth Table*).
—	16, 19, 18, 15	—	NO0A–NO3A	Analog Switch "A" Inputs 0–3
—	—	16	NCC	Analog Switch "C" Normally Closed Input
—	—	17	NOC	Analog Switch "C" Normally Open Input
—	—	18	COMC	Analog Switch "C" Common
20	20	20	V+	Positive Analog and Digital Supply-Voltage Input

NO_, NC_ and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in both directions.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Applications Information

Power-Supply Considerations

Overview

The MAX4530/MAX4531/MAX4532 construction is typical of most CMOS analog switches. They have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-. During normal operation, these and other reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all of the analog leakage current comes from the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages to the V+ and V- pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. For this reason, both sides of a given switch can show leakage currents of either the same or opposite polarity.

The analog-signal paths and GND are not connected.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels into switched V+ and V- signals to drive the analog signals' gates. This drive signal is the only connection between the logic supplies and signals and the analog supplies. V+ and V- have ESD-protection diodes to GND.

The logic-level thresholds are TTL/CMOS compatible when V+ = +5V. As V+ rises, the threshold increases slightly, so when V+ reaches +12V, the threshold is about 3.1V—above the TTL guaranteed, high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4530/MAX4531/MAX4532 operate with bipolar supplies between ±2.0V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the +13V absolute maximum rating.

Single Supply

The MAX4530/MAX4531/MAX4532 operate from a single supply between +2V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. At room temperature, they actually work with a single supply at, near, or below +1.7V, although as supply voltage decreases, switch on-resistance and switching times become very high.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on response has several minor peaks that are highly layout dependent. The problem is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -65dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams

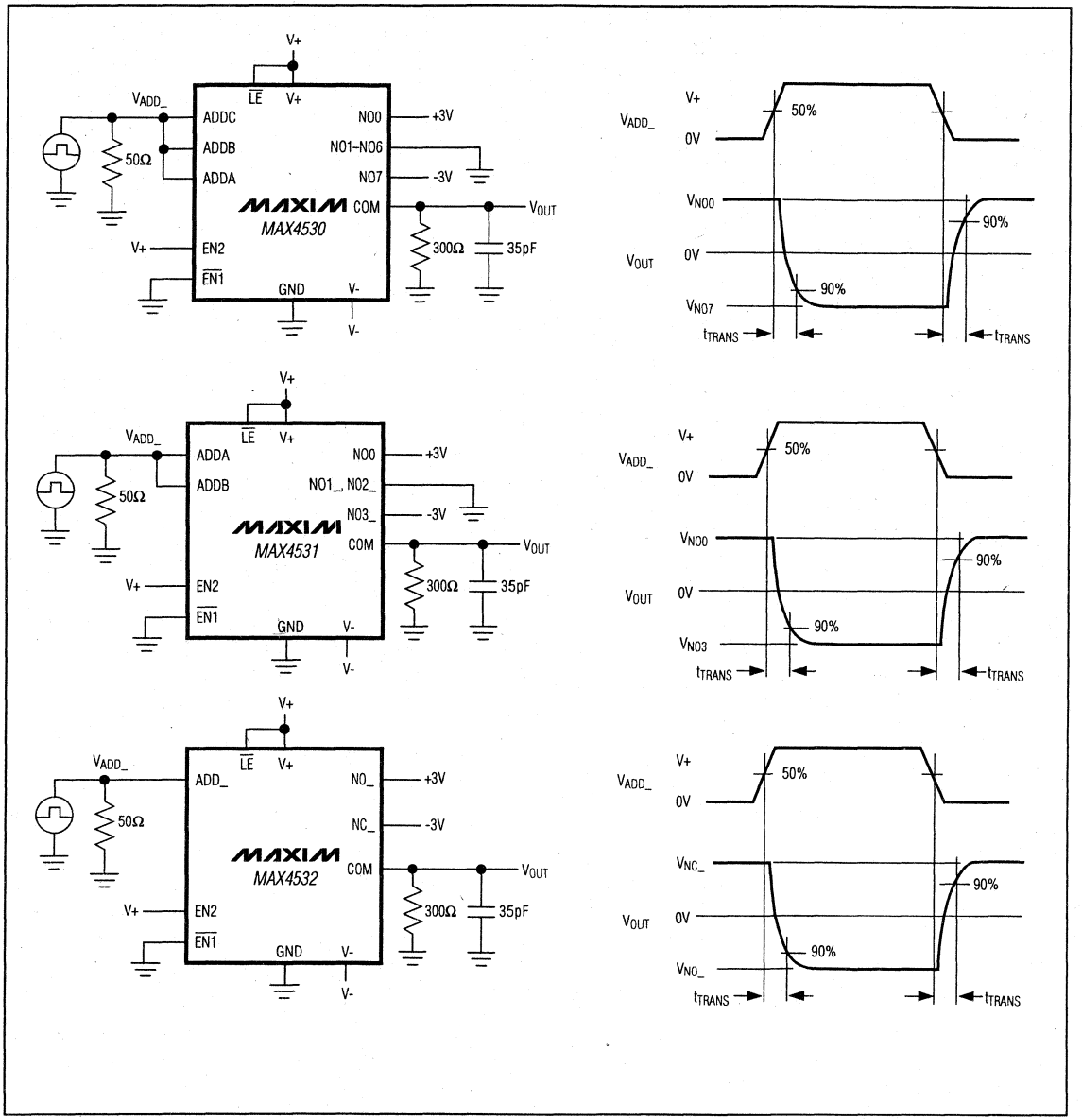


Figure 1. Address Transition Time

Test Circuits/Timing Diagrams (continued)

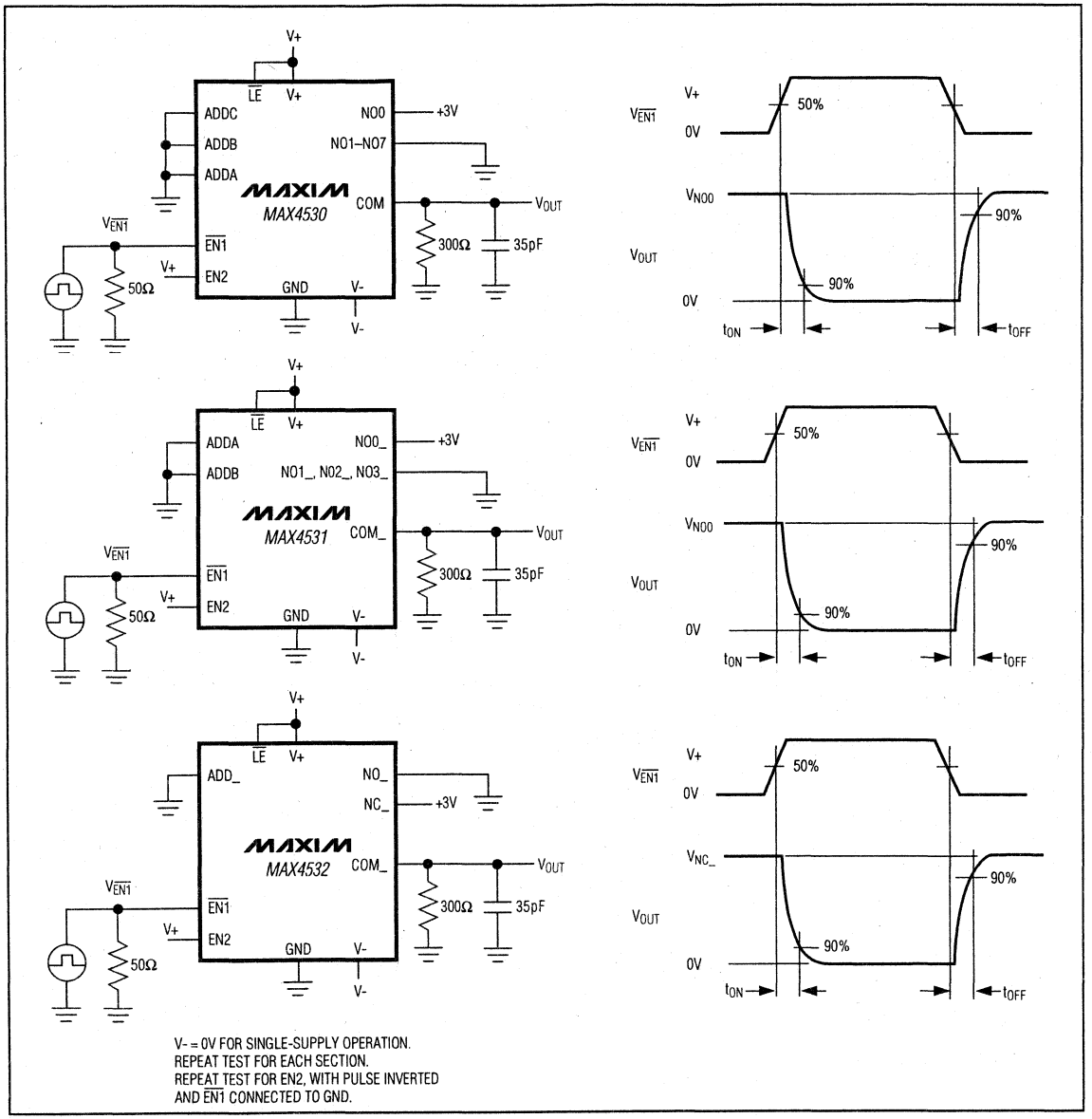
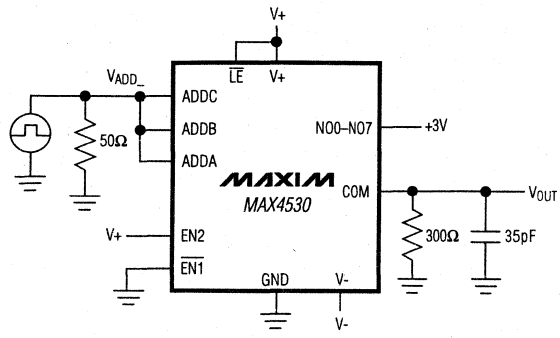
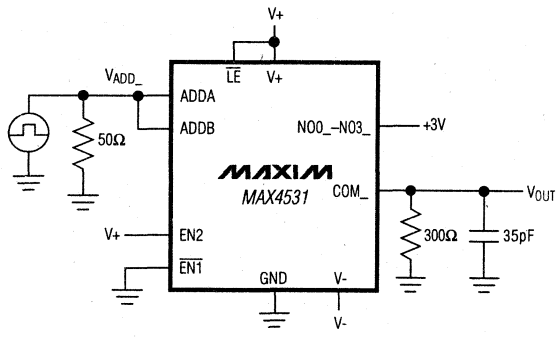


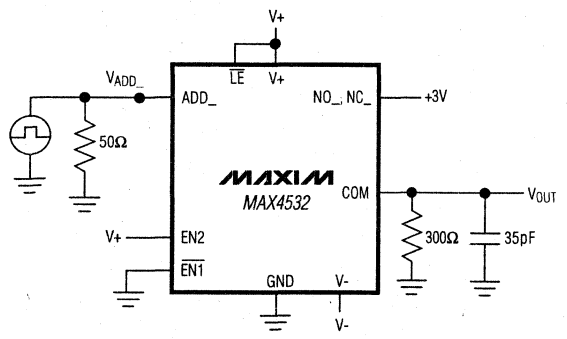
Figure 2. Enable Switching Time

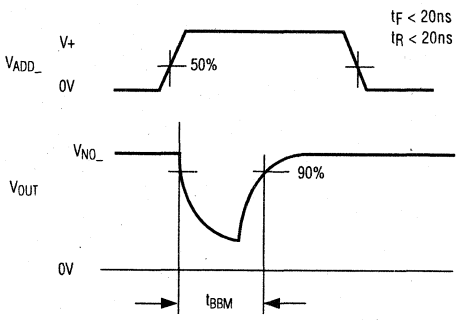
Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams (continued)









V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 3. Break-Before-Make Interval

Test Circuits/Timing Diagrams (continued)

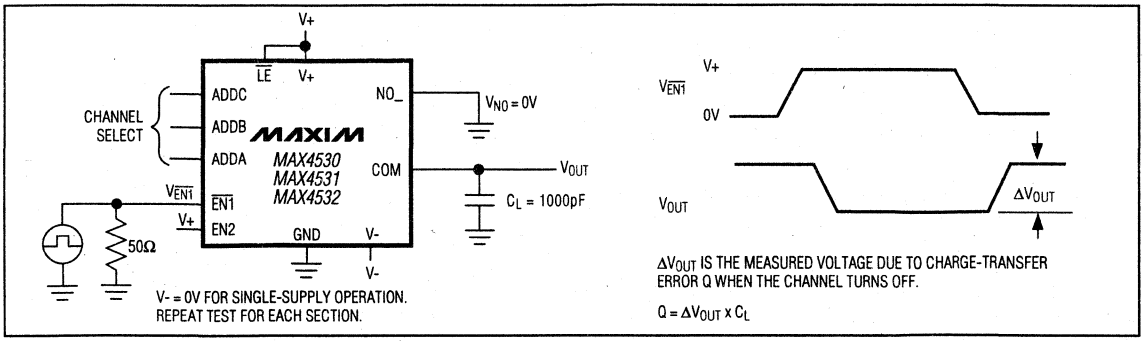


Figure 4. Charge Injection

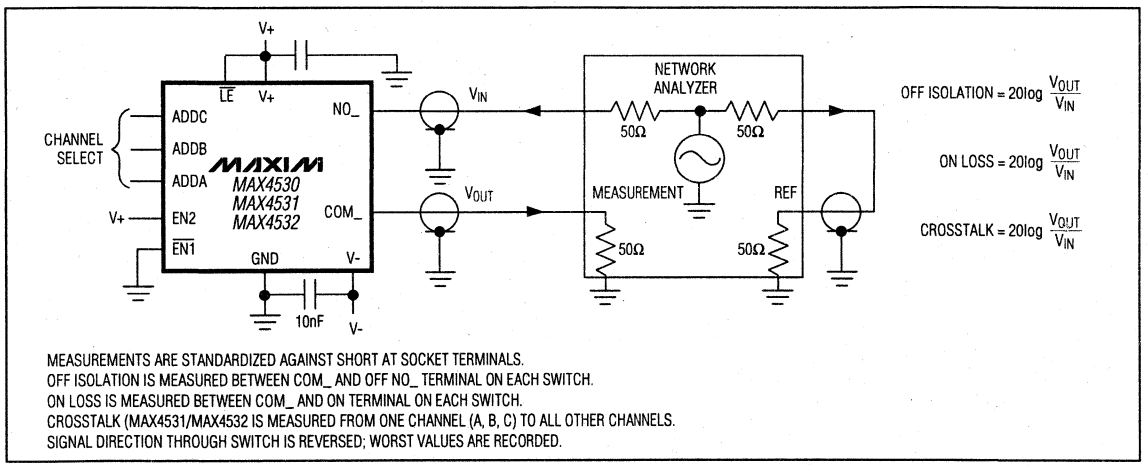


Figure 5. Off Isolation, On Loss, and Crosstalk

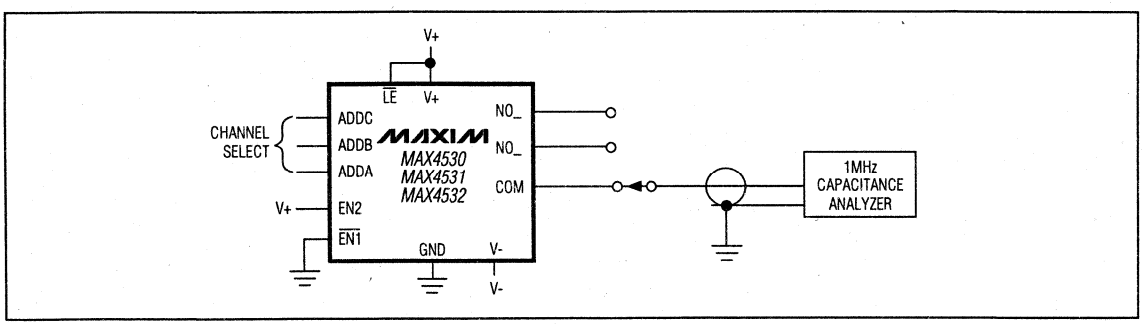
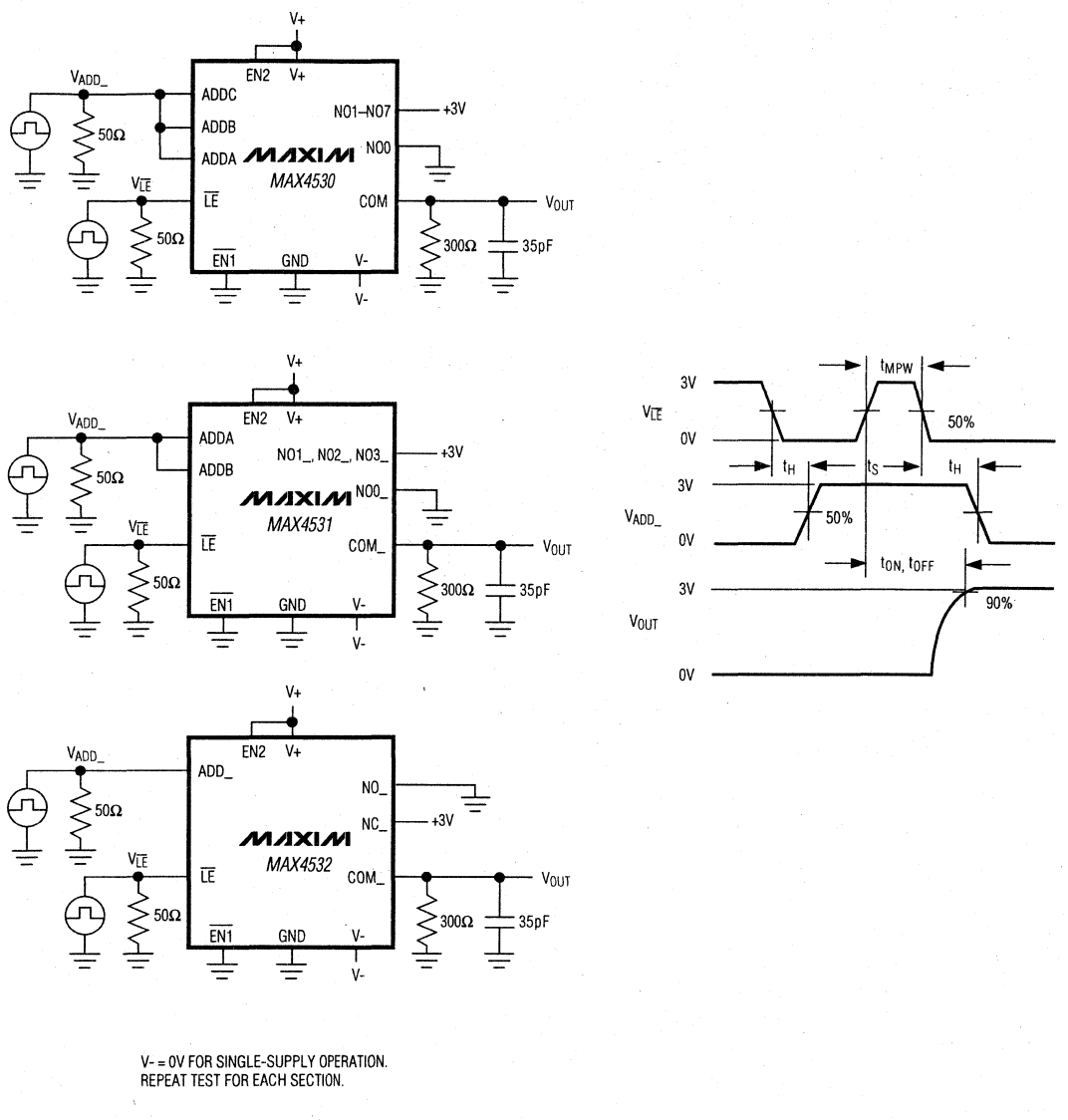


Figure 6. NO/COM Capacitance

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Test Circuits/Timing Diagrams (continued)



V- = 0V FOR SINGLE-SUPPLY OPERATION.
REPEAT TEST FOR EACH SECTION.

Figure 7. Setup and Hold Times, Minimum $\overline{LE}$ Width

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Truth Table/Switch Programming

$\overline{LE}$	EN2	$\overline{EN1}$	ADDRESS BITS			ON SWITCHES		
			ADDC*	ADDB	ADDA	MAX4530	MAX4531	MAX4532
0	1	0	X	X	X	Last address	Last address	Last address
X	0	X	X	X	X	All switches open	All switches open	All switches open
X	X	1	X	X	X	All switches open	All switches open	All switches open
1	1	0	0	0	0	COM–NO0	COMA–NO0A, COMB–NO0B	COMA–NCA, COMB–NCB, COMC–NCC
1	1	0	0	0	1	COM–NO1	COMA–NO1A, COMB–NO1B	COMA–NOA, COMB–NCB, COMC–NCC
1	1	0	0	1	0	COM–NO2	COMA–NO2A, COMB–NO2B	COMA–NCA, COMB–NOB, COMC–NCC
1	1	0	0	1	1	COM–NO3	COMA–NO3A, COMB–NO3B	COMA–NOA, COMB–NOB, COMC–NCC
1	1	0	1	0	0	COM–NO4	COMA–NO0A, COMB–NO0B	COMA–NCA, COMB–NCB, COMC–NOC
1	1	0	1	0	1	COM–NO5	COMA–NO1A, COMB–NO1B	COMA–NOA, COMB–NCB, COMC–NOC
1	1	0	1	1	0	COM–NO6	COMA–NO2A, COMB–NO2B	COMA–NCA, COMB–NOB, COMC–NOC
1	1	0	1	1	1	COM–NO7	COMA–NO3A, COMB–NO3B	COMA–NOA, COMB–NOB, COMC–NOC

X = Don't Care **ADDC not present on MAX4531.*

Note: NO_ and COM_ pins are identical and interchangeable. Either may be considered an input or an output; signals pass equally well in either direction. $\overline{LE}$ is independent of $\overline{EN1}$ and EN2.

Low-Voltage, CMOS Analog Multiplexers/Switches with Enable Inputs and Address Latching

Ordering Information (continued)

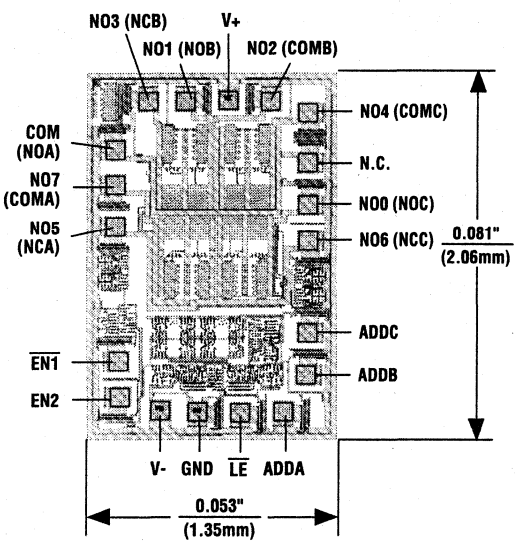
PART	TEMP. RANGE	PIN-PACKAGE
MAX4530EPP	-40°C to +85°C	20 Plastic DIP
MAX4530EWP	-40°C to +85°C	20 SO
MAX4530EAP	-40°C to +85°C	20 SSOP
MAX4531CPP	0°C to +70°C	20 Plastic DIP
MAX4531CWP	0°C to +70°C	20 SO
MAX4531CAP	0°C to +70°C	20 SSOP
MAX4531C/D	0°C to +70°C	Dice*
MAX4531EPP	-40°C to +85°C	20 Plastic DIP
MAX4531EWP	-40°C to +85°C	20 SO
MAX4531EAP	-40°C to +85°C	20 SSOP

PART	TEMP. RANGE	PIN-PACKAGE
MAX4532CPP	0°C to +70°C	20 Plastic DIP
MAX4532CWP	0°C to +70°C	20 SO
MAX4532CAP	0°C to +70°C	20 SSOP
MAX4532C/D	0°C to +70°C	Dice*
MAX4532EPP	-40°C to +85°C	20 Plastic DIP
MAX4532EWP	-40°C to +85°C	20 SO
MAX4532EAP	-40°C to +85°C	20 SSOP

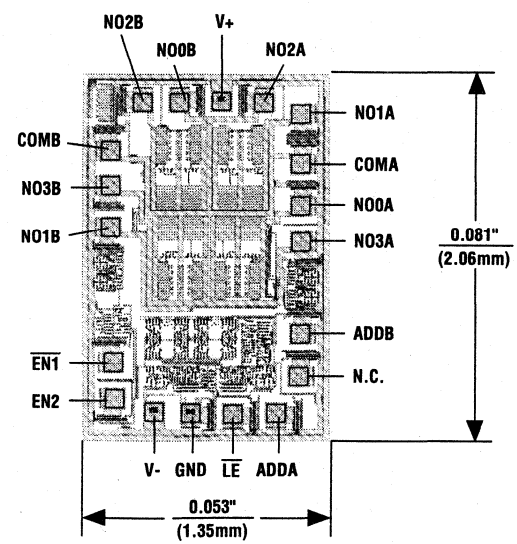
**Contact factory for availability.*

Chip Topographies

MAX4530/MAX4532



MAX4531



( ) ARE FOR MAX4532

TRANSISTOR COUNT: 255

SUBSTRATE CONNECTED TO V+

19-1148; Rev 0; 11/96

MAXIM

Quad, Low-Voltage, SPST Analog Switches with Enable

General Description

The MAX4536/MAX4537/MAX4538 are quad, low-voltage, single-pole/single-throw (SPST) analog switches with a common enable pin. They are pin compatible with the industry-standard 74HC4316. The MAX4536 has four normally open (NO) switches, and the MAX4537 has four normally closed (NC) switches. The MAX4538 has two NO switches and two NC switches.

These switches operate from a +2V to +12V single supply, or from ±2V to ±6V dual supplies. On-resistance (200Ω max) is matched between switches to 4Ω (max) and is flat (10Ω max) over the specified signal range. Each switch can handle rail-to-rail analog signals. The off-leakage current is only 1nA at +25°C and 10nA at +85°C.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility when using a single +5V supply or dual ±5V supplies.

Applications

Battery-Operated Equipment

Low-Voltage Data Acquisition

Test Equipment

Avionics

Portable Equipment

Audio-Signal Routing

Networking

Features

- **Pin Compatible with 74HC4316**
- **±2.0V to ±6V Dual Supplies**
  +2.0V to +12V Single Supply
- **Four Separately Controlled SPST Switches with Common Enable**
- **100Ω Signal Paths with Dual ±5V Supplies**
  200Ω Signal Paths with Single +4.5V Supply
- **Rail-to-Rail Signal Handling**
- **t_{ON} and t_{OFF} = 100ns and 80ns at ±4.5V Supply**
- **Less than 1µW Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**
- **Small Packages: PDIP, QSOP, Narrow SO**

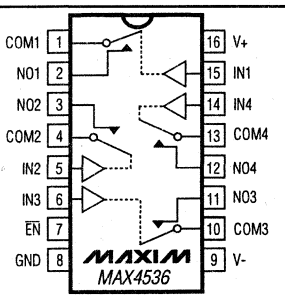
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4536CPE	0°C to +70°C	16 Plastic DIP
MAX4536CSE	0°C to +70°C	16 Narrow SO
MAX4536CEE	0°C to +70°C	16 QSOP
MAX4536C/D	0°C to +70°C	Dice*
MAX4536EPE	-40°C to +85°C	16 Plastic DIP
MAX4536ESE	-40°C to +85°C	16 Narrow SO
MAX4536EEE	-40°C to +85°C	16 QSOP

Ordering Information continued at end of data sheet.

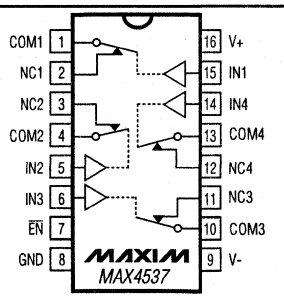
*Contact factory for availability.

Pin Configurations/Functional Diagrams/Truth Tables



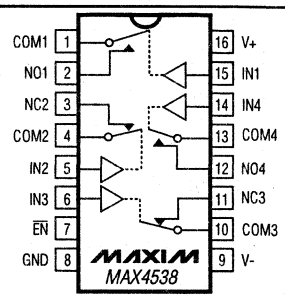
DIP/SO/QSOP

MAX4536		
$\overline{EN}$	IN_	SWITCH_
0	0	OFF
0	1	ON
1	X	OFF



DIP/SO/QSOP

MAX4537		
$\overline{EN}$	IN_	SWITCH_
0	0	ON
0	1	OFF
1	X	OFF



DIP/SO/QSOP

MAX4538			
$\overline{EN}$	IN_	SWITCHES 1, 4	SWITCHES 2, 3
0	0	OFF	ON
0	1	ON	OFF
1	X	OFF	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Quad, Low-Voltage, SPST Analog Switches with Enable

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to GND
V+ .....-0.3V to +13.0V
V- .....-13.0V to +0.3V
V+ to V- .....-0.3V to +13.0V
All Other Pins (Note 1) .....(V- -0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±10mA
Peak Current into Any Terminal
(pulsed at 1ms,10% duty cycle) .....±20mA
ESD per Method 3015.7 .....>2000V

Continuous Power Dissipation (T_A = +70°C) (Note 2)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
QSOP (derate 8.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX453_C_ E .....0°C to +70°C
MAX453_E_ E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NC_, NO_, COM_, $\overline{EN}$, or IN_ exceeding V+ or V- are clamped by internal diodes. Limit forward-diode current to maximum current rating.
Note 2: All leads are soldered or welded to PC boards.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—±5V Dual Supplies

(V+ = 4.5V to 5.5V, V- = -4.5V to -5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	V-		V+	V
COM_ NO_, COM_ NC_ On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		55	100	Ω
			C, E			125	
COM_ NO_, COM_ NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		1	4	Ω
			C, E			6	
COM_ NO_, COM_ NC_ On-Resistance Flatness (Note 6)	$R_{FLAT(ON)}$	V+ = 5.0V, V- = -5.0V, $V_{COM_}$ = -3.0V, 0, +3.0V, $I_{COM_}$ = 1mA	+25°C		4	10	Ω
			C, E			15	
NO_, NC_ Off-Leakage Current (Note 7)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ∓4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Note 7)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ∓4.5V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Note 7)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N__}$ = ±4.5V	+25°C	-2	0.01	2	nA
			C, E	-20		20	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		1.4	2.4	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.8	1.4		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—±5V Dual Supplies (continued)

(V+ = 4.5V to 5.5V, V- = -4.5V to -5.5V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V (Figure 1)	+25°C		35	100	ns
			C, E			125	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 4.5V, V- = -4.5V (Figure 1)	+25°C		15	50	ns
			C, E			60	
Break-Before-Make Time Delay (MAX4538 Only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5.5V, V- = -5.5V (Figure 2)	+25°C	5	15		ns
Charge Injection (Figure 3)	Q	C_L = 1.0nF, $V_{NO_}$ = 0V, R_S = 0Ω	+25°C		1	5	pC
NO_, NC_ Off-Capacitance (Figure 6)	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz	+25°C		2		pF
COM_ Off-Capacitance (Figure 6)	$C_{COM_(OFF)}$	$V_{COM_}$ = GND, f = 1MHz	+25°C		2		pF
COM_ On-Capacitance (Figure 7)	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = GND, f = 1MHz	+25°C		6		pF
Off-Isolation (Note 8, Figure 4)	V_{ISO}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 1MHz	+25°C		-65		dB
Channel-to-Channel Crosstalk (Note 9, Figure 5)	V_{CT}	R_L = 50Ω, C_L = 15pF, $V_{N_}$ = $1V_{RMS}$, f = 1MHz	+25°C		-75		dB
POWER SUPPLY							
Power-Supply Range	V+, V-		C, E	-6		6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	
V- Supply Current	I-	V- = -5.5V	+25°C	-1	0.05	1	µA
			C, E	-10		10	

Quad, Low-Voltage, SPST Analog Switches with Enable

ELECTRICAL CHARACTERISTICS—+5V Single Supply

(V+ = 4.5V to 5.5V, V- = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, $V_{\overline{EN}}$ = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	0		V+	V
COM_ -NO_, COM_ -NC_ On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		90	200	Ω
			C, E			225	
COM_ -NO_, COM_ -NC_ On-Resistance Match Between Channels (Note 5)	ΔR_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		2	8	Ω
			C, E			10	
NO_, NC_ Off-Leakage Current (Notes 7, 10)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V, $V_{N_}$ = +4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ Off-Leakage Current (Notes 7, 10)	$I_{COM_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V, $V_{N_}$ = +4.5V, 1V	+25°C	-1	0.01	1	nA
			C, E	-10		10	
COM_ On-Leakage Current (Note 7, 10)	$I_{COM_(ON)}$	V+ = 5.5V, $V_{COM_}$ = 1V, 4.5V,	+25°C	-2	0.01	2	nA
			C, E	-20		20	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		1.4	2.4	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.8	1.4		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 4.5V (Figure 1)	+25°C		50	100	ns
			C, E		20	125	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 4.5V (Figure 1)	+25°C			80	ns
			C, E			100	
Break-Before-Make Time Delay	t_{BBM}	MAX4538, $V_{COM_}$ = 3V, V+ = 5.5V (Figure 2)	+25°C	5	25		ns
Charge Injection (Figure 3) (Note 4)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	+25°C		1	5	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

ELECTRICAL CHARACTERISTICS—+3V Single Supply

(V+ = 2.7V to 3.6V, V- = 0V, V_{INH} = 2.0V, V_{INL} = 0.5V, $V_{\overline{EN}}$ = 0.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 3)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, V_{NC}	(Note 4)	C, E	0		V+	V
COM_ -NO_, COM_ -NC_ On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1.5V, $I_{COM_}$ = 0.1mA	+25°C		210	500	Ω
			C, E			600	
LOGIC INPUT							
$\overline{EN}$, IN_ Input Logic Threshold High	V_{INH}		C, E		0.9	2.0	V
$\overline{EN}$, IN_ Input Logic Threshold Low	V_{INL}		C, E	0.5	0.9		V
$\overline{EN}$, IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 4)							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V (Figure 1)	+25°C		80	250	ns
			C, E			300	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V (Figure 1)	+25°C		40	100	ns
			C, E			120	
Break-Before-Make Time Delay	t_{BBM}	MAX4538, $V_{COM_}$ = 1.5V, V+ = 3.6V (Figure 2)	+25°C	10	40		ns
Charge Injection (Figure 3)	Q	C_L = 1.0nF, V_{NO} = 0V, R_S = 0Ω	+25°C			3	pC
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

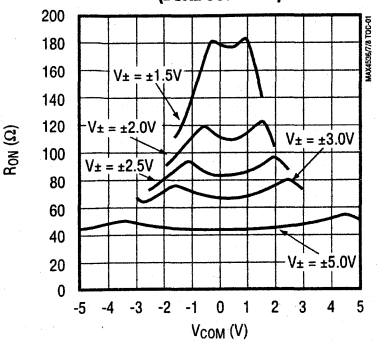
Note 3: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 4: Guaranteed by design.
Note 5: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 6: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog-signal range.
Note 7: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at T_A = +25°C.
Note 8: Off-isolation = $20\log_{10}$ [$V_{COM_}$ / ($V_{NC_}$ or $V_{NO_}$)], $V_{COM_}$ = output, $V_{NC_}$ or $V_{NO_}$ = input to off switch.
Note 9: Between any two switches.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad, Low-Voltage, SPST Analog Switches with Enable

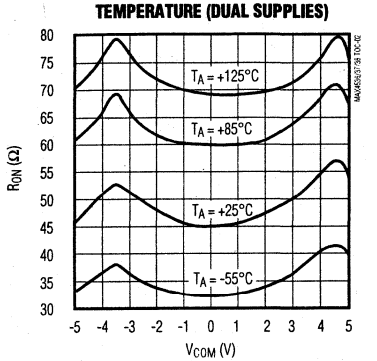
Typical Operating Characteristics

(V+ = +5V, V- = -5V GND = 0V, T_A = +25°C, unless otherwise noted.)

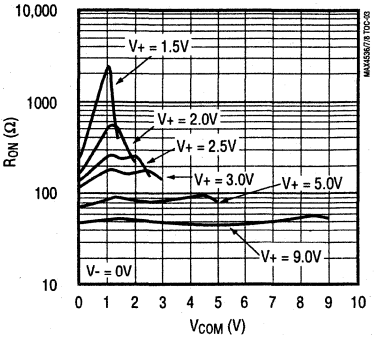
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



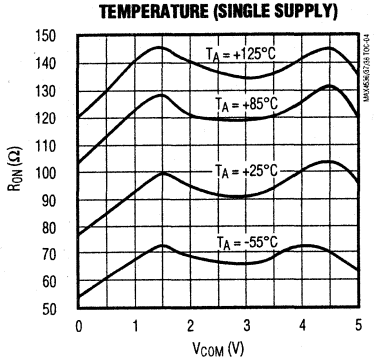
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



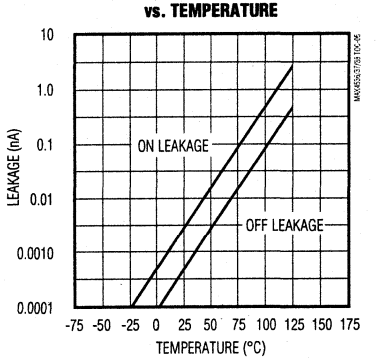
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



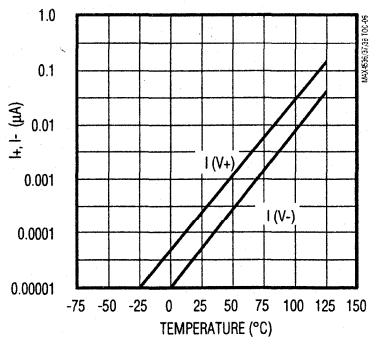
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



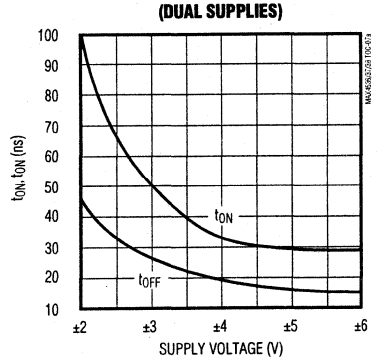
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



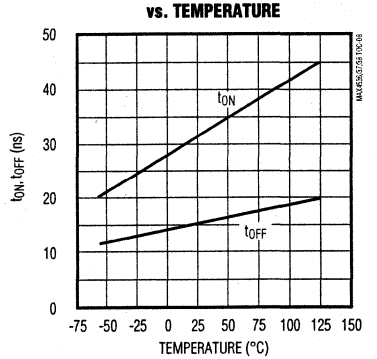
POWER-SUPPLY CURRENT vs. TEMPERATURE



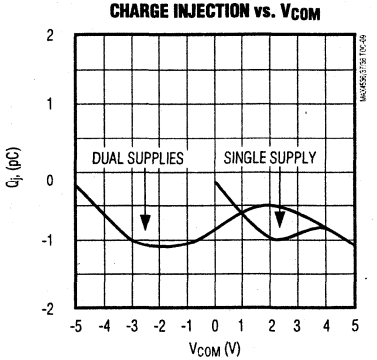
ON/OFF TIME vs. SUPPLY VOLTAGE (DUAL SUPPLIES)



ON/OFF TIME vs. TEMPERATURE



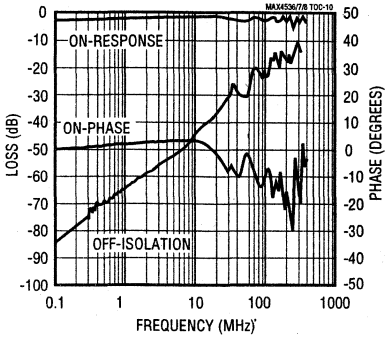
CHARGE INJECTION vs. VCOM



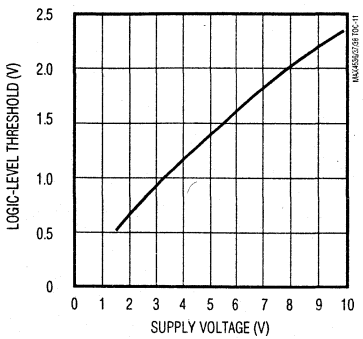
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V GND = 0V, T_A = +25°C, unless otherwise noted.)

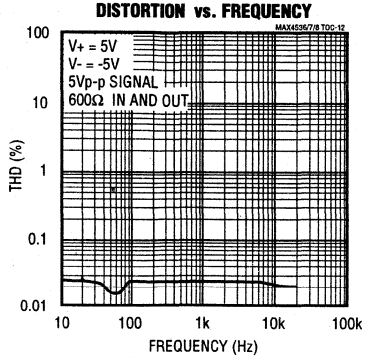
FREQUENCY RESPONSE



LOGIC-LEVEL THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 4, 10, 13	COM1–COM4	Analog Switch Common* Terminals
2, 3, 11, 12	NO1–NO4, or NC1–NC4	Analog Switch Normally Open* or Normally Closed* Terminals (see *Truth Tables*)
5, 6, 14, 15	IN1–IN4	Logic-Control Digital Inputs. Control each switch (see *Truth Tables*), except when $\overline{EN}$ is high.
7	$\overline{EN}$	Disable Logic Input. Connect logic high to $\overline{EN}$ to disable (open) all switches.
8	GND	Ground. Connect to digital ground. (Analog signals have no ground reference; they are limited to V+ and V-.)
9	V-	Negative Analog Supply-Voltage Input. Connect V- to GND for single-supply operation.
16	V+	Positive Analog and Digital Supply-Voltage Input. Internally connected to substrate.

**NO_/NC_ and COM_ pins are identical and interchangeable. Either may be considered as an input or an output; signals pass equally well in either direction.*

Quad, Low-Voltage, SPST Analog Switches with Enable

Applications Information

Power-Supply Considerations

Overview

The MAX4536/MAX4537/MAX4538 construction is typical of most CMOS analog switches. These devices have three supply pins: V+, V-, and GND. V+ and V- drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog-signal pin, and both V+ and V-. One of these diodes conducts if any analog signal exceeds V+ or V-. These reverse-biased ESD diodes leak during normal operation, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog-signal path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog-signal paths and GND. The analog-signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase to V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog switches' gates. This drive signal is the only connection between the logic supplies and the analog supplies. V+, and V- have ESD-protection diodes to GND. The logic-level inputs have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog-signal voltage.

The logic-level thresholds are CMOS/TTL-compatible when V+ is +5V. The threshold increases slightly as V+ is raised. When V+ reaches +12V, the level threshold is about 3.1V, above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The MAX4536/MAX4537/MAX4538 operate with bipolar supplies between ±2.0V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4536/MAX4537/MAX4538's V+ to +3V and then connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs in excess of the absolute maximum ratings can damage the part and/or external circuits.**

CAUTION: The absolute maximum V+ to V- differential voltage is 13.0V. Typical ±6V or +12V supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4536/MAX4537/MAX4538. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single Supplies

The MAX4536/MAX4537/MAX4538 operate from single supplies between +2.0V and +12V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see *Typical Operating Characteristics*). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem with high-frequency operation is not in turning the switch on, but in turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off-isolation is about -44dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off-isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Quad, Low-Voltage, SPST Analog Switches with Enable

Test Circuits/Timing Diagrams

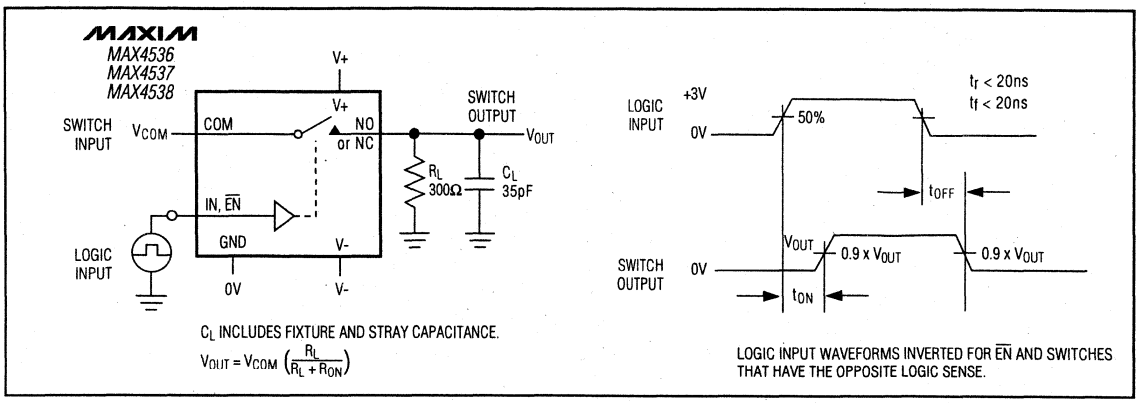


Figure 1. Switching Time

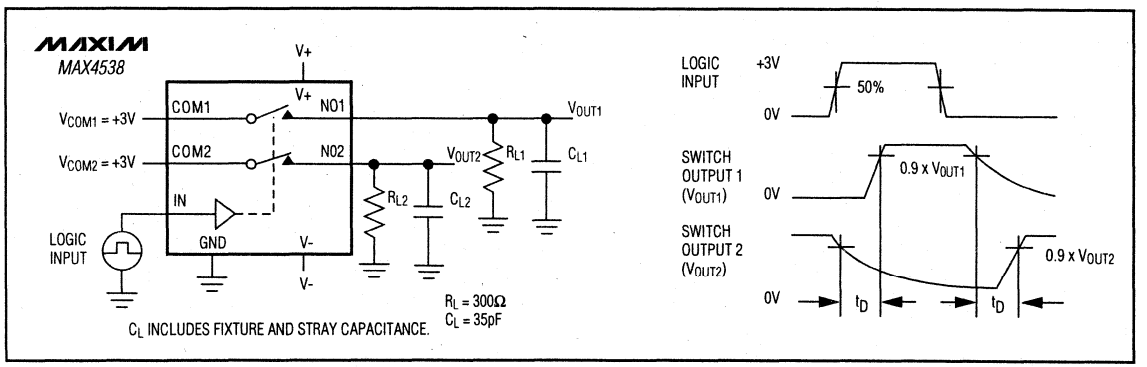


Figure 2. Break-Before-Make Interval (MAX4538 only)

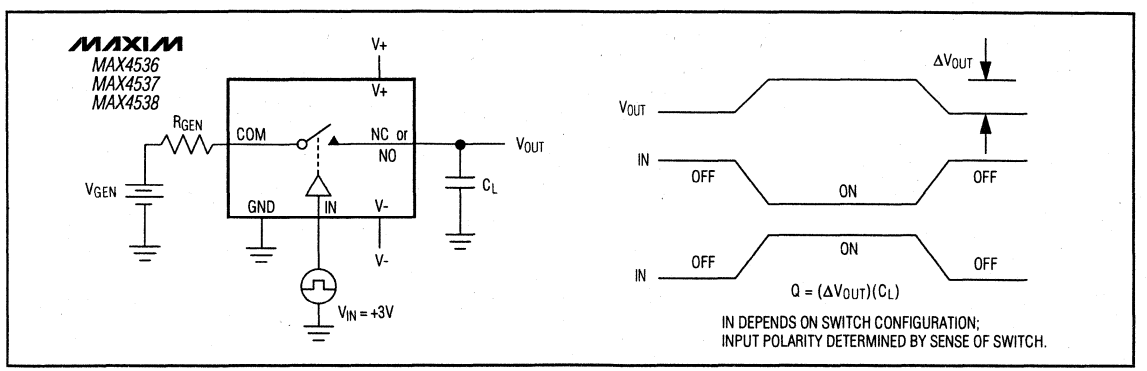


Figure 3. Charge Injection

Quad, Low-Voltage, SPST Analog Switches with Enable

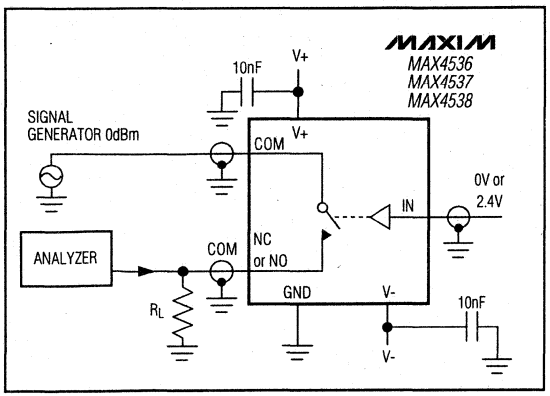


Figure 4. Off Isolation

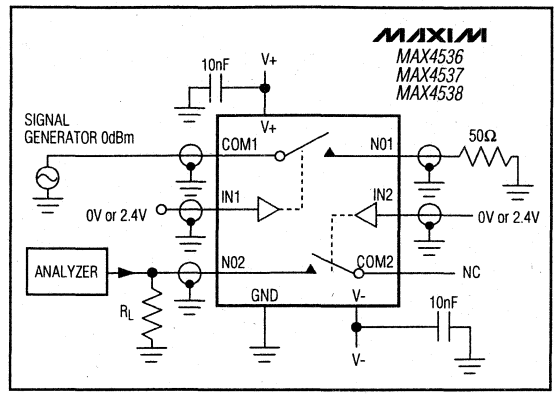


Figure 5. Crosstalk

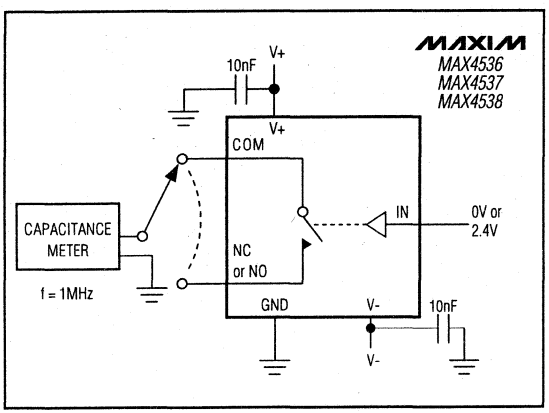


Figure 6. Channel-Off Capacitance

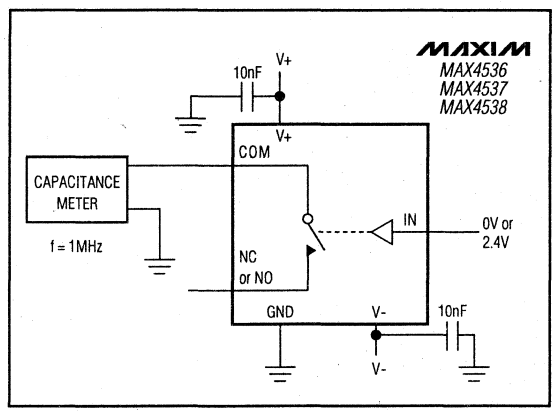


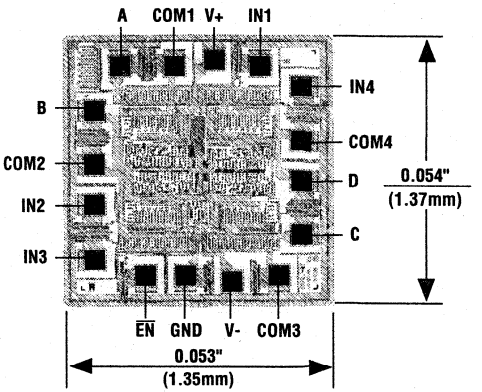
Figure 7. Channel-On Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4537CPE	0°C to +70°C	16 Plastic DIP
MAX4537CSE	0°C to +70°C	16 Narrow SO
MAX4537CEE	0°C to +70°C	16 QSOP
MAX4537C/D	0°C to +70°C	Dice*
MAX4537EPE	-40°C to +85°C	16 Plastic DIP
MAX4537ESE	-40°C to +85°C	16 Narrow SO
MAX4537EEE	-40°C to +85°C	16 QSOP
MAX4538CPE	0°C to +70°C	16 Plastic DIP
MAX4538CSE	0°C to +70°C	16 Narrow SO
MAX4538CEE	0°C to +70°C	16 QSOP
MAX4538C/D	0°C to +70°C	Dice*
MAX4538EPE	-40°C to +85°C	16 Plastic DIP
MAX4538ESE	-40°C to +85°C	16 Narrow SO
MAX4538EEE	-40°C to +85°C	16 QSOP

**Contact factory for availability.*

Chip Topography



MAX4536		MAX4537		MAX4538	
PIN	NAME	PIN	NAME	PIN	NAME
A	NO1	A	NC1	A	NO1
B	NO2	B	NC2	B	NC2
C	NO3	C	NC3	C	NC3
D	NO4	D	NC4	D	NO4

TRANSISTOR COUNT: 121

SUBSTRATE IS INTERNALLY CONNECTED TO V+

19-1202; Rev 0; 4/97

MAXIM

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

General Description

The MAX4541–MAX4544 are precision, dual analog switches designed to operate from a single +2.7V to +12V supply. Low power consumption (5µW) makes these parts ideal for battery-powered equipment. These switches offer low leakage currents (100pA max) and fast switching speeds (t_{ON} = 150ns max, t_{OFF} = 100ns max).

When powered from a +5V supply, the MAX4541–MAX4544 offer 2Ω max matching between channels, 60Ω max on-resistance (R_{ON}), and 6Ω max R_{ON} flatness.

These switches also offer 5pC max charge injection and a minimum of 2000V ESD protection per Method 3015.7.

The MAX4541/MAX4542/MAX4543 are single-pole/single-throw (SPST) devices, and the MAX4544 is a single-pole/double-throw (SPDT) device. The MAX4541 has two normally open (NO) switches, and the MAX4542 has two normally closed (NC) switches. The MAX4543 has one NO and one NC switch and can be used as a SPDT, while the MAX4544/MAX4545 are SPDT.

Applications

Battery-Operated Systems	Sample-and-Hold Circuits
Heads-Up Displays	Guidance and Control Systems
Audio and Video Switching	Military Radios
Test Equipment	Communications Systems
+3V/+5V DACs and ADCs	PBX, PABX

Features

- **Low On-Resistance (R_{ON}): 60Ω Max (33Ω typ)**
- **R_{ON} Matching Between Channels: 2Ω Max**
- **R_{ON} Flatness: 6Ω Max**
- **Guaranteed Charge Injection: 5pC Max**
- **Single-Supply Operation (+2.7V to +12V)**
- **Low Power Consumption: <5µW**
- **Low Leakage Current Over Temperature: 10nA Max at +85°C**
- **Fast Switching: t_{ON} = 35ns, t_{OFF} = 25ns**
- **Guaranteed Break-Before-Make (MAX4543/MAX4544 only)**
- **TTL/CMOS-Logic Compatible**
- **Pin Compatible with MAX323–MAX325**
- **MAX4544 Available in SOT23-6**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4541CPA	0°C to +70°C	8 Plastic DIP
MAX4541CSA	0°C to +70°C	8 SO
MAX4541CUA	0°C to +70°C	8 µMAX
MAX4541C/D	0°C to +70°C	Dice*
MAX4541EPA	-40°C to +85°C	8 Plastic DIP
MAX4541ESA	-40°C to +85°C	8 SO
MAX4541EUA	-40°C to +85°C	8 µMAX

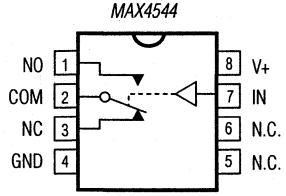
Ordering Information continued at end of data sheet.

**Dice are tested at T_A = +25°C.*

Pin Configurations/Functional Diagrams/Truth Tables

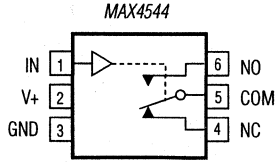
TOP VIEW

MAXIM
MAX4544



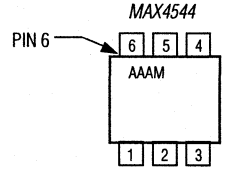
DIP/SO/µMAX

MAXIM
MAX4544



SOT23-6*

MAXIM
MAX4544



*NOTE: SOT23-6 PACKAGE HAS LETTERING NEAREST PIN 6

MAX4544		
LOGIC	**NC**	**NO**
0	ON	OFF
1	OFF	ON

SWITCHES SHOWN FOR "0" INPUT

N.C. = NOT INTERNALLY CONNECTED

MAX4541/MAX4542/MAX4543 SHOWN AT END OF DATA SHEET.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to GND
V+ .....-0.3V to +13V
IN_, COM_, NC_, NO_ (Note 1) .....-0.3V to (V+ + 0.3V)
Continuous Current (any terminal) .....±10mA
Peak Current, COM_, NO_, NC_
(pulsed at 1ms, 10% duty cycle max) .....±20mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
Narrow SO (derate 5.88mW/°C above +70°C) 471mW
μMAX (derate 4.10mW/°C above +70°C) 330mW
SOT23-6 (derate 7.1mW/°C above +70°C) 571mW
Operating Temperature Ranges
MAX454_C_ _ .....0°C to +70°C
MAX454_E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on NC, NO, COM, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 9)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH								
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)			0		V+	V
On-Resistance	R_{ON}	V+ = 4.5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V	T_A = +25°C			30	60	Ω
			T_A = T_{MIN} to T_{MAX}				75	
On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 3.5V	T_A = +25°C			0.8	2	Ω
			T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Notes 3, 5)	$R_{FLAT(ON)}$	V+ = 5V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1V, 2V, 3V	T_A = +25°C			2	6	Ω
			T_A = T_{MIN} to T_{MAX}				8	
NO or NC Off Leakage Current (Note 6)	$I_{NO(OFF)}$ or $I_{NC(OFF)}$	V+ = 5.5V; V_{COM} = 1V, 4.5V; V_{NO} or V_{NC} = 4.5V, 1V	T_A = +25°C		-0.1	0.01	0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
COM Off Leakage Current (Note 6)	$I_{COM(OFF)}$	V+ = 5.5V; V_{COM} = 4.5V, 1V; V_{NO} or V_{NC} = 1V, 4.5V	T_A = +25°C		-0.1		0.1	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-5		5	
COM On Leakage Current (Note 6)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = 1V, 4.5V or V_{NO} or V_{NC} = 1V, 4.5V	T_A = +25°C		-0.2		0.2	nA
			T_A = T_{MIN} to T_{MAX}	C, E	-10		10	

ELECTRICAL CHARACTERISTICS—Single +5V Supply (continued)

(V+ = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 9)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
DYNAMIC							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 3V	T_A = +25°C		35	100	ns
			T_A = T_{MIN} to T_{MAX}			240	
Turn-Off Time	t_{OFF}	V_{NO} or V_{NC} = 3V	T_A = +25°C		25	75	ns
			T_A = T_{MIN} to T_{MAX}			150	
Break-Before-Make Time Delay (Note 3)	t_D	MAX4543/MAX4544 only, R_L = 300Ω, C_L = 35pF		2	10		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V, T_A = +25°C, Figure 4			1	5	pC
Off Isolation (Note 7)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, T_A = +25°C, Figure 5			-76		dB
Crosstalk (Note 8)		R_L = 50Ω, C_L = 5pF, f = 1MHz, T_A = +25°C, Figure 6			-90		dB
NC or NO Capacitance	C_{OFF}	f = 1MHz, T_A = +25°C, Figure 7			8		pF
COM Off Capacitance	$C_{COM(OFF)}$	f = 1MHz, T_A = +25°C, Figure 7			8		pF
COM On Capacitance	$C_{COM(ON)}$	f = 1MHz, T_A = +25°C, Figure 8	MAX4541/2/3		13		pF
			MAX4544		20		
SUPPLY							
Power-Supply Range	V+			2.7		12	V
Positive Supply Current	I+	V+ = 5.5V, V_{IN} = 0V or V+, all channels on or off		-1	0.0001	1	µA
LOGIC INPUT							
Input Voltage Low	V_{INL}					0.8	V
Input Voltage High	V_{INH}			2.4			V

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

ELECTRICAL CHARACTERISTICS—Single +3.3V Supply

(V+ = 3.0V to 3.6V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 9)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	V_{COM}, V_{NO}, V_{NC}	(Note 3)		0		V+	V
Channel On-Resistance	R_{ON}	V+ = 3V, I_{COM} = 1.0mA, V_{NO} or V_{NC} = 1.5V	T_A = +25°C		50	125	Ω
			T_A = T_{MIN} to T_{MAX}			275	
DYNAMIC							
Turn-On Time (Note 3)	t_{ON}	V_{NO} or V_{NC} = 1.5V	T_A = +25°C		80	400	ns
			T_A = T_{MIN} to T_{MAX}			500	
Turn-Off Time (Note 3)	t_{OFF}	V_{NO} or V_{NC} = 1.5V	T_A = +25°C		50	125	ns
			T_A = T_{MIN} to T_{MAX}			175	
Break-Before-Make Time Delay (Note 3)	t_D	MAX4543/MAX4544 only, R_L = 300Ω, C_L = 35pF	T_A = +25°C	2	30		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V	T_A = +25°C		1	5	pC
SUPPLY							
Positive Supply Current	I+	V+ = 3.6V, V_{IN} = 0V or V+, all channels on or off		-1		1	µA

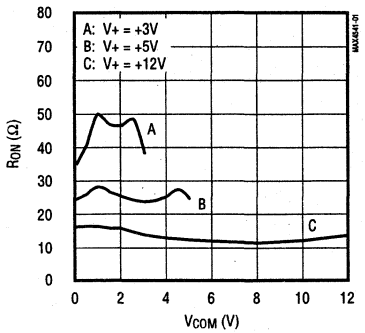
Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min.
Note 5: Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off Isolation = 20 $\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between the two switches.
Note 9: SOT packaged parts are 100% tested at +25°C only and guaranteed by correlation at the full hot rated temperature.

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

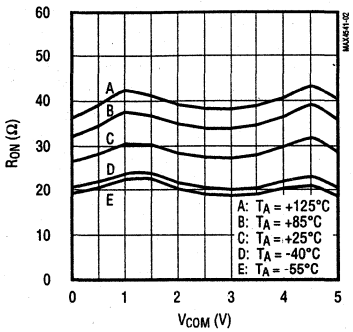
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted).

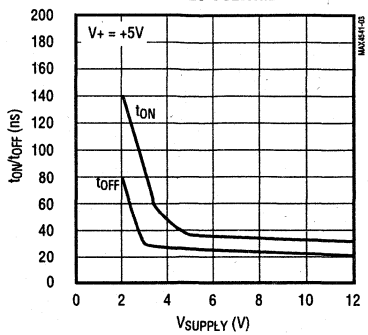
ON-RESISTANCE vs. COM VOLTAGE



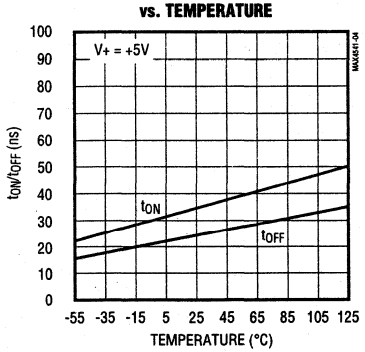
ON-RESISTANCE vs. COM VOLTAGE OVER TEMPERATURE



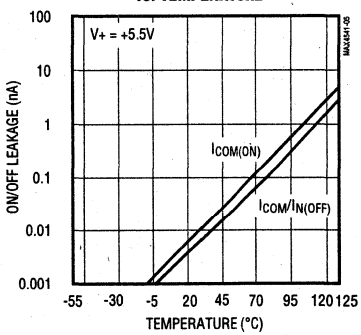
TURN-ON/OFF TIMES vs. SUPPLY VOLTAGE



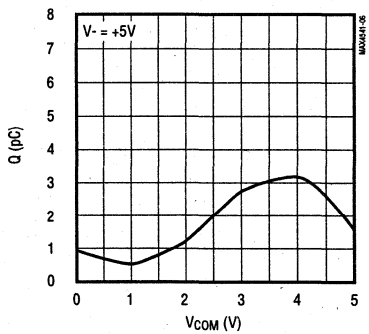
TURN-ON/OFF TIMES vs. TEMPERATURE



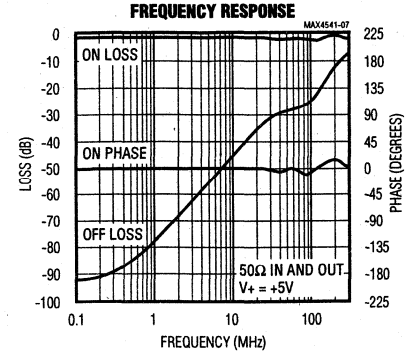
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



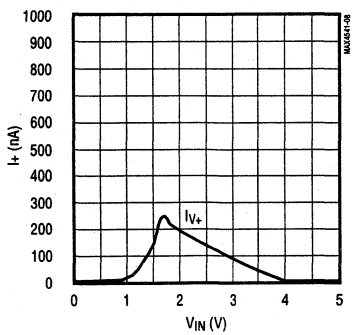
CHARGE INJECTION vs. COM VOLTAGE



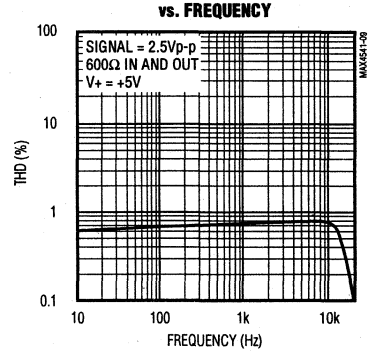
FREQUENCY RESPONSE



INPUT VOLTAGE vs. SUPPLY CURRENT



TOTAL HARMONIC DISTORTION vs. FREQUENCY



Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Pin Description

MAX4541	MAX4542	MAX4543	MAX4544 DIP/SO/µMAX	MAX4544 SOT23-6	NAME	FUNCTION
1	—	1	—	—	NO1	Analog Switch 1—Normally Open
2	2	2	—	—	COM1	Analog Switch 1—Common
3	3	3	—	—	IN2	Digital Control Input 2
4	4	4	4	3	GND	Ground—Negative Supply Input
5	—	—	—	—	NO2	Analog Switch 2—Normally Open
6	6	6	—	—	COM2	Analog Switch 2—Common
7	7	7	—	—	IN1	Digital Control Input 1
8	8	8	8	2	V+	Positive Supply Voltage Input
—	1	—	—	—	NC1	Analog Switch 1—Normally Closed
—	5	5	—	—	NC2	Analog Switch 2—Normally Closed
—	—	—	1	6	NO	Analog Switch—Normally Open
—	—	—	2	5	COM	Analog Switch—Common
—	—	—	3	4	NC	Analog Switch—Normally Closed
—	—	—	5, 6	—	N.C.	Not Connected (open circuit)
—	—	—	7	1	IN	Digital Control Input

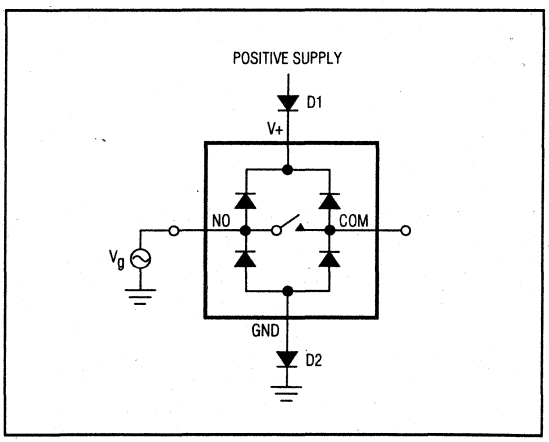


Figure 1. Overvoltage Protection Using Two External Blocking Diodes

Applications Information

Logic Levels

The MAX4541–MAX4544 are TTL compatible when powered from a single +5V supply. When powered from other supply voltages, TTL compatibility is guaranteed, and the logic inputs can be driven from Rail-to-Rail®. For example, with a +12V supply, IN1 and IN2 can be driven low to 0V and high to 12V. With a +3.3V supply, IN1 and IN2 should be driven low to 0V and high to 3.3V.

Driving IN1 and IN2 rail-to-rail minimizes power consumption.

Analog Signal Levels

Analog signals that range over the entire supply voltage (V+ to GND) can be switched with very little change in on-resistance over the entire voltage range (see *Typical Operating Characteristics*). All the switches are bidirectional, so the NO_, NC_, and COM_ pins can be used as either inputs or outputs.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Power-Supply Sequencing and Overvoltage Protection

Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings may cause permanent damage to the devices.

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V+ before applying analog signals or logic inputs, especially if the analog or logic signals are not current limited. If this sequencing is not possible, and if the analog or logic inputs are not current limited to <10mA, add a small-signal diode (D1) as shown in Figure 1. If the analog signal can dip below GND, add D2. Adding protection diodes reduces the analog signal range to a diode drop (about 0.7V) below V+ (for D1), and to a diode drop above ground (for D2). Leakage is unaffected by adding the diodes. On-resistance increases by a small amount at low supply voltages. Maximum supply voltage (V+) must not exceed 13V.

Adding protection diodes causes the logic thresholds to be shifted relative to the power-supply rails. This can be significant when low supply voltages (+5V or less) are used. With a +5V supply, TTL compatibility is not guaranteed when protection diodes are added. Driving IN1 and IN2 all the way to the supply rails (i.e., to a diode drop higher than the V+ pin, or to a diode drop lower than the GND pin) is always acceptable.

Protection diodes D1 and D2 also protect against some overvoltage situations. With Figure 1's circuit, if the supply voltage is below the absolute maximum rating, and if a fault voltage up to the absolute maximum rating is applied to an analog signal pin, no damage will result.

Test Circuits/Timing Diagrams

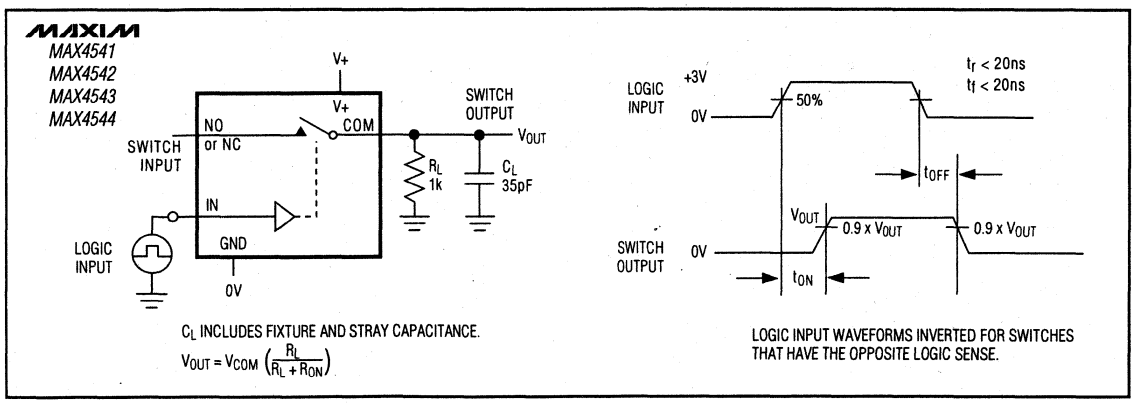


Figure 2. Switching Time

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Test Circuits/Timing Diagrams (continued)

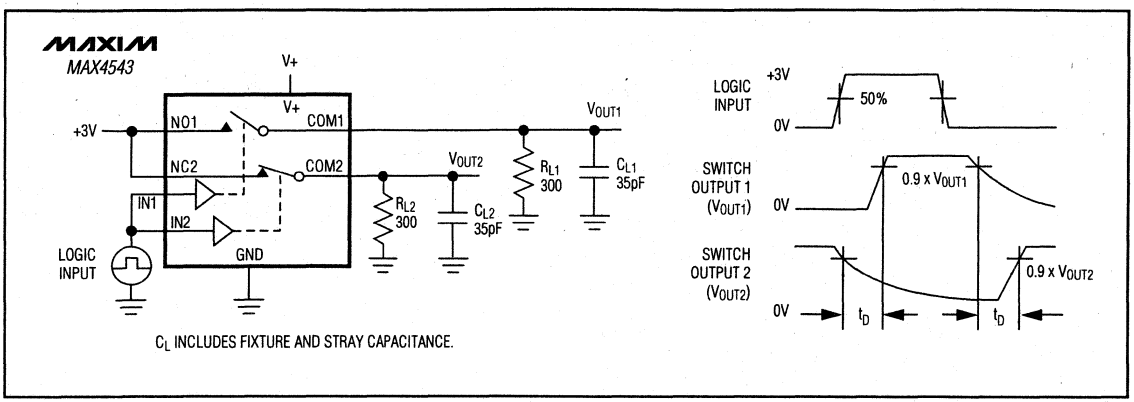


Figure 3a. Break-Before-Make Interval (MAX4543 only)

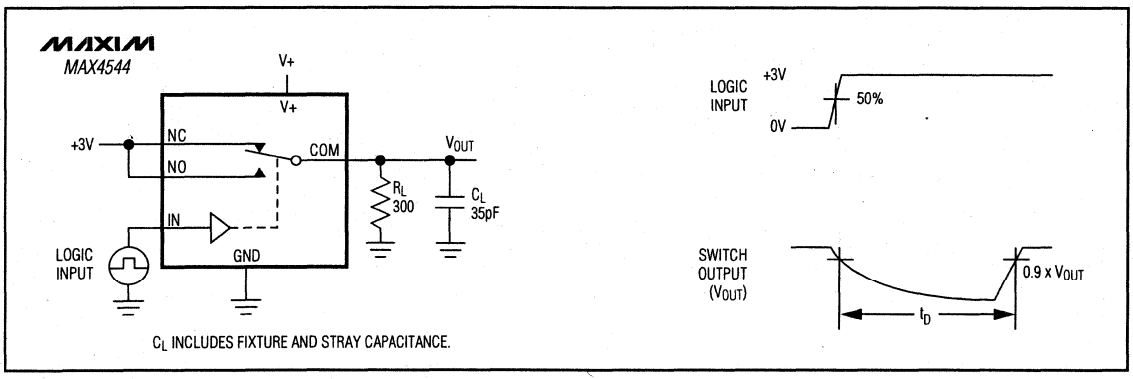


Figure 3b. Break-Before-Make Interval (MAX4544 only)

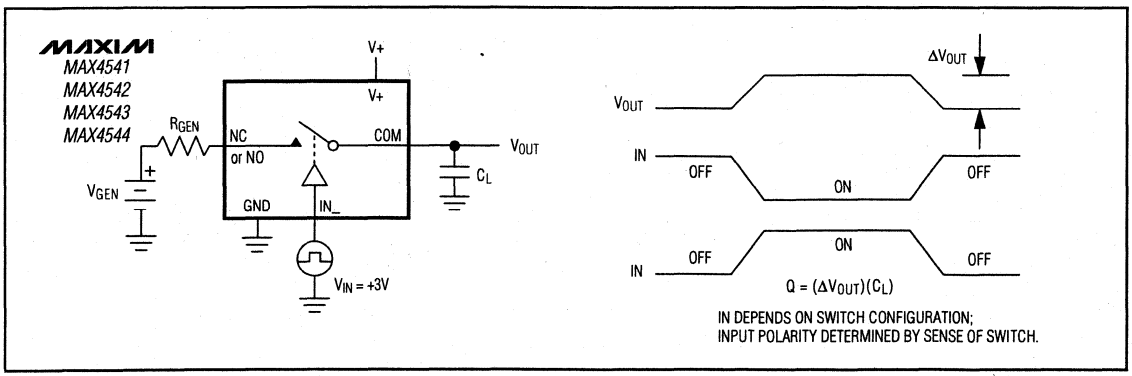


Figure 4. Charge Injection

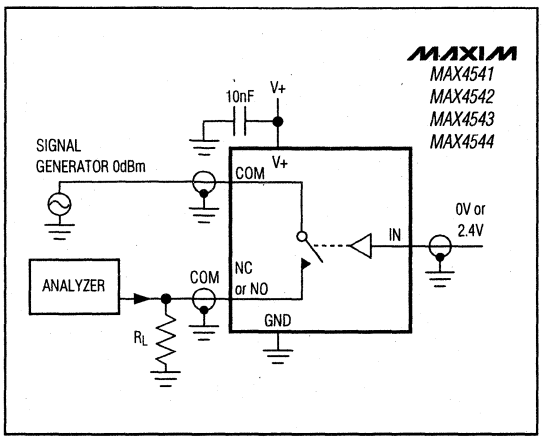


Figure 5. Off Isolation

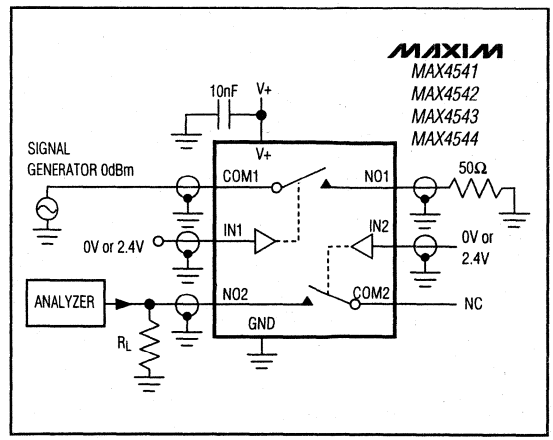


Figure 6. Crosstalk

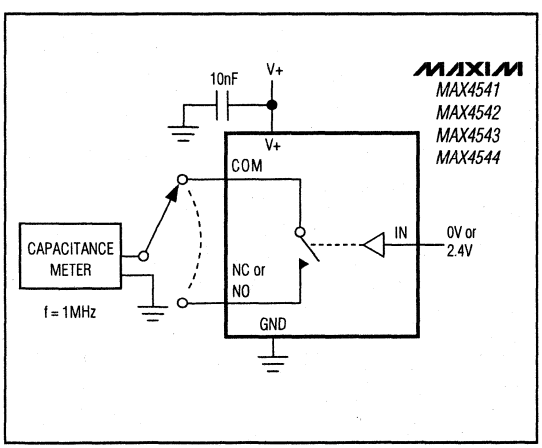


Figure 7. Channel Off/On Capacitance

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Ordering Information (continued)

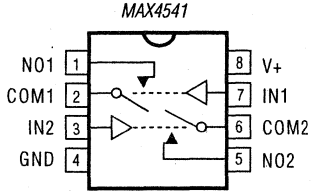
PART	TEMP. RANGE	PIN-PACKAGE
MAX4542CPA	0°C to +70°C	8 Plastic DIP
MAX4542CSA	0°C to +70°C	8 SO
MAX4542CUA	0°C to +70°C	8 µMAX
MAX4542C/D	0°C to +70°C	Dice*
MAX4542EPA	-40°C to +85°C	8 Plastic DIP
MAX4542ESA	-40°C to +85°C	8 SO
MAX4542EUA	-40°C to +85°C	8 µMAX
MAX4543CPA	0°C to +70°C	8 Plastic DIP
MAX4543CSA	0°C to +70°C	8 SO
MAX4543CUA	0°C to +70°C	8 µMAX
MAX4543C/D	0°C to +70°C	Dice*
MAX4543EPA	-40°C to +85°C	8 Plastic DIP
MAX4543ESA	-40°C to +85°C	8 SO
MAX4543EUA	-40°C to +85°C	8 µMAX
MAX4544CPA	0°C to +70°C	8 Plastic DIP
MAX4544CSA	0°C to +70°C	8 SO
MAX4544CUA	0°C to +70°C	8 µMAX
MAX4544C/D	0°C to +70°C	Dice*
MAX4544EPA	-40°C to +85°C	8 Plastic DIP
MAX4544ESA	-40°C to +85°C	8 SO
MAX4544EUA	-40°C to +85°C	8 µMAX
MAX4544EUT-T	-40°C to +85°C	6 SOT23

**Dice are tested at T_A = +25°C.*

Pin Configurations/Functional Diagrams/Truth Tables (continued)

TOP VIEW

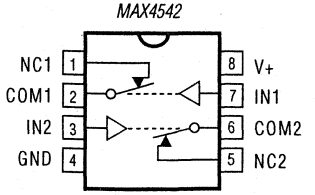
MAXIM
MAX4541



DIP/SO/µMAX

MAX4541	
LOGIC	SWITCH
0	OFF
1	ON

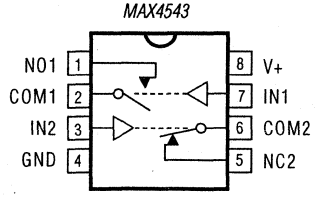
MAXIM
MAX4542



DIP/SO/µMAX

MAX4542	
LOGIC	SWITCH
0	ON
1	OFF

MAXIM
MAX4543



DIP/SO/µMAX

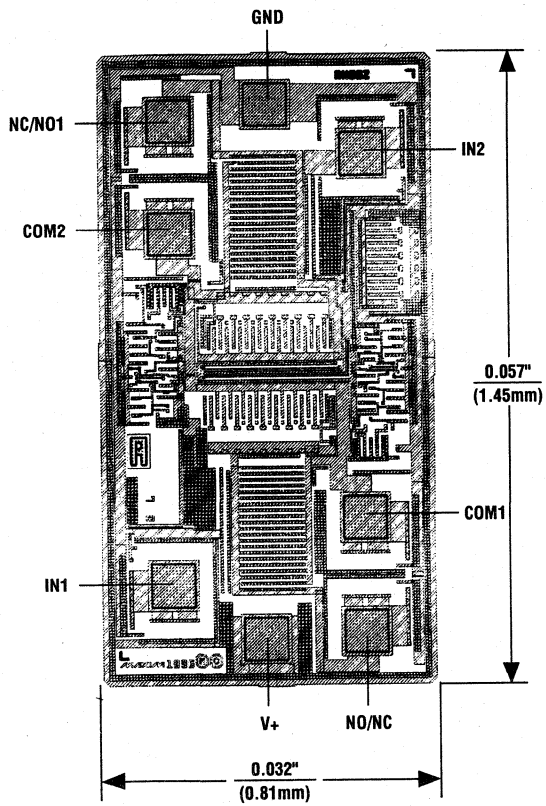
MAX4543		
LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

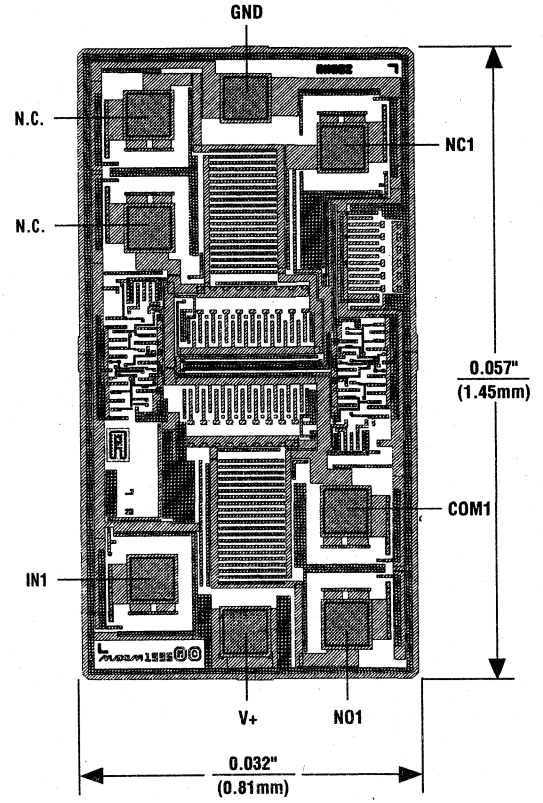
Chip Topographies

MAX4541/2/3



TRANSISTOR COUNT: 76
SUBSTRATE CONNECTED TO V+

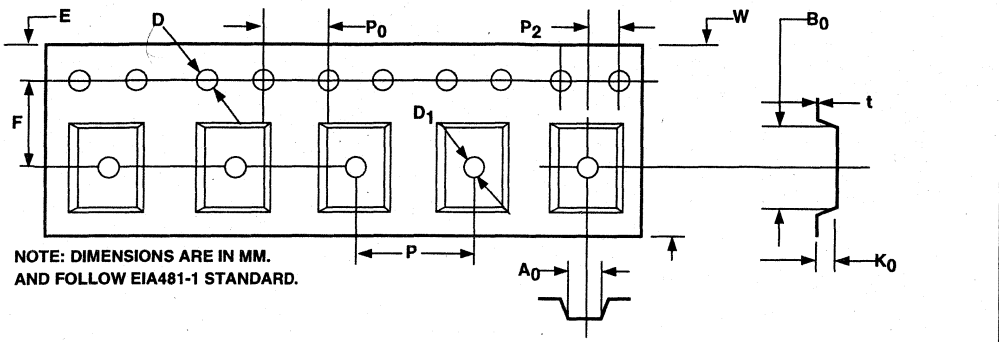
MAX4544



TRANSISTOR COUNT: 76
SUBSTRATE CONNECTED TO V+

Low-Voltage, Single-Supply Dual SPST/SPDT Analog Switches

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1232; Rev 0; 6/97

MAXIM

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

General Description

The MAX4545/MAX4546/MAX4547 are low-voltage T-switches designed for switching RF and video signals from DC to 300MHz in 50Ω and 75Ω systems. The MAX4545 contains four normally open single-pole/single-throw (SPST) switches. The MAX4546 contains two dual SPST switches (one normally open, one normally closed.) The MAX4547 contains two single-pole/double-throw (SPDT) switches.

Each switch is constructed in a "T" configuration, ensuring excellent high-frequency off isolation and crosstalk of -80dB at 10MHz. They can handle Rail-to-Rail® analog signals in either direction. On-resistance (20Ω max) is matched between switches to 1Ω max and is flat (0.5Ω max) over the specified signal range, using ±5V supplies. The off leakage current is less than 5nA at +25°C and 50nA at +85°C.

These CMOS switches can operate with dual power supplies ranging from ±2.7V to ±6V or a single supply between +2.7V and +12V. All digital inputs have 0.8V/2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

RF Switching
Video Signal Routing
High-Speed Data Acquisition
Test Equipment
ATE Equipment
Networking

Features

- **Low 50Ω Insertion Loss: -1dB at 100MHz**
- **High 50Ω Off Isolation: -80dB at 10MHz**
- **Low 50Ω Crosstalk: -80dB at 10MHz**
- **DC to 300MHz -3dB Signal Bandwidth**
- **20Ω Signal Paths with ±5V Supplies**
- **1Ω Signal-Path Matching with ±5V Supplies**
- **0.5Ω Signal-Path Flatness with ±5V Supplies**
- **±2.7V to ±6V Dual Supplies**
  +2.7V to +12V Single Supply
- **Low Power Consumption: <1µW**
- **Rail-to-Rail Bidirectional Signal Handling**
- **Pin Compatible with Industry-Standard DG540, DG542, DG643**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with Single +5V or ±5V**

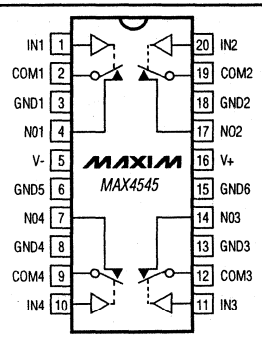
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4545CPP	0°C to +70°C	20 Plastic DIP
MAX4545CWP	0°C to +70°C	20 Wide SO

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

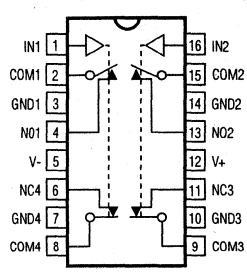


DIP/SO/SSOP

MAX4545	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

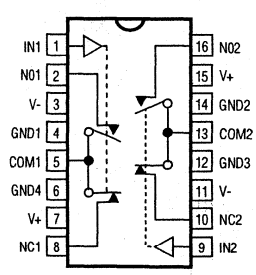
MAXIM
MAX4546



DIP/SO/QSOP

MAX4546		
LOGIC	1, 2	3, 4
0	OFF	ON
1	ON	OFF

MAXIM
MAX4547



DIP/SO/QSOP

MAX4547		
LOGIC	NO-COM	NC-COM
0	OFF	ON
1	ON	OFF

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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For small orders, phone 408-737-7600 ext. 3468.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13.0V
V- .....-13.0V, +0.3V
V+ to V- .....-0.3V, +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±25mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle) .....±50mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP
(derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO
(derate 8.70mW/°C above +70°C) 696mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
20-Pin Plastic DIP (derate 8.0mW/°C above +70°C) 640mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX454_C_ E .....0°C to +70°C
MAX454_E_ E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages on all other pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$,$V_{NC_}$	(Note 3)	C, E	V-		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = ±2V, $I_{COM_}$ = 10mA	+25°C		14	20	Ω
			C, E		18	25	
Signal-Path On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = ±2V, $I_{COM_}$ = 10mA	+25°C		0.5	1	Ω
			C, E			1.25	
Signal-Path On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V; V- = -5V; $V_{COM_}$ = 1V, 0V, -1V; I_{COM} = 10mA	+25°C		0.3	0.5	Ω
NO_, NC_ Off Leakage Current (Note 6)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓4.5V	+25°C	-5	0.02	5	nA
			C, E	-50		50	
COM_ Off Leakage Current (Note 6)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓4.5V	+25°C	-5	0.02	5	nA
			C, E	-50		50	
COM_ On Leakage Current (Note 6)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓4.5V	+25°C	-10	0.04	10	nA
			C, E	-100		100	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 4		+25°C		90	150	ns
				C, E			200	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 4		+25°C		35	100	ns
				C, E			120	
Break-Before-Make Time Delay (MAX4546/MAX4547 only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 5 (Note 3)		+25°C	15	40		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, $V_{NO_}$ = 0V, RS = 0Ω, Figure 6		+25°C		60	150	pC
NO_, NC_ Off Capacitance	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz, Figure 8		+25°C		6		pF
COM_ Off Capacitance	$C_{COM_(OFF)}$	$V_{COM_}$ = 0V, f = 1MHz, Figure 8	MAX4545	+25°C		6		pF
			MAX4546			6		
COM_ On Capacitance	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = 0V, f = 1MHz, Figure 8	MAX4545	+25°C		11.5		pF
			MAX4546			11.5		
			MAX4547			17		
Off Isolation (Note 7)	V_{ISO}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 7	MAX4545	+25°C		-80		dB
			MAX4546			-80		
			MAX4547			-82		
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 7	MAX4545	+25°C		-88		dB
			MAX4546			-80		
			MAX4547			-84		
-3dB Bandwidth	BW	Figure 7, R_L = 50Ω		+25°C		300		MHz
Distortion	THD+N	V_{IN} = 5Vp-p, f < 20kHz, 600Ω in and out		+25°C		0.004		%
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E	-6		+6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+		+25°C	-1	0.05	1	µA
				C, E	-10		10	
V - Supply Current	I-	V- = -5.5V		+25°C	-1	0.05	1	µA
				C, E	-10		10	

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		26	40	Ω
			C, E			60	
Signal-Path On-Resistance Match	ΔR_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C			2	Ω
			C, E			4	
NO_, NC_ Off Leakage Current (Note 9)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, $V_{N_}$ = 4.5V	+25°C	-5	0.02	5	nA
			C, E	-50		50	
COM_ Off Leakage Current (Note 9)	$I_{COM_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, $V_{N_}$ = 4.5V	+25°C	-5	0.02	5	nA
			C, E	-50		50	
COM_ On Leakage Current (Note 9)	$I_{COM_(ON)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V	+25°C	-10	0.04	10	nA
			C, E	-100		100	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 5V, Figure 4	+25°C		130	250	ns
			C, E			350	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 5V, Figure 4	+25°C		40	100	ns
			C, E			150	
Break-Before-Make Time Delay (MAX4546/MAX4547 only)	t_{BBM}	$V_{COM_}$ = 3V, V+ = 5V, Figure 5 (Note 3)	+25°C	20	70		ns
Charge Injection	Q	C_L = 1.0nF, V_{NO} = 2.5V, R_S = 0Ω, Figure 6	+25°C		25		pC
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 7	+25°C		-75		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 7	+25°C		-70		dB
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1V, $I_{COM_}$ = 1mA	+25°C		70	120	Ω
			C, E			150	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}	(Note 3)	C, E		1.0	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}	(Note 3)	C, E	0.8	1.0		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V (Note 3)	C, E	-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 4 (Note 3)	+25°C		300	600	ns
			C, E			800	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 4 (Note 3)	+25°C		50	150	ns
			C, E			200	
Break-Before-Make Time Delay (MAX4546/MAX4547 only)	t_{BBM}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 5 (Note 3)	+25°C	15	100		ns
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

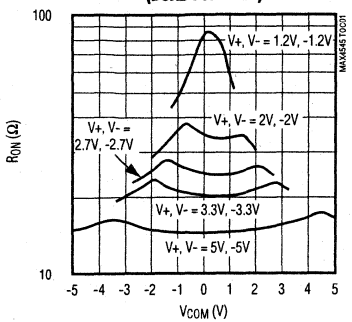
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.
Note 9: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

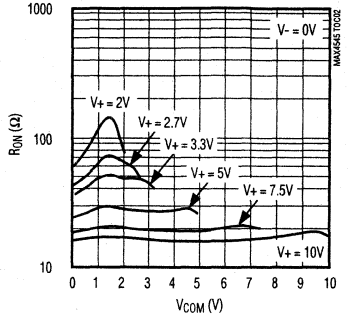
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

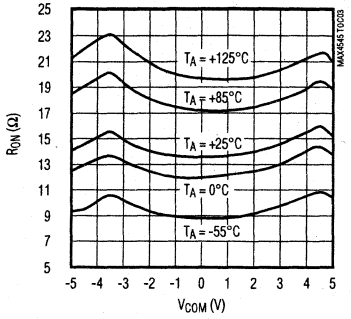
ON-RESISTANCE vs. VCOM (DUAL SUPPLIES)



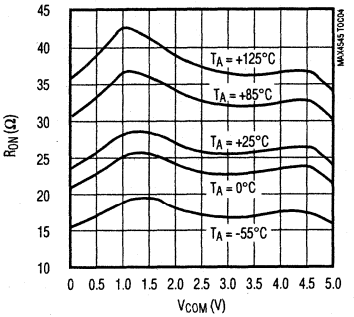
ON-RESISTANCE vs. VCOM (SINGLE SUPPLY)



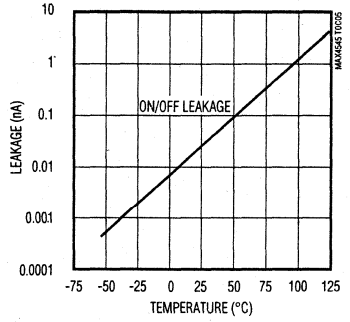
ON-RESISTANCE vs. VCOM AND TEMPERATURE (DUAL SUPPLIES)



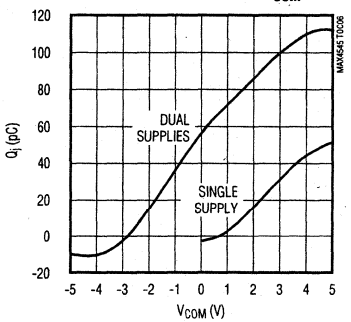
ON-RESISTANCE vs. VCOM AND TEMPERATURE (SINGLE SUPPLY)



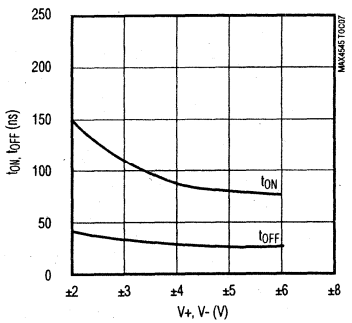
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



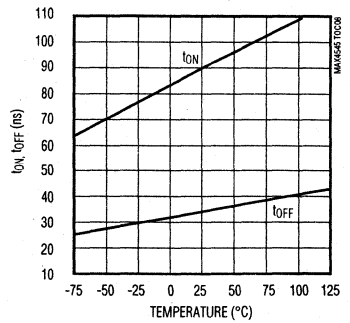
CHARGE INJECTION vs. VCOM



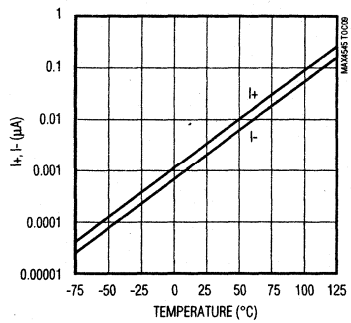
ON/OFF TIME vs. SUPPLY VOLTAGE



ON/OFF TIME vs. TEMPERATURE



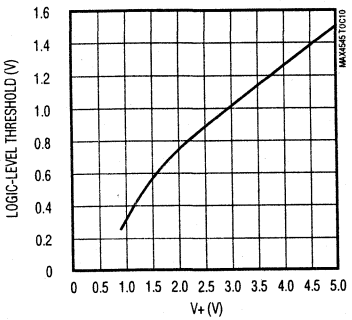
POWER-SUPPLY CURRENT vs. TEMPERATURE



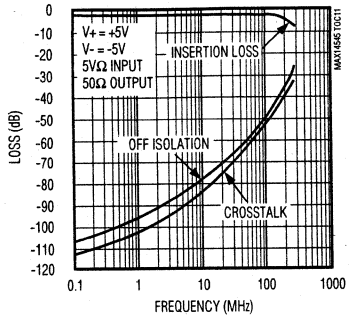
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

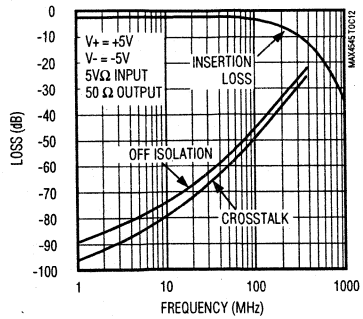
LOGIC-LEVEL THRESHOLD vs. POSITIVE SUPPLY VOLTAGE



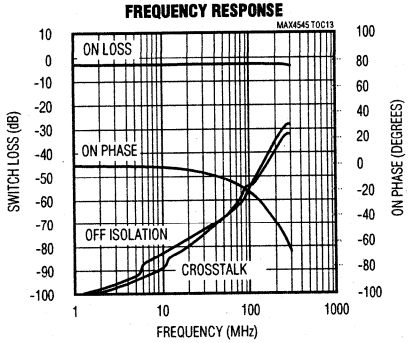
MAX4545 FREQUENCY RESPONSE



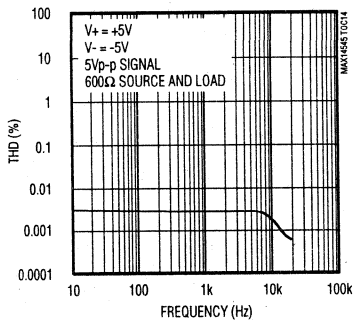
MAX4546 FREQUENCY RESPONSE



FREQUENCY RESPONSE



MAX4547 TOTAL HARMONIC DISTORTION vs. FREQUENCY



Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Pin Description

PIN			NAME	FUNCTION*
MAX4545	MAX4546	MAX4547		
1, 10, 11, 20	1, 16	1, 9	IN_	Digital Control Input
3, 6, 8, 13, 15, 18	3, 7, 10, 14	4, 6, 12, 14	GND_	RF and Logic Ground. Grounds are not internally connected to each other, and should all be connected to a ground plane (see *Grounding* section).
16	12	7, 15	V+	Positive Supply-Voltage Input (analog and digital)
5	5	3, 11	V-	Negative Supply-Voltage Input. Connect to ground plane for single-supply operation.
4, 7, 14, 17	4, 13	2, 16	NO_	Analog Switch Normally Open** Terminals
—	6, 11	8, 10	NC_	Analog Switch Normally Closed** Terminals
2, 9, 12, 19	2, 8, 9, 15	5, 13	COM_	Analog Switch Common** Terminals

* All pins have ESD diodes to V- and V+.

** NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.

Theory of Operation

Logic-Level Translators

The MAX4545/MAX4546/MAX4547 are constructed as high-frequency "T" switches, as shown in Figure 1. The logic-level input, IN_, is translated by amplifier A1 into a V+ to V- logic signal that drives amplifier A2. (Amplifier A2 is an inverter for normally closed switches.) Amplifier A2 drives the gates of N-channel MOSFETs N1 and N2 from V+ to V-, turning them fully on or off. The same signal drives inverter A3 (which drives the P-channel MOSFETs P1 and P2) from V+ to V-, turning them fully on or off, and drives the N-channel MOSFET N3 off and on.

The logic-level threshold is determined by V+ and GND_. The voltage on GND_ is usually at ground potential, but it may be set to any voltage between (V+ - 2V) and V-. When the voltage between V+ and GND_ is less than 2V, the level translators become very slow and unreliable. Since individual switches in each package have individual GND_ pins, they may be set to different voltages. Normally, however, they should all be connected to the ground plane.

Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off. The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical

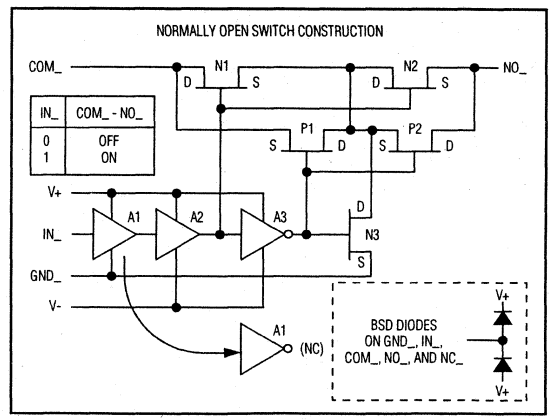


Figure 1. T-Switch Construction

(i.e., signals may pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small amount of capacitance to GND_. The four on MOSFETs also have capacitance to ground that, together with the series resistance, forms a lowpass filter. All of these capacitances are distributed evenly along the series resistance, so they act as a transmission line rather than a simple R-C filter. This helps to explain the exceptional 300MHz bandwidth when the switches are on.

Typical attenuation in 50Ω systems is -1dB and is reasonably flat up to 100MHz. Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's internal resistance.

The MAX4545/MAX4546/MAX4547 are optimized for ±5V operation. Using lower supply voltages or a single supply increases switching time, increases on-resistance (and therefore on-state attenuation), and increases nonlinearity.

Switch Off Condition

When the switch is off, MOSFETs N1, N2, P1, and P2 are off and MOSFET N3 is on. The signal path is through the off-capacitances of the series MOSFETs, but it is shunted to ground by N3. This forms a high-pass filter whose exact characteristics are dependent on the source and load impedances. In 50Ω systems, and below 10MHz, the attenuation can exceed 80dB. This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout have a major role in determining overall performance.

Applications Information

Power-Supply Considerations

Overview

The MAX4545/MAX4546/MAX4547 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. All pins have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog signal voltage.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly; when V+ reaches +12V, the level threshold is about 3.1V, which is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar-Supply Operation

The MAX4545/MAX4546/MAX4547 operate with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4545/MAX4546/MAX4547 V+ pin to +3V and connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs can exceed the absolute maximum ratings, causing damage to the part and/or external circuits.**

CAUTION:

The absolute maximum V+ to V- differential voltage is 13.0V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4545/MAX4546/MAX4547. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Single-Supply Operation

The MAX4545/MAX4546/MAX4547 operate from a single supply between +2.7V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. Note, however, that these parts are optimized for ±5V operation, and most AC and DC characteristics are degraded significantly when departing from ±5V. As the overall supply voltage (V+ to V-) is lowered, switching speed, on-resistance, off isolation, and distortion are degraded. (See *Typical Operating Characteristics*.)

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Single-supply operation also limits signal levels and interferes with grounded signals. When V- = 0V, AC signals are limited to -0.3V. Voltages below -0.3V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

Power Off

When power to the MAX4545/MAX4546/MAX4547 is off (i.e., V+ = 0V and V- = 0V), the Absolute Maximum Ratings still apply. This means that neither logic-level inputs on IN_ nor signals on COM_, NO_, or NC_ can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, and the parts can be damaged if excessive current flows.

Grounding

DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. **For most applications, a ground plane is strongly recommended, and all GND_ pins should be connected to it with solid copper.** While the V+ and V- power-supply pins are common to all switches in a given package, each switch has separate ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance and provides added flexibility in some applications, but it can cause problems if it is overlooked. All the GND_ pins have ESD diodes to V+ and V-.

In systems that have separate digital and analog (signal) grounds, connect these switch GND_ pins to analog ground. Preserving a good signal ground is much more important than preserving a digital ground. Ground current is only a few nanoamps.

The logic-level inputs, IN_, have voltage thresholds determined by V+ and GND_. (V- does not influence the logic-level threshold.) With +5V and 0V applied to V+ and GND_, the threshold is about 1.6V, ensuring compatibility with TTL- and CMOS-logic drivers.

The various GND_ pins can be connected to separate voltage potentials if any or all of the logic-level inputs is not a normal logic signal. (The GND_ voltages cannot exceed (V+ - 2V) or V-.) Elevating GND_ reduces off isolation. For example, using the MAX4545, if GND2–GND6 are connected to 0V and GND1 is connected to V-, then switches 2, 3, and 4 would be TTL/CMOS compatible, but switch 1 (IN1) could be driven with the rail-to-rail output of an op amp operating from V+ and V-. Note, however, that IN_ can be driven more negative than GND_, as far as V-. GND_ does not have to be removed from 0V when IN_ is driven from bipolar sources, but the voltage on IN_ should never exceed V-. GND_ should be separated from 0V only if the logic-level threshold has to be changed.

Any GND_ pin not connected to 0V should be bypassed to the ground plane with a surface-mount 10nF capacitor to maintain good RF grounding. DC current in the IN_ and GND_ pins is less than 1nA, but increases with switching frequency.

On the MAX4545 only, two extra ground pins—GND5 and GND6—are provided to improve isolation and crosstalk. They are not connected to the logic-level circuit. These pins should always be connected to the ground plane with solid copper.

AC Ground and Bypassing

A ground plane is mandatory for satisfactory high-frequency operation. (Prototyping using hand wiring or wire-wrap boards is strongly discouraged.) Connect all 0V GND_ pins to the ground plane with solid copper. (The GND_ pins extend the high-frequency ground through the package wire-frame, into the silicon itself, thus improving isolation.) The ground plane should be solid metal underneath the device, without interruptions. There should be no traces under the device itself. For DIP packages, this applies to both sides of a two-sided board. Failure to observe this will have a minimal effect on the "on" characteristics of the switch at high frequencies, but it will degrade the off isolation and crosstalk.

All V+ and V- pins should be bypassed to the ground plane with surface-mount 10nF capacitors. For DIP packages, they should be mounted as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors. For surface-mount packages, the pins are so close to each other that the bypass capacitors should be mounted on the opposite side of the board from the device. In this case, use short feedthroughs or vias, directly under the V+ and V- pins. Any GND_ pin not connected to 0V should be similarly bypassed. If V- is 0V, connect it directly to the ground plane with solid copper. Keep all leads short.

The MAX4547 has two V+ and V- pins. Make DC connections to only one of each to minimize crosstalk. Do not route DC current into one of the V+ or V- pins and out the other V+ or V- pin to other devices. The second set of V+ and V- pins is for AC bypassing only.

For dual-supply operation, the MAX4547 should have four 10nF bypass capacitors connected to each V+ and V- pin, as close to the package as possible. For single-supply operation, the MAX4547 should have two 10nF bypass capacitors connected (one to each V+ pin), as close to the package as possible.

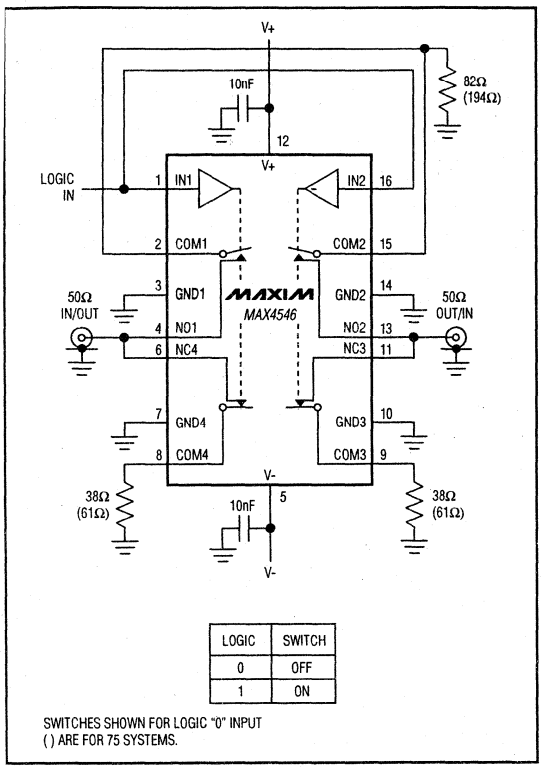


Figure 2. Impedance Matching On/Off Switch

On the MAX4545, GND5 and GND6 should always be connected to the ground plane with solid copper to improve isolation and crosstalk.

Signal Routing

Keep all signal leads as short as possible. Separate all signal leads from each other and other traces with the ground plane on both sides of the board. Where possible, use coaxial cable instead of printed circuit board traces.

Board Layout

IC sockets degrade high-frequency performance and should not be used if signal bandwidth exceeds 5MHz. Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Such grounds tend to be wedge-shaped as they get closer to the device. Use vias to connect the ground planes on each side of the board, and place the vias in the apex of the wedge-shaped grounds that separate signal leads. Logic-level signal lead placement is not critical.

Impedance Matching

The typical on-resistances of the switches in the MAX4545/MAX4546/MAX4547 are 14Ω, but the off-state impedances are approximately equal to a 6pF capacitor. In coaxial systems, therefore, it is impossible to match any impedance for both the on and off state. If impedance matching is critical, the MAX4546 is best suited, since its two sections can be configured as a single on/off switch, as shown in Figure 2. This circuit "wastes" switches and has higher losses, but has better off isolation and maintains good impedance matching in both the on and off states. The resistance values shown in Figure 3 are optimized with ±5V supplies for both 50Ω and 75Ω systems at room temperature.

Multiplexer

With its excellent off isolation, the MAX4545 is ideal for use in high-frequency video multiplexers. Figure 3 shows such an application for switching any one of four video inputs to a single output. The same circuit may be used as a demultiplexer by simply reversing the signal direction.

Stray capacitance of traces and the output capacitance of switches placed in parallel reduces bandwidth, so the outputs of no more than four individual switches should be placed in parallel if high bandwidth is to be maintained. If more than four mux channels are needed, the 4-channel circuit should be duplicated and cascaded.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

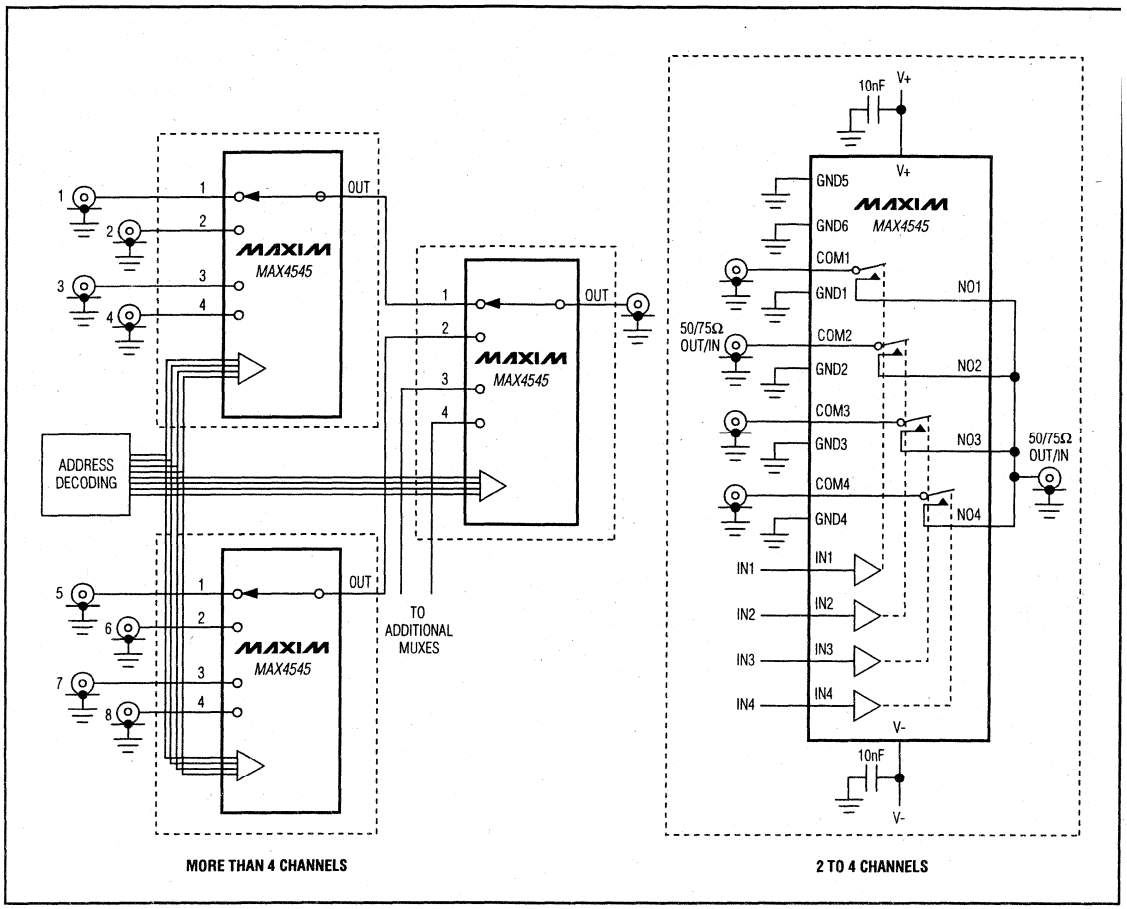


Figure 3. 4-Channel Multiplexer

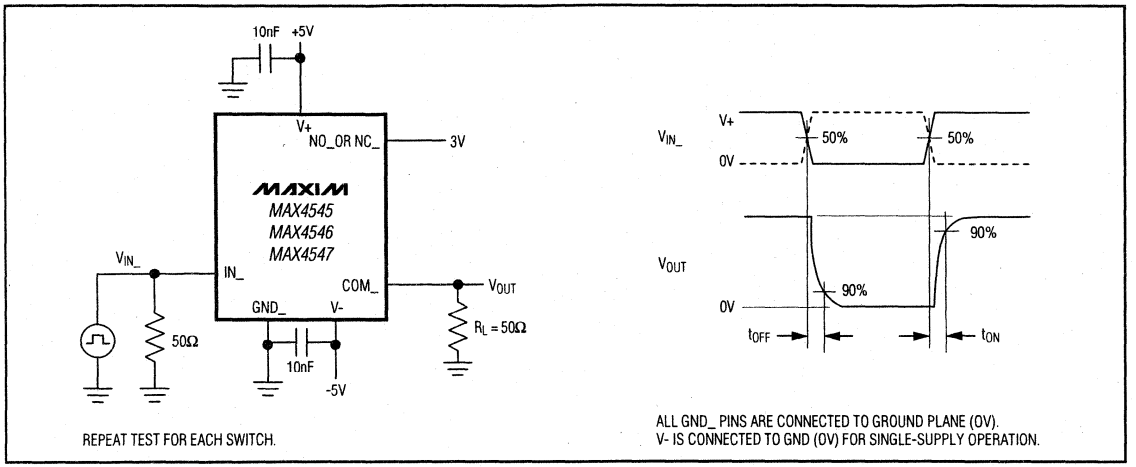


Figure 4. Switching Time

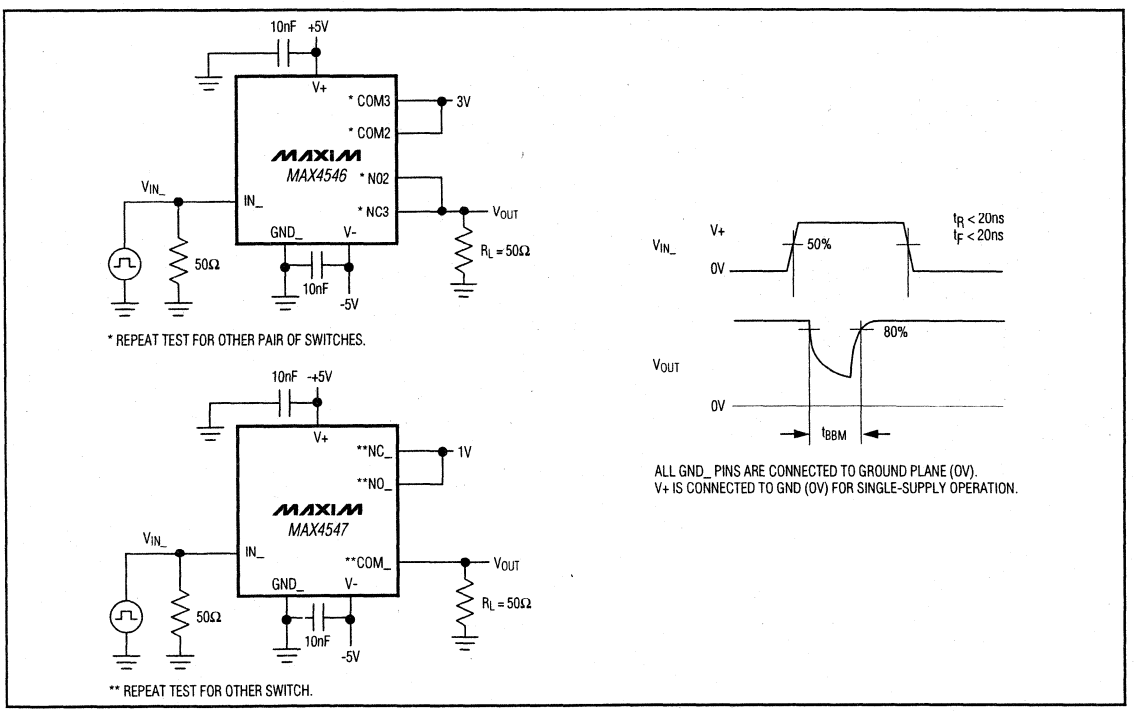


Figure 5. Break-Before-Make Interval (MAX4546/MAX4547 only)

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Test Circuits/Timing Diagrams (continued)

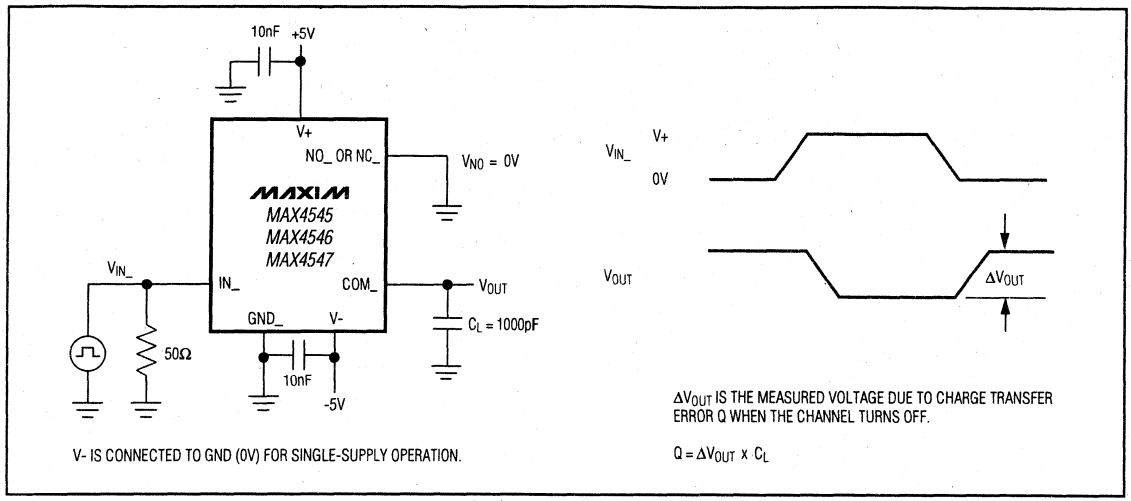


Figure 6. Charge Injection

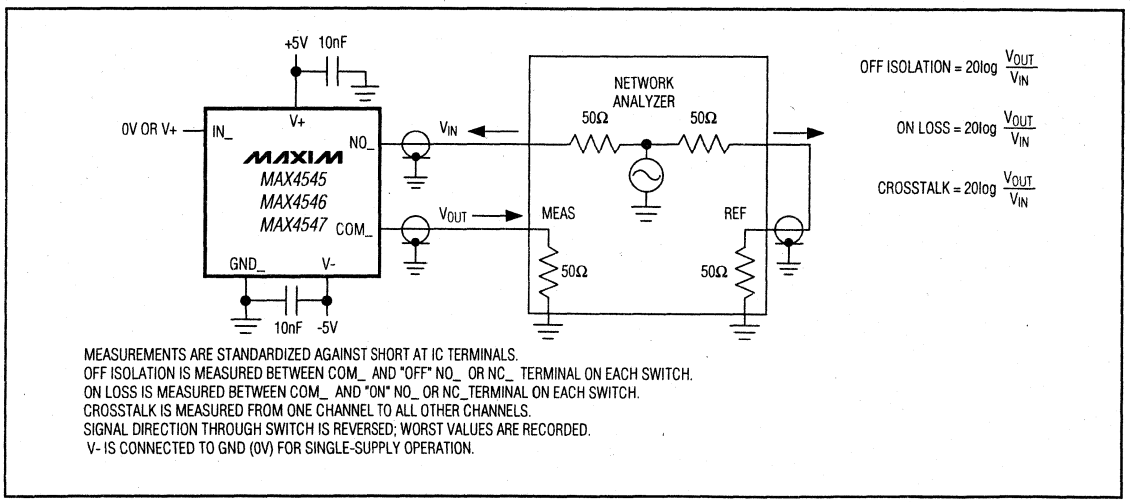


Figure 7. On Loss, Off Isolation, and Crosstalk

Test Circuits/Timing Diagrams (continued)

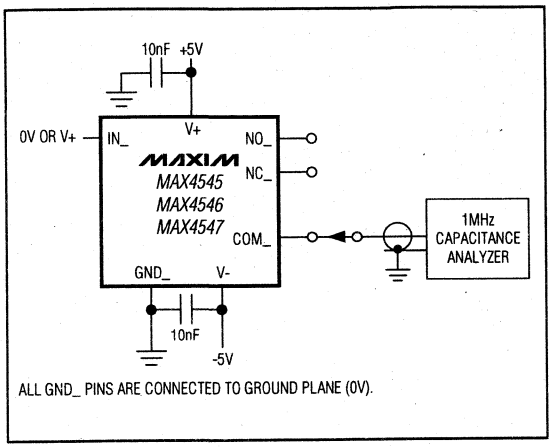
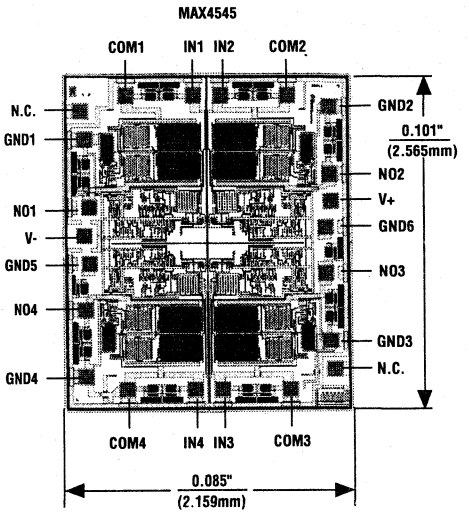
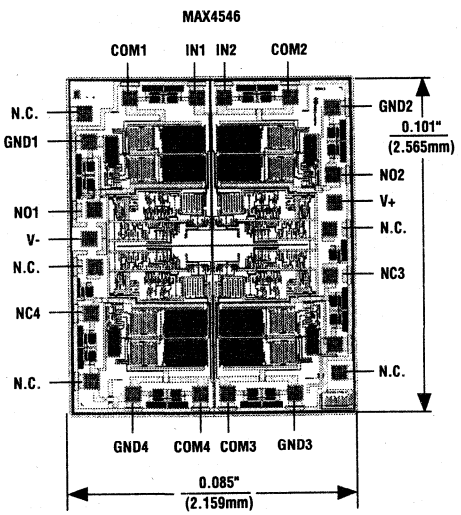
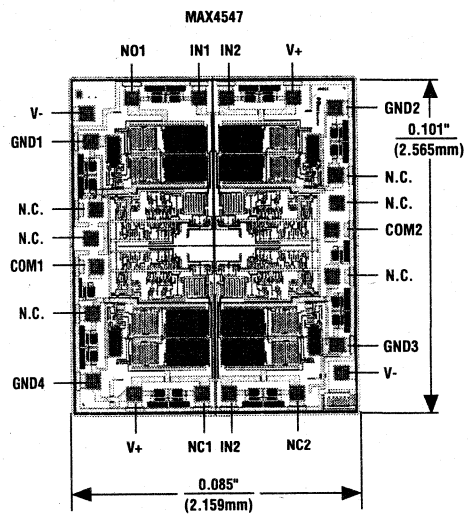


Figure 8. NO_, NC_, COM_ Capacitance

Chip Topographies







N.C. = NO INTERNAL CONNECTION

TRANSISTOR COUNT: 253
SUBSTRATE INTERNALLY CONNECTED TO V-

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4545CAP	0°C to +70°C	20 SSOP
MAX4545C/D	0°C to +70°C	Dice*
MAX4545EPP	-40°C to +85°C	20 Plastic DIP
MAX4545EWP	-40°C to +85°C	20 Wide SO
MAX4545EAP	-40°C to +85°C	20 SSOP
MAX4546CPE	0°C to +70°C	16 Plastic DIP
MAX4546CSE	0°C to +70°C	16 Narrow SO
MAX4546CEE	0°C to +70°C	16 QSOP
MAX4546C/D	0°C to +70°C	Dice*
MAX4546EPE	-40°C to +85°C	16 Plastic DIP
MAX4546ESE	-40°C to +85°C	16 Narrow SO

PART	TEMP. RANGE	PIN-PACKAGE
MAX4546EEE	-40°C to +85°C	16 QSOP
MAX4547CPE	0°C to +70°C	16 Plastic DIP
MAX4547CSE	0°C to +70°C	16 Narrow SO
MAX4547CEE	0°C to +70°C	16 QSOP
MAX4547C/D	0°C to +70°C	Dice*
MAX4547EPE	-40°C to +85°C	16 Plastic DIP
MAX4547ESE	-40°C to +85°C	16 Narrow SO
MAX4547EEE	-40°C to +85°C	16 QSOP

Contact factory for dice specifications.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Force-Sense Switches

General Description

The MAX4554/MAX4555/MAX4556 are CMOS analog ICs configured as force-sense switches. Each part contains several low-resistance switches for forcing current, and higher-resistance switches for sensing voltage. The MAX4554 contains two force switches, two sense switches, and two guard switches configured as two three-pole/single throw switches. The MAX4555 contains four independent single-pole/single-throw switches, two force switches, and two sense switches. The MAX4556 contains three independent single-pole/double-throw switches; one is a force switch, and two are sense switches.

The MAX4554/MAX4555/MAX4556 operate from a single 4.5V to 30V supply or from dual ±4.5V to ±18V supplies. On-resistance (6Ω max) is matched between switches to 1Ω (max). Each switch can handle Rail-to-Rail® analog signals. Off-leakage current is only 1nA at +25°C and 5nA at +85°C.

The MAX4554 is also fully specified for +20V and -10V operation.

All digital inputs have +0.8V and +2.4V logic thresholds, ensuring TTL/CMOS-logic compatibility.

Applications

Automated Test Equipment (ATE)

Calibrators

Precision Power Supplies

Automatic Calibration Circuits

Audio-Signal Routing

Features

- **6Ω Force-Signal Paths with ±15V Supplies**
- **1Ω Force-Signal Matching with ±15V Supplies**
- **30Ω Sense/Guard-Signal Paths with ±15V Supplies**
- **4.5Ω Sense/Guard-Signal Matching with ±15V Supplies**
- **Fully Specified at +20V/-10V for ATE (MAX4554)**
- **Pin Compatible with DG412 (MAX4555)**
- **Rail-to-Rail Signal Handling**
- **Break-Before-Make Switching**
- **t_{ON}/t_{OFF} = 225ns/185ns at a ±15V Supply**
- **5µA Power Consumption**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4554CPE	0°C to +70°C	16 Plastic DIP
MAX4554CSE	0°C to +70°C	16 SO
MAX4554CAE	0°C to +70°C	16 SSOP
MAX4554C/D	0°C to +70°C	Dice
MAX4554EPE	-40°C to +85°C	16 Plastic DIP
MAX4554ESE	-40°C to +85°C	16 SO
MAX4554EAE	-40°C to +85°C	16 SSOP
MAX4555CPE	0°C to +70°C	16 Plastic DIP
MAX4555CSE	0°C to +70°C	16 SO
MAX4555CAE	0°C to +70°C	16 SSOP
MAX4555C/D	0°C to +70°C	Dice
MAX4555EPE	-40°C to +85°C	16 Plastic DIP
MAX4555ESE	-40°C to +85°C	16 SO
MAX4555EAE	-40°C to +85°C	16 SSOP
MAX4556CPE	0°C to +70°C	16 Plastic DIP
MAX4556CSE	0°C to +70°C	16 SO
MAX4556CAE	0°C to +70°C	16 SSOP
MAX4556C/D	0°C to +70°C	Dice
MAX4556EPE	-40°C to +85°C	16 Plastic DIP
MAX4556ESE	-40°C to +85°C	16 SO
MAX4556EAE	-40°C to +85°C	16 SSOP

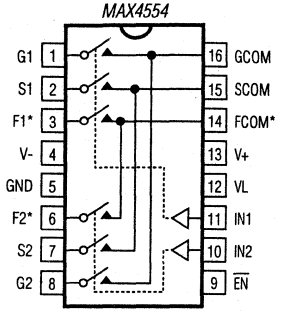
Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

Pin Configurations/Functional Diagram/Truth Tables

TOP VIEW

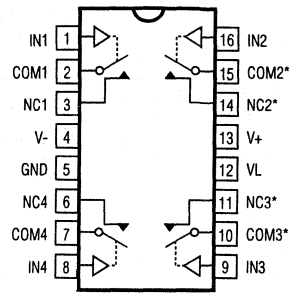
MAXIM
MAX4554



DIP/SO/SSOP

MAX4554					
$\overline{EN}$	IN1	IN2	GCOM	SCOM	FCOM*
1	X	X	OFF	OFF	OFF
0	0	0	OFF	OFF	OFF
0	0	1	G2	S2	F2
0	1	0	G1	S1	F1
0	1	1	G1 & G2	S1 & S2	F1 & F2

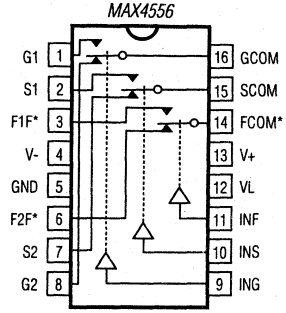
MAXIM
MAX4555



DIP/SO/SSOP

MAX4555	
IN_	SWITCH
0	OFF
1	ON

MAXIM
MAX4556



DIP/SO/SSOP

MAX4556	
INx	xCOM
0	x2
1	x1

WHERE x = F, S, G

NOTE: SWITCH POSITIONS SHOWN WITH IN_ = LOW.
*INDICATES HIGH-CURRENT, LOW-RESISTANCE FORCE SWITCH.

19-1252; Rev 0; 7/97

MAXIM

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

General Description

The MAX4565/MAX4566/MAX4567 are low-voltage T-switches designed for switching RF and video signals from DC to 350MHz in 50Ω and 75Ω systems. The MAX4565 contains four normally open single-pole/single-throw (SPST) switches. The MAX4566 contains two dual SPST switches (one normally open, one normally closed.) The MAX4567 contains two single-pole/double-throw (SPDT) switches.

Each switch is constructed in a "T" configuration, ensuring excellent high-frequency off isolation and crosstalk of -83dB at 10MHz. They can handle Rail-to-Rail® analog signals in either direction. On-resistance (60Ω max) is matched between switches to 2.5Ω max and is flat (2Ω max) over the specified signal range, using ±5V supplies. The off leakage current is less than 5nA at +25°C and 50nA at +85°C.

These CMOS switches can operate with dual power supplies ranging from ±2.7V to ±6V or a single supply between +2.7V and +12V. All digital inputs have 0.8V/2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V or a single +5V supply.

Applications

RF Switching
Video Signal Routing
High-Speed Data Acquisition
Test Equipment
ATE Equipment
Networking

Features

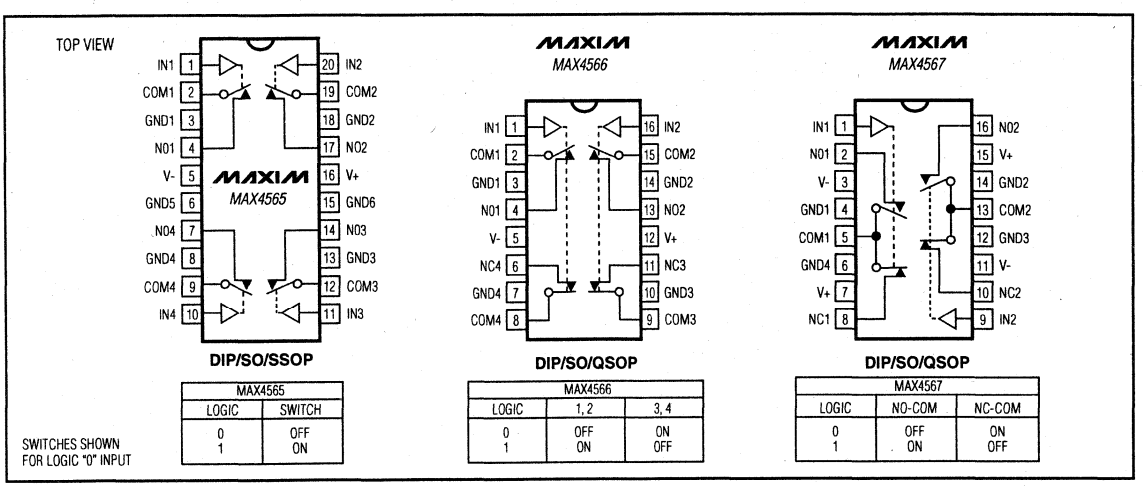
- **High 50Ω Off Isolation: -83dB at 10MHz**
- **Low 50Ω Crosstalk: -87dB at 10MHz**
- **DC to 350MHz -3dB Signal Bandwidth**
- **60Ω Signal Paths with ±5V Supplies**
- **2.5Ω Signal-Path Matching with ±5V Supplies**
- **2Ω Signal-Path Flatness with ±5V Supplies**
- **Low 50Ω Insertion Loss: 2.5dB at 100MHz**
- **±2.7V to ±6V Dual Supplies**
  +2.7V to +12V Single Supply
- **Low Power Consumption: <1µW**
- **Rail-to-Rail Bidirectional Signal Handling**
- **Pin Compatible with Industry-Standard DG540, DG542, DG643**
- **>2kV ESD Protection per Method 3015.7**
- **TTL/CMOS-Compatible Inputs with Single +5V or ±5V**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4565CPP	0°C to +70°C	20 Plastic DIP
MAX4565CWP	0°C to +70°C	20 Wide SO

Ordering Information continued at end of data sheet.

Pin Configurations/Functional Diagrams/Truth Tables



MAX4565	
LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "0" INPUT

MAX4566		
LOGIC	1, 2	3, 4
0	OFF	ON
1	ON	OFF

MAX4567		
LOGIC	NO-COM	NC-COM
0	OFF	ON
1	ON	OFF

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Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
V+ .....-0.3V, +13.0V
V- .....-13.0V, +0.3V
V+ to V- .....-0.3V, +13.0V
All Other Pins (Note 1) .....(V- - 0.3V) to (V+ + 0.3V)
Continuous Current into Any Terminal .....±25mA
Peak Current into Any Terminal
(pulsed at 1ms, 10% duty cycle) .....±50mA
ESD per Method 3015.7 .....>2000V
Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP
(derate 10.53mW/°C above +70°C) 842mW
16-Pin Narrow SO
(derate 8.70mW/°C above +70°C) 696mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
20-Pin Plastic DIP (derate 8.0mW/°C above +70°C) ...640mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin SSOP (derate 8.0mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX456_C_ E .....0°C to +70°C
MAX456_E_ E .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Voltages on all other pins exceeding V+ or V- are clamped by internal diodes. Limit forward diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	C, E	V-		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = ±2V, $I_{COM_}$ = 10mA	+25°C		46	60	Ω
			C, E			80	
Signal-Path On-Resistance Match Between Channels (Note 4)	ΔR_{ON}	V+ = 4.5V, V- = -4.5V, $V_{COM_}$ = ±2V, $I_{COM_}$ = 10mA	+25°C		1	2.5	Ω
			C, E			3	
Signal-Path On-Resistance Flatness (Note 5)	$R_{FLAT(ON)}$	V+ = 5V; V- = -5V; $V_{COM_}$ = 1V, 0V, -1V; I_{COM} = 10mA	+25°C		0.3	2	Ω
NO_, NC_ Off Leakage Current (Note 6)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓4.5V	+25°C	-1	0.02	1	nA
			C, E	-10		10	
COM_ Off Leakage Current (Note 6)	$I_{COM_(OFF)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V, $V_{N_}$ = ∓4.5V	+25°C	-1	0.02	1	nA
			C, E	-10		10	
COM_ On Leakage Current (Note 6)	$I_{COM_(ON)}$	V+ = 5.5V, V- = -5.5V, $V_{COM_}$ = ±4.5V	+25°C	-2	0.04	2	nA
			C, E	-20		20	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.03	1	µA

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		T_A	MIN	TYP (Note 2)	MAX	UNITS
SWITCH DYNAMIC CHARACTERISTICS								
Turn-On Time	t_{ON}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 3		+25°C		75	150	ns
				C, E			200	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 3		+25°C		30	100	ns
				C, E			120	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM_}$ = ±3V, V+ = 5V, V- = -5V, Figure 4		+25°C	5	30		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, $V_{NO_}$ = 0V, R_S = 0Ω, Figure 5		+25°C		25	60	pC
NO_, NC_ Off Capacitance	$C_{N_(OFF)}$	$V_{NO_}$ = GND, f = 1MHz, Figure 7		+25°C		2.5		pF
COM_ Off Capacitance	$C_{COM_(OFF)}$	$V_{COM_}$ = 0V, f = 1MHz, Figure 7	MAX4565, MAX4566	+25°C		2.5		pF
COM_ On Capacitance	$C_{COM_(ON)}$	$V_{COM_}$ = $V_{NO_}$ = 0V, f = 1MHz, Figure 7	MAX4565	+25°C		6		pF
			MAX4566			6		
			MAX4567			7		
Off Isolation (Note 7)	V_{ISO}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 6	MAX4565	+25°C		-83		dB
			MAX4566			-82		
			MAX4567			-83		
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, $V_{COM_}$ = $1V_{RMS}$, f = 10MHz, Figure 6	MAX4565	+25°C		-92		dB
			MAX4566			-85		
			MAX4567			-87		
-3dB Bandwidth (Note 9)	BW	Figure 6, R_L = 50Ω		+25°C		350		MHz
Distortion	THD+N	V_{IN} = 5Vp-p, f < 20kHz, 600Ω in and out		+25°C		0.02		%
POWER SUPPLY								
Power-Supply Range	V+, V-			C, E	-6		+6	V
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+		+25°C	-1	0.05	1	µA
				C, E	-10		10	
V - Supply Current	I-	V- = -5.5V		+25°C	-1	0.05	1	µA
				C, E	-10		10	

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

ELECTRICAL CHARACTERISTICS—Single +5V Supply

(V+ = +4.5V to +5.5V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		68	120	Ω
			C, E			150	
Signal-Path On-Resistance Match	ΔR_{ON}	V+ = 4.5V, $V_{COM_}$ = 3.5V, $I_{COM_}$ = 1mA	+25°C		2	5	Ω
			C, E			6	
NO_, NC_ Off Leakage Current (Notes 6, 10)	$I_{NO_(OFF)}$, $I_{NC_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, $V_{N_}$ = 4.5V	+25°C	-1		1	nA
			C, E	-10		10	
COM_ Off Leakage Current (Notes 6, 10)	$I_{COM_(OFF)}$	V+ = 5.5V, $V_{COM_}$ = 1V, $V_{N_}$ = 4.5V	+25°C	-1		1	nA
			C, E	-10		10	
COM_ On Leakage Current (Notes 6, 10)	$I_{COM_(ON)}$	V+ = 5.5V; $V_{COM_}$ = 1V, 4.5V	+25°C	-2		2	nA
			C, E	-20		20	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}		C, E		1.5	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}		C, E	0.8	1.5		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V	C, E	-1	0.001	1	µA
SWITCH DYNAMIC CHARACTERISTICS							
Turn-On Time	t_{ON}	$V_{COM_}$ = 3V, V+ = 5V, Figure 3	+25°C		130	200	ns
			C, E			250	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 3V, V+ = 5V, Figure 3	+25°C		30	120	ns
			C, E			150	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM_}$ = 3V, V+ = 5V, Figure 4	+25°C	10	90		ns
Charge Injection	Q	C_L = 1.0nF, V_{NO} = 2.5V, R_S = 0Ω, Figure 5	+25°C		7	25	pC
Off-Isolation (Note 7)	V_{ISO}	R_L = 50Ω, f = 10MHz, $V_{COM_}$ = $1V_{RMS}$, Figure 6	+25°C		-81		dB
Channel-to-Channel Crosstalk (Note 8)	V_{CT}	R_L = 50Ω, f = 10MHz, $V_{COM_}$ = $1V_{RMS}$, Figure 6	+25°C		-86		dB
-3dB Bandwidth (Note 9)	BW	R_L = 50Ω, Figure 6	+25°C		320		MHz
POWER SUPPLY							
V+ Supply Current	I+	V+ = 5.5V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

ELECTRICAL CHARACTERISTICS—Single +3V Supply

(V+ = +2.7V to +3.6V, V- = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, $V_{GND_}$ = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP (Note 2)	MAX	UNITS
ANALOG SWITCH							
Analog Signal Range	$V_{COM_}$, $V_{NO_}$, $V_{NC_}$	(Note 3)	+25°C	0		V+	V
Signal-Path On-Resistance	R_{ON}	V+ = 2.7V, $V_{COM_}$ = 1V, $I_{COM_}$ = 1mA	+25°C		150	350	Ω
			C, E			450	
LOGIC INPUT							
IN_ Input Logic Threshold High	V_{IN_H}	(Note 3)	C, E		1.0	2.4	V
IN_ Input Logic Threshold Low	V_{IN_L}	(Note 3)	C, E	0.8	1.0		V
IN_ Input Current Logic High or Low	$I_{INH_}$, $I_{INL_}$	$V_{IN_}$ = 0.8V or 2.4V (Note 3)	C, E	-1		1	µA
SWITCH DYNAMIC CHARACTERISTICS (Note 3)							
Turn-On Time	t_{ON}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 3 (Note 3)	+25°C		270	500	ns
			C, E			600	
Turn-Off Time	t_{OFF}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 3 (Note 3)	+25°C		40	100	ns
			C, E			120	
Break-Before-Make Time Delay (MAX4566/MAX4567 only)	t_{BBM}	$V_{COM_}$ = 1.5V, V+ = 2.7V, Figure 4 (Note 3)	+25°C	10	120		ns
POWER SUPPLY							
V+ Supply Current	I+	V+ = 3.6V, all $V_{IN_}$ = 0V or V+	+25°C	-1	0.05	1	µA
			C, E	-10		10	

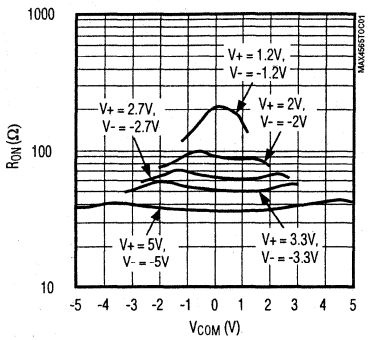
Note 2: The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
Note 3: Guaranteed by design.
Note 4: $\Delta R_{ON} = \Delta R_{ON(MAX)} - \Delta R_{ON(MIN)}$.
Note 5: Resistance flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured over the specified analog signal range.
Note 6: Leakage parameters are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 7: Off isolation = $20\log_{10}$ [V_{COM} / (V_{NC} or V_{NO})], V_{COM} = output, V_{NC} or V_{NO} = input to off switch.
Note 8: Between any two switches.
Note 9: -3dB bandwidth is measured relative to 100kHz.
Note 10: Leakage testing for single-supply operation is guaranteed by testing with dual supplies.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

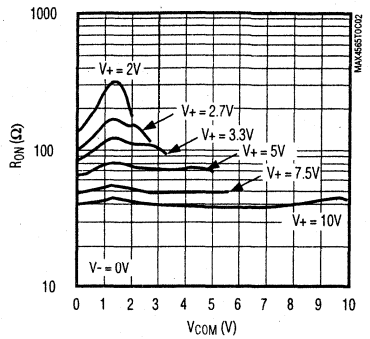
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

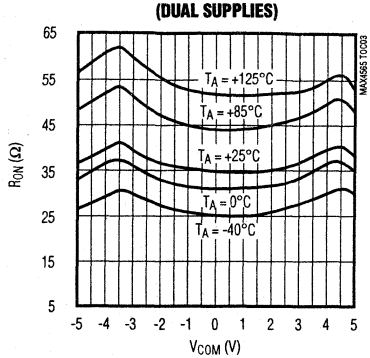
ON RESISTANCE vs. V_{COM} (DUAL SUPPLIES)



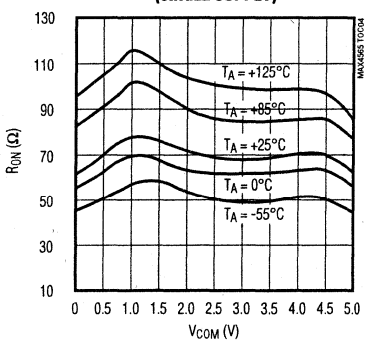
ON RESISTANCE vs. V_{COM} (SINGLE SUPPLY)



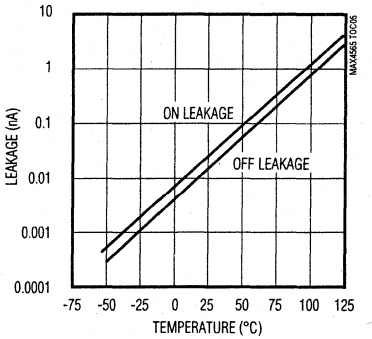
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (DUAL SUPPLIES)



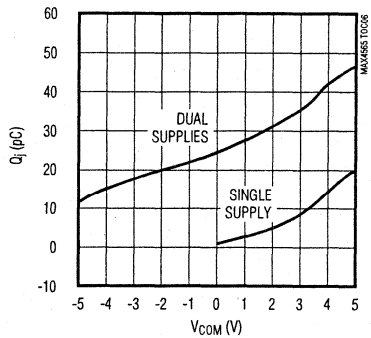
ON-RESISTANCE vs. V_{COM} AND TEMPERATURE (SINGLE SUPPLY)



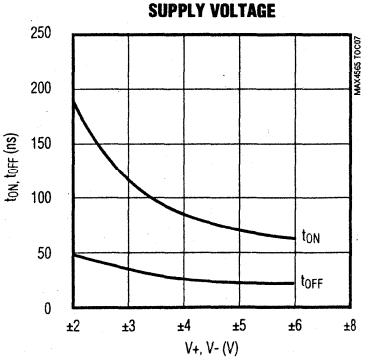
ON/OFF-LEAKAGE CURRENT vs. TEMPERATURE



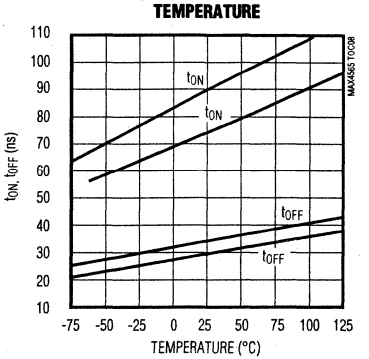
CHARGE INJECTION vs. V_{COM}



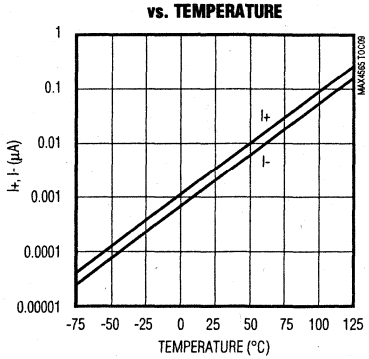
ON/OFF TIME vs. SUPPLY VOLTAGE



ON/OFF TIME vs. TEMPERATURE



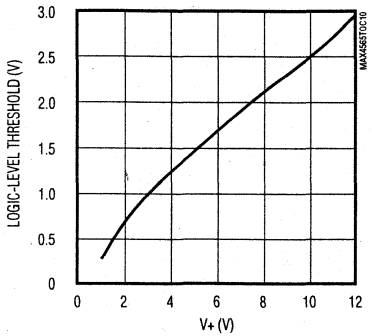
POWER-SUPPLY CURRENT vs. TEMPERATURE



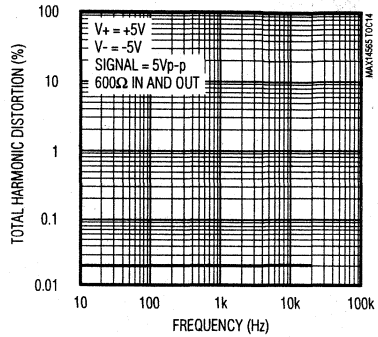
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, GND = 0V, packages are surface mount, unless otherwise noted.)

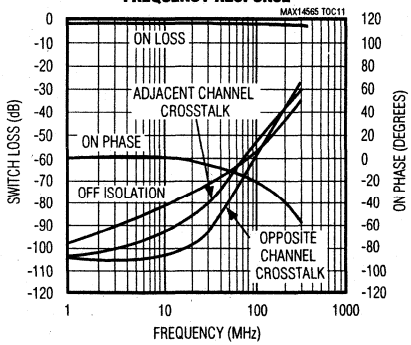
LOGIC-LEVEL THRESHOLD VOLTAGE vs. V+ SUPPLY VOLTAGE



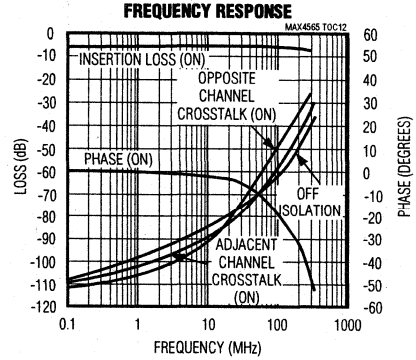
MAX4567 TOTAL HARMONIC DISTORTION vs. FREQUENCY



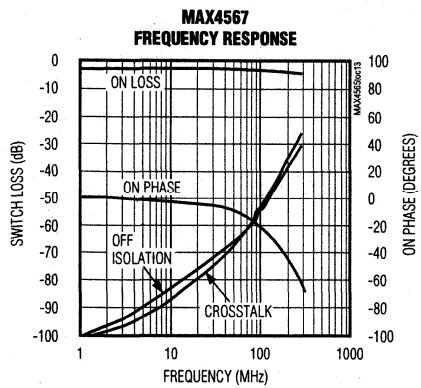
MAX4565 FREQUENCY RESPONSE



MAX4566 FREQUENCY RESPONSE



MAX4567 FREQUENCY RESPONSE



Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Pin Description

PIN			NAME	FUNCTION*
MAX4565	MAX4566	MAX4567		
1, 10, 11, 20	1, 16	1, 9	IN_	Digital Control Input
3, 6, 8, 13, 15, 18	3, 7, 10, 14	4, 6, 12, 14	GND_	RF and Logic Ground. Grounds are not internally connected to each other, and should all be connected to a ground plane (see *Grounding* section).
16	12	7, 15	V+	Positive Supply-Voltage Input (analog and digital)
5	5	3, 11	V-	Negative Supply-Voltage Input. Connect to ground plane for single-supply operation.
4, 7, 14, 17	4, 13	2, 16	NO_	Analog Switch Normally Open** Terminals
—	6, 11	8, 10	NC_	Analog Switch Normally Closed** Terminals
2, 9, 12, 19	2, 8, 9, 15	5, 13	COM_	Analog Switch Common** Terminals

* All pins have ESD diodes to V- and V+.

** NO_ (or NC_) and COM_ pins are identical and interchangeable. Either may be considered as an input or output; signals pass equally well in either direction.

Theory of Operation

The MAX4565/MAX4566/MAX4567 are high-frequency "T" switches. Each "T" switch consists of two series CMOS switches, with a third N-channel switch at the junction that shunts capacitively-coupled signals to ground when the series switches are off. This produces superior high-frequency signal isolation when the switch is turned off.

Logic-Level Translators

The MAX4565/MAX4566/MAX4567 are constructed as high-frequency "T" switches, as shown in Figure 1. The logic-level input, IN_, is translated by amplifier A1 into a V+ to V- logic signal that drives amplifier A2. (Amplifier A2 is an inverter for normally closed switches.) Amplifier A2 drives the gates of N-channel MOSFETs N1 and N2 from V+ to V-, turning them fully on or off. The same signal drives inverter A3 (which drives the P-channel MOSFETs P1 and P2) from V+ to V-, turning them fully on or off, and drives the N-channel MOSFET N3 off and on.

The logic-level threshold is determined by V+ and GND_. The voltage on GND_ is usually at ground potential, but it may be set to any voltage between (V+ - 2V) and V-. When the voltage between V+ and GND_ is less than 2V, the level translators become very slow and unreliable. Since individual switches in each package have individual GND_ pins, they may be set to different voltages. Normally, however, they should all be connected to the ground plane.

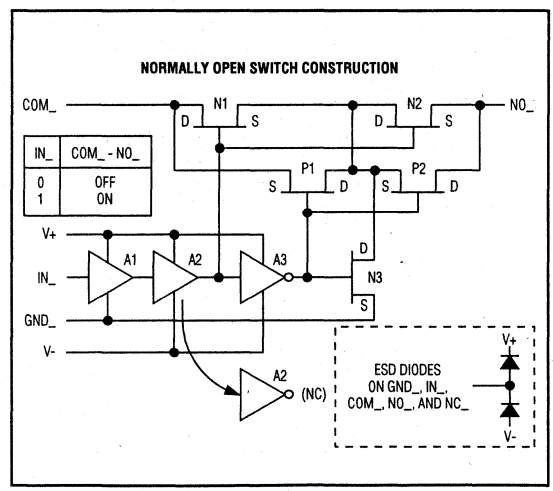


Figure 1. T-Switch Construction

Switch On Condition

When the switch is on, MOSFETs N1, N2, P1, and P2 are on and MOSFET N3 is off. The signal path is COM_ to NO_, and because both N-channel and P-channel MOSFETs act as pure resistances, it is symmetrical (i.e., signals may pass in either direction). The off MOSFET, N3, has no DC conduction, but has a small

amount of capacitance to GND_. The four on MOSFETs also have capacitance to ground that, together with the series resistance, forms a lowpass filter. All of these capacitances are distributed evenly along the series resistance, so they act as a transmission line rather than a simple R-C filter. This helps to explain the exceptional 350MHz bandwidth when the switches are on.

Typical attenuation in 50Ω systems is -2.5dB and is reasonably flat up to 300MHz. Higher-impedance circuits show even lower attenuation (and vice versa), but slightly lower bandwidth due to the increased effect of the internal and external capacitance and the switch's internal resistance.

The MAX4565/MAX4566/MAX4567 are optimized for ±5V operation. Using lower supply voltages or a single supply increases switching time, increases on-resistance (and therefore on-state attenuation), and increases nonlinearity.

Switch Off Condition

When the switch is off, MOSFETs N1, N2, P1, and P2 are off and MOSFET N3 is on. The signal path is through the off-capacitances of the series MOSFETs, but it is shunted to ground by N3. This forms a high-pass filter whose exact characteristics are dependent on the source and load impedances. In 50Ω systems, and below 10MHz, the attenuation can exceed 80dB. This value decreases with increasing frequency and increasing circuit impedances. External capacitance and board layout have a major role in determining overall performance.

Applications Information

Power-Supply Considerations

Overview

The MAX4565/MAX4566/MAX4567 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and set the limits of the analog voltage on any switch. Reverse ESD protection diodes are internally connected between each analog signal pin and both V+ and V-. If the voltage on any pin exceeds V+ or V-, one of these diodes will conduct. During normal operation these reverse-biased ESD diodes leak, forming the only current drawn from V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The *difference* in the two diode leakages from the signal path to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This explains how both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND. The analog signal paths consist of an N-channel and P-channel MOSFET with their sources and drains paralleled and their gates driven out of phase with V+ and V- by the logic-level translators.

V+ and GND power the internal logic and logic-level translators, and set the input logic thresholds. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the gates of the analog switches. This drive signal is the only connection between the logic supplies and the analog supplies. All pins have ESD protection to V+ and to V-.

Increasing V- has no effect on the logic-level thresholds, but it does increase the drive to the P-channel switches, reducing their on-resistance. V- also sets the negative limit of the analog signal voltage.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly; when V+ reaches +12V, the level threshold is about 3.1V, which is above the TTL output high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar-Supply Operation

The MAX4565/MAX4566/MAX4567 operate with bipolar supplies between ±2.7V and ±6V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 13.0V. **Do not connect the MAX4565/MAX4566/MAX4567 V+ pin to +3V and connect the logic-level input pins to TTL logic-level signals. TTL logic-level outputs can exceed the absolute maximum ratings, causing damage to the part and/or external circuits.**

CAUTION:

The absolute maximum V+ to V- differential voltage is 13.0V. Typical "±6-Volt" or "12-Volt" supplies with ±10% tolerances can be as high as 13.2V. This voltage can damage the MAX4565/MAX4566/MAX4567. Even ±5% tolerance supplies may have overshoot or noise spikes that exceed 13.0V.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Single-Supply Operation

The MAX4565/MAX4566/MAX4567 operate from a single supply between +2.7V and +12V when V- is connected to GND. All of the bipolar precautions must be observed. Note, however, that these parts are optimized for ±5V operation, and most AC and DC characteristics are degraded significantly when departing from ±5V. As the overall supply voltage (V+ to V-) is lowered, switching speed, on-resistance, off isolation, and distortion are degraded. (See *Typical Operating Characteristics*.)

Single-supply operation also limits signal levels and interferes with grounded signals. When V- = 0V, AC signals are limited to -0.3V. Voltages below -0.3V can be clipped by the internal ESD-protection diodes, and the parts can be damaged if excessive current flows.

Power Off

When power to the MAX4565/MAX4566/MAX4567 is off (i.e., V+ = 0V and V- = 0V), the Absolute Maximum Ratings still apply. This means that neither logic-level inputs on IN_ nor signals on COM_, NO_, or NC_ can exceed ±0.3V. Voltages beyond ±0.3V cause the internal ESD-protection diodes to conduct, and the parts can be damaged if excessive current flows.

Grounding

DC Ground Considerations

Satisfactory high-frequency operation requires that careful consideration be given to grounding. **For most applications, a ground plane is strongly recommended, and all GND_ pins should be connected to it with solid copper.** While the V+ and V- power-supply pins are common to all switches in a given package, each switch has separate ground pins that are not internally connected to each other. This contributes to the overall high-frequency performance and provides added flexibility in some applications, but it can cause problems if it is overlooked. All the GND_ pins have ESD diodes to V+ and V-.

In systems that have separate digital and analog (signal) grounds, connect these switch GND_ pins to analog ground. Preserving a good signal ground is much more important than preserving a digital ground.

The logic-level inputs, IN_, have voltage thresholds determined by V+ and GND_. (V- does not influence the logic-level threshold.) With +5V and 0V applied to V+ and GND_, the threshold is about 1.6V, ensuring compatibility with TTL- and CMOS-logic drivers.

The various GND_ pins can be connected to separate voltage potentials if any or all of the logic-level inputs is not a normal logic signal. (The GND_ voltages cannot exceed (V+ - 2V) or V-.) Elevating GND_ reduces off isolation. For example, using the MAX4565, if GND2–GND6 are connected to 0V and GND1 is connected to V-, then switches 2, 3, and 4 would be TTL/CMOS compatible, but switch 1 (IN1) could be driven with the rail-to-rail output of an op amp operating from V+ and V-. Note, however, that IN_ can be driven more negative than GND_, as far as V-. GND_ does not have to be removed from 0V when IN_ is driven from bipolar sources, but the voltage on IN_ should never exceed V-. GND_ should be separated from 0V only if the logic-level threshold has to be changed.

Any GND_ pin not connected to 0V should be bypassed to the ground plane with a surface-mount 10nF capacitor to maintain good RF grounding. DC current in the IN_ and GND_ pins is less than 1nA, but increases with switching frequency.

On the MAX4565 only, two extra ground pins—GND5 and GND6—are provided to improve isolation and crosstalk. They are not connected to the logic-level circuit. These pins should always be connected to the ground plane with solid copper.

AC Ground and Bypassing

A ground plane is mandatory for satisfactory high-frequency operation. (Prototyping using hand wiring or wire-wrap boards is strongly discouraged.) Connect all 0V GND_ pins to the ground plane with solid copper. (The GND_ pins extend the high-frequency ground through the package wire-frame, into the silicon itself, thus improving isolation.) The ground plane should be solid metal underneath the device, without interruptions. There should be no traces under the device itself. **For DIP packages, this applies to both sides of a two-sided board.** Failure to observe this will have a minimal effect on the "on" characteristics of the switch at high frequencies, but it will degrade the off isolation and crosstalk.

Bypass all V+ and V- pins to the ground plane with surface-mount 10nF capacitors. For DIP packages, mount the capacitors as close as possible to the pins on the same side of the board as the device. Do not use feedthroughs or vias for bypass capacitors.

For surface-mount packages, bypass capacitors should be mounted on the opposite side of the board from the device. In this case, use short feedthroughs or vias, directly under the V+ and V- pins. Any GND_ pin not connected to 0V should be similarly bypassed. If V- is 0V, connect it directly to the ground plane with solid copper. Keep all leads short.

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

The MAX4567 has two V+ and two V- pins. Make DC connections to only one of each to minimize crosstalk. Do not route DC current into one of the V+ or V- pins and out the other V+ or V- pin to other devices. The second set of V+ and V- pins is for AC bypassing only.

For dual-supply operation, the MAX4567 should have four 10nF bypass capacitors connected to each V+ and V- pin as close to the package as possible. For single-supply operation, the MAX4567 should have two 10nF bypass capacitors connected (one to each V+ pin) as close to the package as possible.

On the MAX4565, GND5 and GND6 should always be connected to the ground plane with solid copper to improve isolation and crosstalk.

Signal Routing

Keep all signal leads as short as possible. Separate all signal leads from each other and other traces with the ground plane on both sides of the board. Where possible, use coaxial cable instead of printed circuit board traces.

Board Layout

IC sockets degrade high-frequency performance and should not be used if signal bandwidth exceeds 5MHz. Surface-mount parts, having shorter internal lead frames, provide the best high-frequency performance. Keep all bypass capacitors close to the device, and separate all signal leads with ground planes. Such grounds tend to be wedge-shaped as they get closer to the device. Use vias to connect the ground planes on each side of the board, and place the vias in the apex of the wedge-shaped grounds that separate signal leads. Logic-level signal lead placement is not critical.

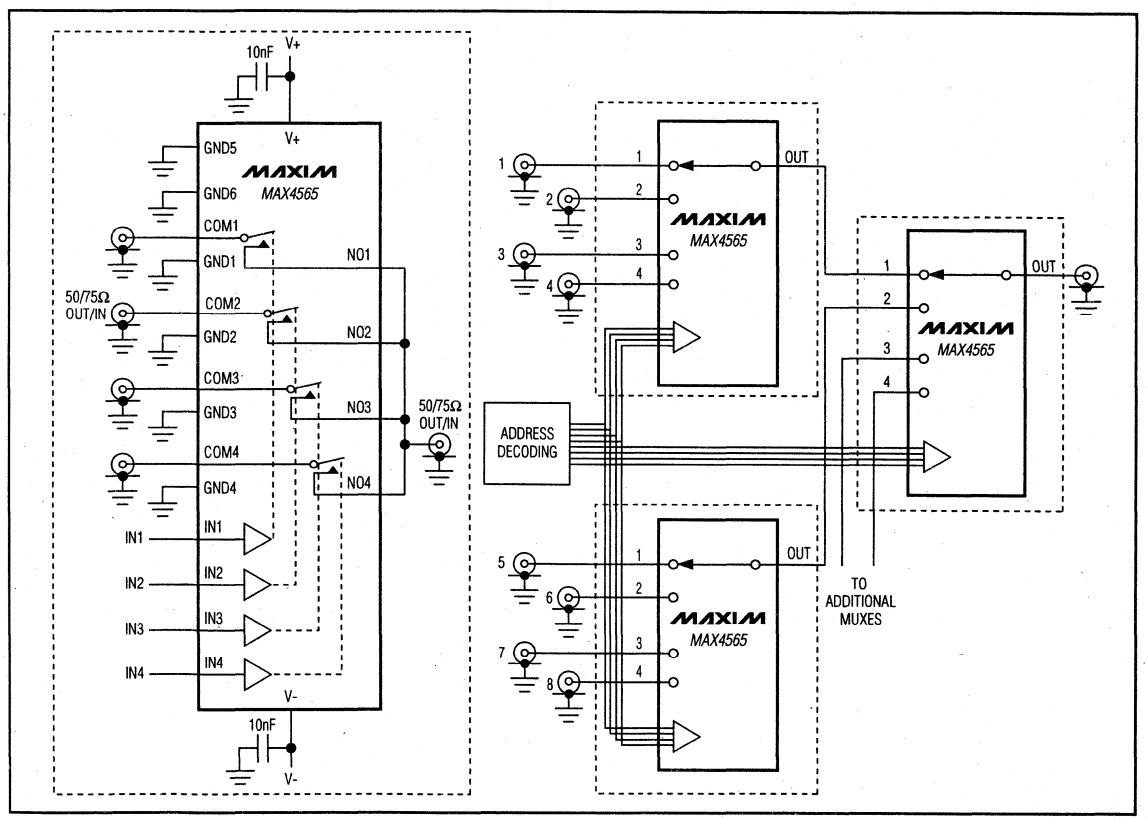


Figure 2. 4-Channel Multiplexer

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Multiplexer

With its excellent off isolation, the MAX4565 is ideal for use in high-frequency video multiplexers. Figure 2 shows such an application for switching any one of four video inputs to a single output. The same circuit may be used as a demultiplexer by simply reversing the signal direction.

Stray capacitance of traces and the output capacitance of switches placed in parallel reduces bandwidth, so the outputs of no more than four individual switches should be placed in parallel to maintain a high bandwidth. If more than four mux channels are needed, the 4-channel circuit should be duplicated and cascaded.

Test Circuits/Timing Diagrams

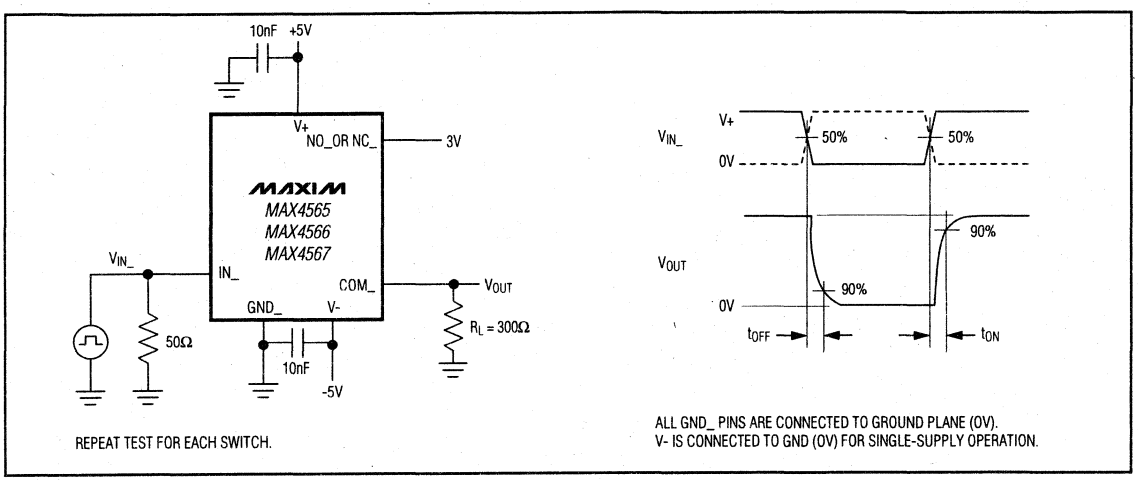


Figure 3. Switching Time

Test Circuits/Timing Diagrams (continued)

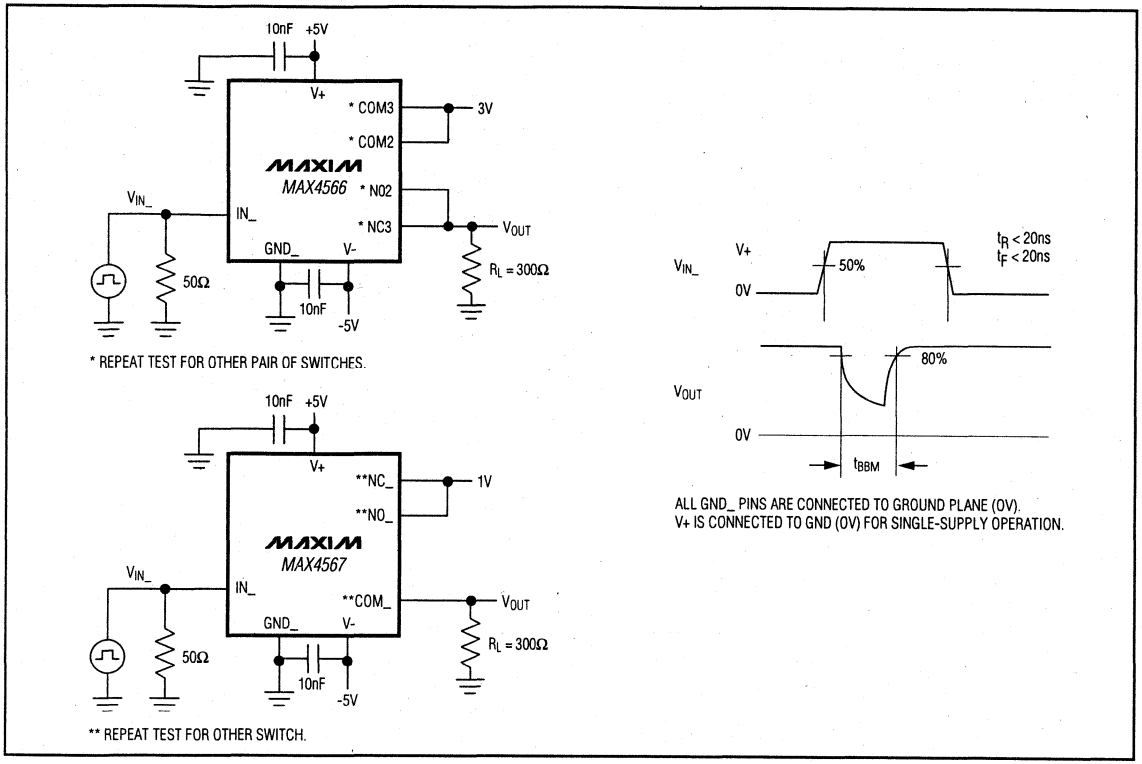


Figure 4. Break-Before-Make Interval (MAX4566/MAX4567 only)

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Test Circuits/Timing Diagrams (continued)

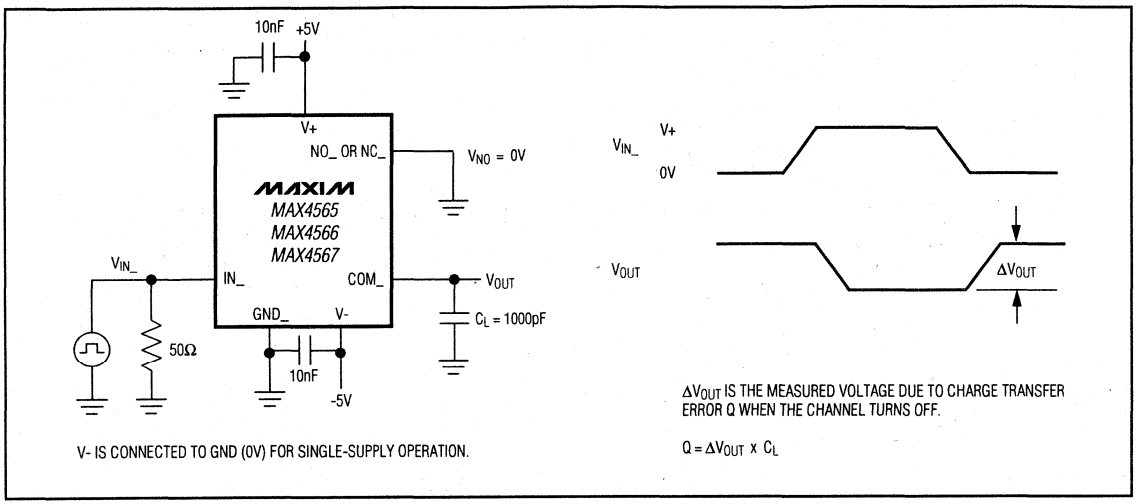


Figure 5. Charge Injection

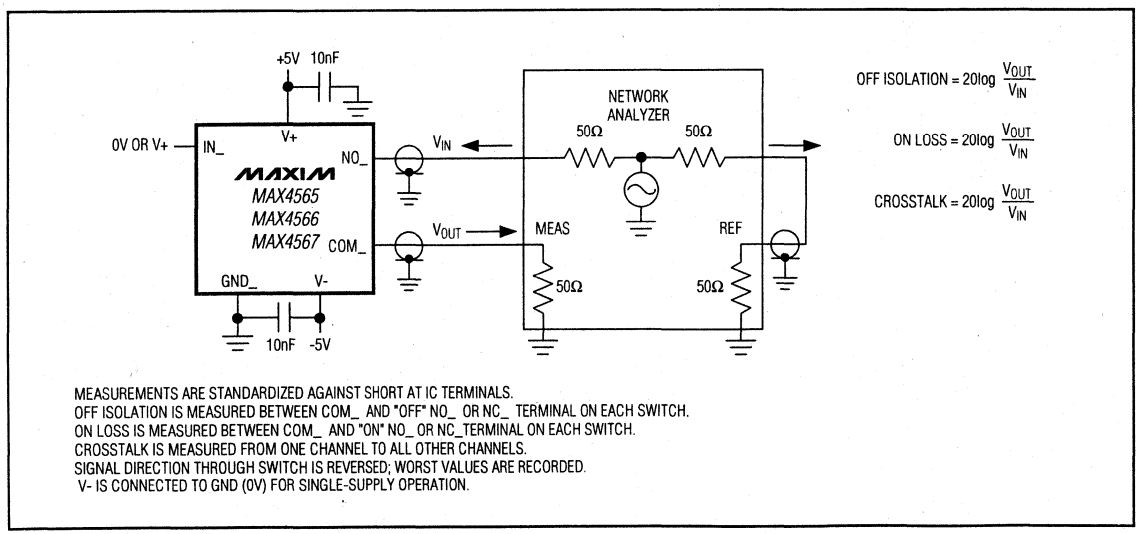


Figure 6. On Loss, Off Isolation, and Crosstalk

Test Circuits/Timing Diagrams (continued)

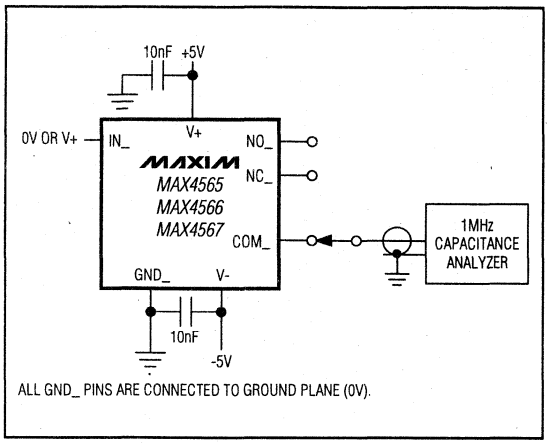
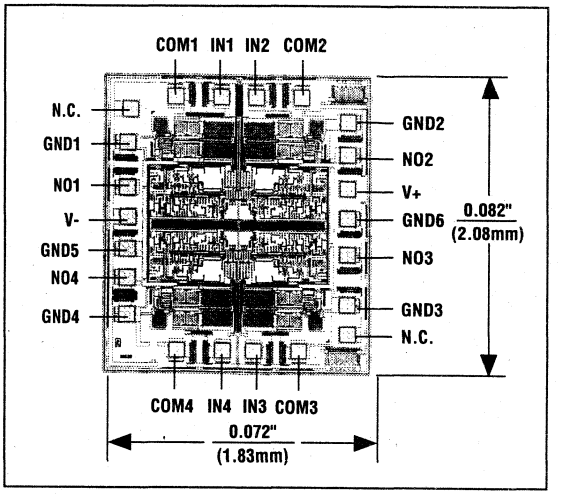


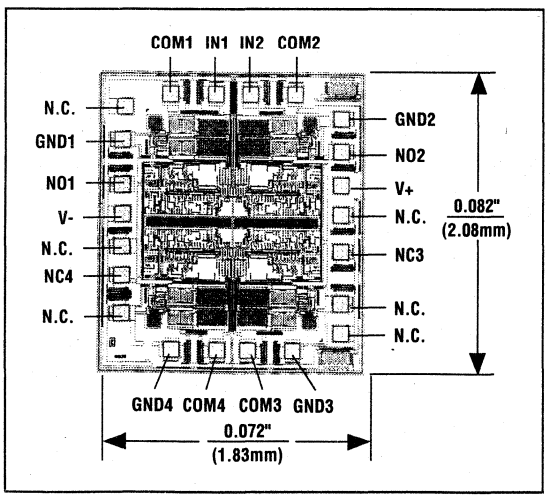
Figure 7. NO_, NC_, COM_ Capacitance

Chip Topographies

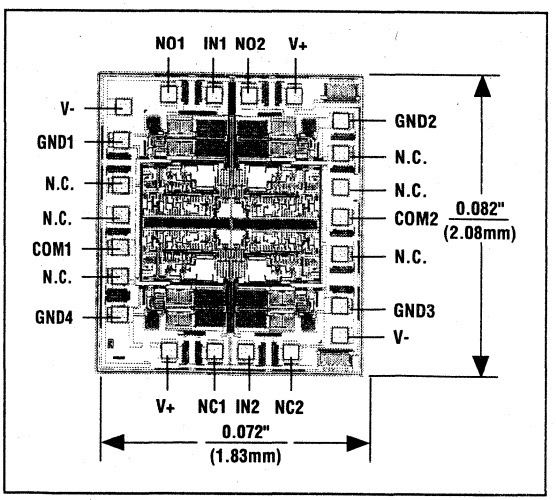
MAX4565



MAX4566



MAX4567



TRANSISTOR COUNT: 257
SUBSTRATE INTERNALLY CONNECTED TO V+

Quad/Dual, Low-Voltage, Bidirectional RF/Video Switches

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX4565CAP	0°C to +70°C	20 SSOP
MAX4565C/D	0°C to +70°C	Dice*
MAX4565EPP	-40°C to +85°C	20 Plastic DIP
MAX4565EWP	-40°C to +85°C	20 Wide SO
MAX4565EAP	-40°C to +85°C	20 SSOP
MAX4566CPE	0°C to +70°C	16 Plastic DIP
MAX4566CSE	0°C to +70°C	16 Narrow SO
MAX4566CEE	0°C to +70°C	16 QSOP
MAX4566C/D	0°C to +70°C	Dice*
MAX4566EPE	-40°C to +85°C	16 Plastic DIP
MAX4566ESE	-40°C to +85°C	16 Narrow SO
MAX4566EEE	-40°C to +85°C	16 QSOP
MAX4567CPE	0°C to +70°C	16 Plastic DIP
MAX4567CSE	0°C to +70°C	16 Narrow SO
MAX4567CEE	0°C to +70°C	16 QSOP
MAX4567C/D	0°C to +70°C	Dice*
MAX4567EPE	-40°C to +85°C	16 Plastic DIP
MAX4567ESE	-40°C to +85°C	16 Narrow SO
MAX4567EEE	-40°C to +85°C	16 QSOP

Contact factory for dice specifications.

Interface Products

Interface Products, Product Tables and Trees 2-2

MAX3100 SPI/Microwire-Compatible UART in QSOP-16 2-9

MAX3187 ±15kV ESD-Protected, EMC-Compliant, 230kbps Dual RS-232 Serial Port for Motherboards/Desktops 2-33

MAX3243E 15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown 2-41

MAX3244 1µA Supply Current, 3.0V to 5.5V, 250kbps RS-232 Transceiver with AutoShutdown Plus 2-59

MAX3244E ±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus 2-41

MAX3245 1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with with AutoShutdown Plus 2-59

MAX3245E ±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus and 24V/µs Slew Rate 2-41

MAX3320A/B/L/T 3V to 5.5V, 250kbps, True RS-232 Transceiver with 4mA AutoShutdown Plus and Power-On Reset 2-73

Line Drivers/Receivers

see next page for RS-485/RS-422

AppleTalk™

MAX216 (1 single-ended Tx/2 single-ended Rx, 1 differential Tx/1 differential Rx)

MegaBaud™ Mode

MAX3237 (5Tx/3Rx)

★ MAX3245 (3Tx/5Rx, 1µA AutoShutown Plus)

★ MAX3245E (3Tx, 5Rx, 1µA AutoShutown Plus, ±15kV ESD per human body model & IEC 1000-4-2)

2 DRVRs, 2 RCVRs

MAX218 (1.8V to 4.25V V_{CC} in, true RS-232 out)

MAX563 (120kbps data rate, 2Rx active in shutdown)

MAX3222 (true RS-232, 0.1µF caps, 2Rx active in shutdown)

MAX3232 (true RS-232, 0.1µF caps)

4 DRVRs, 5 RCVRs

MAX560 (2Rx active in shutdown)

MAX561 (shutdown)

Complete PC Serial Ports

☆ MAX212 (true RS-232, 3mA I_{CC} max)

MAX562 (2.7V to 5.25V operation)

MAX3241 (true RS-232, 0.1µF caps, 1mA I_{CC} max)

+3V Powered

1µA Supply Current

MAX3212 (3Tx/5Rx, 2.7V to 3.6V operation)

MAX3218 (2Tx/2Rx, 1.8V to 4.25V operation)

MAX3221 (1Tx/1Rx, 3.0V to 5.5V operation, 0.1µF caps)

MAX3223 (2Tx/2Rx, 3.0V to 5.5V operation, 0.1µF caps)

MAX3238 (5Tx/3Rx, 3.0V to 5.5V operation, 0.1µF caps)

MAX3243 (3Tx/5Rx, 3.0V to 5.5V operation, 0.1µF caps)

MAX3243E (3Tx/5Rx, 1µA AutoShutdown, ±15kV ESD protection per human body model & IEC 1000-4-2)

MAX3244 (3Tx/5Rx, 1µA AutoShutdown Plus)

MAX3244E (3Tx/5Rx, 1µA AutoShutdown Plus, ±15kV ESD protection per human body model & IEC 1000-4-2)

MAX3245 (3Tx/5Rx, 1µA AutoShutdown Plus)

MAX3245E (3Tx/5Rx, 1Mbps, 1µs AutoShutdown Plus, ±15kV ESD protection per human body model & IEC 1000-4-2)

MAX3320A/B/L/T (precise monitoring of 3.3V and 5V supply voltage, 100ms (min) power-on RESET, 2Tx/2Rx)

Integrated µP Supervisory

★ MAX3320A/B/L/T (precise monitoring of 3.3V and 5V supply voltage, 100ms (min) power-on RESET, 2Tx/2Rx)

+5V, 4 Ext. Caps

2 DRVRs, 2 RCVRs

MAX202 (0.1µF caps, low cost)

MAX220 (ultra-low power)

MAX222 (I_Q = 10µA in shutdown)

MAX232 (industry standard)

MAX232A (116kbits/sec data rate, 0.1µF caps)

MAX242 (receivers active in shutdown)

MAX243 (simplified cabling)

Complete PC Serial Ports

MAX211 (pin compatible with MAX241, 0.1µF caps)

MAX213 (2Rx active in shutdown, 0.1µF caps)

MAX214 (programmable DTE/DCE port)

MAX223 (2Rx active in shutdown)

MAX241 (industry standard)

High DRVR/RCVR Count

MAX200 (5Tx/0Rx, 0.1µF caps)

MAX204 (4Tx/0Rx, 0.1µF caps)

MAX206 (4Tx/3Rx, 0.1µF caps)

MAX207 (5Tx/3Rx, 0.1µF caps)

MAX208 (4Tx/4Rx, 0.1µF caps)

MAX230 (5Tx/0Rx)

MAX234 (4Tx/0Rx)

MAX236 (4Tx/3Rx)

MAX237 (5Tx/3Rx)

MAX238 (4Tx/4Rx)

MAX240 (5Tx/5Rx)

MAX244 (8Tx/10Rx)

MAX248 (8Tx/8Rx)

MAX249 (8Tx/10Rx)

RS-232

+5V, Internal Caps

2 DRVRs, 2 RCVRs

MAX203 (available in SO)

MAX233

MAX233A (116kbits/sec)

High DRVR/RCVR Count

MAX205 (5Tx/5Rx)

MAX225 (5Tx/5Rx, SO package)

MAX235 (5Tx/5Rx)

MAX245 (8Tx/10Rx)

MAX246 (8Tx/10Rx)

MAX247 (8Tx/9Rx)

±15kV ESD Protection per Human Body Model & IEC 1000-4-2

+5V, ±12V

MAX1406 (3Tx/3Rx)

MAX1488E (4Tx)

MAX1489E (4Rx)

MAX3185 (3Tx/5Rx)

MAX3186 (5Tx/3Rx)

★ MAX3187 (6Tx/10Rx)

+5V

MAX202E (2Tx/2Rx)

MAX203E (2Tx/2Rx, no external caps)

MAX205E (5Tx/5Rx, no external caps)

MAX206E (4Tx/3Rx)

MAX207E (5Tx/3Rx)

MAX208E (4Tx/4Rx)

MAX211E (4Tx/5Rx)

MAX213E (4Tx/5Rx)

MAX232E (2Tx/2Rx)

MAX241E (4Tx/5Rx)

+3V

MAX3241E (3Tx/5Rx)

MAX3243E (3Tx/5Rx, 1µA AutoShutdown)

MAX3244E (3Tx/5Rx, 1µA AutoShutdown Plus)

MAX3245E (3Tx/5Rx, 1Mbps, 1µs AutoShutdown Plus)

Isolation Products

2-Chip Set

MAX250

MAX251

Complete Module

MAX252A (UL recognized)

MAX252B (500V isolation)

+5V/+12V or Battery Power, 2 Ext. Caps

2 DRVRs, 2 RCVRs

MAX201 (0.1µF caps)

MAX231

Complete PC Serial Ports

MAX209 (3Tx/5Rx, 0.1µF caps)

MAX239 (3Tx/5Rx)

★ New product
☆ Evaluation kit available

AppleTalk is a trademark of Apple Computer, Inc.

Line Drivers/Receivers

see previous page for RS-232/AppleTalk™

RS-485/RS-422

+5V Powered

Fail-Safe Operation

MAX3080
(full-duplex, 115kbps)

MAX3081
(full-duplex, 115kbps)

MAX3082
(half-duplex, 115kbps)

MAX3083
(full-duplex, 0.5Mbps)

MAX3084
(full-duplex, 0.5Mbps)

MAX3085
(half-duplex, 0.5Mbps)

MAX3086
(full-duplex, 10Mbps)

MAX3087
(full-duplex, 10Mbps)

MAX3088
(half-duplex, 10Mbps)

MAX3089
(full/half-duplex selectability, selectable data rate)

Logic-Selectable Half-/Full-Duplex

★ MAX1485
(250kbps, reduces EMI by 100x, 256 Tx on the bus)

★ MAX1486
(12Mbps guaranteed, 256 Tx on the bus)

MAX3089
(selectable 115kbps/500kbps/10Mbps, true fail-safe operation, low-power shutdown, 256 Tx on the bus)

±15kV, ESD Protection

MAX481E
(1µA shutdown, half duplex)

MAX483E
(250kbps, reduces EMI by 100x)

MAX485E
(industry standard with ±15kV ESD protection)

MAX487E
(MAX483E plus 1/4-unit load)

MAX488E
(250kbps, reduces EMI by 100x)

MAX489E
(MAX488E plus Tx/Rx enable)

MAX490E
(2.5Mbps)

MAX491E
(MAX490E plus Tx/Rx enable)

MAX1487E
(MAX485E plus 1/4-unit load)

1 DRVR, 1 RCVR Full Duplex

MAX488
(250kbps, reduces EMI by 100x)

MAX489
(MAX488 plus Tx/Rx enable)

MAX490
(direct LTC490 replacement)

MAX491
(direct LTC491 replacement)

★ MAX1481
(10-pin µMAX package, 250kbps, reduces EMI by 100x, 256 Tx on the bus)

MAX1482
(250kbps, 256 transceivers on the bus, 20µA supply current)

★ MAX1484
(10-pin µMAX package, 12Mbps guaranteed, 256 Tx on the bus)

1 DRVR, 1 RCVR Half Duplex

MAX481
(MAX485 plus 1µA shutdown)

MAX483
(250kbps, reduces EMI by 100x)

MAX485
(direct LTC485 replacement)

MAX487
(MAX483 plus 1/4-unit load)

MAX1483
(250kbps, 256 Tx on the bus)

MAX1487
(2.5Mbps, 128 Tx on the bus)

Isolation Products

MAX253, MAX845
(isolation transformer driver)

MAX1480A
(complete 2.5Mbps isolated RS-485 in one package)

MAX1480B
(complete 250kbps isolated RS-485 in one package)

MAX1490A
(complete 2.5Mbps isolated RS-485 in one package)

MAX1490B
(complete 250kbps isolated RS-485 in one package)

MAX3480A
(complete 2.5Mbps isolated 3.3V RS-485 in one package)

MAX3480B
(complete 250kbps isolated 3.3V RS-485 in one package)

+3V Powered

1 DRVR, 1 RCVR Full Duplex

MAX3488
(250kbps, reduces EMI by 100x)

MAX3490
(10Mbps, 8-pin package)

MAX3491
(10Mbps, Tx/Rx enable)

1 DRVR, 1 RCVR Half Duplex

MAX3483
(250kbps, reduces EMI by 100x)

MAX3485
(10Mbps guaranteed data rate)

MAX3486
(2.5Mbps guaranteed data rate)

Isolation Products

MAX3480A
(complete 2.5Mbps, isolated RS-485 in one package)

MAX3480B
(complete 250kbps, isolated RS-485 in one package)

SPI™/Microwire™ UARTs

+3V Powered

★ MAX3100
(smallest UART available, 16-pin QSOP, 2.7V to 5.5V operation, IrDA SIR timing compatible, 8-word receive FIFO, up to 230kbps)

SPI is a trademark of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
+3V RS-232 PRODUCTS										
MAX212	+3 to +3.6	3/5	1.5	2	0.33/0.68	Yes	✔	Yes	250	5 receivers active in shutdown, I_{CC} = 1.5mA, chip inductor
MAX218	+1.8 to +4.25	2/2	1.9	3	0.47/1	Yes	✔	Yes	235	True RS-232 performance from 1.8V to 4.25V input
MAX560	+3 to +3.6	4/5	5	4	1	Yes	✔	No	116	+3V, MAX561 with receivers active in shutdown
MAX561	+3 to +3.6	4/5	5	4	1	Yes		No	116	+3V, complete IBM PC serial port
MAX562	+2.7 to +5.25	3/5	20	5	0.33/0.68	Yes	✔	No	280	+2.7V to +5.25V operation, 230kbps guaranteed data rate
MAX563	+3 to +3.6	2/2	3	4	0.1	Yes	✔	No	200	2 receivers active in shutdown
MAX3212	+2.7 to +3.6	3/5	1µA	2	0.33/0.68	Yes	✔	Yes	250	AutoShutdown™ reduces supply current to 1µA
MAX3218	+1.8 to +4.25	2/2	1µA	3	0.47/1	Yes	✔	Yes	235	AutoShutdown™ reduces supply current to 1µA
MAX3221	+3 to +5.5	1/1	1µA	4	0.1	Yes	✔	Yes	235	AutoShutdown™ reduces supply current to 1µA
MAX3222	+3 to +5.5	2/2	300µA	4	0.1	Yes	✔	Yes	235	2 receivers active in shutdown, 0.5mA I_{CC}, true RS-232
MAX3223	+3 to +5.5	2/2	1µA	4	0.1	Yes	✔	Yes	235	AutoShutdown™ reduces supply current to 1µA
MAX3232	+3 to +5.5	2/2	300µA	4	0.1	No		Yes	235	Industry-standard MAX232 pinout, true RS-232
MAX3237	+3 to +5.5	5/3	500µA	4	0.1	Yes	✔	Yes	1Mbps	World's fastest RS-232 transceiver at 1Mbps
MAX3238	+3 to +5.5	5/3	1µA	4	0.1	Yes	✔	Yes	250	AutoShutdown Plus™ reduces supply current to 1µA
MAX3241	+3 to +5.5	3/5	300µA	4	0.1	Yes	✔	Yes	235	Mouse driveability, 2 spare receivers active in shutdown, true RS-232
MAX3243	+3 to +5.5	3/5	1µA	4	0.1	Yes	✔	Yes	230	AutoShutdown™ reduces supply current to 1µA
MAX3244	+3 to +5.5	3/5	1µA	4	0.1	Yes	✔	Yes	250	AutoShutdown™ Plus reduces supply current to 1µA
MAX3245	+3 to +5.5	3/5	1µA	4	0.1	Yes	✔	Yes	1Mbps	MegaBaud™ (1Mbps) operation, AutoShutdown Plus reduces supply current to 1µA
+5V RS-232 PRODUCTS										
MAX200(MAX230)	+5	5/0	11(7)	4	0.1(1)	Yes		Yes	120	5 drivers with shutdown
MAX201(MAX231)	+5 and +7.5 to +13.2	2/2	400µA	2	0.1(1)	No		Yes	120	Standard +5/+12V or battery supplies; same functions as MAX232
MAX202(MAX232)	+5	2/2	8(5)	4	0.1(1)	No		Yes	120	Industry standard
MAX203(MAX233)	+5	2/2	8(5)	0	–	No		Yes	120	No external caps, MAX203 available in SOIC
MAX204(MAX234)	+5	4/0	11(7)	4	0.1(1)	No		Yes	120	Replaces 1488
MAX205(MAX235)	+5	5/5	11(7)	0	–	Yes		Yes	120	No external caps
MAX206(MAX236)	+5	4/3	11(7)	4	0.1(1)	Yes		Yes	120	Shutdown, three-state
MAX207(MAX237)	+5	5/3	11(7)	4	0.1(1)	No		Yes	120	Complements IBM PC serial port
MAX208(MAX238)	+5	4/4	11(7)	4	0.1(1)	No		Yes	120	Replaces 1488 and 1489
MAX209(MAX239)	+5 and +7.5 to +13.2	3/5	400µA	2	0.1(1)	No		Yes	120	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX211(MAX241)	+5	4/5	11(7)	4	0.1(1)	Yes		Yes	120	Complete IBM PC serial port, industry standard
MAX213(MAX223)	+5	4/5	11(7)	4	0.1(1)	Yes	2	Yes	120	MAX241 + receivers active in shutdown
MAX214	+5	3/5 or 5/3	9	4	1	Yes	✔	Yes	200	Programmable DTE/DCE port
MAX220	+5	2/2	500µA	4	4.7/10	No		Yes	22	Ultra-low power, industry-standard pinout
MAX222	+5	2/2	4	4	0.1	Yes		Yes	200	+5V IBM PC serial port with receivers active in shutdown
MAX225	+5	5/5	10	0	–	Yes	✔	Yes	120	Available in 28-pin SO package
MAX232A	+5	2/2	4	4	0.1	No		Yes	200	High slew rate, small caps, guaranteed 120kbps data rate
MAX233A	+5	2/2	4	0	–	No		Yes	200	No external caps, high slew rate
MAX240	+5	5/5	7	4	1	Yes		Yes	120	DIP or flatpack package
MAX242	+5	2/2	4	4	0.1	Yes	✔	Yes	200	Separate shutdown and enable
MAX243	+5	2/2	4	4	0.1	No		Yes	200	Open-line detection simplifies cabling
MAX244	+5	8/10	11	4	1	No		Yes	120	High slew rate
MAX245	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, two shutdown modes
MAX246	+5	8/10	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, three shutdown modes
MAX247	+5	8/9	11	0	–	Yes	✔	Yes	120	High slew rate, int. caps, nine operating modes
MAX248	+5	8/8	11	4	1	Yes	✔	Yes	120	High slew rate, selective half-chip enables

MegaBaud is a trademark of Maxim Integrated Products.
AutoShutdown is a trademark of Maxim Integrated Products.
AutoShutdown Plus is a trademark of Maxim Integrated Products.

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Supply Current (mA)	No. of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & Three-State	Receivers Active in Shutdown	True RS-232	Data Rate (kbps)	Features
RS-232 ISOLATION PRODUCTS										
MAX250	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX251	+5	2/2	100µA	–	–	Yes		Yes	120	Isolated RS-232 chip set
MAX252A	+5	2/2	60	0	–	Yes		Yes	20	UL recognized, 1500V isolation
MAX252B	+5	2/2	60	0	–	Yes		Yes	20	Eccnomical 500V isolation

Part Number	Power Supply (V)	No. of RS-232 Tx/Rx	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	$\overline{\text{RESET}}$ Valid to V_{CC} = 1V	Supply Current (µA)	No. of Ext. Caps	Nominal Cap Value (µF)	Shutdown and Three-State	Receivers Active in Shutdown	AutoShutdown Plus	True RS-232	Data Rate (kbps)
RS-232 PRODUCTS WITH INTEGRATED µP SUPERVISORY FUNCTION													
MAX3320A	+3 to +5.5	2/2	4.25	100	✔	4	4	0.1	Yes	✔	✔	Yes	250
MAX3320B	+3 to +5.5	2/2	2.85	100	✔	4	4	0.1	Yes	✔	✔	Yes	250
MAX3320L	+3 to +5.5	2/2	4.63	100	✔	4	4	0.1	Yes	✔	✔	Yes	250
MAX3320T	+3 to +5.5	2/2	3.08	100	✔	4	4	0.1	Yes	✔	✔	Yes	250

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
+5V RS-485/RS-422 PRODUCTS							
MAX481	2.5	1/1	300	0.1	Half	32	MAX485 + 1µA shutdown mode
MAX483	0.25	1/1	120	0.1	Half	32	Slew-rate limiting reduces EMI and reflections
MAX485	2.5	1/1	300	–	Half	32	Direct LTC485 replacement
MAX487	0.25	1/1	120	0.1	Half	128	MAX483 plus 1/4-unit load
MAX488	0.25	1/1	120	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX489	0.25	1/1	120	–	Full	32	MAX488 plus driver/receiver enable
MAX490	2.5	1/1	300	–	Full	32	Direct LTC490 replacement
MAX491	2.5	1/1	300	–	Full	32	Direct LTC491 replacement
MAX1481	0.25	1/1	300	0.1	Full	256	10-pin µMAX package
MAX1482	0.25	1/1	20	0.1	Full	256	250kbps, 256 transceivers on bus
MAX1483	0.25	1/1	20	0.1	Half	256	250kbps, 256 transceivers on bus
MAX1484	12	1/1	300	0.1	Full	256	10-pin µMAX package
MAX1487	2.5	1/1	230	–	Half	128	2.5Mbps, 128 transceivers on bus
+3V (+3.0V to +3.6V) RS-485/RS-422 PRODUCTS							
MAX3483	0.25	1/1	1mA	2nA	Half	32	Slew-rate limiting reduces EMI and reflections
MAX3485	10	1/1	1mA	2nA	Half	32	Guaranteed 10Mbps data rate
MAX3486	2.5	1/1	1mA	2nA	Half	32	Guaranteed 2.5Mbps data rate
MAX3488	0.25	1/1	1mA	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX3490	10	1/1	1mA	–	Full	32	Guaranteed 10Mbps data rate
MAX3491	10	1/1	1mA	2nA	Full	32	MAX3490 plus driver/receiver enable

Part Number	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	ESD Voltage (kV)	Supply Current (µA)	Shutdown Supply Current (µA)	Duplex	No. of Rx/Tx On Bus	Features
HIGH-ESD RS-485 PRODUCTS								
MAX481E	2.5	1/1	±15	500	1	Half	32	MAX485 + 1µA shutdown mode
MAX483E	0.25	1/1	±15	350	1	Half	32	Slew-rate limiting reduces EMI and reflections
MAX485E	2.5	1/1	±15	500	300	Half	32	Direct LTC485 replacement
MAX487E	0.25	1/1	±15	250	1	Half	128	MAX483 plus 1/4-unit load
MAX488E	0.25	1/1	±15	350	–	Full	32	Slew-rate limiting reduces EMI and reflections
MAX489E	0.25	1/1	±15	350	1	Full	32	MAX488 plus driver/receiver enable
MAX490E	2.5	1/1	±15	500	–	Full	32	Direct LTC490 replacement
MAX491E	2.5	1/1	±15	500	300	Full	32	Direct LTC491 replacement
MAX1487E	2.5	1/1	±15	250	300	Half	128	2.5Mbps, 128 transceivers on bus

Part Number	Half/Full Duplex	Data Rate (Mbps)	Slew-Rate Limited	Low-Power Shutdown	Receiver/ Driver Enable	Quiescent Current (µA)	No. of Transceivers on Bus	Pin Count	Industry-Standard Pinout
TRUE FAIL-SAFE RS-485 PRODUCTS									
MAX3080	Full	0.115	Yes	Yes	Yes	375	256	14	75180
MAX3081	Full	0.115	Yes	No	No	375	256	8	75179
MAX3082	Half	0.115	Yes	Yes	Yes	375	256	8	75176
MAX3083	Full	0.5	Yes	Yes	Yes	375	256	14	75180
MAX3084	Full	0.5	Yes	No	No	375	256	8	75179
MAX3085	Half	0.5	Yes	Yes	Yes	375	256	8	75176
MAX3086	Full	10	No	Yes	Yes	375	256	14	75180
MAX3087	Full	10	No	No	No	375	256	8	75179
MAX3088	Half	10	No	Yes	Yes	375	256	8	75176
MAX3089	Selectable	Selectable	Selectable	Yes	Yes	375	256	14	75180*

Part Number	Data Rate (Mbps)	Slew-Rate Limited	Driver Enable	Receiver Enable	Quiescent Current (µA)	No. of Transceivers on Bus	Features
LOGIC SELECTABLE HALF-/FULL-DUPLEX PRODUCTS							
MAX1485	0.25	Yes	Yes	No	300	256	10-pin µMAX package
MAX1486	12	No	Yes	No	300	256	10-pin µMAX package
MAX3089	0.115/0.5/10	Selectable	Yes	Yes	375	256	True fail-safe operation

Part Number	Power Supply (V)	Data Rate (Mbps)	No. of RS-485 Drivers/ Receivers	Supply Current (mA)	Isolated Power (mW)	Isolation Voltage (V)	Shutdown Supply Current (µA)	Full Duplex	Features
RS-485 ISOLATION PRODUCTS									
MAX253	+5	–	–	5	750	–	1	–	Isolated power driver for RS-485
MAX1480A	+5	2.5	1/1	55	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX1480B	+5	0.25	1/1	28	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX1490A	+5	2.5	1/1	100	–	1500	0.2	Yes	Complete isolated RS-485 in one package
MAX1490B	+5	0.25	1/1	65	–	1500	0.2	Yes	Complete isolated RS-485 in one package
MAX3480A	+3.3	2.5	1/1	180	–	1500	0.2	No	Complete isolated RS-485 in one package
MAX3480B	+3.3	0.25	1/1	120	–	1500	0.2	No	Complete isolated RS-485 in one package

Part Number	Power Supply (V)	No. of Single-Ended Drivers/Receivers	No. of Differential Drivers/Receivers	Shutdown	Single-Ended Data Rate (kbps)	Differential Data Rate (Mbps)	Features
APPLETALK™ TRANSCEIVER							
MAX216	±5	1/2	1/1	Yes	120	1	Complete AppleTalk™ interface

Part Number	Power Supply (V)	Pins-Package	Supply Current (µA)	Low-Power Shutdown (µA)	Receive FIFO Width (words)	IrDA SIR Timing Compatible	Maximum Data Rate (kbps)	Features
SPI/MICROWIRE UARTs								
MAX3100	2.7 to 5.5	16-QSOP	150	10	8	✔	230	16-pin QSOP package, 9-bit address-recognition interrupt, receive-activity interrupt in shutdown, Schmitt-trigger inputs for optocouplers

AppleTalk is a trademark of Apple Computer, Inc.

Part Number	Power Supply (V)	No. of RS-232 Drivers/ Receivers	ESD Voltage (kV)	Ext. Caps (µF)	Shutdown & Three-State	Rx Active in Shutdown	Data Rate (kbps)	Features
HIGH-ESD RS-232 PRODUCTS								
MAX202E	+5	2/2	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX203E	+5	2/2	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX205E	+5	5/5	±15	None	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX206E	+5	4/3	±15	4 x 0.1	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX207E	+5	5/3	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX208E	+5	4/4	±15	4 x 0.1			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX211E	+5	4/5	±15	4 x 0.1	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX213E	+5	4/5	±15	4 x 0.1	Yes	✔	120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX232E	+5	2/2	±15	4 x 1.0			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX241E	+5	4/5	±15	4 x 1.0	Yes		120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX1406	+5, ±12	3/3	±15	None			230	Ideal for telecom, printers, modems
MAX1488E	+5, ±12	4/0	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX1489E	+5	0/4	±15	None			120	±15kV ESD per human body model and ±15kV per IEC 1000-4-2
MAX3185	+5, ±12	3/5	±15	None			230	Ideal for desktop PCs and motherboards
MAX3186	+5, ±12	5/3	±15	None			230	Ideal for modems
MAX3187	+5, ±12	6/10	±15	None			230	Dual RS-232 serial port, ideal for desktop PCs and motherboards
MAX3241E	+3 to +5.5	3/5	±15	4 x 0.1	Yes	✔	250	±15kV ESD protection, 3V to 5.5V serial port
MAX3243E	+3 to +5.5	3/5	±15	4 x 0.1	Yes	✔	250	1µA supply current using AutoShutdown™
MAX3244E	+3 to +5.5	3/5	±15	4 x 0.1	Yes	✔	250	1µA supply current using AutoShutdown Plus™
MAX3245E	+3 to +5.5	3/5	±15	4 x 0.1	Yes	✔	1Mbps	Megabaud™ (1Mbps) operation, 1µA supply current using Autoshutdown Plus™

19-1259; Rev 0; 7/97

MAXIM

SPI/Microwire-Compatible UART in QSOP-16

General Description

The MAX3100 universal asynchronous receiver transmitter (UART) is the first UART specifically optimized for small microcontroller-based systems. Using an SPI™/Microwire™ interface for communication with the host microcontroller (µC), the MAX3100 comes in a compact 16-pin QSOP. The asynchronous I/O is suitable for use in RS-232, RS-485, IR, and opto-isolated data links. IR-link communication is easy with the MAX3100's infrared data association (IrDA) timing mode.

The MAX3100 includes a crystal oscillator and a baud-rate generator with software-programmable divider ratios for all common baud rates from 300 baud to 230k baud. A software- or hardware-invoked shutdown lowers quiescent current to 10µA, while allowing the MAX3100 to detect receiver activity.

An 8-word-deep first-in/first-out (FIFO) buffer minimizes processor overhead. This device also includes a flexible interrupt with four maskable sources, including address recognition on 9-bit networks. Two hardware-handshaking control lines are included (one input and one output).

The MAX3100 is available in 14-pin plastic DIP and small, 16-pin QSOP packages in the commercial and extended temperature ranges.

Applications

Hand-Held Instruments

Intelligent Instrumentation

UART in SPI Systems

Small Networks in HVAC or Building Control

Isolated RS-232/RS-485: Directly Drives Opto-Couplers

Low-Cost IR Data Links for Computers/Peripherals

Features

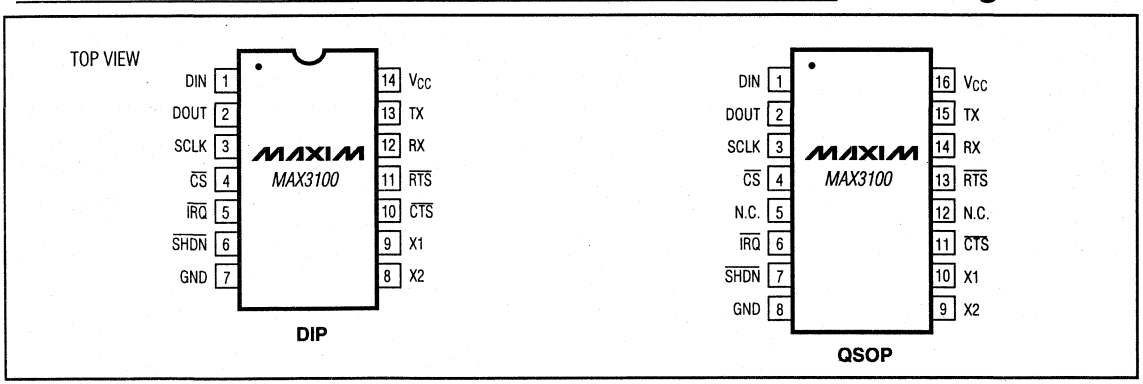
- **16-Pin QSOP Package (8-pin SO footprint): Smallest UART Available**
- **Full-Featured UART:**
  - **—IrDA SIR Timing Compatible**
  - **—8-Word FIFO Minimizes Processor Overhead at High Data Rates**
  - **—Up to 230k Baud with a 3.6864MHz Crystal**
  - **—9-Bit Address-Recognition Interrupt**
  - **—Receive Activity Interrupt in Shutdown**
- **SPI/Microwire-Compatible µC Interface**
- **Lowest Power:**
  - **—150µA Operating Current at 3.3V**
  - **—10µA in Shutdown with Receive Interrupt**
- **+2.7V to +5.5V Supply Voltage in Operating Mode**
- **Schmitt-Trigger Inputs for Opto-Couplers**
- **TX and $\overline{RTS}$ Outputs Sink 25mA for Opto-Couplers**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3100CPD	0°C to +70°C	14 Plastic DIP
MAX3100CEE	0°C to +70°C	16 QSOP
MAX3100EPD	-40°C to +85°C	14 Plastic DIP
MAX3100EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit appears at end of data sheet.

Pin Configurations



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For small orders, phone 408-737-7600 ext. 3468.

SPI/Microwire-Compatible UART in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....+6V
Input Voltage to GND
($\overline{CS}$, $\overline{SHDN}$, X1, $\overline{CTS}$, RX, DIN, SCLK) ....-0.3V to (V_{CC} + 0.3V)
Output Voltage to GND
(DOUT, $\overline{RTS}$, TX, X2) .....-0.3V to (V_{CC} + 0.3V)
$\overline{IRQ}$.....-0.3V to 6V
TX, $\overline{RTS}$ Output Current 100mA
X2, DOUT, $\overline{IRQ}$ Short-Circuit Duration
(to V_{CC} or GND) .....Indefinite

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.00mW/°C above +70°C) 800mW
QSOP (derate 8.30mW/°C above +70°C).....667mW
Operating Temperature Ranges
MAX3100C_ _ .....0°C to +70°C
MAX3100E_ _ .....-40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are measured at 9600 baud at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$, $\overline{CTS}$, RX)							
Input High Voltage	V_{IH}			0.7 x V_{CC}			V
Input Low Voltage	V_{IL}					0.3 x V_{CC}	V
Input Hysteresis	V_{HYST}	V_{CC} = 3.3V			0.05 x V_{CC}		V
Input Leakage	I_{IL}					±1	µA
Input Capacitance	C_{IN}				5		pF
OSCILLATOR INPUT (X1)							
Input High Voltage	V_{IH}			0.7 x V_{CC}	V_{CC} / 2		V
Input Low Voltage	V_{IL}				V_{CC} / 2	0.2 x V_{CC}	V
Input Current	I_{IN}	V_{X1} = 0V and 5.5V	Active mode			25	µA
			Shutdown mode			2	
Input Capacitance	C_{IN}	V_{X1} = 0V and 5.5V			5		pF
OUTPUTS (DOUT, TX, $\overline{RTS}$)							
Output High Voltage	V_{OH}	I_{SOURCE} = 5mA		V_{CC} - 0.5			V
		I_{SOURCE} = 25µA, TX only		V_{CC} - 0.5			
Output Low Voltage	V_{OL}	TX, $\overline{RTS}$: I_{SINK} = 25mA				0.9	V
		DOUT, TX, $\overline{RTS}$: I_{SINK} = 4mA				0.4	
Output Leakage	I_{LK}	DOUT only, $\overline{CS}$ = V_{CC}				±1	µA
Output Capacitance	C_{OUT}				5		pF
$\overline{IRQ}$ OUTPUT (Open Drain)							
Output Low Voltage	V_{OL}	I_{SINK} = 4mA				0.4	V
Output Leakage	I_{LK}	$V_{\overline{IRQ}}$ = 5.5V				±1	µA
Output Capacitance	C_{OUT}				5		pF
POWER REQUIREMENTS							
V_{CC} Supply Current in Normal Mode	I_{CC}	With 1.8432MHz crystal; all other logic inputs are at 0V or V_{CC}	V_{CC} = 5V		0.27	1	mA
			V_{CC} = 3.3V		0.15	0.4	
V_{CC} Supply Current in Shutdown	I_{CC}	SHDN bit = 1 or $\overline{SHDN}$ = 0, logic inputs are at 0V or V_{CC}				10	µA
Supply Voltage	V_{CC}			2.7		5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AC TIMING (Figure 1)						
$\overline{CS}$ Low to DOUT Valid	t_{DV}	C_{LOAD} = 100pF			100	ns
$\overline{CS}$ High to DOUT Tri-State	t_{TR}	C_{LOAD} = 100pF, $R\overline{CS}$ = 10kΩ			100	ns
$\overline{CS}$ to SCLK Setup Time	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Hold Time	t_{CSH}		0			ns
SCLK Fall to DOUT Valid	t_{DO}	C_{LOAD} = 100pF			100	ns
DIN to SCLK Setup Time	t_{DS}		100			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Period	t_{CP}		238			ns
SCLK High Time	t_{CH}		100			ns
SCLK Low Time	t_{CL}		100			ns
SCLK Rising Edge to $\overline{CS}$ Falling	t_{CS0}	(Note 1)	100			ns
$\overline{CS}$ Rising Edge to SCLK Rising	t_{CS1}	(Note 1)	200			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		200			ns
Output Rise Time	t_r	TX, $\overline{RTS}$, DOUT: C_{LOAD} = 100pF		10		ns
Output Fall Time	t_f	TX, $\overline{RTS}$, DOUT, $\overline{IRQ}$: C_{LOAD} = 100pF		10		ns

Note 1: t_{CS0} and t_{CS1} specify the minimum separation between SCLK rising edges used to write to other devices on the SPI bus and the $\overline{CS}$ used to select the MAX3100. A separation greater than t_{CS0} and t_{CS1} ensures that the SCLK edge is ignored.

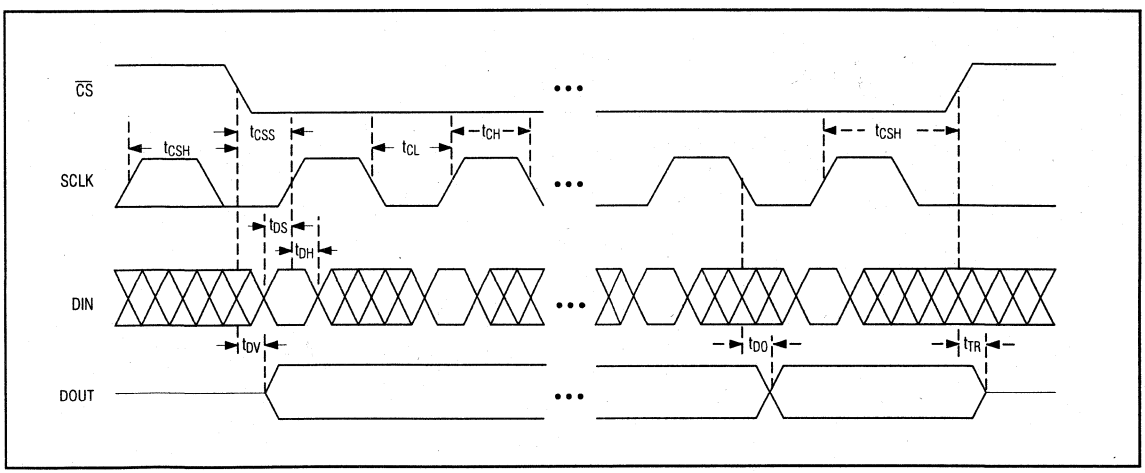


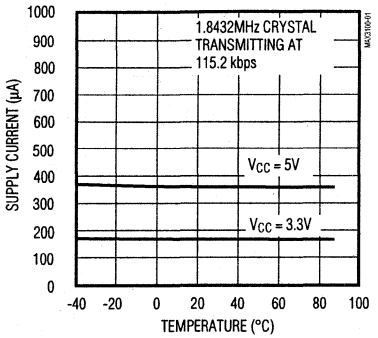
Figure 1. Detailed Serial-Interface Timing

SPI/Microwire-Compatible UART in QSOP-16

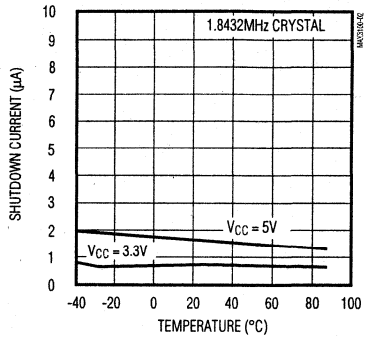
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

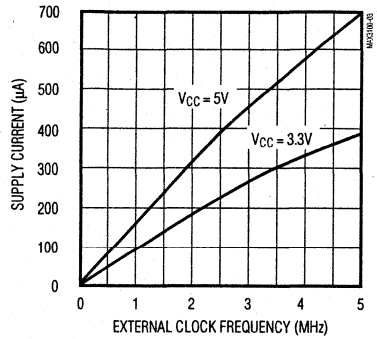
SUPPLY CURRENT vs. TEMPERATURE



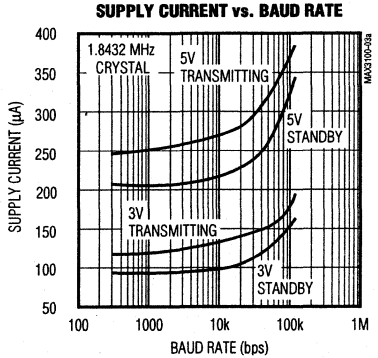
SHUTDOWN CURRENT vs. TEMPERATURE



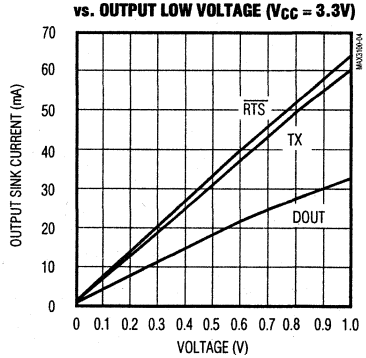
SUPPLY CURRENT vs. EXTERNAL CLOCK FREQUENCY



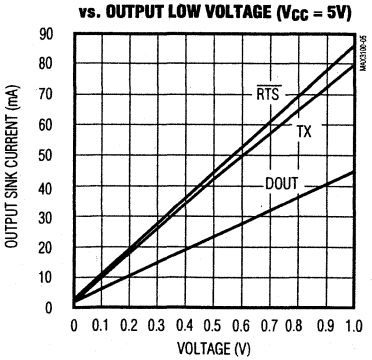
SUPPLY CURRENT vs. BAUD RATE



TX, $\overline{RTS}$, DOUT OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE (V_{CC} = 3.3V)



TX, $\overline{RTS}$, DOUT OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE (V_{CC} = 5V)



Pin Description

PIN		NAME	FUNCTION
QSOP	DIP		
1	1	DIN	SPI/Microwire Serial-Data Input. Schmitt-trigger input.
2	2	DOUT	SPI/Microwire Serial-Data Output. High impedance when $\overline{CS}$ is high.
3	3	SCLK	SPI/Microwire Serial-Clock Input. Schmitt-trigger input.
4	4	$\overline{CS}$	Active-Low Chip-Select Input. DOUT goes high impedance when $\overline{CS}$ is high. $\overline{IRQ}$, TX, and $\overline{RTS}$ are always active. Schmitt-trigger input.
6	5	$\overline{IRQ}$	Active-Low Interrupt Output. Open-drain interrupt output to microprocessor.
7	6	$\overline{SHDN}$	Hardware-Shutdown Input. When shut down ($\overline{SHDN}$ = 0), the oscillator turns off immediately without waiting for the current transmission to end, reducing supply current to just leakage currents.
8	7	GND	Ground
9	8	X2	Crystal Connection. Leave X2 unconnected for external clock. See *Crystal-Oscillator Operation—X1, X2 Connection* section.
10	9	X1	Crystal Connection. X1 also serves as an external clock input. See *Crystal-Oscillator Operation—X1, X2 Connection* section.
11	10	$\overline{CTS}$	General-Purpose Active-Low Input. Read via the $\overline{CTS}$ register bit; often used for RS-232 clear-to-send input (Table 1).
13	11	$\overline{RTS}$	General-Purpose Active-Low Output. Controlled by the $\overline{RTS}$ register bit. Often used for RS-232 request-to-send output or RS-485 driver enable.
14	12	RX	Asynchronous Serial-Data (receiver) Input. The serial information received from the modem or RS-232/RS-485 receiver. A transition on RX while in shutdown generates an interrupt (Table 5).
15	13	TX	Asynchronous Serial-Data (transmitter) Output
16	14	V_{CC}	Positive Supply Pin (2.7V to 5.5V)
5, 12	—	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX3100 universal asynchronous receiver transmitter (UART) interfaces the SPI/Microwire-compatible, synchronous serial data from a microprocessor (µP) to asynchronous, serial-data communication ports (RS-232, RS-485, IrDA). Figure 2 shows the MAX3100 functional diagram.

The MAX3100 combines a simple UART and a baud-rate generator with an SPI interface and an interrupt generator. Configure the UART by writing a 16-bit word to a write-configuration register, which contains the baud rate, data-word length, parity enable, and enable of the 8-word receive first-in/first-out (FIFO). The write configuration selects between normal UART timing and IrDA timing, controls shutdown, and contains 4 interrupt mask bits.

Transmit data by writing a 16-bit word to a write-data register, where the last 7 or 8 bits are actual data to be transmitted. Also included is the state of the transmitted parity bit (if enabled). This register controls the state of the $\overline{RTS}$ output pin. Received words generate an interrupt if the receive-bit interrupt is enabled.

Read data from a 16-bit register that holds the oldest data from the receive FIFO, the received parity data, and the logic level at the $\overline{CTS}$ input pin. This register also contains a bit that is the framing error in normal operation and a receive-activity indicator in shutdown.

The baud-rate generator determines the rate at which the transmitter and receiver operate. Bits B0 to B3 in the write-configuration register determine the baud-rate divisor (BRD), which divides down the X1 oscillator frequency. The baud clock is 16 times the data rate (baud rate).

The transmitter section accepts SPI/Microwire data, formats it, and transmits it in asynchronous serial format from the TX output. Data is loaded into the transmit-buffer register from the SPI/Microwire interface. The MAX3100 adds start and stop bits to the data and clocks the data out at the selected baud rate (Table 7).

SPI/Microwire-Compatible UART in QSOP-16

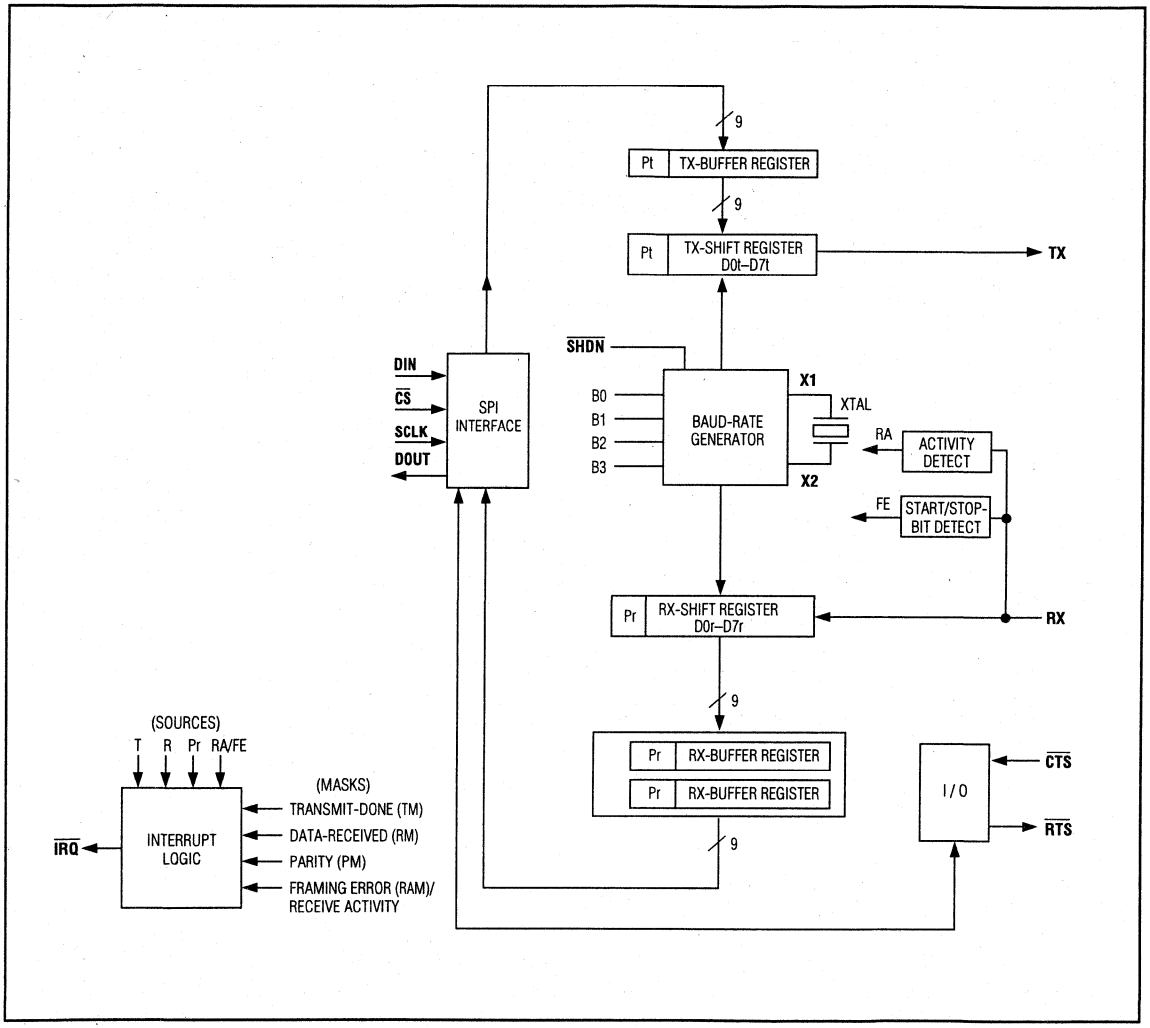


Figure 2. Functional Diagram

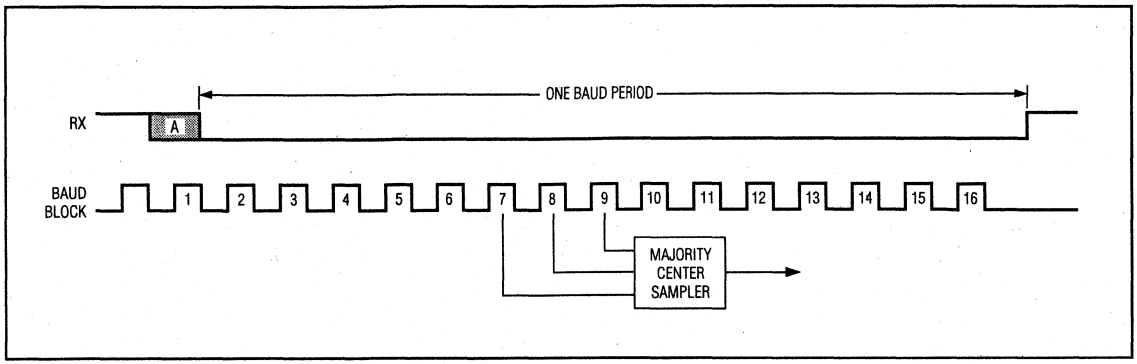


Figure 3. Start-Bit Timing

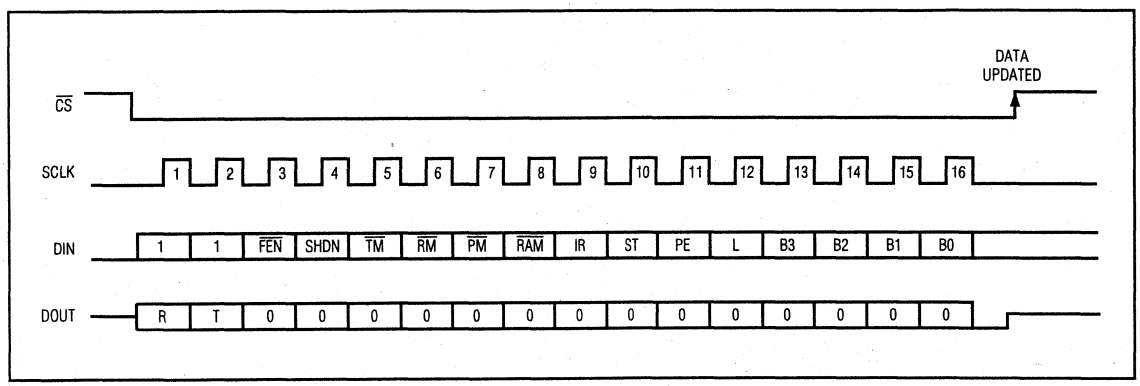


Figure 4. SPI Interface (Write Configuration)

The receiver section receives data in serial form. The MAX3100 detects a start bit on a high-to-low RX transition (Figure 3). An internal clock samples data at 16 times the data rate. The start bit can occur as much as one clock cycle before it is detected, as indicated by the shaded portion. The state of the start bit is defined as the majority of the 7th, 8th, and 9th sample of the internal 16x baud clock. Subsequent bits are also majority sampled. Receive data is stored in an 8-word FIFO. The FIFO is cleared if it overflows.

The on-board oscillator can use a 1.8432MHz or 3.6864MHz crystal, or it can be driven at X1 with a 45% to 55% duty-cycle square wave.

SPI Interface

The bit streams for DIN and DOUT consist of 16 bits, with bits assigned as shown in the *MAX3100 Operations* section. DOUT transitions on SCLK's falling edge, and DIN is latched on SCLK's rising edge (Figure 4). Most operations, such as the clearing of internal registers, are executed only on $\overline{CS}$'s rising edge. The DIN stream is monitored for its first two bits to tell the UART the type of data transfer being executed (Write Config, Read Config, Write Data, Read Data).

Only 16-bit words are expected. If $\overline{CS}$ goes high in the middle of a transmission (any time before the 16th bit), the sequence is aborted (i.e., data does not get written to individual registers). Every time $\overline{CS}$ goes low, a new 16-bit stream is expected. An example of a write configuration is shown in Figure 4.

SPI/Microwire-Compatible UART in QSOP-16

MAX3100 Operations

Write Operations

Table 1 shows write-configuration data. A 16-bit SPI/Microwire write configuration clears the receive FIFO and the R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, and Pt registers. $\overline{RTS}$ and $\overline{CTS}$ remain unchanged. The new configuration is valid on $\overline{CS}$'s rising edge if the transmit buffer is empty (T = 1) and transmission is over. If the latest transmission has not been completed, the registers are updated when the transmission is over (T = 0).

The write-configuration bits ($\overline{FEN}$, SHDNi, IR, ST, PE, L, B3–B0) take effect after the current transmission is over. The mask bits ($\overline{TM}$, $\overline{RM}$, $\overline{PM}$, $\overline{RAM}$) take effect immediately after the 16th clock's rising edge at SCLK.

Read Operations

Table 2 shows read-configuration data. This register reads back the last configuration written to the MAX3100. The device enters test mode if bit 0 = 1. In this mode, if $\overline{CS}$ = 0, the $\overline{RTS}$ pin acts as the 16x clock generator's output. This may be useful for direct baud-rate generation (in this mode, TX and RX are in digital loopback).

Normally, the write-data register loads the TX-buffer register. To change the $\overline{RTS}$ pin's state without writing data, set the $\overline{TE}$ bit. Setting the $\overline{TE}$ bit high inhibits the write command (Table 3).

Reading data clears the R bit and interrupt $\overline{IRQ}$ (Table 4).

Register Functions

Table 5 shows read/write operation and power-on reset state (POR), and describes each bit used in programming the MAX3100. Figure 5 shows parity and word-length control.

Table 1. Write Configuration (D15, D14 = 1, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	1	$\overline{FEN}$	SHDNi	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0
DOUT	R	T	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2. Read Configuration (D15, D14 = 0, 1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST
DOUT	R	T	$\overline{FEN}$	SHDNo	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR	ST	PE	L	B3	B2	B1	B0

Table 3. Write Data (D15, D14 = 1, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	1	0	0	0	0	$\overline{TE}$	RTS	Pt	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

Table 4. Read Data (D15, D14 = 0, 0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DOUT	R	T	0	0	0	RA/FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

Table 5. Bit Descriptions

BIT NAME	READ/ WRITE	POR STATE	DESCRIPTION
B0–B3	w	0000	Baud-Rate Divisor Select Bits. Sets the baud clock's value (Table 6).
B0–B3	r	0000	Baud-Rate Divisor Select Bits. Reads the 4-bit baud clock value assigned to these registers.
CTS	r	No change	Clear-to-Send-Input. Records the state of the $\overline{CTS}$ pin (CTS bit = 0 implies $\overline{CTS}$ pin = logic high).
D0t–D7t	w	X	Transmit-Buffer Register. Eight data bits written into the transmit-buffer register. D7t is ignored when L = 1.
D0r–D7r	r	00000000	Eight data bits read from the receive FIFO or the receive register. These will be all 0s when the receive FIFO or the receive registers are empty. When L = 1, D7r is always 0.
$\overline{FEN}$	w	0	FIFO Enable. Enables the receive FIFO when $\overline{FEN}$ = 0. When $\overline{FEN}$ = 1, FIFO is disabled.
$\overline{FEN}$	r	0	FIFO-Enable Readback. $\overline{FEN}$'s state is read.
IR	w	0	Enables the IrDA timing mode when IR = 1.
IR	r	0	Reads the value of the IR bit.
L	w	0	Bit for setting the word length of the transmitted or received data. L = 0 results in 8-bit words (9-bit words if PE = 1), see Figure 5. L = 1 results in 7-bit words (8-bit words if PE = 1).
L	r	0	Reads the value of the L bit.
Pt	w	X	Transmit-Parity Bit. This bit is treated as an extra bit that will be transmitted if PE = 1. To be useful in 9-bit networks, the MAX3100 does not calculate parity. If PE = 0, then this bit (Pt) is ignored in transmit mode (see the *Nine-Bit Networks* section).
Pr	r	X	Receive-Parity Bit. This bit is the extra bit received if PE = 1. Therefore, PE = 1 results in 9-bit transmissions (L = 0). If PE = 0, then Pr is set to 0. Pr is stored in the FIFO with the receive data (see the *Nine-Bit Networks* section).
PE	w	0	Parity-Enable Bit. Appends the Pt bit to the transmitted data when PE = 1, and sends the Pt bit as written. No parity bit is transmitted when PE = 0. With PE = 1, an extra bit is expected to be received. This data is put into the Pr register. Pr = 0 when PE = 0. The MAX3100 does not calculate parity.
PE	r	0	Reads the value of the Parity-Enable bit.
$\overline{PM}$	w	0	Mask for Pr bit. $\overline{IRQ}$ is asserted if $\overline{PM}$ = 1 and Pr = 1 (Table 6).
$\overline{PM}$	r	0	Reads the value of the $\overline{PM}$ bit (Table 6).
R	r	0	Receive Bit or FIFO Not Empty Flag. R = 1 means new data is available to be read from the receive register or FIFO.
$\overline{RM}$	w	0	Mask for R bit. $\overline{IRQ}$ is asserted if $\overline{RM}$ = 1 and R = 1 (Table 6).
$\overline{RM}$	r	0	Reads the value of the $\overline{RM}$ bit (Table 6).
$\overline{RAM}$	w	0	Mask for RA/FE bit. $\overline{IRQ}$ is asserted if $\overline{RAM}$ = 1 and RA/FE = 1 (Table 6).
$\overline{RAM}$	r	0	Reads the value of the $\overline{RAM}$ bit (Table 6).
RTS	w	0	Request-to-Send Bit. Controls the state of the $\overline{RTS}$ output. This bit is reset on power-up (RTS bit = 0 sets the $\overline{RTS}$ pin = logic high).

Table 5. Bit Descriptions (continued)

BIT NAME	READ/ WRITE	POR STATE	DESCRIPTION
RA/FE	r	0	Receiver-Activity/Framing-Error Bit. In shutdown mode, this is the RA bit. In normal operation, this is the FE bit. In shutdown mode, a transition on RX sets RA = 1. In normal mode, a framing error sets FE = 1. A framing error occurs if a zero is received when the first stop bit is expected. FE is set when a framing error occurs, and cleared upon receipt of the next properly framed character independent of the FIFO being enabled. When the device wakes up, it is likely that a framing error will occur. This error can be cleared with a write configuration. The FE bit is not cleared on a Read Data operation. When an FE is encountered, the UART resets itself to the state where it is looking for a start bit.
SHDNi	w	0	Software-Shutdown Bit. Enter software shutdown with a write configuration where SHDNi = 1. Software shutdown takes effect after $\overline{CS}$ goes high, and causes the oscillator to stop as soon as the transmitter becomes idle. Software shutdown also clears R, T, RA/FE, D0r–D7r, D0t–D7t, Pr, Pt, and all data in the receive FIFO. RTS and CTS can be read and updated while in shutdown. Exit software shutdown with a write configuration where SHDNi = 0. The oscillator restarts typically within 50ms of $\overline{CS}$ going high. RTS and CTS are unaffected. Refer to the *Pin Description* for hardware shutdown ($\overline{SHDN}$ input).
SHDNo	r	0	Shutdown Read-Back Bit. The read-configuration register outputs SHDNo = 1 when the UART is in shutdown. Note that this bit is not sent until the current byte in the transmitter is sent (T = 1). This tells the processor when it may shut down the RS-232 driver. This bit is also set immediately when the device is shut down through the $\overline{SHDN}$ pin.
ST	w	0	Transmit-Stop Bit. One stop bit will be transmitted when ST = 0. Two stop bits will be transmitted when ST = 1. The receiver only requires one stop bit.
ST	r	0	Reads the value of the ST bit.
T	r	1	Transmit-Buffer-Empty Flag. T = 1 means that the transmit buffer is empty and ready to accept another data word.
$\overline{TE}$	w	0	Transmit-Enable Bit. If $\overline{TE}$ = 1, then only the $\overline{RTS}$ pin will be updated on $\overline{CS}$'s rising edge. The contents of $\overline{RTS}$, Pt, and D0t–D7t transmit on $\overline{CS}$'s rising edge when $\overline{TE}$ = 0.
$\overline{TM}$	w	0	Mask for T bit. $\overline{IRQ}$ is asserted if $\overline{TM}$ = 1 and T = 1 (Table 6).
$\overline{TM}$	r	0	Reads the value of the $\overline{TM}$ bit (Table 6).

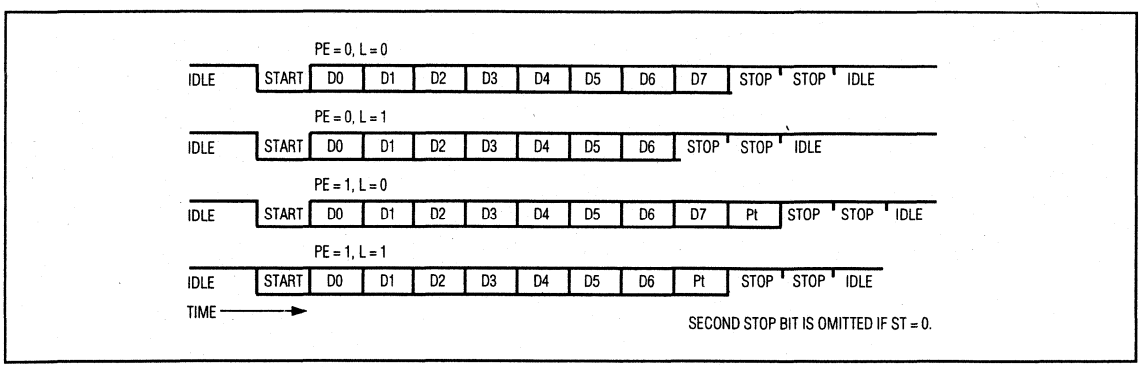


Figure 5. Parity and Word-Length Control

Interrupt Sources and Masks

A Read Data operation clears the interrupt $\overline{IRQ}$. Table 6 gives the details for each interrupt source. Figure 6 shows the functional diagram for the interrupt sources and mask blocks.

Table 6. Interrupt Sources and Masks—Bit Descriptions

BIT NAME	MASK BIT	MEANING WHEN SET	DESCRIPTION
Pr	$\overline{PM}$	Received parity bit = 1	The Pr bit reflects the value in the word currently in the receive-buffer register (oldest data available). The Pr bit is set when parity is enabled (PE = 1) and the received parity bit is 1. The Pr bit is cleared either when parity is not enabled (PE = 0), or when parity is enabled and the received bit is 0. An interrupt is issued based on the oldest Pr value in the receiver FIFO. The oldest Pr value is the next value that will be read by a Read Data operation.
R	$\overline{RM}$	Data available	The R bit is set when new data is available to be read from the receive register/ FIFO. FIFO is cleared when all data has been read. An interrupt is asserted as long as R = 1 and $\overline{RM}$ = 1.
RA/FE	$\overline{RAM}$	Transition on RX when in shutdown; framing error when not in shutdown	This is the RA (RX-transition) bit in shutdown, and the FE (framing-error) bit in operating mode. RA is set if there has been a transition on RX since entering shutdown. RA is cleared when the MAX3100 exits shutdown. $\overline{IRQ}$ is asserted when RA is set and $\overline{RAM}$ = 1. FE is determined solely by the currently received data, and is not stored in FIFO. The FE bit is set if a zero is received when the first stop bit is expected. FE is cleared upon receipt of the next properly framed character. $\overline{IRQ}$ is asserted when FE is set and RAM = 1.
T	$\overline{TM}$	Transmit buffer is empty	The T bit is set when the transmit buffer is ready to accept data. $\overline{IRQ}$ is asserted low if $\overline{TM}$ = 1 and the transmit buffer becomes empty. This source is cleared on $\overline{CS}$'s rising edge during a Read Data operation. Although the interrupt is cleared, T may be polled to determine transmit-buffer status.

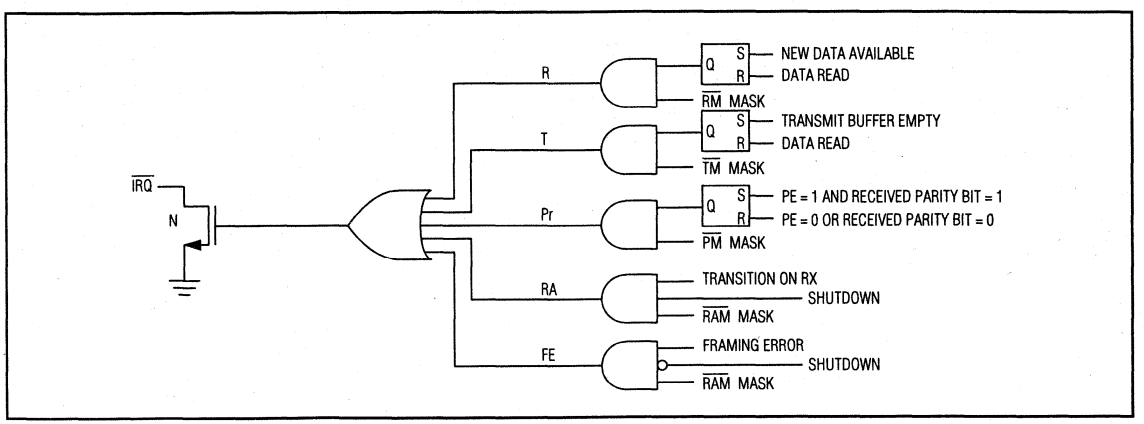


Figure 6. Interrupt Sources and Masks Functional Diagram

SPI/Microwire-Compatible UART in QSOP-16

Table 7. Baud-Rate Selection Table*

B3	B2	B1	B0	DIVISION RATIO	BAUD RATE (fosc = 1.8432MHz)	BAUD RATE (fosc = 3.6864MHz)
0	0	0	0**	1	**115.2k****	**230.4k****
0	0	0	1	2	**57.6k**	**115.2k**
0	0	1	0	4	28.8k	**57.6k**
0	0	1	1	8	14.4k	28.8k
0	1	0	0	16	7200	14.4k
0	1	0	1	32	3600	7200
0	1	1	0	64	1800	3600
0	1	1	1	128	900	1800
1	0	0	0	3	**38.4k**	76.8k
1	0	0	1	6	**19.2k**	**38.4k**
1	0	1	0	12	**9600**	**19.2k**
1	0	1	1	24	**4800**	**9600**
1	1	0	0	48	**2400**	**4800**
1	1	0	1	96	**1200**	**2400**
1	1	1	0	192	**600**	**1200**
1	1	1	1	384	**300**	**600**

**Standard baud rates shown in bold*
***Default baud rate*

Clock-Oscillator Baud Rates

Bits B0–B3 of the write-configuration register determine the baud rate. Table 7 shows baud-rate divisors for given input codes, as well as the given baud rate for 1.8432MHz and 3.6864MHz crystals. Note that the baud rate = crystal frequency / 16x division ratio.

Shutdown Mode

In shutdown, the oscillator turns off to reduce power dissipation (I_{CC} < 10µA). The MAX3100 enters shutdown in one of two ways: by a software command (SHDNi bit = 1) or by a hardware command ($\overline{SHDN}$ = logic low). The hardware shutdown is effective immediately and will immediately terminate any transmission in progress. The software shutdown, requested by setting SHDNi bit = 1, is entered upon completing the transmission of the data in both the transmit register and the transmit-buffer register. The SHDNo bit is set when the MAX3100 enters shutdown (either hardware or software). The microcontroller (µC) can monitor the SHDNo bit to determine when all data has been transmitted, and shut down any external circuitry (such as RS-232 transceivers) at that time.

Shutdown clears the receive FIFO, R, A, RA/FE, D0r–D7r, Pr, and Pt registers and sets the T bit high. Configuration bits ($\overline{RM}$, $\overline{TM}$, $\overline{PM}$, $\overline{RAM}$, IR, ST, PE, L, B0-3, and $\overline{RTS}$) can be modified when SHDNo = 1 and $\overline{CTS}$ can also be read. Even though RA is reset upon entering shutdown, it will go high when any transitions are detected on the RX pin. This allows the UART to monitor activity on the receiver when in shutdown.

The command to power up (SHDNi = 0) turns on the oscillator when $\overline{CS}$ goes high if $\overline{SHDN}$ pin = logic high, with a start-up time of about 25ms. This is done through a write configuration, which clears all registers but $\overline{RTS}$ and $\overline{CTS}$. Since the crystal oscillator typically requires 25ms to start, the first received characters will be garbled, and a framing error may occur.

Applications Information

Driving Opto-Couplers

Figure 7 shows the MAX3100 in an isolated serial interface. The MAX3100 Schmitt-trigger inputs are driven directly by opto-coupler outputs. Isolated power is provided by the MAX845 transformer driver and linear regulator shown. A significant feature of this application is that the opto-coupler's skew does not affect the asynchronous serial output's timing. Only the set-up and hold times of the SPI interface need to be met.

Figure 8 shows a bidirectional opto-isolated interface using only two opto-isolators. Over 81% power savings is realized using IrDA mode due to its 3/16-wide baud periods.

Crystal-Oscillator Operation—X1, X2 Connection

The MAX3100 includes a crystal oscillator for baud-rate generation. For standard baud rates, use a 1.8432MHz or 3.6864MHz crystal. The 1.8432MHz crystal results in lower operating current; however, the 3.6864MHz crystal may be more readily available in surface mount.

Ceramic resonators are low-cost alternatives to crystals and operate similarly, though the "Q" and accuracy are lower. Some ceramic resonators are available with integral load capacitors, which can further reduce cost. The tradeoff between crystals and ceramic resonators is in initial frequency accuracy and temperature drift. The total error in the baud-rate generator should be kept below 1% for reliable operation with other systems. This is accomplished easily with a crystal, and in most cases can be achieved with ceramic resonators. Table 8 lists the different types of crystals and resonators and their suppliers.

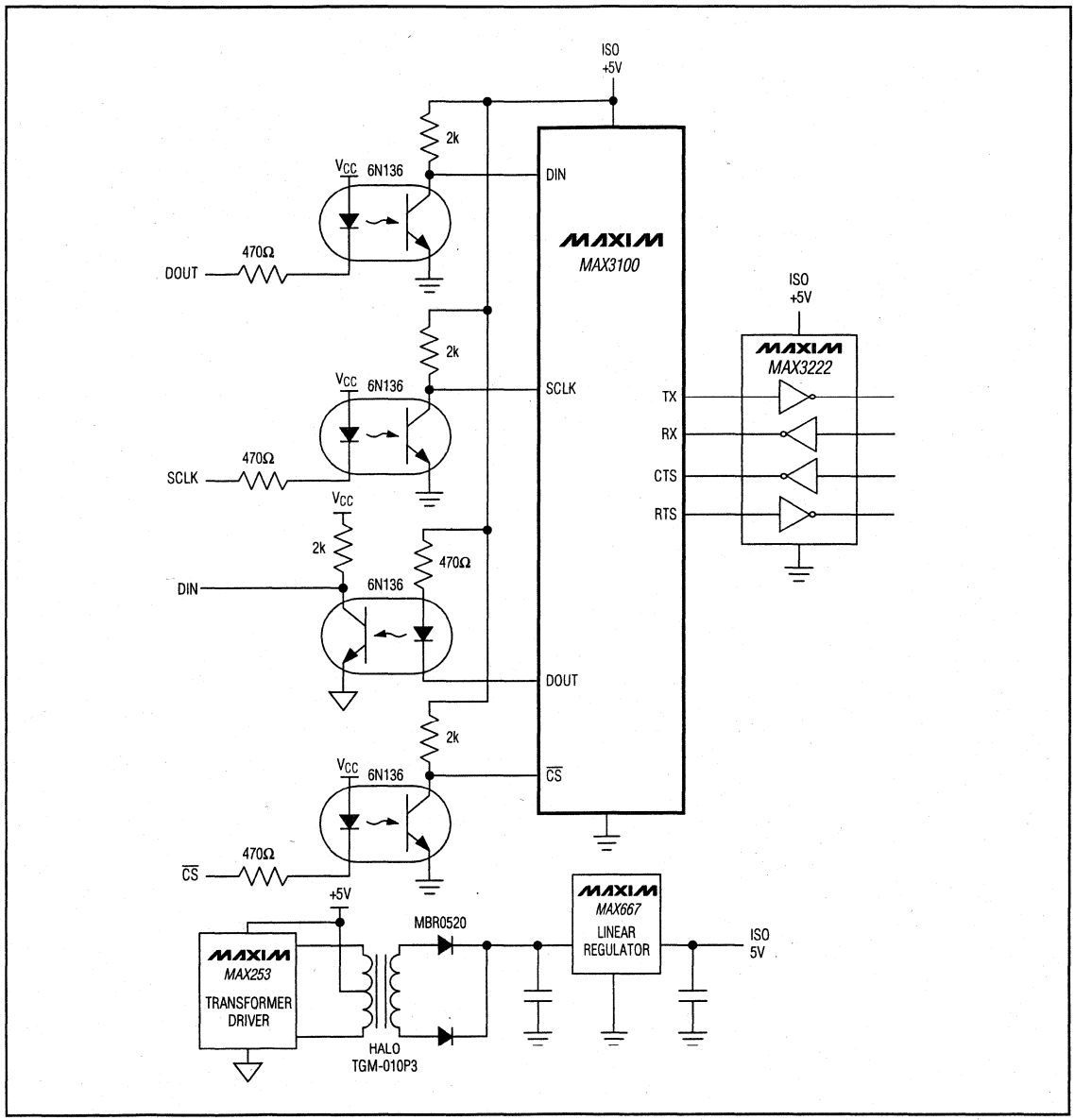


Figure 7. Driving Optocouplers

SPI/Microwire-Compatible UART in QSOP-16

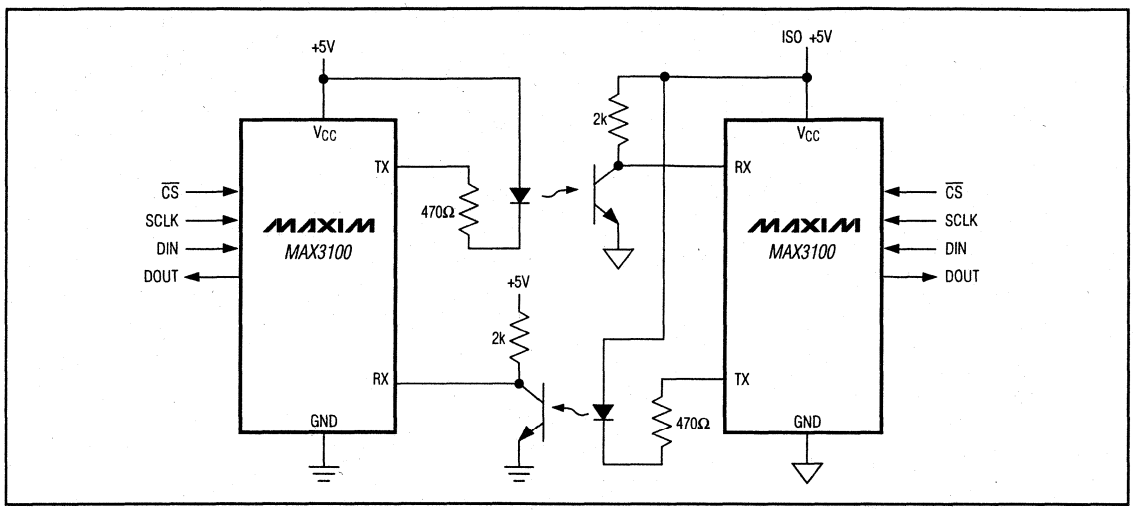


Figure 8. Bidirectional Opto-Isolated Interface

Table 8. Component and Supplier List

DESCRIPTION	FREQUENCY (MHz)	TYPICAL C1, C2 (pF)	SUPPLIER	PART NUMBER	PHONE NUMBER
Through-Hole Crystal (HC-49/U)	1.8432	25	ECS International, Inc.	ECS-18-13-1	(913) 782-7787
Through-Hole Resonator	1.8432	47	Murata North America	CSA1.84MG	(800) 831-9172
Through-Hole Crystal (HC-49/US)	3.6864	33	ECS International, Inc.	ECS-36-18-4	(913) 782-7787
SMT Crystal	3.6864	39	ECS International, Inc.	ECS-36-20-5P	(913) 782-7787
SMT Resonator	3.6864	None (integral)	AVX/Kyocera	PBRC-3.68B	(803) 448-9411

This oscillator supports parallel-resonant mode crystals and ceramic resonators, or can be driven from an external clock source. Internally, the oscillator consists of an inverting amplifier with its input, X1, tied to its output, X2, by a bias network that self-biases the inverter at approximately V_{CC} / 2. The external feedback circuit, usually a crystal, from X2 to X1 provides 180° of phase shift, causing the circuit to oscillate. As shown in the standard application circuit, the crystal or resonator is connected between X1 and X2, with the load capacitance for the crystal being the series combination of C1 and C2. For example, a 1.8432MHz crystal with a specified load capacitance of 11pF would use capacitors of 22pF on either side of the crystal to ground. Series-resonant mode crystals have a slight frequency error, typically oscillating 0.03% higher than specified series-resonant frequency, when operated in parallel mode.

It is **very important** to keep crystal, resonator, and load-capacitor leads and traces as short and direct as possible. The X1 and X2 trace lengths and ground tracks should be tight, with no other intervening traces. This helps minimize parasitic capacitance and noise pickup in the oscillator, and reduces EMI. Minimize capacitive loading on X2 to minimize supply current.

The MAX3100 X1 input can be driven directly by an external CMOS clock source. The trip level is approximately equal to V_{CC} / 2. No connection should be made to X2 in this mode. If a TTL or non-CMOS clock source is used, AC couple with a 10nF capacitor to X1. The peak-to-peak swing on the input should be at least 2V for reliable operation.

9-Bit Networks

The MAX3100 supports a common multidrop communication technique referred to as 9-bit mode. In this mode, the parity bit is set to indicate a message that contains a header with a destination address. The MAX3100 parity mask can be set to generate interrupts for this condition. Operating a network in this mode reduces the processing overhead of all nodes by enabling the slave controllers to ignore most message traffic. This can relieve the remote processor to handle more useful tasks.

In 9-bit mode, the MAX3100 is set up with 8 bits plus parity. The parity bit in all normal messages is clear, but is set in an address-type message. The MAX3100 parity-interrupt mask is enabled to generate an interrupt on high parity. When the master sends an address message with the parity bit set, all MAX3100 nodes issue an interrupt. All nodes then retrieve the received byte to compare to their assigned address. Once addressed, the node continues to process each received byte. If the node was not addressed, it ignores all message traffic until a new address is sent out by the master.

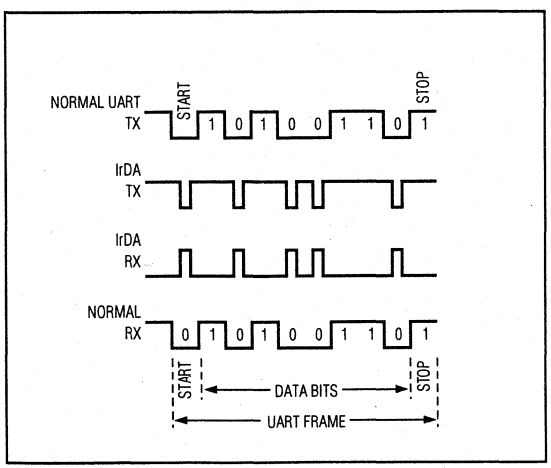


Figure 9. IrDA Timing

The parity/9th-bit interrupt is controlled only by the data in the receive register, and is not affected by data in the FIFO, so the most effective use of the parity/9th-bit interrupt is with FIFO disabled. With the FIFO disabled, received nonaddress words can be ignored and not even read from the UART.

SIR IrDA Mode

The MAX3100's IrDA mode can be used to communicate with other IrDA SIR-compatible devices, or to reduce power consumption in opto-isolated applications.

In IrDA mode, a bit period is shortened to 3/16 of a baud period (1.6µs at 115,200 baud) (Figure 9). A data zero is transmitted as a pulse of light (TX pin = logic low, RX pin = logic high).

In receive mode, the RX signal's sampling is done halfway into the transmission of a high level. The sampling is done once, instead of three times, as in normal mode. The MAX3100 ignores pulses shorter than approximately 1/16 of the baud period. The IrDA device that is communicating with the MAX3100 must be set to transmit pulses at 3/16 of the baud period. For compatibility with other IrDA devices, set the format to 8-bit data, one stop, no parity.

IrDA Module

The MAX3100 was optimized for direct optocoupler drive, whereas IrDA modules contain inverting buffers. Invert the RX and TX outputs as shown in Figure 10.

8051 Example: IrDA to RS-232 Converter

Figure 10 shows the MAX3100 with an 8051 µC. This circuit receives IrDA data and outputs standard RS-232 data. Although the 8051 contains an internal UART, it does not support IrDA or high-speed communications. The MAX3100 can easily interface to the 8051 to support these high-performance communications modes. The 8051 does not have an SPI interface, so communication with the MAX3100 is accomplished with port pins and a short software routine (Figure 12a).

The software routine polls the $\overline{IRQ}$ output to see if data is available from the MAX3100 UART. It then shifts the data out, using the 8051 port pins, and transmits it out the RS-232 side through the MAX3221 driver. The 8051 simultaneously monitors its internal UART for incoming communications from the RS-232 side, and transmits this data out the IrDA side through the MAX3100. The low-level routine (UTLK) is the core routine that sends and receives data over the port pins to simulate an SPI port on the 8051. This technique is useful for any 8051-based MAX3100 port-pin-interfaced application.

SPI/Microwire-Compatible UART in QSOP-16

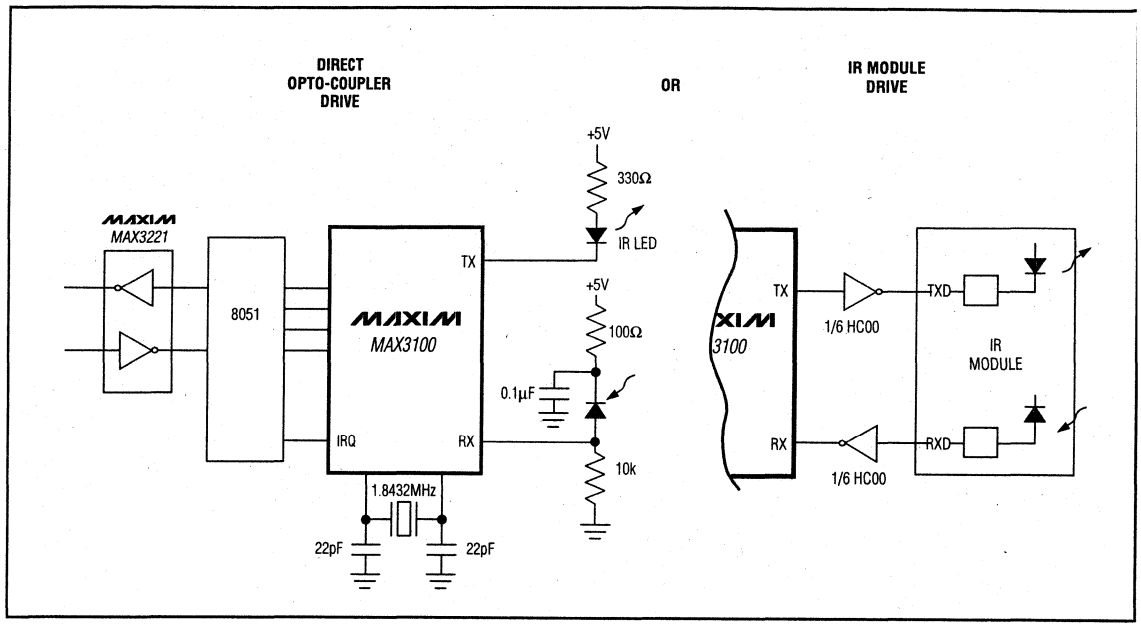


Figure 10. Bidirectional RS-232 IrDA Using an 8051

Interface to PIC Processor ("Quick Brown Fox" Generator)

Figure 11 illustrates the use of the MAX3100 with the PIC®. This circuit is a "Quick Brown Fox" generator that repeatedly transmits "THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG" (covering the entire alphabet) over an RS-232 link with adjustable baud rate, word length, and delay. Although a software-based UART could be implemented on the PIC, features like accurate variable baud rates, high baud rates, and simple protocol selection would be difficult to implement reliably. The 16C54 in the example is the most basic of the PICs. Thus, it is possible to implement the example on any member of the PIC family.

The software routine (Figure 12) begins by reading the DIP switch on port RB. The switch data includes 4 bits for the baud rate, 1 bit for number of stop bits, 1 bit for a word length of 7 or 8 bits, and 1 bit for delay between messages. The PIC reads the switch only at initialization (reset), and programs the parameters into the MAX3100. It then begins sending the message repeatedly. If the delay bit is set, it inserts a 1sec delay between transmissions. As in the 8051 example, the main routine is called UTLK, and can be used in any PIC-based, port-pin-interfaced application.

PIC is a registered trademark of Microchip Corporation.

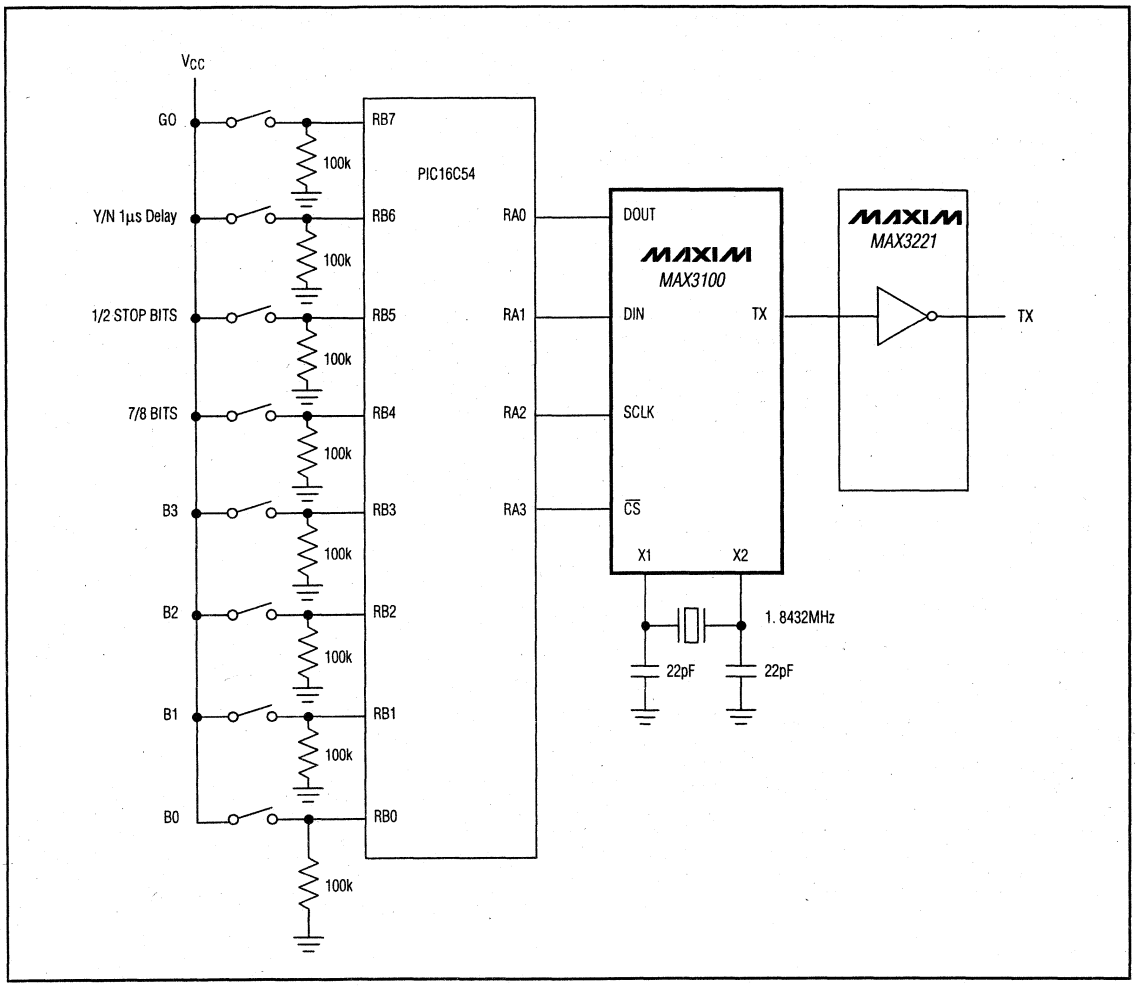


Figure 11. Quick Brown Fox Generator

SPI/Microwire-Compatible UART in QSOP-16

MAX3100 Synchronous-to-Asynchronous SPI UART at a Glance

Table 9. Synchronous Data Input Format (DIN pin from microprocessor, SPI MOSI)

Operation	Bit Number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write Config	1	1	$\overline{FEN}$	SHDNi	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR (IrDA)	ST	PE	L	B3	B2	B1	B0
Read Config	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	TEST
Write Data	1	0	0	0	0	$\overline{TE}$	RTS	Pt	D7t	D6t	D5t	D4t	D3t	D2t	D1t	D0t
Read Data	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10. Synchronous Data Output Format (DOUT pin to microprocessor, SPI MISO)

Operation	Bit Number															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write Config	R	T	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read Config	R	T	$\overline{FEN}$	SHDNo	$\overline{TM}$	$\overline{RM}$	$\overline{PM}$	$\overline{RAM}$	IR (IrDA)	ST	PE	L	B3	B2	B1	B0
Write Data	R	T	0	0	0	RA/ FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r
Read Data	R	T	0	0	0	RA/ FE	CTS	Pr	D7r	D6r	D5r	D4r	D3r	D2r	D1r	D0r

Table 11. Bit Definitions*

Register	Bit Name	Bit Set (1)	Bit Clear (0)
Config	$\overline{FEN}$	Disable FIFO buffer	Enable FIFO buffer
Config	SHDNi	Shutdown	Operate
Config	$\overline{TM}$	Enable transmit-done interrupt	Disable transmit-done interrupt
Config	$\overline{RM}$	Enable data-received interrupt	Disable data-received interrupt
Config	$\overline{PM}$	Enable parity interrupt	Disable parity interrupt
Config	$\overline{RAM}$	Enable framing-error interrupt	Disable framing-error interrupt
Config	IR	Enable IrDA timing mode	Standard timing
Config	ST	Two stop bits	One stop bit
Config	PE	Parity enabled	Parity disabled
Config	L	Word length = 7 bits	Word length = 8 bits
Write Data	$\overline{TE}$	Inhibit TX output	Enable normal operation
Write Data	RTS	Drive $\overline{RTS}$ output pin low	Drive $\overline{RTS}$ output pin high
Write Data	Pt	Transmit parity = 1	Transmit parity = 0
Read Data	RA/FE	Data overrun or framing error	Normal
Read Data	CTS	$\overline{CTS}$ input pin is low	$\overline{CTS}$ input pin is high
All	R	Data has been received	Data buffer is empty
All	T	Transmit buffer is empty	UART is busy transmitting

**Default setting is clear*

Table 12. Field Definitions

Register	Field Name	Meaning
Config	B3–B0	Baud-rate divisor
Write Data	D7t–D0t	Transmit data
Read Data	Pr	Received parity bit
Read Data	D7r–D0r	Received data

Table 13. 1.8432MHz Baud Rates

B3...B0	BRD	Baud	B3...B0	BRD	Baud
0 0 0 0	1	115.2k	1 0 0 0	3	38.4k
0 0 0 1	2	56k	1 0 0 1	6	19.2k
0 0 1 0	4	28k	1 0 1 0	12	9600
0 0 1 1	8	14k	1 0 1 1	24	4800
0 1 0 0	16	7200	1 1 0 0	48	2400
0 1 0 1	32	3600	1 1 0 1	96	1200
0 1 1 0	64	1800	1 1 1 0	192	600
0 1 1 1	128	900	1 1 1 1	384	300

SPI/Microwire-Compatible UART in QSOP-16

```
;IrDA CODE FOR MAX-3100 UART- 8051 based
;*****************************************************************
; CONSTANTS
PCON EQU 87H
;PORT PIN DEFINITIONS- BIT BANGING IF
DOUT BIT P1.0          ;data out (from uart)
DIN BIT P1.1           ;data in (from UART)
SCLK BIT P1.2          ;serial clock
CS BIT P1.3            ;chip select- act low
IRQ BIT P3.2           ;(irq) polled in this code
;RAM LOCATIONS
TX1 EQU 10H            ;transmit regs
TX2 EQU 11H
RX1 EQU 12H            ;receive regs
RX2 EQU 13H
;*****************************************************************
        ORG     0H
BEGIN: MOV SP,#70H          ;initialize stack
 CLR SCLK             ;clear sclk - normally low
;initialize 8051 internal uart
 MOV TMOD,#20H        ;t1 baud
 MOV TH1,#253         ;reload value baud 9600/xtal 5.5M
 MOV SCON,#50H        ;uart- m1, tx and rx
 MOV PCON,#80H        ;double baud rate bit
 MOV TCON,#40H        ;start baud timer
;initialize max3100 uart- irda mode at 9600 baud
 MOV TX1,#0E4H        ;high byte of config- R ints
 MOV TX2,#0CAh        ;9600 baud irda mode and two stops
 CALL UTLK           ;send to uart- write config
;************** MAIN ROUTINE LOOP **********************
LOOP: JNB IRQ,URCV          ;data avail from 3100 uart?
NRECV: JBC RI,RCV51          ;check for 8051 rcv- tx out irda
 JMP LOOP           ;hang here forever
;byte recieved from 3100 uart- get it and send out 8051 uart
URCV: MOV TX1,#0            ;read data
 MOV TX2,#0          ;read data
 CALL UTLK           ;send to 8051 uart- get data to rx
 MOV A,RX2           ;get data to acc
 MOV SBUF,A           ;send out on RS-232 side 9600 baud
 JMP LOOP           ;back to top
;byte recieved from 8051 uart- get it and send out 3100 uart
RCV51: MOV A,SBUF           ;data from 8051 uart
 MOV TX1,#80H          ;tx data
 MOV TX2,A           ;data to irda
 CALL UTLK           ;send to uart- send data out IrDA
 JMP LOOP           ;back to top
;*************************************************************
;SUBROUTINES
; UTLK- talk to uart- main routine
; send 16 bits from TX1 TX2 and rcv 16 to RX1 RX2
UTLK: CLR CS           ;activate cs
 MOV A,TX1           ;get high byte
 CALL BYT8           ;send out
 MOV RX1,A           ;get received 1
 MOV A,TX2           ;get high byte
 CALL BYT8           ;send out
 MOV RX2,A           ;get received 2
 SETB CS            ;set CS high
 RET           ;DONE
;*************************
; BYT8- shift out & in 8 bits with spi clocking- from and to acc
BYT8:   MOV     R4,#8           ;8 bits to send
 SETB DIN            ;make sure din is input
B8LP: RLC A             ;get msb of acc to carry
        MOV     DOUT,C          ;put out on pin
        SETB    SCLK            ;clock high- clock
 MOV C,DIN           ;get data after clk high
 CLR SCLK           ;clock low
 MOV ACC.0,C           ;put in lsbit of a
        DJNZ    R4,B8LP         ;loop til 8 bits
        RET                     ;done
; end of code
 END
```

Figure 12a. 8051 IrDA/RS-232 Code

```
; MAX-3100 UART WITH PIC "QUICK BROWN FOX GENERATOR CODE"
;*****************************************************************************
       DEVICE  PIC16C54,XT_OSC,WDT_OFF,PROTECT_OFF
;RAM LOCATIONS
TX1     EQU     10H             ;data to uart byte 1
TX2     EQU     11H             ;data to uart byte 2
RX1     EQU     12h             ;data from uart byte 1
RX2     EQU     13h             ;data from uart byte 2

LPCNT   EQU     14H             ;loop counter
SHFTO   EQU     15H             ;shift out temp variable
SHFTI   EQU     16H             ;shift in  temp variable
DLVAL   EQU     17H             ;delay value
TEMP    EQU     18H             ;temp variable
GP1     EQU     19H             ;temp variable
GP2     EQU     1AH             ;temp variable
CHPTR   EQU     1BH             ;character pointer

; constants/literals
Cy      EQU     0               ;carry bit
Zr      EQU     2               ;zero bit

; i/o equates
;uart connected to pic on port RA
DOUT    EQU     0               ;data out (to uart)
DIN     EQU     1               ;data in (from uart)
SCLK    EQU     2               ;serial clock
CS      EQU     3               ;chip select- act low
;Configuration dip switch connected to RB
;  RB0 to RB3 are baud rate B0-B3
;  RB4 is 7 or 8 data bits
;  RB5 is 1/2 stop bits
;  RB6 is speed of sending about 100cps or 2.5 cps
;  RB7 is run/stop
; note configuration bits are only read on reset
;*****************************************************************
;subroutine area- pic must have these in low memory
;
;UART SERIAL (SPI) support routines
;send 16 bits from tx1 and tx2, receive 16 to rx1 and rx2
UTLK    BCF     RA,CS           ;activate cs
        MOVF    TX1,0   ;get tx1 to w
        CALL    BYT8            ;send byte 1, recieve byte 1
        MOVWF   RX1             ;stash byte 1
        MOVF    TX2,0           ;get tx1 to w
        CALL    BYT8            ;send byte 1, recieve byte 1
        MOVWF   RX2             ;stash byte 1
        BSF     RA,CS           ;activate cs
        RETLW   0               ;all done

;LOCAL SUB FOR SHIFTING IN/OUT 8 BITS- CORE OF SPI SUPPORT
; BYT8- shift out/in 8 bits w/spi- from and to w, temp shfti,shfto
BYT8    MOVWF   SHFTO           ;put in shift out
        MOVLW   8               ;load loop counter
        MOVWF   LPCNT           ;stash it
B8LP    RLF     SHFTO,1         ;get high bit to send
        BCF     RA,DOUT         ;preclear dout
        BTFSC   STATUS,CY       ;if in low then skip
        BSF     RA,DOUT         ;set dout
        BSF     RA,SCLK         ;clock high- clock out/get input
        BCF     STATUS,CY       ;preclear carry
        BTFSC   RA,DIN          ;if in low then skip
        BSF     STATUS,CY       ;set carry
        RLF     SHFTI,1         ;rotate into place- shfti
        BCF     RA,SCLK         ;clock low
        DECFSZ  LPCNT,1         ;do loop counter
        GOTO    B8LP            ;loop til 8
        MOVF    SHFTI,0         ;put shfto to w- result
        RETLW   0
;end spi serial support
```

Figure 12b. MAX3100 Using PIC µC

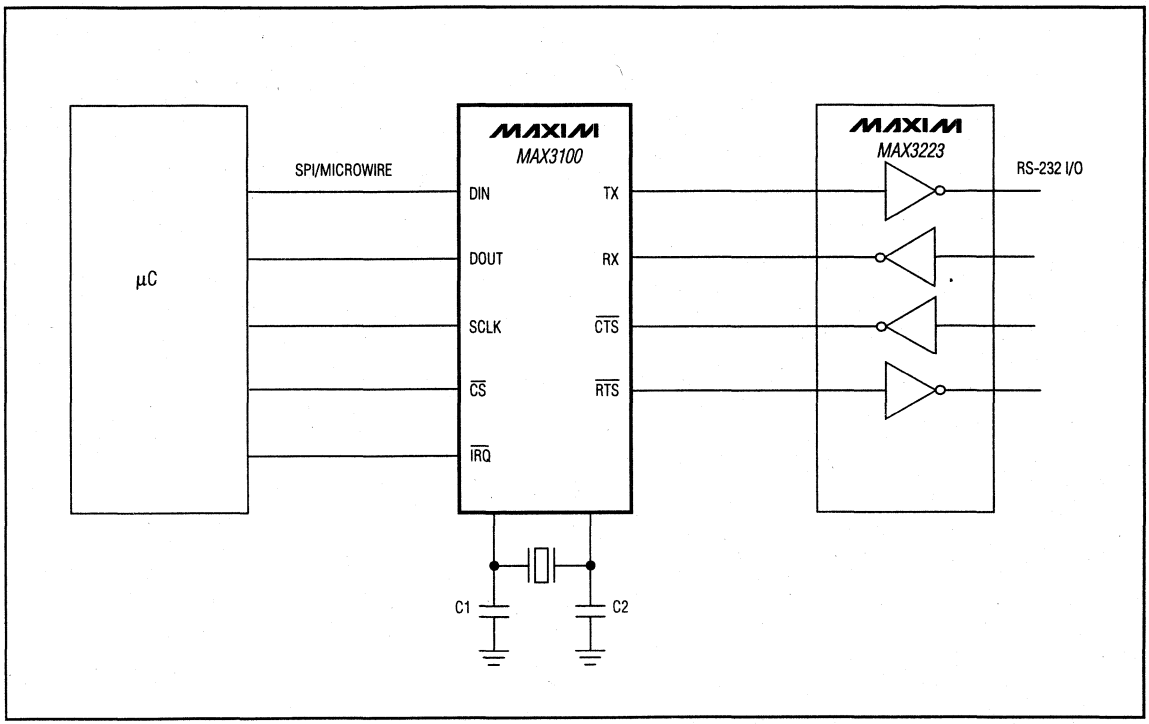
SPI/Microwire-Compatible UART in QSOP-16

```
;delay routine- counts down dlval (loaded at init)
DELAY   MOVF    DLVAL,0         ;load delay
DLY2X   MOVWF   GP2             ;put it in
DLLP2   CLRF    GP1             ;use gp1 to count off ticks
DLLP1   DECFSZ  GP1,1           ;dec gp1 value til 10 ms
        GOTO    DLLP1           ;just loop
        DECFSZ  GP2,1           ;dec gp2 value
        GOTO    DLLP2           ;do another 10 ms til gp2=0
        RETLW   0               ;return

;this "subroutine" returns literal of pc+chptr
;this is the only way to pull out rom literals on the pic...
QBF     MOVF    CHPTR,W         ;GET IN W
        ADDWF   PC              ;JUMP TO TABLE
;QUICK BROWN FOX MESSAGE
        RETLW   "THE QUICK BROWN FOX JUMPS OVER THE LAZY DOG"
The above sentence needs a single line for a single letter or space ie. RETLW
RETLW   0DH             ;carriage return
        RETLW   0AH             ;line feed
        RETLW   0H              ;end of message


;*****************************************************************
;MAIN ROUTINE-
START   MOVLW   0FFH            ;all of rb is input- dip switch
        TRIS    RB              ;set it
        MOVLW   08              ;init port a with cs high only
        MOVWF   RA              ;output to port register
        MOVLW   02H             ;ra is output except din
        TRIS    RA              ;set it- now has
        MOVLW   08H             ;no wdt- rtcc from clock
        OPTION                  ;put in option register


;read switches and bit twiddle to configure uart- tx2 (ls byte)
        MOVF    RB,0            ;get port b to w
        ANDLW   1FH             ;and for 1 and b0-b3
        MOVWF   TX2             ;stash in tx2
        BSF     TX2,6           ;preset the stop bit bit
        BTFSC   RB,5            ;check the switch
        BCF     TX2,6           ;clear if set
        MOVLW   5               ;preload short delay-
        BTFSS   RB,6            ;check the switch
        MOVLW   250             ;overload long delay-
        MOVWF   DLVAL           ;stash in delay value
        MOVLW   0C0H            ;upper byte of config
        MOVWF   TX1             ;stash to tx1
        CALL    UTLK            ;send to uart- configured
;uart is now configured as set on dip switch

;***** MAIN LOOP *****
;go must stay high for run- else stop and reset string ptr
HOLD    MOVLW   0               ;clear pointer with offset 1
        MOVWF   CHPTR           ;load pointer
HANG    BTFSS   RB,7            ;wait high
        JMP     HOLD            ;go to reinit and hold
        CALL    QBF             ;get character to w
        ANDLW   0FFH            ;check for end of message (zero)
        BTFSC   STATUS,Zr       ;bail
        GOTO    HOLD            ;bail to reinit pointer
        MOVWF   TX2             ;load data to tx2
        MOVLW   080H            ;write data
        MOVWF   TX1             ;put in place
        CALL    UTLK            ;send it
        INCF    CHPTR,1         ;next character
        CALL    DELAY           ;delay
        JMP     HANG            ;loop
;*********************************************************************
; VECTORS- start
        ORG     1FFH            ;reset vector
       GOTO    START
       END
```

Figure 12b. MAX3100 Using PIC µC (continued)

SPI/Microwire-Compatible UART in QSOP-16

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 6848

SUBSTRATE CONNECTED TO GND

19-1186; Rev 0; 2/97

MAXIM

±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

General Description

The MAX3187 complete, dual DTE RS-232 serial port meets the stringent ESD requirements of the European Community. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The MAX3187's six RS-232 transmitters and ten RS-232 receivers require no charge pump. Guaranteed to run at data rates up to 230kbps, the MAX3187 is optimized for desktop PC and motherboard applications, and is compatible with popular software for PC communications. Power-supply current is less than 1mA for I_{DD} and I_{SS}, and less than 3mA for I_{CC}.

The MAX3187 is available in a space-saving 36-pin SSOP package.

Applications

Desktop PC

Motherboards

Instruments

Equipment Meeting IEC 1000-4-2

Features

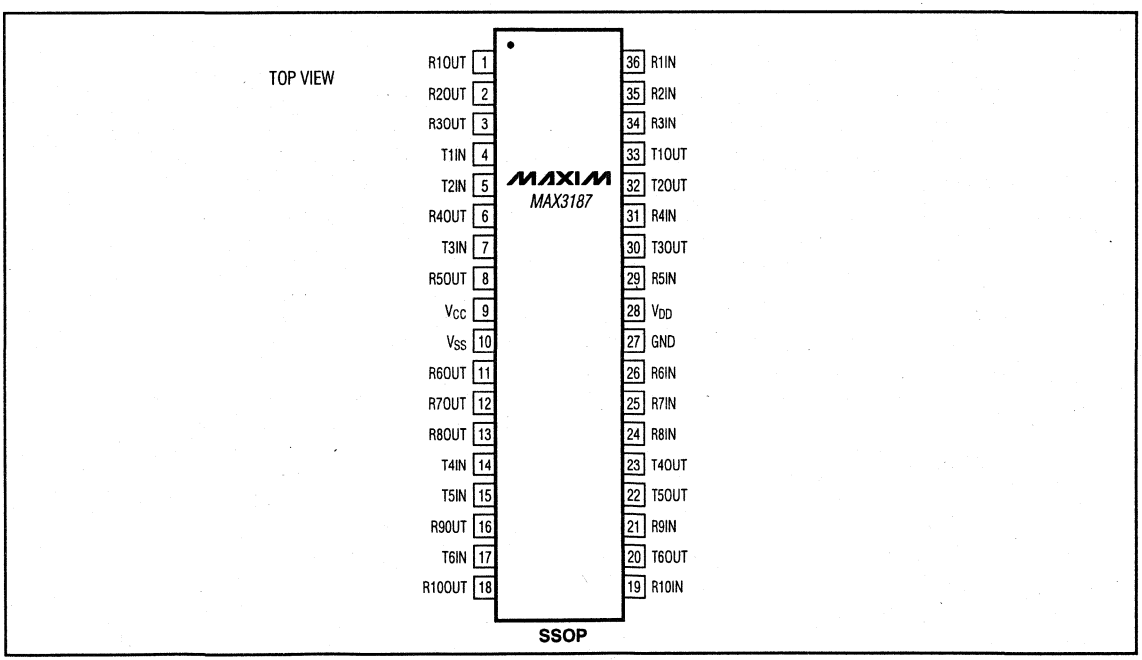
- **Enhanced ESD Protection:**
  - **±15kV—Human Body Model**
  - **±8kV—IEC 1000-4-2, Contact Discharge**
  - **±15kV—IEC 1000-4-2, Air-Gap Discharge**
- **Latchup Free During an ESD Event**
- **36-Pin SSOP Package**
- **Guaranteed 230kbps Data Rate**
- **Flow-Through Pinout**
- **Two Complete DTE Serial Ports**
- **6 RS-232 Drivers and 10 RS-232 Receivers**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3187CAX	0°C to +70°C	36 SSOP
MAX3187EAX	-40°C to +85°C	36 SSOP

Typical Operating Circuit appears at end of data sheet.

Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +7V
V_{DD} ..... -0.3V to +14V
V_{SS} ..... +0.3V to -14V
Input Voltages
  T_IN ..... -0.3V to +6V
  R_IN ..... ±30V
Output Voltages
  T_OUT ..... ±15V
  R_OUT ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_OUT (one at a time) ..... Continuous
  R_OUT (one at a time) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SSOP (derate 11.76mW/°C above +70°C) 762mW
Operating Temperature Ranges
  MAX3187CAX ..... 0°C to +70°C
  MAX3187EAX ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Operating Voltage Range	V_{CC}		4.5		5.5	V
	V_{DD}		10.8		13.2	
	V_{SS}		-13.2		-10.8	
Supply Current	I_{CC}	No load		750	3000	mA
	I_{DD}	No load		370	1000	
	I_{SS}	No load		370	1000	
LOGIC						
Input Logic Threshold Low	V_{ILT}	T_IN			0.8	V
Input Logic Threshold High	V_{IHT}	T_IN	2.0			V
Input Leakage Current				0.01	1	µA
Output Voltage Low	V_{OLR}	R_OUT; I_{SINK} = 3.2mA			0.4	V
Output Voltage High	V_{OHR}	R_OUT; I_{SOURCE} = 1mA	V_{CC} - 0.6			V
TRANSMITTER OUTPUTS						
Output Voltage Swing		V_{DD} = 7.0V, V_{SS} = -7.0V, R_L = 3kΩ	±5.0			V
		V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ	±9.5			
Transmitter Output Resistance		V_{CC} = V_{DD} = V_{SS} = 0V, V_{T_OUT} = ±2V	300			Ω
RS-232 Output Short-Circuit Current				±35	±60	mA
RECEIVER INPUTS						
Receiver Input Voltage Range			-25		25	V
RS-232 Input Threshold Low			0.75			V
RS-232 Input Threshold High					2.4	V
RS-232 Input Hysteresis				0.65		V
RS-232 Input Resistance			3	5	7	kΩ
Receiver Output Short-Circuit Current				±10		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +4.5V to +5.5V, V_{DD} = +10.8V to +13.2V, V_{SS} = -10.8V to -13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

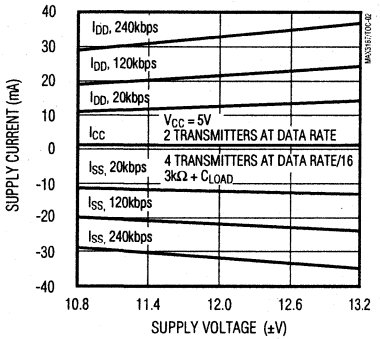
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ESD CHARACTERISTICS							
ESD Protection		Human Body Model			±15		kV
		IEC 1000-4-2 (Contact Discharge)			±8		
		IEC 1000-4-2 (Air-Gap Discharge)			±15		
TIMING CHARACTERISTICS							
Transmitter Output Propagation Delay, Low to High	t_{PLHT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Output Propagation Delay, High to Low	t_{PHLT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				4	µs
Transmitter Propagation Delay Skew, | t_{PLHT} - t_{PHLT} |	t_{SKT}	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ, C_L = 1000pF, T_A = +25°C				0.4	µs
Transition Output Slew Rate	SR	V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V, Figure 1, T_A = +25°C	C_L = 150pF to 2500pF	4		30	V/µs
			C_L = 50pF to 1000pF	8		30	
Receiver Output Propagation Delay, Low to High	t_{PLHR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Output Propagation Delay, High to Low	t_{PHLR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				4.0	µs
Receiver Propagation Delay Skew, | t_{PLHR} - t_{PHLR} |	t_{SKR}	V_{CC} = 5V, C_L = 50pF, T_A = +25°C				0.4	µs
Guaranteed Data Rate	DR	V_{CC} = 5V, V_{DD} = 12V, V_{SS} = -12V, R_L = 3kΩ to 7kΩ, T_A = +25°C, any two transmitters switching	C_L = 50pF to 2500pF	120			kbps
			C_L = 50pF to 1000pF	230			
Mouse Driveability		T3OUT = -5mA, T1OUT = T2OUT = 5mA		±7.5			V

±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

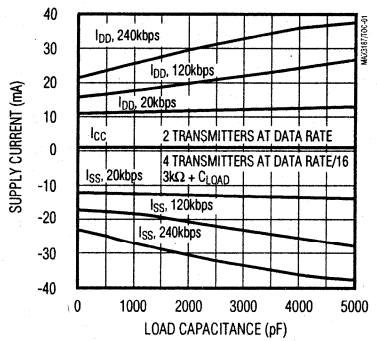
Typical Operating Characteristics

(V_{CC} = +5V, V_{DD} = +12V, V_{SS} = -12V, T_A = +25°C, unless otherwise noted.)

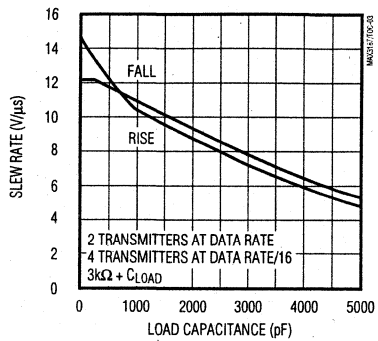
SUPPLY CURRENT vs. SUPPLY VOLTAGE



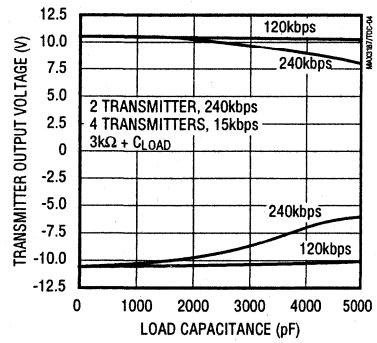
SUPPLY CURRENT vs. LOAD CAPACITANCE



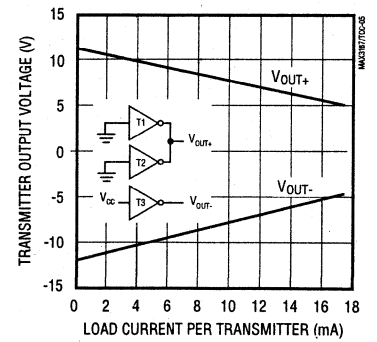
SLEW RATE vs. LOAD CAPACITANCE



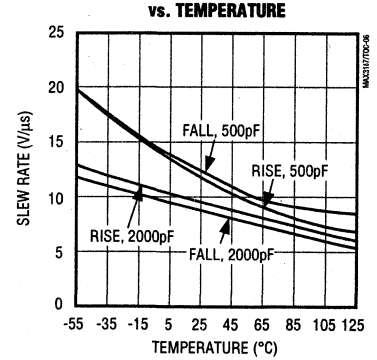
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



TRANSMITTER OUTPUT VOLTAGE vs. LOAD CURRENT PER TRANSMITTER



SLEW RATE vs. TEMPERATURE



±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

Pin Description

PIN	NAME	FUNCTION
1, 2, 3, 6, 8, 11, 12, 13, 16, 18	R1OUT–R10OUT	Receiver Outputs, swing between GND and V_{CC}
4, 5, 7, 14, 15, 17	T1IN–T6IN	Transmitter Inputs
9	V_{CC}	Supply-Voltage Input, 4.5V to 5.5V
10	V_{SS}	Supply-Voltage Input, -10.8V to -13.2V
27	GND	Ground. Connect system to ground.
28	V_{DD}	Supply-Voltage Input, 10.8V to 13.2V
19, 21, 24, 25, 26, 29, 31, 34, 35, 36	R10IN–R1IN	Receiver Inputs
20, 22, 23, 30, 32, 33	T6OUT–T1OUT	Transmitter Outputs, swing between V_{DD} and V_{SS}

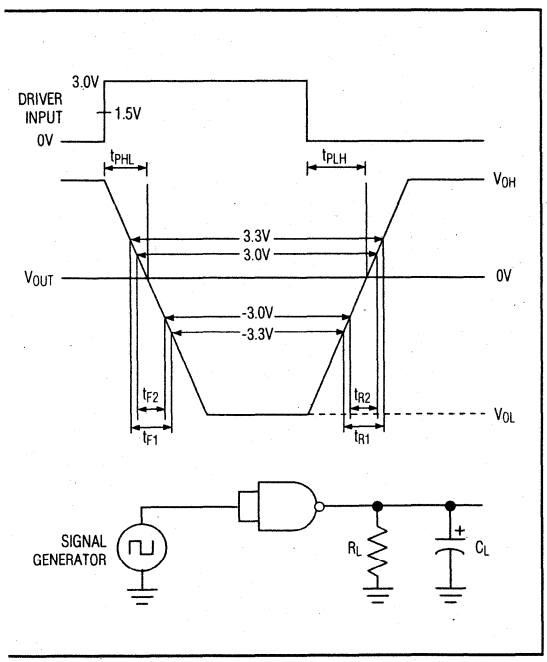


Figure 1. Slew-Rate Test Circuit and Timing Diagram

Detailed Description

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges (ESD) encountered during handling and assembly. The MAX3187 driver outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ±15kV ESD, without damage. After an ESD event, the MAX3187 continues working without latchup.

ESD protection can be tested in several ways. The transmitter outputs and receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact-Discharge Method specified in IEC 1000-4-2 (formerly IEC 801-2)
3) ±15kV using the Air-Gap Method specified in IEC 1000-4-2 (formerly IEC 801-2)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

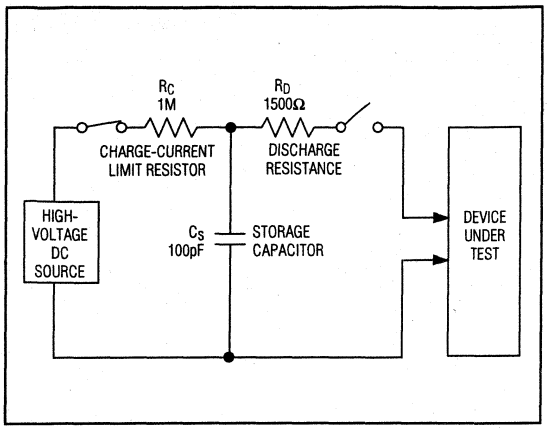


Figure 2a. Human Body ESD Test Model

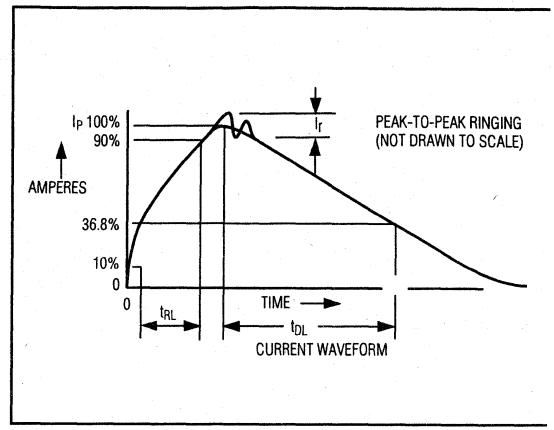


Figure 2b. Human Body Model Current Waveform

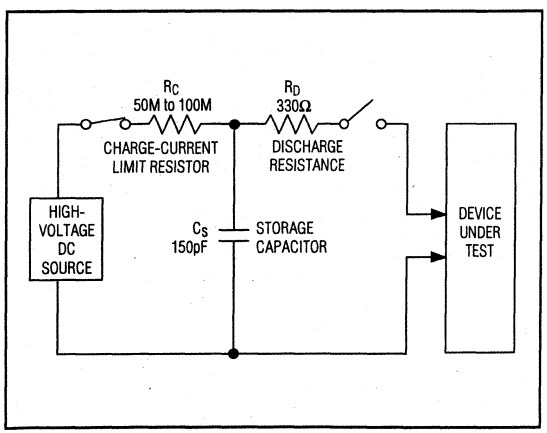


Figure 3a. IEC 1000-4-2 ESD Test Model

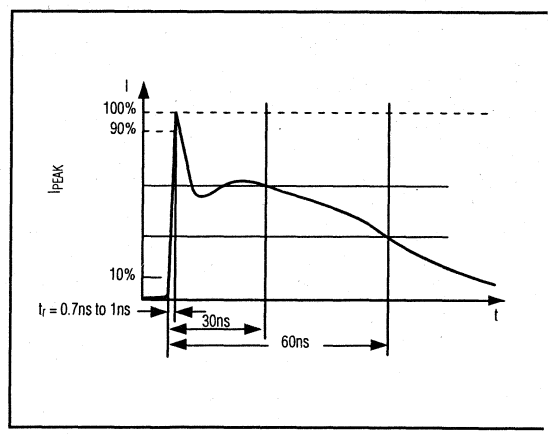


Figure 3b. IEC 1000-4-2 ESD-Generator Current Waveform

Human Body Model

Figure 2a shows the Human Body Model, and Figure 2b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 1000-4-2

Since January 1996, all equipment manufactured and/or sold in the European community has been required to meet the stringent IEC 1000-4-2 specification. The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3187 helps you design equipment that meets Level 4 (the highest level) of IEC 1000-4-2, without additional ESD protection components.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 3a), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 3b shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact-Discharge test.

The Air-Gap test involves approaching the device with a charge probe. The Contact-Discharge method connects the probe to the device before the probe is energized.

±15kV ESD-Protected, EMC-Compliant, 230kbps, Dual RS-232 Serial Port for Motherboards/Desktops

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. Of course, all pins (not just RS-232 inputs and outputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC 1000-4-2.

Applications Information

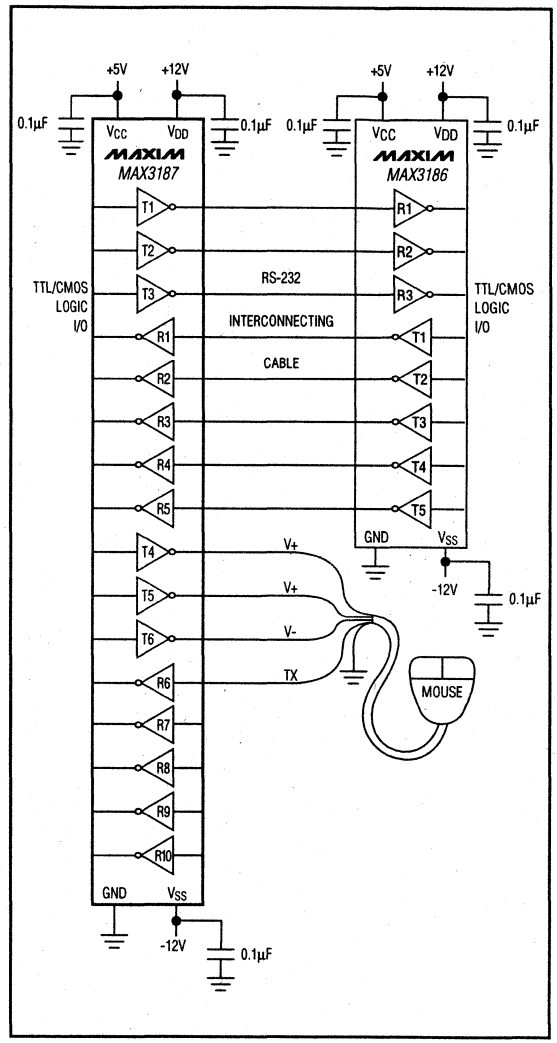
Use proper layout to ensure other devices on your board are not damaged in an ESD strike. Currents as high as 60A can instantaneously pass into ground, so be sure to minimize the ground-lead return path to the power supply. A separate return path to the power supply is recommend. Trace widths should be greater than 40 mils. Bypass V_{CC}, V_{DD}, and V_{SS} with 0.1µF capacitors as close to the part as possible to ensure maximum ESD protection.

Connect any unused transmitter inputs to GND or V_{CC}. The MAX3187 is not sensitive to power-supply sequencing, and therefore requires no external protection diodes.

Chip Information

TRANSISTOR COUNT: 419

Typical Operating Circuit



19-1283; Rev 1; 10/97

MAXIM

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

General Description

The MAX3243E/MAX3244E/MAX3245E are 3V-powered EIA/TIA-232 and V.28/V.24 communications interfaces with automatic shutdown/wakeup features, high data-rate capabilities, and enhanced electrostatic discharge (ESD) protection. All transmitter outputs and receiver inputs are protected to ±15kV using IEC 1000-4-2 Air-Gap Discharge, ±8kV using IEC 1000-4-2 Contact Discharge, and ±15kV using the Human Body Model.

The transceivers have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. The MAX3243E and MAX3244E are guaranteed to run at data rates of 250kbps while maintaining RS-232 output levels. The MAX3245E is guaranteed to run at a data rate of 1Mbps using Maxim's MegaBaud™ feature. The devices are complete serial ports (3 drivers, 5 receivers) intended for notebook or subnotebook computers.

The MAX3243E/MAX3244E/MAX3245E achieve 1µA supply current using Maxim's revolutionary AutoShutdown™ and AutoShutdown Plus™ features, which automatically save power without changes to the existing BIOS or operating system.

The MAX3243E (with AutoShutdown) shuts down if the RS-232 cable is disconnected or if the transmitters of the connected peripherals are off. The device turns on again when a valid level is applied to any receiver input.

The MAX3244E/MAX3245E (with AutoShutdown Plus) shut down after 30sec if the RS-232 cable is disconnected or if the transmitters of the connected peripherals are idle. The device turns on again when a valid edge is applied to any transmitter or receiver input.

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Features

- ♦ **Enhanced ESD Protection:**
  ±15kV (Human Body Model)
  ±8kV (IEC 1000-4-2, Contact Discharge)
  ±15kV (IEC 1000-4-2, Air-Gap Discharge)
- ♦ **1µA Supply Current Achieved with AutoShutdown (MAX3243E) and AutoShutdown Plus (MAX3244E/MAX3245E)**
- ♦ **Guaranteed Data Rate:**
  250kbps (MAX3243E/MAX3244E)
  1Mbps (MAX3245E)
- ♦ **Meets EIA/TIA-232 Specifications Down to 3.0V**
- ♦ **Guaranteed Slew Rate:**
  6V/µs (MAX3243E/MAX3244E)
  24V/µs (MAX3245E)
- ♦ **Guaranteed Mouse Driveability**
- ♦ **Small, 0.1µF Capacitors**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3243ECWI	0°C to +70°C	28 SO
MAX3243ECAI	0°C to +70°C	28 SSOP
MAX3243EEWI	-40°C to +85°C	28 SO
MAX3243EEAI	-40°C to +85°C	28 SSOP
MAX3244ECWI	0°C to +70°C	28 SO
MAX3244ECAI	0°C to +70°C	28 SSOP
MAX3244EEWI	-40°C to +85°C	28 SO
MAX3244EEAI	-40°C to +85°C	28 SSOP
MAX3245ECWI	0°C to +70°C	28 SO
MAX3245ECAI	0°C to +70°C	28 SSOP
MAX3245EEWI	-40°C to +85°C	28 SO
MAX3245EEAI	-40°C to +85°C	28 SSOP

Selector Guide

PART	NO. OF DRIVERS/ RECEIVERS	VCC RANGE (V)	AUTOSHUTDOWN	AUTOSHUTDOWN PLUS	MEGABAUD	±15kV ESD PROTECTION
MAX3243E	3/5	3.0 to 5.5	✔			✔
MAX3244E	3/5	3.0 to 5.5		✔		✔
MAX3245E	3/5	3.0 to 5.5		✔	✔	✔

Typical Operating Circuit and Pin Configuration appear at end of data sheet.

AutoShutdown, AutoShutdown Plus and MegaBaud are trademarks of Maxim Integrated Products.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... -0.3V to +7V
V- ..... +0.3V to -7V
V+ + |V-| ..... +13V
Input Voltages
  T_IN, FORCEON, $\overline{FORCEOFF}$ ..... -0.3V to +6V
  R_IN ..... ±25V
Output Voltages
  T_OUT ..... ±13.2V
  R_OUT, R2OUTB, $\overline{INVALID}$ ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_OUT (one at a time) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SO (derate 12.5mW/°C above +70°C) 1000mW
  SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
  MAX324_EC_ I ..... 0°C to +70°C
  MAX324_EE_ I ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{CC} = 3.3V or 5.0V, T_A = +25°C, no load)						
Supply Current	FORCEON = $\overline{FORCEOFF}$ = V_{CC}			0.3	1.0	mA
Shutdown Supply Current	$\overline{FORCEOFF}$ = GND			1.0	10.0	µA
AutoShutdown Supply Current (MAX3243E)	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}, all R_IN open or grounded			1.0	10.0	µA
AutoShutdown Plus Supply Current (MAX3244E/MAX3245E)	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}, all R_IN idle, all T_IN idle			1.0	10.0	µA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_IN, FORCEON, $\overline{FORCEOFF}$				0.8	V
Input Logic Threshold High	T_IN, FORCEON, $\overline{FORCEOFF}$	V_{CC} = 3.3V	2.0			V
		V_{CC} = 5.0V	2.4			
Transmitter Input Hysteresis				0.5		V
Input Leakage Current	T_IN, FORCEON, $\overline{FORCEOFF}$			±0.01	±1.0	µA
Output Leakage Current	Receivers disabled			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	V_{CC} = 3.3V		0.6	1.1		V
	V_{CC} = 5.0V		0.8	1.4		
Input Threshold High	V_{CC} = 3.3V			1.6	2.4	V
	V_{CC} = 5.0V			1.9	2.4	
Input Hysteresis				0.5		V
Input Resistance	T_A = +25°C		3	5	7	kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TRANSMITTER OUTPUTS							
Output Voltage Swing		All transmitter outputs loaded with 3kΩ to ground		±5	±5.4		V
Output Resistance		V_{CC} = V+ = V- = 0V, transmitter output = ±2V		300	10M		Ω
Output Short-Circuit Current					±35	±60	mA
Output Leakage Current		V_{CC} = 0V to 5.5V, transmitter output = ±12V, transmitters disabled				±25	µA
MOUSE DRIVEABILITY							
Transmitter Output Voltage		T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to ground, T1OUT and T2OUT loaded with 2.5mA each		±5			V
ESD CHARACTERISTICS							
ESD Protection		R_IN, T_OUT	Human Body Model		±15		kV
			IEC 1000-4-2 (Contact Discharge)		±8		
			IEC 1000-4-2 (Air-Gap Discharge)		±15		
AUTOSHUTDOWN: MAX3243E (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})							
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage High		Figure 4	Positive threshold			2.7	V
			Negative threshold	-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage Low		1µA supply current, Figure 4		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low		I_{OUT} = 1.6mA				0.4	V
$\overline{INVALID}$ Output Voltage High		I_{OUT} = -1.0mA		V_{CC} - 0.6			V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High	t_{INVH}	Figure 4			1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low	t_{INVL}	Figure 4			30		µs
Receiver or Transmitter Edge to Transmitters Enabled	t_{WU}	Figure 4			100		µs
AUTOSHUTDOWN PLUS: MAX3244E/MAX3245E (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})							
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage High		Figure 4	Positive threshold			2.7	V
			Negative threshold	-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage Low		Figure 4		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low		I_{OUT} = 1.6mA				0.4	V
$\overline{INVALID}$ Output Voltage High		I_{OUT} = -1.0mA		V_{CC} - 0.6			V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High	t_{INVH}	Figure 5			1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low	t_{INVL}	Figure 5			30		µs
Receiver or Transmitter Edge to Transmitters Enabled	t_{WU}	Figure 5			100		µs
Receiver or Transmitter Edge to Transmitters Shut Down	$t_{AUTOSHDN}$	Figure 5		15	30	60	sec

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

TIMING CHARACTERISTICS—MAX3243E/MAX3244E

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.15		µs
		t_{PLH}		0.15		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			100		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, T_A = +25°C, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 1000pF	6		30	V/µs
		C_L = 150pF to 2500pF	4		30	

TIMING CHARACTERISTICS—MAX3245E

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

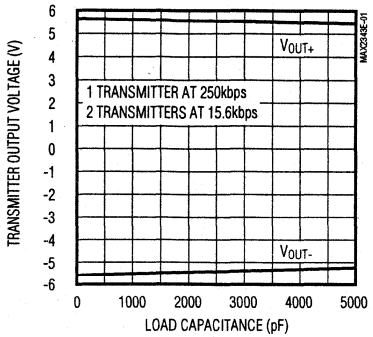
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
	V_{CC} = 3.0V to 4.5V, R_L = 3kΩ, C_L = 250pF, one transmitter switching		1000			
	V_{CC} = 4.5V to 5.5V, R_L = 3kΩ, C_L = 1000pF, one transmitter switching		1000			
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.15		µs
		t_{PLH}		0.15		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			25		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, T_A = +25°C, R_L = 3kΩ to 7kΩ, C_L = 150pF to 1000pF, measured from +3V to -3V or -3V to +3V		24		150	V/µs

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

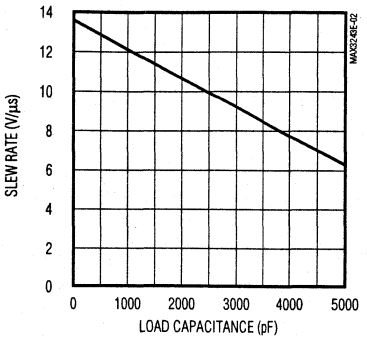
Typical Operating Characteristics

(V_{CC} = +3.3V, 250kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

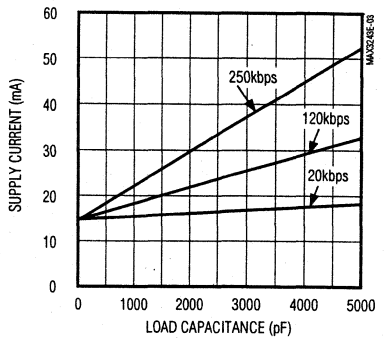
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



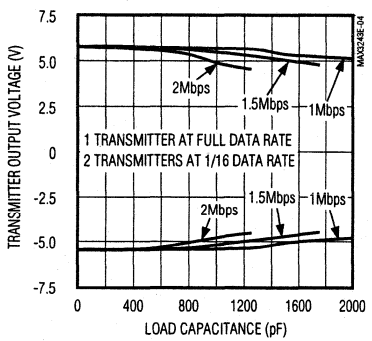
MAX3243E/MAX3244E SLEW RATE vs. LOAD CAPACITANCE



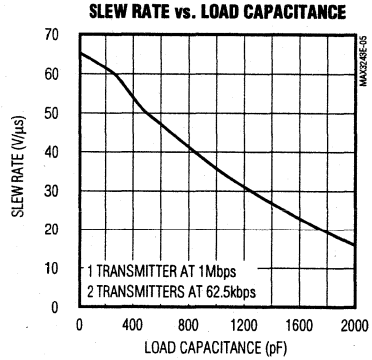
MAX3243E/MAX3244E SUPPLY CURRENT vs. LOAD CAPACITANCE



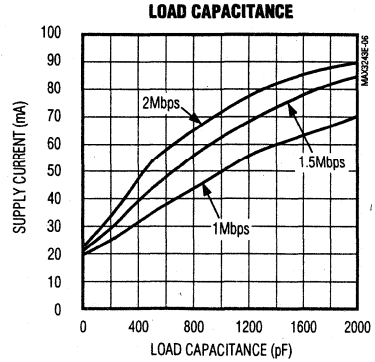
MAX3245E TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



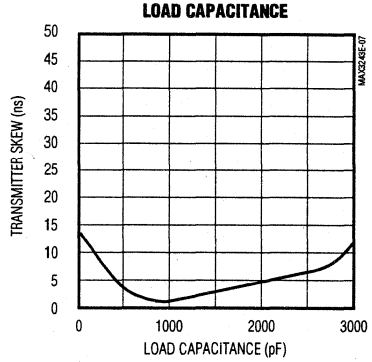
MAX3245E SLEW RATE vs. LOAD CAPACITANCE



MAX3245E SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX3245E TRANSMITTER SKEW vs. LOAD CAPACITANCE



±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

Pin Description

PIN	NAME	FUNCTION
1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
2	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
3	V-	-5.5V Generated by the Charge Pump
4–8	R1IN–R5IN	RS-232 Receiver Inputs
9, 10, 11	T1OUT, T2OUT, T3OUT	RS-232 Transmitter Outputs
12, 13, 14	T3IN, T2IN, T1IN	TTL/CMOS Transmitter Inputs
15–19	R5OUT–R1OUT	TTL/CMOS Receiver Outputs
20	R2OUTB	Noninverting Complementary Receiver Output, always active
21	$\overline{\text{INVALID}}$	Active-Low Output of the Valid Signal Detector. A logic high indicates that a valid RS-232 level is present on a receiver input.
22	$\overline{\text{FORCEOFF}}$	Active-Low Force-Off Input. Drive low to shut down transmitters, receivers (except R2OUTB), and on-board supply. This overrides AutoShutdown and FORCEON (Table 1).
23	FORCEON	Force-On Input. Drive high to override AutoShutdown, keeping transmitters and receivers on ($\overline{\text{FORCEOFF}}$ must be high) (Table 1).
24	C1-	Negative Terminal of Voltage-Doubler Charge-Pump Capacitor
25	GND	Ground
26	V_{CC}	+3.0V to +5.5V Supply Voltage
27	V+	+5.5V Generated by the Charge Pump
28	C1+	Positive Terminal of Voltage-Doubler Charge-Pump Capacitor

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3243E/MAX3244E/MAX3245E's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump) for input voltages (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode: if the output voltages are less than 5.5V, the charge pumps are enabled; if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels. The MAX3243E/MAX3244E transmitters guarantee a 250kbps data rate (1Mbps for the MAX3245E) with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled to drive multiple receivers.

When FORCEON = GND and $\overline{FORCEOFF}$ = V_{CC} in the MAX3243E, if the AutoShutdown circuitry does not sense a valid voltage level at any receiver input, the part shuts down and the transmitter outputs are high impedance. When FORCEON = GND and $\overline{FORCEOFF}$ = V_{CC} in the MAX3244E/MAX3245E, if the AutoShutdown Plus circuitry does not sense a valid transition on any receiver or transmitter for 30sec, the part shuts down and the transmitter outputs are high impedance.

When powered off or shut down, the MAX3243E/MAX3244E/MAX3245E permit the outputs to be driven up to ±12V. The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. All receivers have inverting three-state outputs, and can be active or inactive (Table 1). The devices feature an extra, always-active noninverting output, R2OUTB. This allows ring indicator applications to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 1).

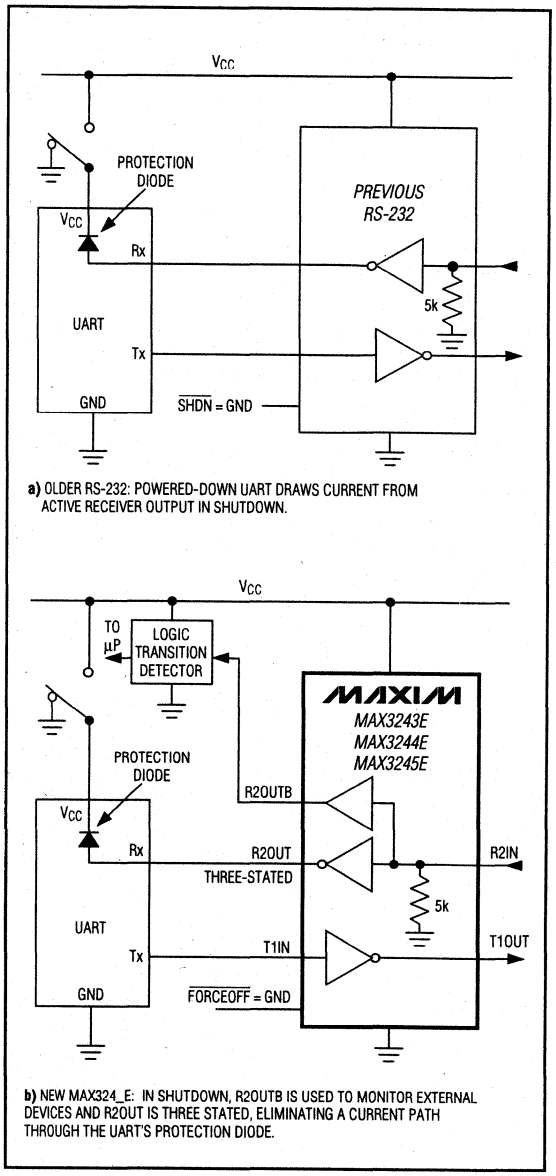


Figure 1. Detection of RS-232 Activity when the UART and Interface are Shut Down

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±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

Table 1a. MAX3243E Output Control Truth Table

FORCEON	$\overline{\text{FORCEOFF}}$	VALID RECEIVER LEVEL	OPERATION STATUS	T_OUT	R_OUT	R2OUTB
X	0	X	Shutdown (Forced Off)	High-Z	High-Z	Active
1	1	X	Normal Operation (Forced On)	Active	Active	Active
0	1	Yes	Normal Operation (AutoShutdown)	Active	Active	Active
0	1	No	Shutdown (AutoShutdown)	High-Z	Active	Active

Table 1b. MAX3244E/MAX3245E Output Control Truth Table

FORCEON	$\overline{\text{FORCEOFF}}$	TRANSMITTER OR RECEIVER EDGE WITHIN 30sec	OPERATION STATUS	T_OUT	R_OUT	R2OUTB
X	0	X	Shutdown (Forced Off)	High-Z	High-Z	Active
1	1	X	Normal Operation (Forced On)	Active	Active	Active
0	1	Yes	Normal Operation (AutoShutdown Plus)	Active	Active	Active
0	1	No	Shutdown (AutoShutdown Plus)	High-Z	Active	Active

Table 2. $\overline{\text{INVALID}}$ Truth Table

RS-232 SIGNAL PRESENT AT ANY RECEIVER INPUT	$\overline{\text{INVALID}}$ OUTPUT
Yes	H
No	L

AutoShutdown Mode (MAX3243E)

The MAX3243E achieves a 1µA supply current with Maxim's AutoShutdown feature, which operates when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. When the MAX3243E does not sense a valid voltage level on any receiver input for 30µs, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if the RS-232 cable is disconnected or the connected peripheral transmitters are off. The device turns on again when a valid level is applied to any receiver input. As a result, the system saves power without changes to the existing BIOS or operating system. When using AutoShutdown, the $\overline{\text{INVALID}}$ output is high when the device is on and low when the device is shut down. Because $\overline{\text{INVALID}}$ indicates the receiver inputs' condition, it is independent of FORCEON and $\overline{\text{FORCEOFF}}$ states (Figure 2).

Figure 2 and Tables 1a and 2 summarize the MAX3243E's operating modes. FORCEON and $\overline{\text{FORCEOFF}}$ override the AutoShutdown circuitry. When neither control is asserted, the IC selects between these states automatically, based on the receiver input levels. Figures 2a and 2b depict valid and invalid RS-232 receiver levels. Figure 4 shows the input levels and timing diagram for AutoShutdown operation.

A mouse or other system with AutoShutdown may need time to wake up. Figure 3 shows a circuit that forces the transmitters on for 100ms, allowing enough time for the other system to realize that the MAX3243E is awake. If the other system outputs valid RS-232 signals within that time, the RS-232 ports on both systems remain enabled.

When shut down, the device's charge pumps are turned off, V+ is pulled to V_{CC}, V- is pulled to ground, and the transmitter outputs are high impedance. The time required to exit shutdown is typically 100µs (Figure 10).

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

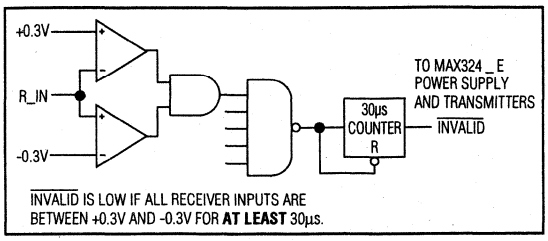


Figure 2a. Invalid Receiver Levels

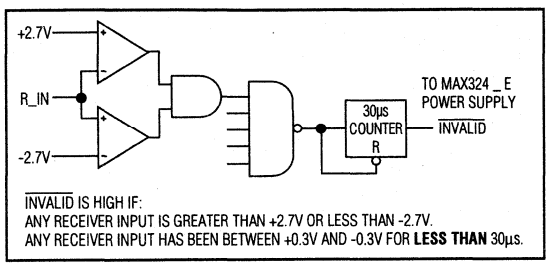


Figure 2b. Valid Receiver Levels

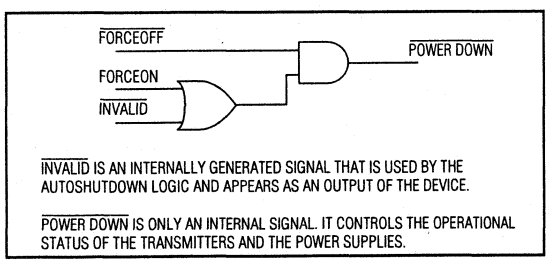


Figure 2c. AutoShutdown Logic

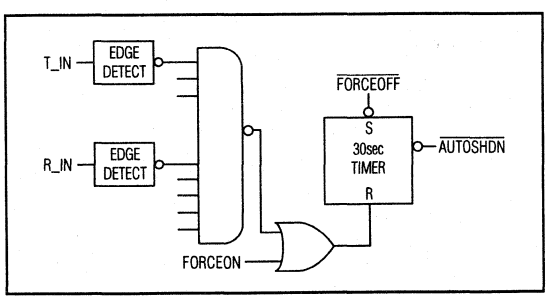


Figure 2d. AutoShutdown Plus Edge Detection

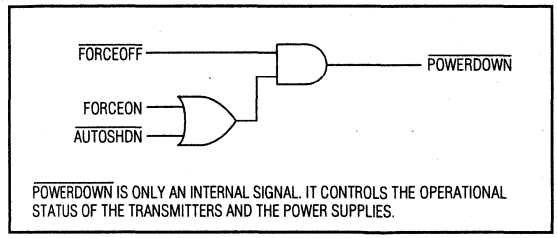


Figure 2e. AutoShutdown Plus Logic

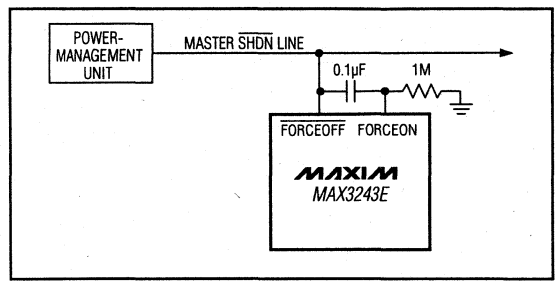


Figure 3. AutoShutdown with Initial Turn-On to Wake up a Mouse or Another System

AutoShutdown Plus Mode (MAX3244E/MAX3245E)

The MAX3244E/MAX3245E achieve a 1µA supply current with Maxim's AutoShutdown Plus feature, which operates when FORCEON is low and FORCEOFF is high. When the MAX3244E/MAX3245E do not sense a valid signal transition on any receiver or transmitter input for 30sec, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if all transmitter and receiver inputs are idle. The system turns on again when a valid transition is applied to any receiver or transmitter input. As a result, the system saves power without changes to the existing BIOS or operating system.

Figures 2a and 2b depict valid and invalid RS-232 receiver levels. INVALID indicates the receiver inputs' condition, and it is independent of the FORCEON and FORCEOFF states. Figure 2 and Tables 1b and 2 summarize the MAX3244E/MAX3245E operating modes. FORCEON and FORCEOFF override the AutoShutdown Plus circuitry. When neither control is asserted, the IC selects between these states automatically based on the last receiver or transmitter input edge received.

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

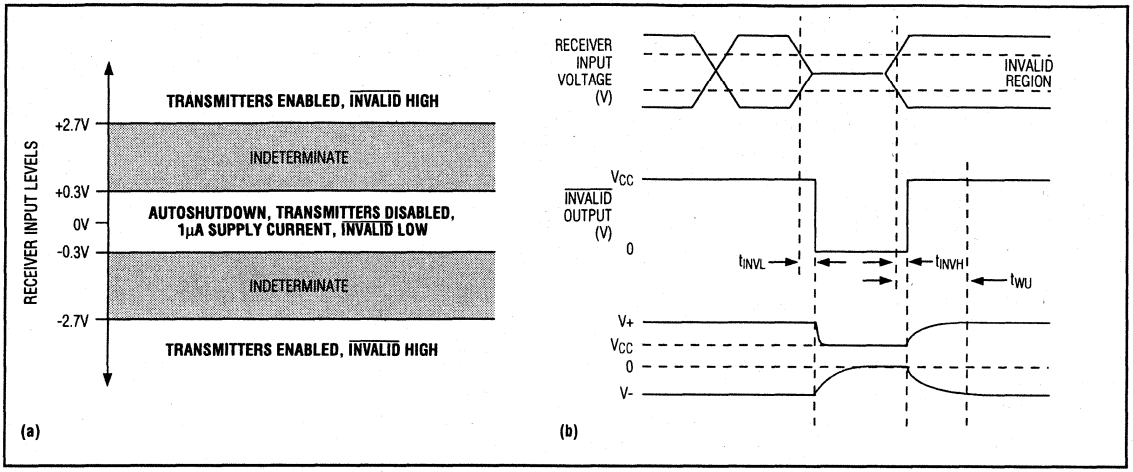


Figure 4. AutoShutdown Input Levels and Timing

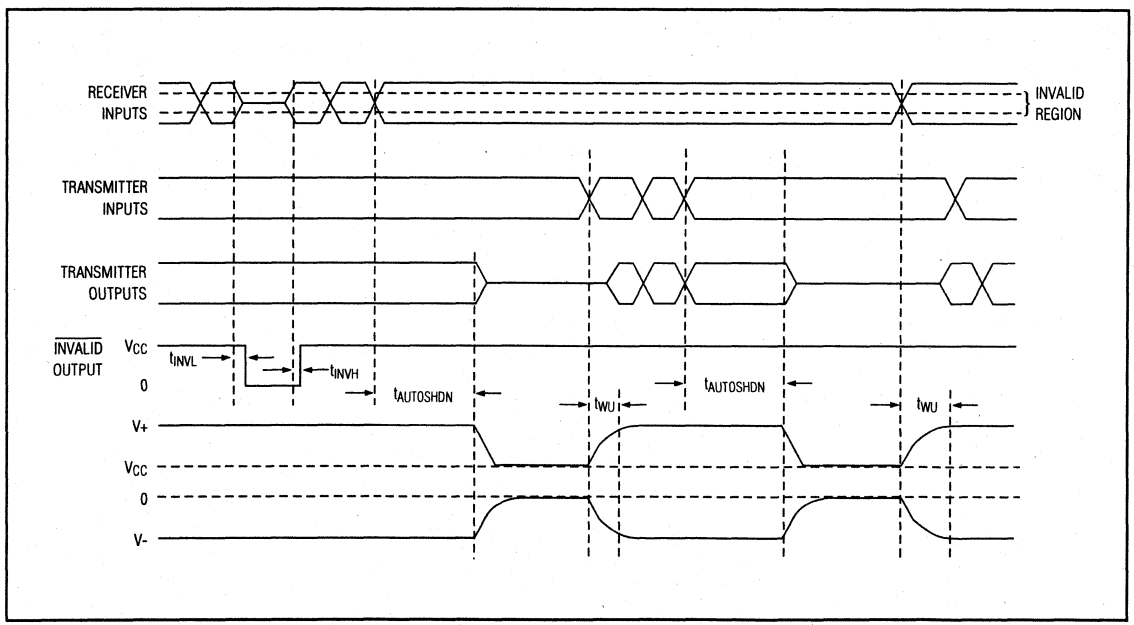


Figure 5. AutoShutdown Plus and INVALID Timing Diagram

Figure 5 shows a timing diagram for AutoShutdown Plus operation. The time required to exit shutdown is typically 100µs (Figure 10).

When shut down, the device's charge pumps are turned off, V+ is pulled to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance).

By connecting $\overline{INVALID}$ to FORCEON, the MAX3244E/MAX3245E shut down when no valid receiver level and no receiver or transmitter edge is detected for 30sec, and wake up when a valid receiver level or receiver or transmitter edge is detected.

By connecting $\overline{INVALID}$ to FORCEON and $\overline{FORCEOFF}$, the MAX3244E/MAX3245E shut down when no valid receiver level is detected, and wake up when a valid receiver level is detected (same as AutoShutdown operation).

Software-Controlled Shutdown

If direct software control is desired, $\overline{INVALID}$ can be used to indicate DTR or ring indicator signal. Tie $\overline{FORCEOFF}$ and FORCEON together to bypass AutoShutdown so the line acts like a $\overline{SHDN}$ input.

±15kV ESD Protection

As with all Maxim devices, ESD protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The MAX3243E/MAX3244E/MAX3245E transmitter outputs and receiver inputs have extra protection against static electricity found in normal operation. Maxim's engineers have developed state-of-the-art structures to protect these pins against ESD of ±15kV without damage.

ESD protection can be tested in various ways. Transmitter outputs and receiver inputs are characterized for protection to the following:

1) ±15kV using the Human Body Model
2) ±8kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
3) ±15kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2).

ESD Test Conditions

Contact Maxim for a reliability report that documents test setup, methodology, and results.

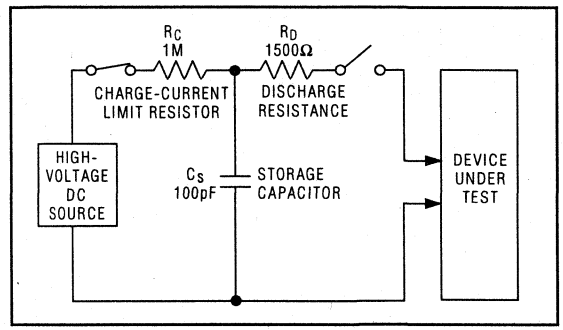


Figure 6. Human Body ESD Test Model

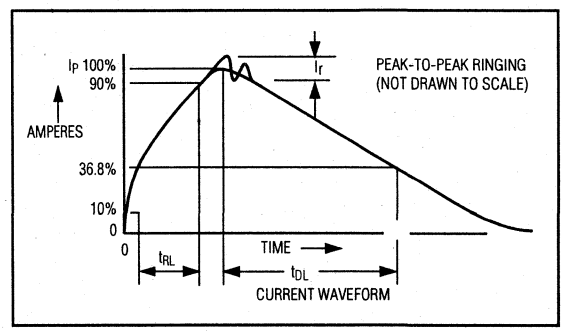


Figure 7. Human Body Model Current Waveform

Human Body Model

Figure 6 shows the Human Body Model, and Figure 7 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the test device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 100-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits. The MAX3243E/MAX3244E/MAX3245E enable the design of equipment that meets Level 4 (the highest level) of IEC 1000-4-2, without additional ESD protection components.

The major difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is

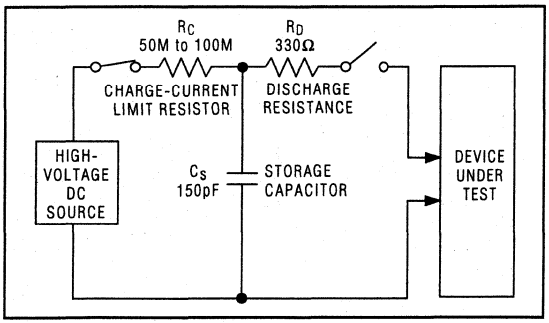


Figure 8. IEC 1000-4-2 ESD Test Model

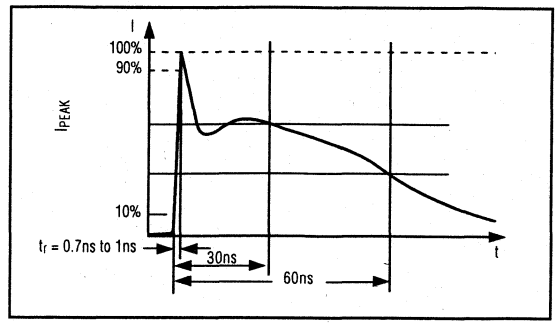


Figure 9. IEC 1000-4-2 ESD Generator Current Waveform

lower in the IEC 1000-4-2 ESD test model (Figure 8), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. Figure 9 shows the current waveform for the ±8kV IEC 1000-4-2 Level 4 ESD Contact Discharge test.

The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. **However, do not increase C1 without also increasing the values of C2, C3, C4, and C_{BYPASS}, to maintain the proper ratios (C1 to the other capacitors).**

When using the minimum required capacitor values, make sure the capacitance value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as reservoir capacitors C2, C3, and C4. Connect the bypass capacitor as close to the IC as possible.

Transmitter Outputs when Exiting Shutdown

Figure 10 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 1000pF.

Table 3. Required Minimum Capacitance Values

SUPPLY VOLTAGE (V)	C1 (µF)	C2, C3, C4, C_{BYPASS} (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

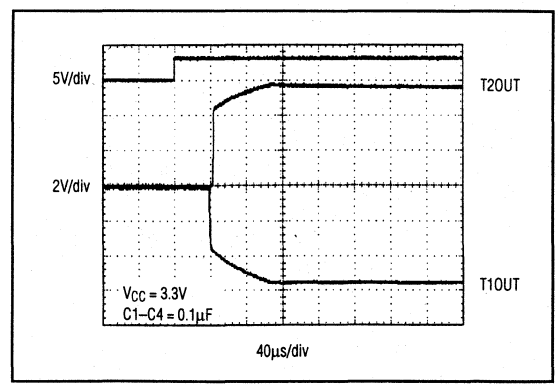


Figure 10. Transmitter Outputs Exiting Shutdown or Powering Up

The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when V- exceeds approximately -3V.

High Data Rates

The MAX3243E/MAX3244E maintain the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 11 shows a transmitter loopback test circuit. Figure 12 shows a loopback test result at 120kbps, and Figure 13 shows the same test at 250kbps. For Figure 12, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 13, a single transmitter was driven at 250kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

The MAX3245E maintains the RS-232 ±5.0V minimum transmitter output voltage with data rates up to 1Mbps (MegaBaud). Figure 14 shows a loopback test result with a single transmitter driven at 1Mbps, and all transmitters loaded with an RS-232 receiver in parallel with 250pF.

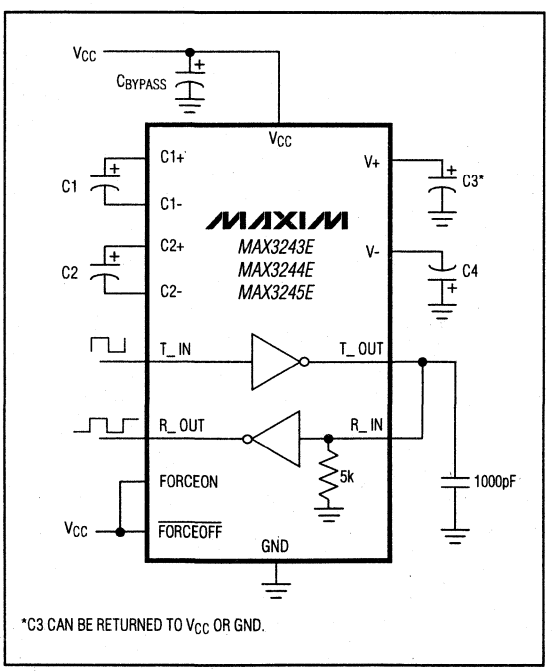


Figure 11. Loopback Test Circuit

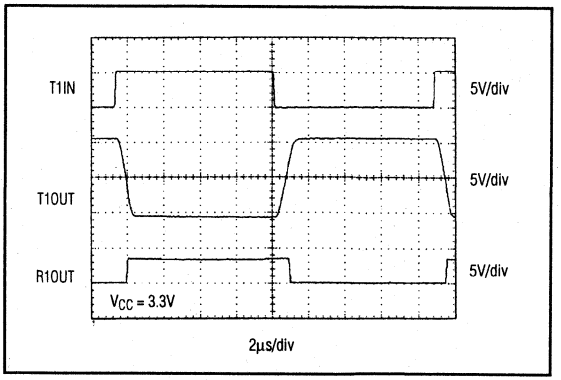


Figure 12. MAX3243E/MAX3244E Loopback Test Result at 120kbps

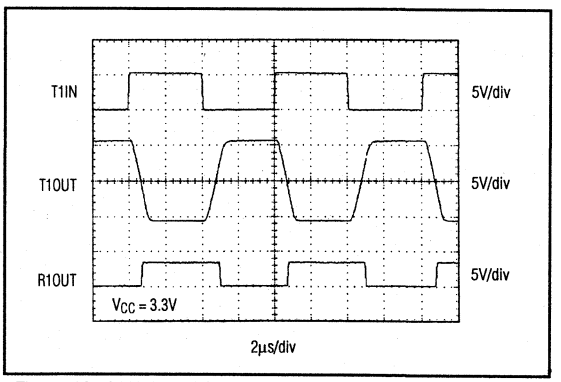


Figure 13. MAX3243E/MAX3244E Loopback Test Result at 250kbps

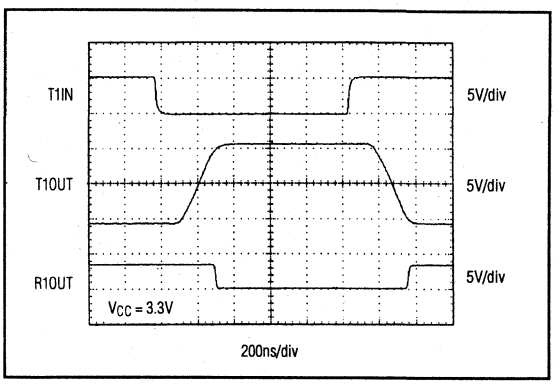


Figure 14. MAX3245E Loopback Test Result at 1Mbps

Table 4. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS families
5	3.3	Compatible with ACT and HCT CMOS, and with AC, HC, or CD4000 CMOS.

Interconnection with 3V and 5V Logic

The MAX3243E/MAX3244E/MAX3245E can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

Mouse Driveability

The MAX3243E/MAX3244E/MAX3245E have been specifically designed to power serial mice while operating from low-voltage power supplies. They have been tested with leading mouse brands from manufacturers such as Microsoft and Logitech. The MAX3243E/MAX3244E/MAX3245E successfully drove all serial mice tested and met their respective current and voltage requirements. Figure 15a shows the transmitter outputs under increasing load current. The MAX3243E/MAX3244E/MAX3245E switching regulator ensures the transmitters will supply at least ±5V under worst-case conditions. Figure 15b shows a typical mouse connection.

The AutoShutdown Plus feature does not work with a mouse; connect FORCEON and $\overline{\text{FORCEOFF}}$ to VCC.

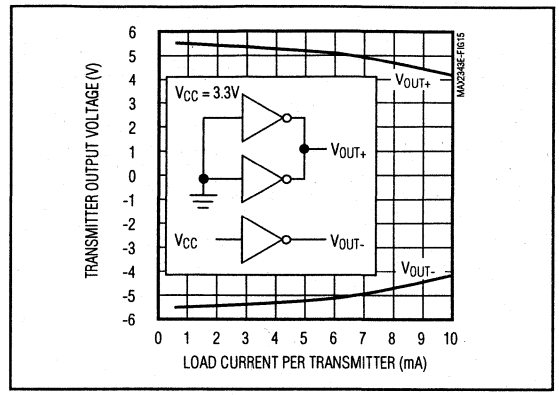


Figure 15a. MAX324_E Transmitter Output Voltage vs. Load Current per Transmitter

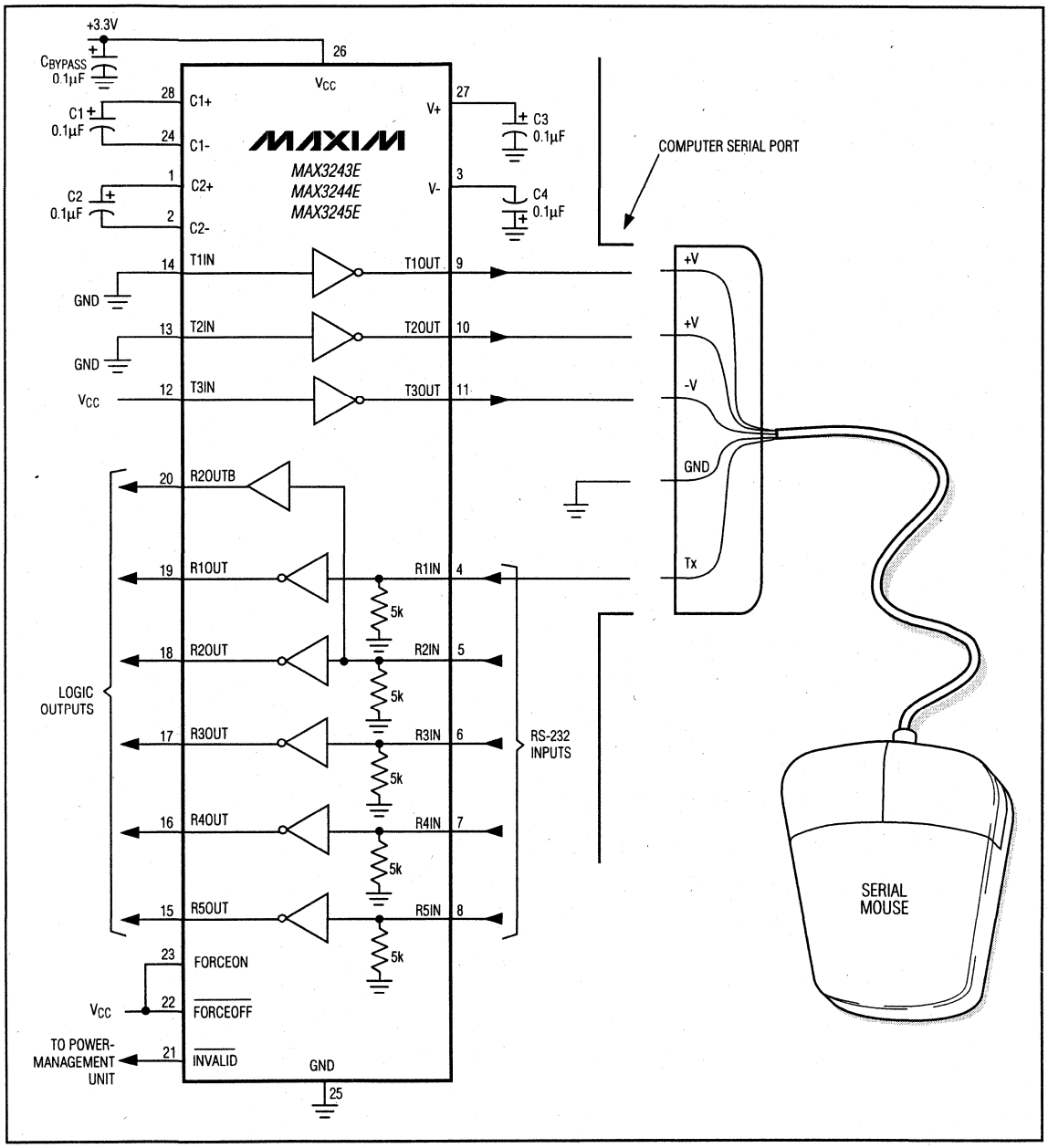
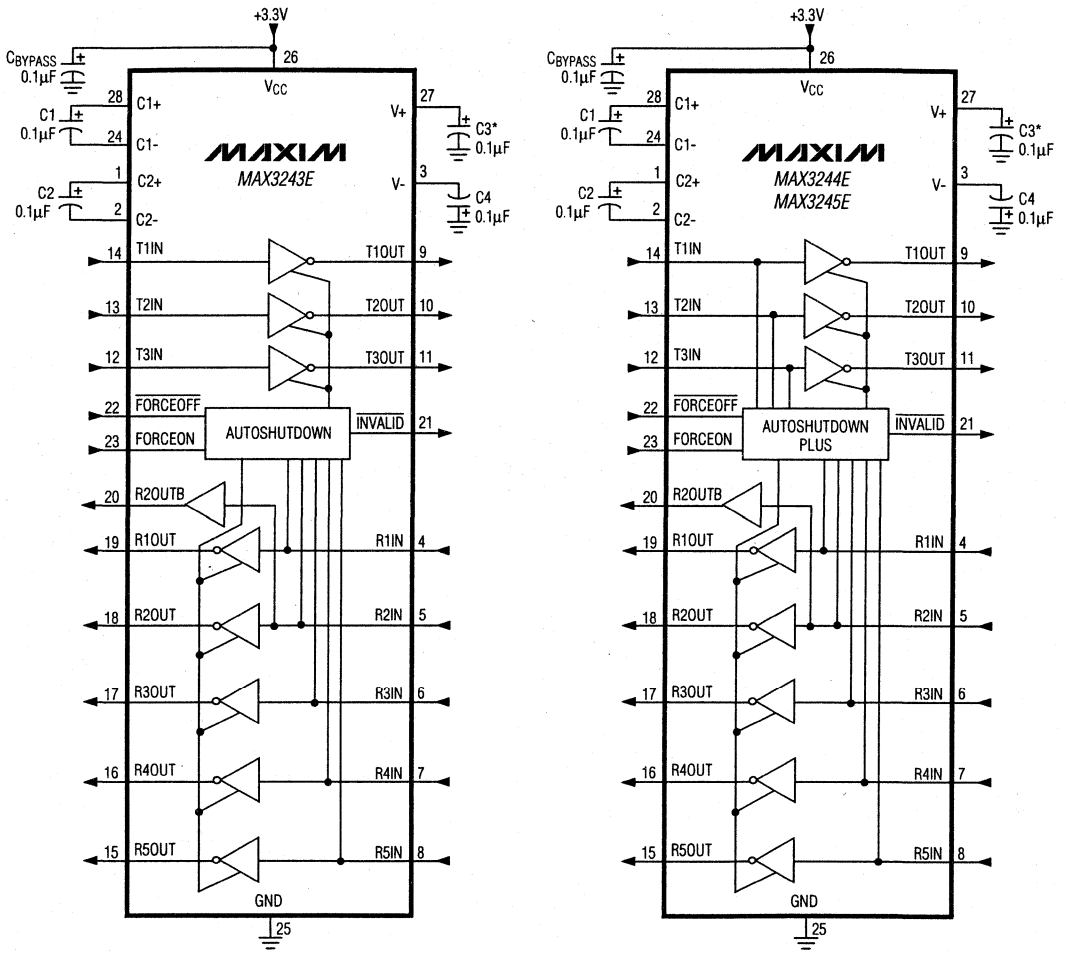


Figure 15b. Mouse Driver Test Circuit

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

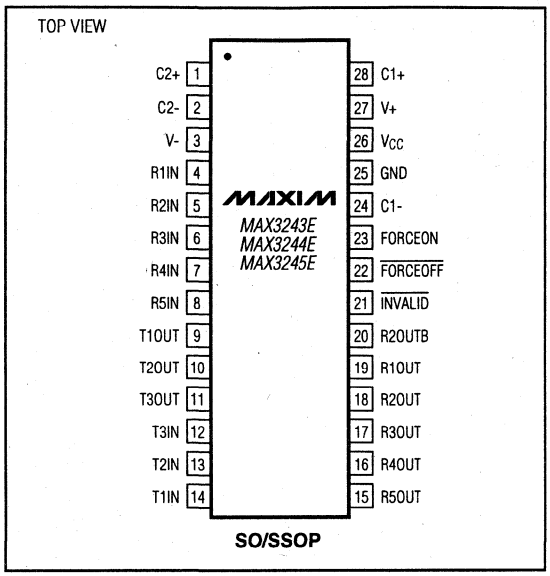
Typical Operating Circuit



*C3 CAN BE RETURNED TO V_{CC} OR GND.

±15kV ESD-Protected, 1µA, 3.0V to 5.5V, 1Mbps RS-232 Transceivers with AutoShutdown Plus

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1335

19-1289; Rev 0; 10/97

MAXIM

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

General Description

The MAX3244/MAX3245 are 3V-powered EIA/TIA-232 and V.28/V.24 communications interfaces with automatic shutdown/wakeup features and high data-rate capabilities.

The transceivers have a proprietary low-dropout transmitter output stage enabling true RS-232 performance from a 3.0V to 5.5V supply with a dual charge pump. The MAX3244 is guaranteed to run at a data rate of 250kbps while maintaining RS-232 output levels. The MAX3245 is guaranteed to run at a data rate of 1Mbps using Maxim's MegaBaud™ feature. The devices are complete serial ports (3 drivers, 5 receivers) intended for notebook or subnotebook computers.

The MAX3244/MAX3245 achieve a 1µA supply current using Maxim's revolutionary AutoShutdown Plus™ feature, which automatically saves power without changes to the existing BIOS or operating system. They shut down after 30sec if the RS-232 cable is disconnected or if the transmitters of the connected peripherals are idle. The devices turn on again when a valid edge is applied to any transmitter or receiver input.

Applications

Notebook, Subnotebook, and Palmtop Computers

Battery-Powered Equipment

Hand-Held Equipment

Peripherals

Printers

Typical Operating Circuit appears at end of data sheet.

AutoShutdown Plus and MegaBaud are trademarks of Maxim Integrated Products.

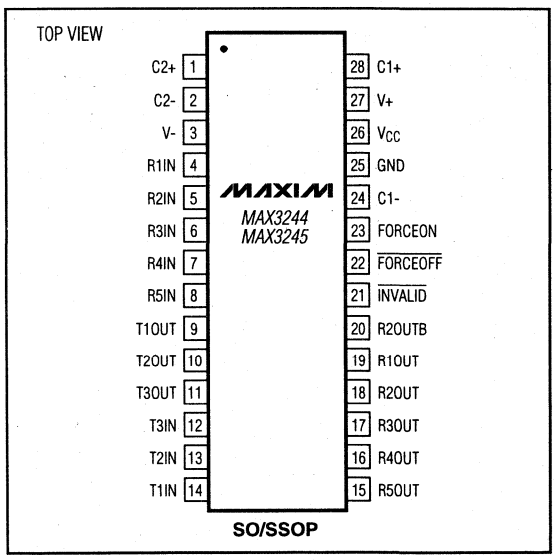
Features

- **1µA Supply Current Achieved with AutoShutdown Plus**
- **Guaranteed Data Rate:**
  250kbps (MAX3244)
  1Mbps (MAX3245)
- **Meets EIA/TIA-232 Specifications Down to 3.0V**
- **Guaranteed Slew Rate:**
  6V/µs (MAX3244)
  24V/µs (MAX3245)
- **Guaranteed Mouse Driveability**
- **Small, 0.1µF Capacitors**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3244CWI	0°C to +70°C	28 SO
MAX3244CAI	0°C to +70°C	28 SSOP
MAX3244EWI	-40°C to +85°C	28 SO
MAX3244EAI	-40°C to +85°C	28 SSOP
MAX3245CWI	0°C to +70°C	28 SO
MAX3245CAI	0°C to +70°C	28 SSOP
MAX3245EWI	-40°C to +85°C	28 SO
MAX3245EAI	-40°C to +85°C	28 SSOP

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... -0.3V to +7V
V- ..... +0.3V to -7V
V+ + |V-| ..... +13V
Input Voltages
  T_IN, FORCEON, $\overline{FORCEOFF}$ ..... -0.3V to +6V
  R_IN ..... ±25V
Output Voltages
  T_OUT ..... ±13.2V
  R_OUT, R2OUTB, $\overline{INVALID}$ ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_OUT (one at a time) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SO (derate 12.5mW/°C above +70°C) 1000mW
  SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges
  MAX324_C_ I ..... 0°C to +70°C
  MAX324_E_ I ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{CC} = 3.3V or 5.0V, T_A = +25°C, no load)						
Supply Current	FORCEON = $\overline{FORCEOFF}$ = V_{CC}			0.3	1.0	mA
Shutdown Supply Current	$\overline{FORCEOFF}$ = GND			1.0	10.0	µA
AutoShutdown Plus Supply Current	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}, all R_IN idle, all T_IN idle			1.0	10.0	µA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_IN, FORCEON, $\overline{FORCEOFF}$				0.8	V
Input Logic Threshold High	T_IN, FORCEON, $\overline{FORCEOFF}$	V_{CC} = 3.3V	2.0			V
		V_{CC} = 5.0V	2.4			
Transmitter Input Hysteresis				0.5		V
Input Leakage Current	T_IN, FORCEON, $\overline{FORCEOFF}$			±0.01	±1.0	µA
Output Leakage Current	Receivers disabled			±0.05	±10	µA
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1.0mA		V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	V_{CC} = 3.3V		0.6	1.1		V
	V_{CC} = 5.0V		0.8	1.4		
Input Threshold High	V_{CC} = 3.3V			1.6	2.4	V
	V_{CC} = 5.0V			1.9	2.4	
Input Hysteresis				0.5		V
Input Resistance	T_A = +25°C		3	5	7	kΩ
TRANSMITTER OUTPUTS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = 0V, transmitter output = ±2V		300	10M		Ω
Output Short-Circuit Current				±35	±60	mA
Output Leakage Current	V_{CC} = 0V to 5.5V, transmitter output = ±12V, transmitters disabled				±25	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MOUSE DRIVEABILITY					
Transmitter Output Voltage	T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to ground, T1OUT and T2OUT loaded with 2.5mA each	±5			V
AUTOSHUTDOWN PLUS (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})					
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage High	Positive threshold			2.7	V
	Negative threshold	-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Voltage Low		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA			0.4	V
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1.0mA	V_{CC} - 0.6			V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High, t_{INVH}	Figure 3		1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low, t_{INVL}	Figure 3		30		µs
Receiver or Transmitter Edge to Transmitters Enabled, t_{WU}	Figure 3		100		µs
Receiver or Transmitter Edge to Transmitters Shut Down, $t_{AUTOSHDN}$	Figure 3	15	30	60	sec

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

TIMING CHARACTERISTICS—MAX3244

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.15		µs
		t_{PLH}		0.15		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			100		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, T_A = +25°C, R_L = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V	C_L = 150pF to 1000pF	6		30	V/µs
		C_L = 150pF to 2500pF	4		30	

TIMING CHARACTERISTICS—MAX3245

(V_{CC} = +3.0V to +5.5V; C1–C4 = 0.1µF, tested at 3.3V ±10%; C1 = 0.047µF, C2–C4 = 0.33µF, tested at 5.0V ±10%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.)

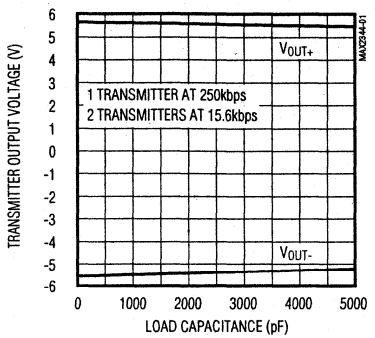
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	R_L = 3kΩ, C_L = 1000pF, one transmitter switching		250			kbps
	V_{CC} = 3.0V to 4.5V, R_L = 3kΩ, C_L = 250pF, one transmitter switching		1000			
	V_{CC} = 4.5V to 5.5V, R_L = 3kΩ, C_L = 1000pF, one transmitter switching		1000			
Receiver Propagation Delay	R_IN to R_OUT, C_L = 150pF	t_{PHL}		0.15		µs
		t_{PLH}		0.15		
Receiver Output Enable Time	Normal operation			200		ns
Receiver Output Disable Time	Normal operation			200		ns
Transmitter Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			25		ns
Receiver Skew	$\lvert t_{PHL} - t_{PLH} \rvert$			50		ns
Transition-Region Slew Rate	V_{CC} = 3.3V, T_A = +25°C, R_L = 3kΩ to 7kΩ, C_L = 150pF to 1000pF, measured from +3V to -3V or -3V to +3V		24		150	V/µs

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

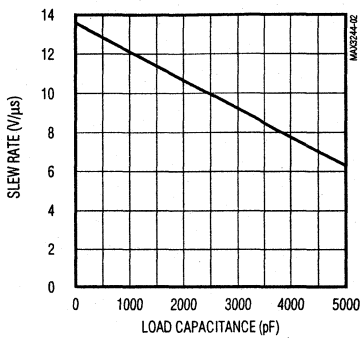
Typical Operating Characteristics

(V_{CC} = +3.3V, 250kbps data rate, 0.1µF capacitors, all transmitters loaded with 3kΩ, T_A = +25°C, unless otherwise noted.)

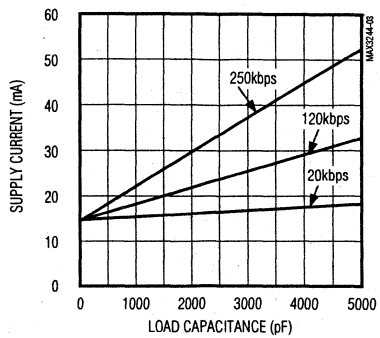
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



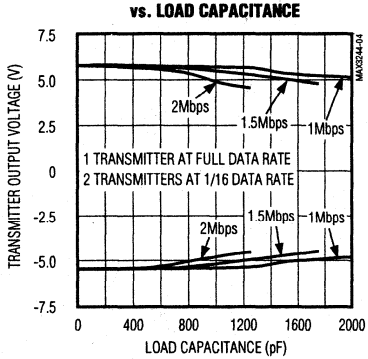
MAX3244 SLEW RATE vs. LOAD CAPACITANCE



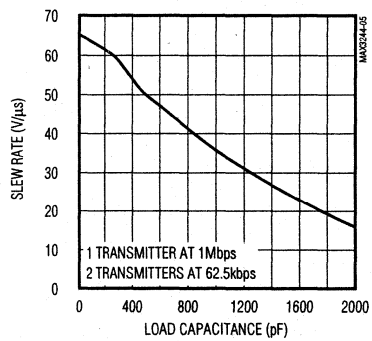
MAX3244 SUPPLY CURRENT vs. LOAD CAPACITANCE



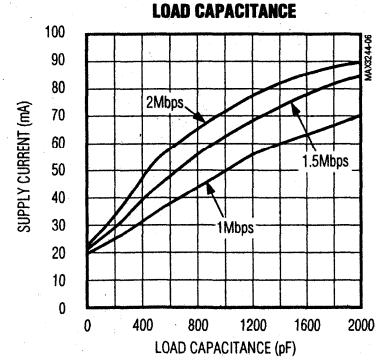
MAX3245 TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



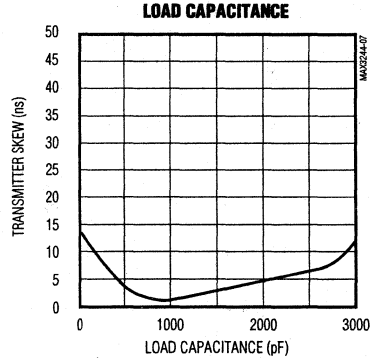
MAX3245 SLEW RATE vs. LOAD CAPACITANCE



MAX3245 SUPPLY CURRENT vs. LOAD CAPACITANCE



MAX3245 TRANSMITTER SKEW vs. LOAD CAPACITANCE



1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

Pin Description

PIN	NAME	FUNCTION
1	C2+	Positive Terminal of Inverting Charge-Pump Capacitor
2	C2-	Negative Terminal of Inverting Charge-Pump Capacitor
3	V-	-5.5V Generated by the Charge Pump
4–8	R1IN–R5IN	RS-232 Receiver Inputs
9, 10, 11	T1OUT, T2OUT, T3OUT	RS-232 Transmitter Outputs
12, 13, 14	T3IN, T2IN, T1IN	TTL/CMOS Transmitter Inputs
15–19	R5OUT–R1OUT	TTL/CMOS Receiver Outputs
20	R2OUTB	Noninverting Complementary Receiver Output, always active
21	$\overline{\text{INVALID}}$	Active-Low Output of the Valid Signal Detector. A logic high indicates that a valid RS-232 level is present on a receiver input.
22	$\overline{\text{FORCEOFF}}$	Active-Low Force-Off Input. Drive low to shut down transmitters, receivers (except R2OUTB), and on-board supply. This overrides AutoShutdown Plus and FORCEON (Table 1).
23	FORCEON	Force-On Input. Drive high to override AutoShutdown Plus, keeping transmitters and receivers on ($\overline{\text{FORCEOFF}}$ must be high) (Table 1).
24	C1-	Negative Terminal of Voltage-Doubler Charge-Pump Capacitor
25	GND	Ground
26	V_{CC}	+3.0V to +5.5V Supply Voltage
27	V+	+5.5V Generated by the Charge Pump
28	C1+	Positive Terminal of Voltage-Doubler Charge-Pump Capacitor

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3244/MAX3245's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump) for input voltages (V_{CC}) over the 3.0V to 5.5V range. The charge pumps operate in a discontinuous mode: if the output voltages are less than 5.5V, the charge pumps are enabled; if the output voltages exceed 5.5V, the charge pumps are disabled. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5.0V EIA/TIA-232 levels. The MAX3244 transmitters guarantee a 250kbps data rate (1Mbps for the MAX3245) with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled to drive multiple receivers.

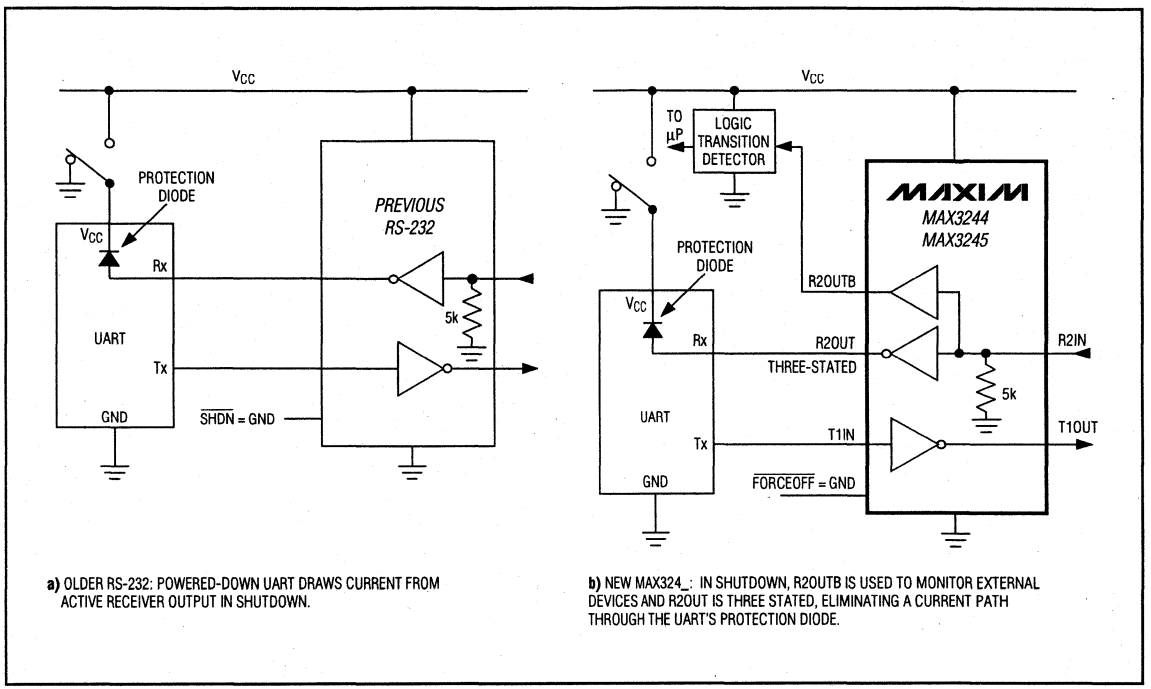
LapLink is a trademark of Traveling Software.

When FORCEON = GND and $\overline{\text{FORCEOFF}}$ = V_{CC}, if the AutoShutdown Plus circuitry does not sense a valid transition on any receiver or transmitter for 30sec, the part shuts down and the transmitter outputs are high impedance.

When powered off or shut down, the MAX3244/MAX3245 permit the outputs to be driven up to ±12V. The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. All receivers have inverting three-state outputs, and can be active or inactive (Table 1). The devices feature an extra, always-active noninverting output, R2OUTB. This allows ring indicator applications to be monitored without forward biasing other devices connected to the receiver outputs. This is ideal for systems where V_{CC} is set to 0V in shutdown to accommodate peripherals, such as UARTs (Figure 1).



a) OLDER RS-232: POWERED-DOWN UART DRAWS CURRENT FROM ACTIVE RECEIVER OUTPUT IN SHUTDOWN.

b) NEW MAX324_: IN SHUTDOWN, R2OUTB IS USED TO MONITOR EXTERNAL DEVICES AND R2OUT IS THREE STATED, ELIMINATING A CURRENT PATH THROUGH THE UART'S PROTECTION DIODE.

Figure 1. Detection of RS-232 Activity when the UART and Interface are Shut Down

Table 1. Output Control Truth Table

FORCEON	$\overline{\text{FORCEOFF}}$	TRANSMITTER OR RECEIVER EDGE WITHIN 30sec	OPERATION STATUS	T_OUT	R_OUT	R2OUTB
X	0	X	Shutdown (Forced Off)	High-Z	High-Z	Active
1	1	X	Normal Operation (Forced On)	Active	Active	Active
0	1	Yes	Normal Operation (AutoShutdown Plus)	Active	Active	Active
0	1	No	Shutdown (AutoShutdown Plus)	High-Z	Active	Active

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

Table 2. $\overline{\text{INVALID}}$ Truth Table

RS-232 SIGNAL PRESENT AT ANY RECEIVER INPUT	$\overline{\text{INVALID}}$ OUTPUT
Yes	H
No	L

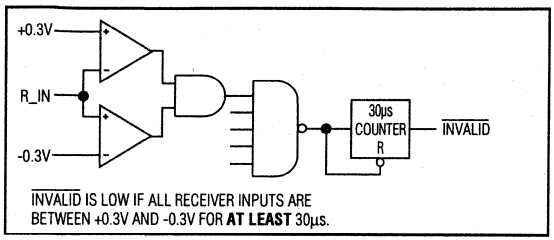


Figure 2a. Invalid Receiver Levels

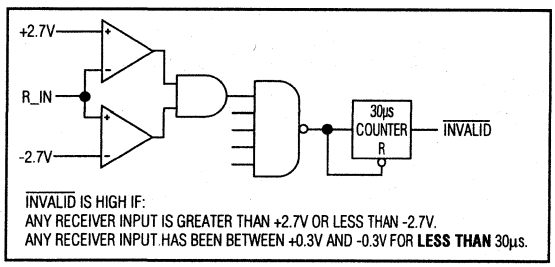


Figure 2b. Valid Receiver Levels

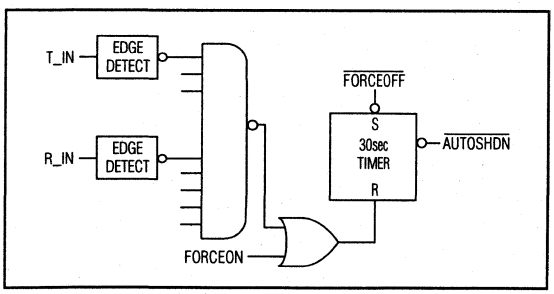


Figure 2c. AutoShutdown Plus Edge Detection

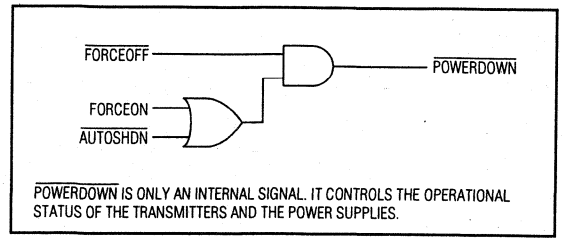


Figure 2d. AutoShutdown Plus Logic

AutoShutdown Plus Mode

The MAX3244/MAX3245 achieve a 1µA supply current with Maxim's AutoShutdown Plus feature, which operates when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. When the MAX3244/MAX3245 do not sense a valid signal transition on any receiver or transmitter input for 30sec, the on-board power supply and drivers are shut off, reducing supply current to 1µA. This occurs if all transmitter and receiver inputs are idle. The system turns on again when a valid transition is applied to any receiver or transmitter input. As a result, the system saves power without changes to the existing BIOS or operating system.

Figures 2a and 2b depict valid and invalid RS-232 receiver levels. $\overline{\text{INVALID}}$ indicates the receiver inputs' condition, and it is independent of the FORCEON and $\overline{\text{FORCEOFF}}$ states. Figure 2 and Tables 1 and 2 summarize the MAX3244/MAX3245 operating modes. FORCEON and $\overline{\text{FORCEOFF}}$ override the AutoShutdown Plus circuitry. When neither control is asserted, the IC selects between these states automatically based on the last receiver or transmitter input edge received. Figure 3 shows a timing diagram for AutoShutdown Plus operation. The time required to exit shutdown is typically 100µs (Figure 4).

When shut down, the device's charge pumps are turned off, V+ is pulled to V_{CC}, V- is pulled to ground, and the transmitter outputs are disabled (high impedance).

By connecting $\overline{\text{INVALID}}$ to FORCEON, the MAX3244/MAX3245 shut down when no valid receiver level and no receiver or transmitter edge is detected for 30sec, and wake up when a valid receiver level or receiver or transmitter edge is detected.

By connecting $\overline{\text{INVALID}}$ to FORCEON and $\overline{\text{FORCEOFF}}$, the MAX3244/MAX3245 shut down when no valid receiver level is detected, and wake up when a valid receiver level is detected.

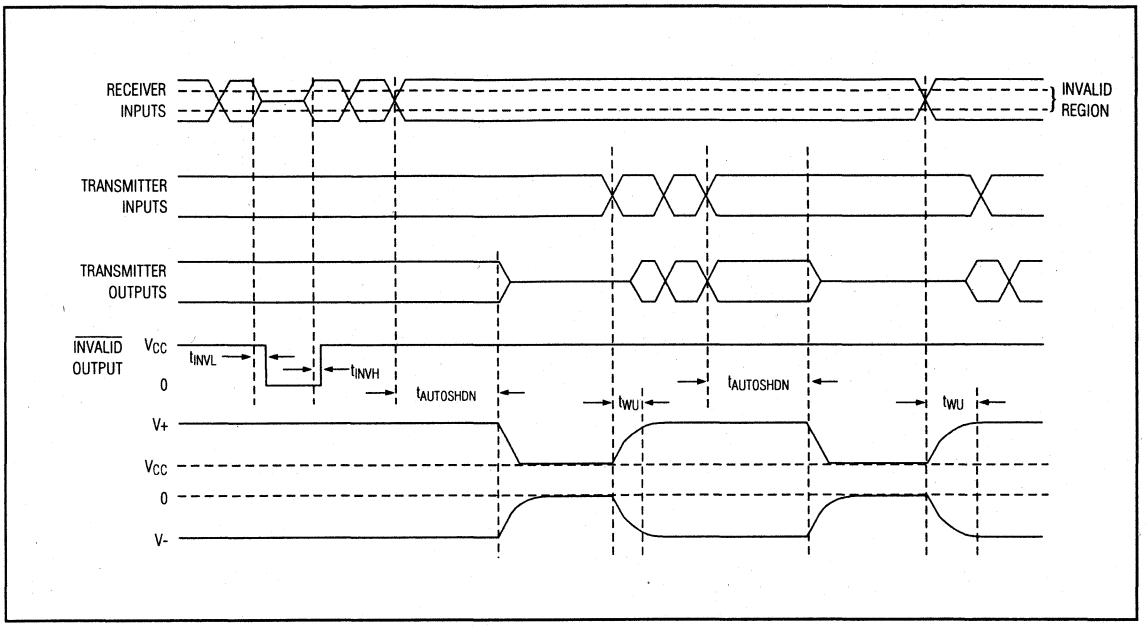


Figure 3. AutoShutdown Plus and INVALID Timing Diagram

Software-Controlled Shutdown

If direct software control is desired, INVALID can be used to indicate DTR or ring indicator signal. Tie FORCEOFF and FORCEON together to bypass AutoShutdown so the line acts like a SHDN input.

Applications Information

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; polarized or nonpolarized capacitors can be used. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. **However, do not increase C1 without also increasing the values of C2, C3, C4, and CBYPASS, to maintain the proper ratios (C1 to the other capacitors).**

Table 3. Required Minimum Capacitance Values

SUPPLY VOLTAGE (V)	C1 (µF)	C2, C3, C4, CBYPASS (µF)
3.0 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3.0 to 5.5	0.1	0.47

When using the minimum required capacitor values, make sure the capacitance value does not degrade excessively with temperature. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple VCC to ground with a capacitor of the same value as reservoir capacitors C2, C3, and C4. Connect the bypass capacitor as close to the IC as possible.

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

Transmitter Outputs when Exiting Shutdown

Figure 4 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs are shown going to opposite RS-232 levels (one transmitter input is high, the other is low). Each transmitter is loaded with 3kΩ in parallel with 1000pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown. Note that the transmitters are enabled only when V- exceeds approximately -3V.

High Data Rates

The MAX3244 maintains the RS-232 ±5.0V minimum transmitter output voltage even at high data rates. Figure 5 shows a transmitter loopback test circuit. Figure 6 shows a loopback test result at 120kbps, and Figure 7 shows the same test at 250kbps. For Figure 6, all transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 7, a single transmitter was driven at 250kbps, and all transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

The MAX3245 maintains the RS-232 ±5.0V minimum transmitter output voltage with data rates up to 1Mbps (MegaBaud). Figure 8 shows a loopback test result with a single transmitter driven at 1Mbps, and all transmitters loaded with an RS-232 receiver in parallel with 250pF.

Interconnection with 3V and 5V Logic

The MAX3244/MAX3245 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

Mouse Driveability

The MAX3244/MAX3245 have been specifically designed to power serial mice while operating from low-voltage power supplies. They have been tested with leading mouse brands from manufacturers such as Microsoft and Logitech. The MAX3244/MAX3245 successfully drove all serial mice tested and met their respective current and voltage requirements. Figure 9a shows the transmitter outputs under increasing load current. The MAX3244/MAX3245 switching regulator ensures the transmitters will supply at least ±5V under worst-case conditions. Figure 9b shows a typical mouse connection.

The AutoShutdown Plus feature does not work with a mouse; connect FORCEON and $\overline{\text{FORCEOFF}}$ to V_{CC}.

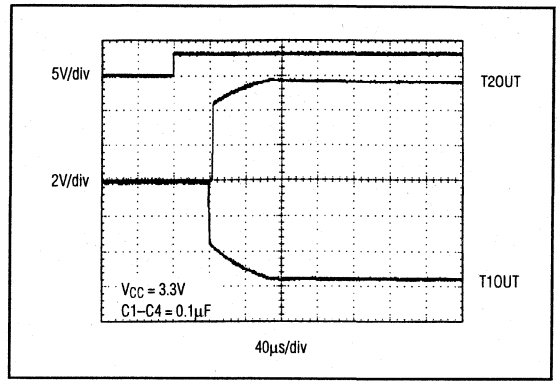


Figure 4. Transmitter Outputs Exiting Shutdown or Powering Up

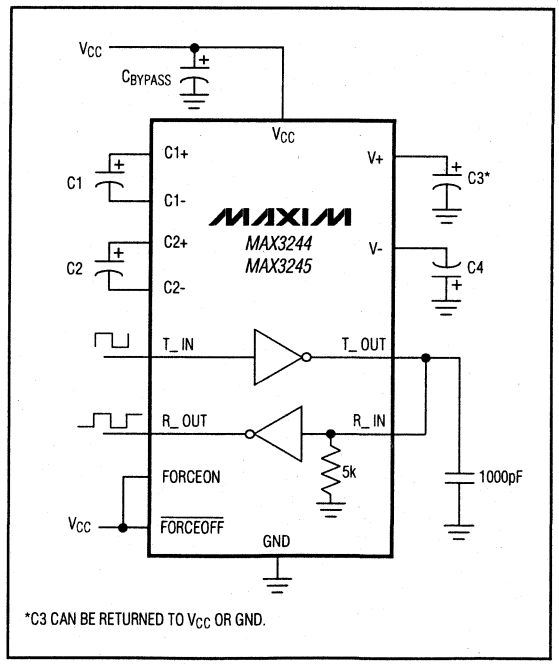


Figure 5. Loopback Test Circuit

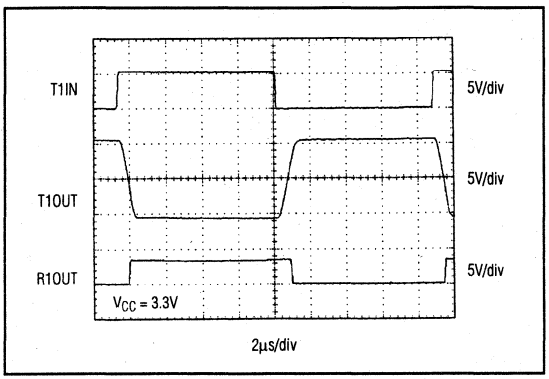


Figure 6. MAX3244 Loopback Test Result at 120kbps

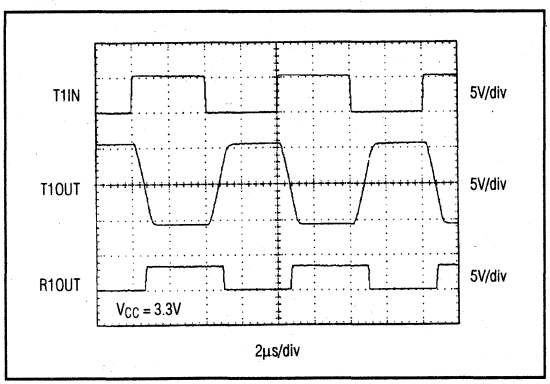


Figure 7. MAX3244 Loopback Test Result at 250kbps

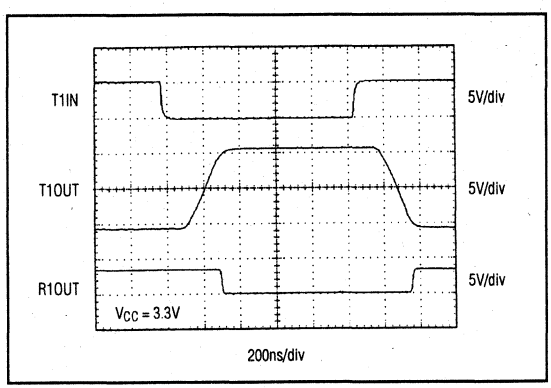


Figure 8. MAX3245 Loopback Test Result at 1Mbps

Table 4. Logic Family Compatibility with Various Supply Voltages

SYSTEM POWER-SUPPLY VOLTAGE (V)	VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families.
5	5	Compatible with all TTL and CMOS families
5	3.3	Compatible with ACT and HCT CMOS, and with AC, HC, or CD4000 CMOS.

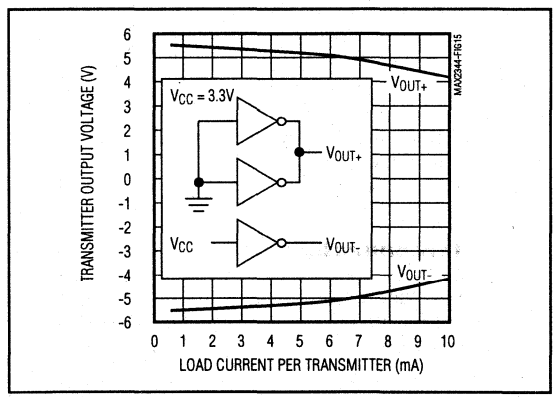


Figure 9a. MAX324_ Transmitter Output Voltage vs. Load Current per Transmitter

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

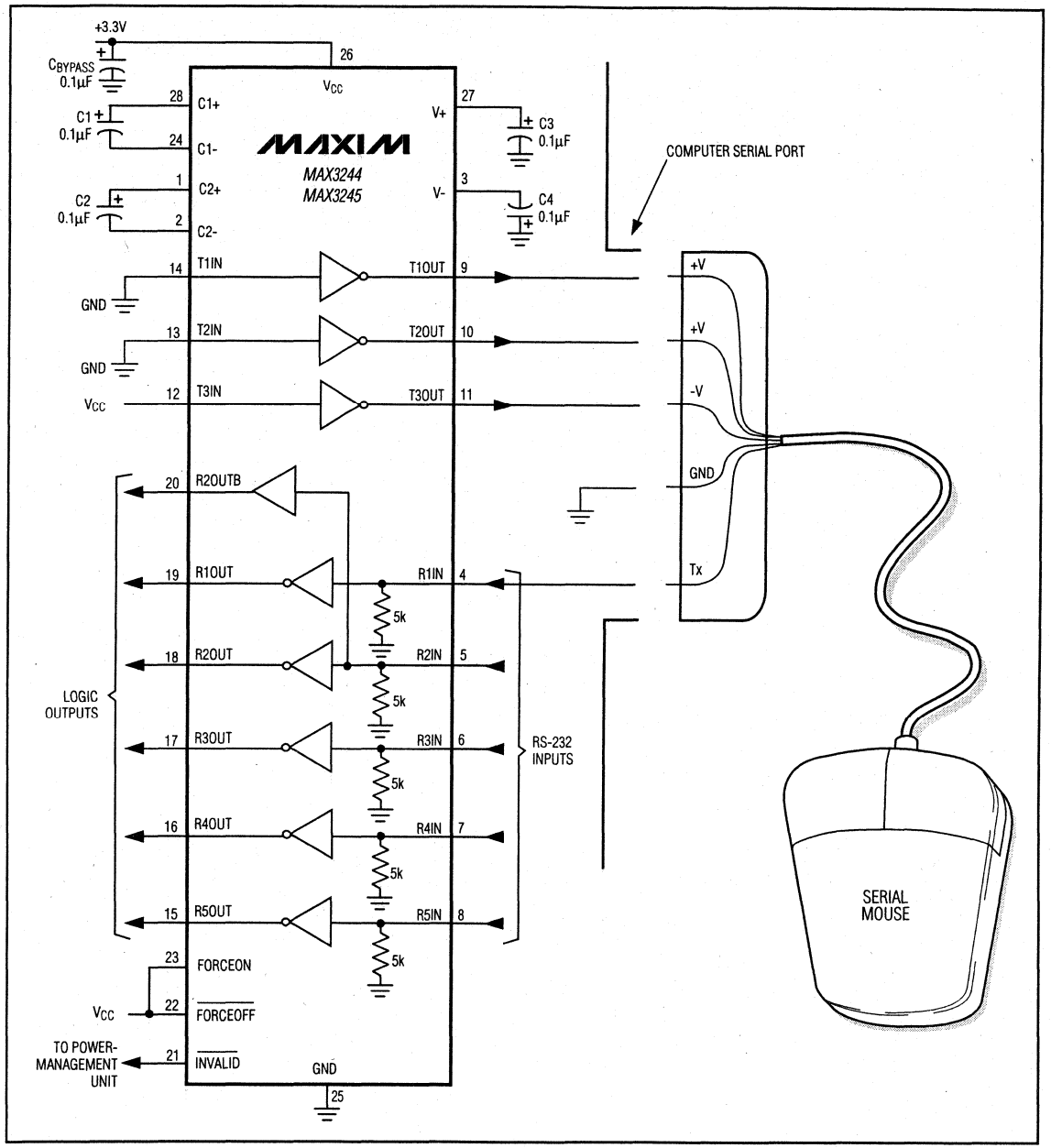
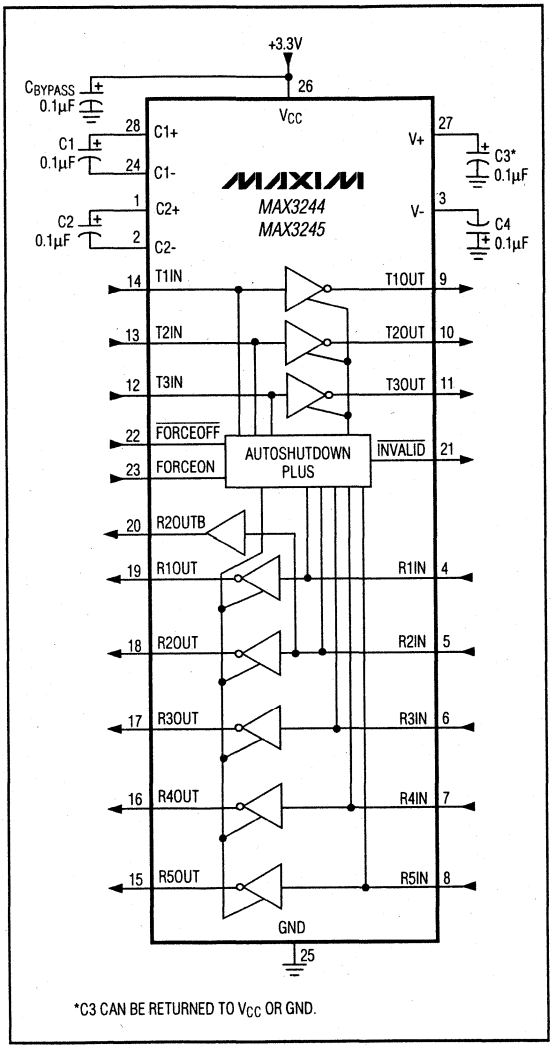


Figure 9b. Mouse Driver Test Circuit

1µA Supply Current, 3.0V to 5.5V, 1Mbps RS-232 Transceiver with AutoShutdown Plus

Typical Operating Circuit



*C3 CAN BE RETURNED TO V_{CC} OR GND.

Chip Information

TRANSISTOR COUNT: 1335

19-1253; Rev 0; 8/97

MAXIM

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

General Description

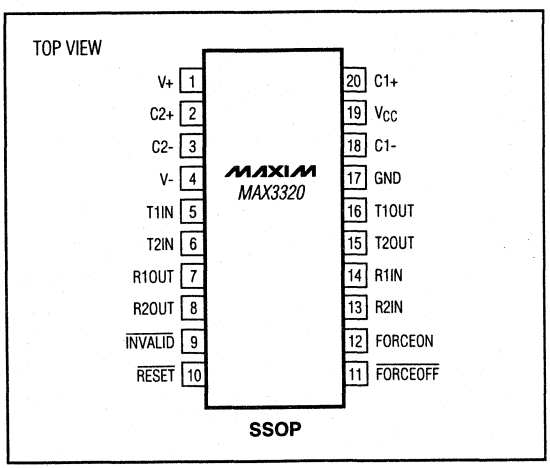
The MAX3320 combines a microprocessor (µP) supervisory circuit with an RS-232 transceiver. The power-on reset performs a single function: it asserts a reset signal whenever the VCC supply voltage declines below a preset threshold, staying asserted for at least 100ms after VCC rises above the reset threshold. The MAX3320 has an active-low $\overline{RESET}$ output, which is guaranteed to be in the correct state for VCC down to 1V. The reset comparator is designed to ignore fast transients on VCC. Reset thresholds suitable for operation with a variety of supply voltages are available.

The MAX3320 transceivers have a proprietary low-dropout transmitter output stage, enabling true RS-232 performance with a dual charge pump powered from a +3V to +5.5V supply. The device requires only four small 0.1µF external charge-pump capacitors, and is guaranteed to run at data rates of up to 250kbps. It comes in the space-saving 20-pin SSOP package.

Applications

Palmtop Computers
Portable/Battery-Powered Equipment
Hand-Held Equipment
Peripherals
Printers

Pin Configuration



Features

- **Precise Monitoring of 5V and 3.3V Power-Supply Voltages:**
  - **— 100ms (min) Power-On $\overline{RESET}$ Pulse Width**
  - **— Power-Supply Transient Immunity**
  - **— Guaranteed $\overline{RESET}$ Valid to VCC = 1V**
- **4µA Supply Current Achieved with AutoShutdown Plus**
- **Receivers Always Active**
- **Power-On Reset Always Active**
- **4µA Low-Power Shutdown**
- **250kbps Guaranteed Data Rate**

Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX3320_CAP	0°C to +70°C	20 SSOP
MAX3320_EAP	-40°C to +85°C	20 SSOP

* *This part offers a choice of reset threshold voltage. From the table below, select the suffix corresponding to the desired threshold and insert it into the blank to complete the part number.*

SUFFIX	RESET THRESHOLD (V)
A	4.25
B	2.85
L	4.63
T	3.08

Typical Operating Circuit appears at end of data sheet.

AutoShutdown Plus is a trademark of Maxim Integrated Products.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to 6V
V+ (Note 1) ..... -0.3V to 7V
V- (Note 1) ..... 0.3V to -7V
V+ + |V-| (Note 1) 13V
Input Voltages
  T_IN, $\overline{FORCEOFF}$, FORCEON ..... -0.3V to 6V
  R_IN ..... ±25V
Output Voltages
  T_OUT ..... ±13.2V
  R_OUT, $\overline{INVALID}$, $\overline{RESET}$ ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
  T_OUT ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
  SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
  MAX3320_CAP ..... 0°C to +70°C
  MAX3320_EAP ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: V+ and V- can have a magnitude of +7V (max), but their absolute difference cannot exceed +13V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V to 5.5V, C1–C4 = 0.1µF (tested at 3.3V ±10%), C1 = 0.047µF, C2–C4 = 0.33µF (tested at 5V ±10%), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Power-Supply Current	No load, V_{CC} = 3.3V or 5V, T_A = +25°C			0.45	1.0	mA
Shutdown Supply Current	$\overline{FORCEOFF}$ = GND, T_A = +25°C			4.0	10	µA
AutoShutdown Plus Supply Current	All R_IN unconnected, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}, all T_IN = V_{CC} or GND, T_A = +25°C			4.0	10	µA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold Low	T_IN, FORCEON, $\overline{FORCEOFF}$				0.8	V
Input Logic Threshold High	T_IN, FORCEON, $\overline{FORCEOFF}$	V_{CC} = 3.3V	2.0			V
		V_{CC} = 5V	2.4			
Input Leakage Current	T_IN, FORCEON, $\overline{FORCEOFF}$			±0.01	±1.0	µA
Input Hysteresis	T_IN, FORCEON, $\overline{FORCEOFF}$			250		mV
Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
Output Voltage High	I_{OUT} = -1mA		V_{CC} - 0.6	V_{CC} - 0.1		V
RECEIVER INPUTS						
Input Voltage Range			-25		25	V
Input Threshold Low	V_{CC} = 3.3V		0.6	1.2		V
	V_{CC} = 5V		0.8	1.5		
Input Threshold High	V_{CC} = 3.3V			1.5	2.4	V
	V_{CC} = 5V			1.8	2.4	
Input Hysteresis				0.3		V
Input Resistance	T_A = +25°C		3	5	7	kΩ
$\overline{INVALID}$ OUTPUT						
Receiver Input Threshold to $\overline{INVALID}$ Output High	Figure 3, positive threshold				2.7	V
	Figure 3, negative threshold		-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Low	Figure 3		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low	I_{OUT} = 1.6mA				0.4	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 5.5V, C1–C4 = 0.1µF (tested at 3.3V ±10%), C1 = 0.047µF, C2–C4 = 0.33µF (tested at 5V ±10%), T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{INVALID}$ Output Voltage High	I_{OUT} = -1mA	V_{CC} - 0.6			V
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High	Figure 3		0.1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low	Figure 3		90		µs
AUTOSHUTDOWN PLUS (FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC})					
Receiver or Transmitter Edge to Transmitters Enabled	Figure 5		25		µs
Receiver or Transmitter Edge to Shutdown	Figure 3	15	30	60	sec
TRANSMITTER OUTPUTS					
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5.0	±5.4		V
Output Resistance	V_{CC} = V+ = V- = GND, V_{T_OUT} = ±2V	300	10M		Ω
Output Short-Circuit Current	T_OUT = GND, T_IN = V_{CC} or GND		±35	±60	mA
Output Leakage Current	V_{T_OUT} = ±12V, V_{CC} = 0 to 5.5V, transmitters disabled			±25	µA
$\overline{RESET}$ OUTPUT					
$\overline{RESET}$ Operating Voltage Range	MAX3320_C	1.0		5.5	V
	MAX3320_E	1.2		5.5	
$\overline{RESET}$ Threshold	MAX3320A	4.00	4.25	4.50	V
	MAX3320B	2.70	2.85	3.00	
	MAX3320L	4.50	4.63	4.75	
	MAX3320T	3.00	3.08	3.15	
$\overline{RESET}$ Output Voltage	I_{SINK} = 1.2mA, V_{CC} = reset threshold, MAX3320B/T			0.3	V
	I_{SINK} = 3.2mA, V_{CC} = reset threshold, MAX3320A/L			0.4	
	I_{SINK} = 50µA, V_{CC} > 1V, MAX3320_C			0.3	
	I_{SINK} = 100µA, V_{CC} > 1.2V, MAX3320_E			0.4	

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

TIMING CHARACTERISTICS

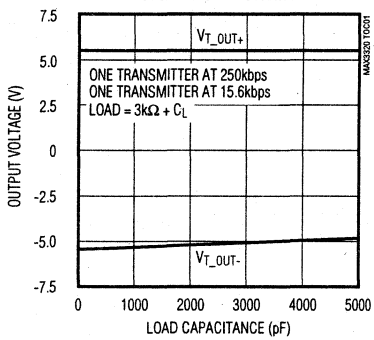
(VCC = 3V to 5.5V, C1–C4 = 0.1µF, C1–C4 = 0.1µF (for 3.3V ±10%), C1 = 0.047µF, C2–C4 = 0.33µF (tested at 5V ±10%), TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Data Rate	RL = 3kΩ, CL = 1000pF, one transmitter switching		250			kbps
Receiver Propagation Delay	R_IN to R_OUT, CL = 150pF	tPHL		0.3		µs
		tPLH		0.3		
Transmitter Skew	| tPHL - tPLH |			100		ns
Receiver Skew	| tPHL - tPLH |			200		ns
Transition-Region Slew Rate	VCC = 3.3V, RL = 3kΩ to 7kΩ, measured from +3V to -3V or -3V to +3V, TA = +25°C	CL = 150pF to 1000pf	6		30	V/µs
		CL = 150pF to 2500pf	4		30	
VCC to $\overline{\text{RESET}}$ Delay	100mV overdrive from reset threshold			40		µs
$\overline{\text{RESET}}$ Active Timeout Period	VCC = reset threshold		100		280	ms

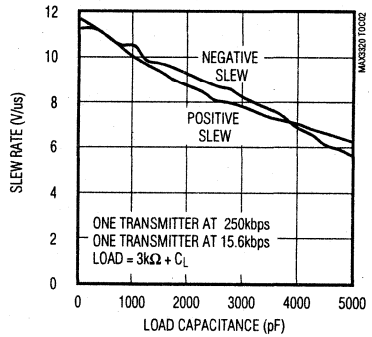
Typical Operating Characteristics

(VCC = 3.3V, 250kbps data rate, C1–C4 = 0.1µF, all transmitters loaded with 3kΩ. Typical values are at TA = +25°C, unless otherwise noted.)

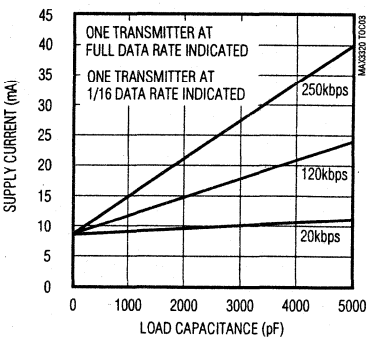
TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE



SLEW RATE vs. LOAD CAPACITANCE



SUPPLY CURRENT vs. LOAD CAPACITANCE WHEN TRANSMITTING DATA

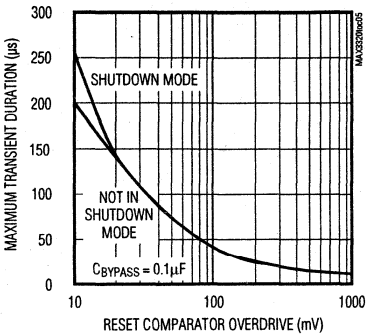


3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

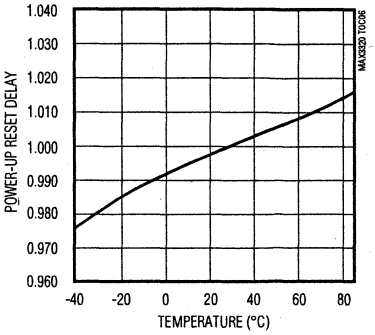
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, 250kbps data rate, C1–C4 = 0.1µF, all transmitters loaded with 3kΩ. Typical values are at T_A = +25°C, unless otherwise noted.)

MAXIMUM TRANSIENT DURATION vs. RESET COMPARATOR OVERDRIVE



NORMALIZED POWER-UP RESET DELAY vs. TEMPERATURE



Pin Description

2

PIN	NAME	FUNCTION
1	V+	5.5V generated by the charge pump
2	C2+	Positive terminal of inverting charge-pump capacitor
3	C2-	Negative terminal of inverting charge-pump capacitor
4	V-	-5.5V generated by the charge pump
5, 6	T_IN	TTL/CMOS Transmitter Inputs (T1IN and T2IN)
7, 8	R_OUT	TTL/CMOS Receiver Outputs (R1OUT and R2OUT)
9	$\overline{\text{INVALID}}$	Output of the Valid Signal Detector. Asserts when no valid RS-232 levels are present on any of the receiver inputs for 90µs.
10	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$ Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold, and for 280ms (max) after V_{CC} rises above the reset threshold.
11	$\overline{\text{FORCEOFF}}$	Force-Off Input. Drive $\overline{\text{FORCEOFF}}$ low to shut down transmitters and on-board power supply. This overrides AutoShutdown Plus and FORCEON (Table 1).
12	FORCEON	Force-On Input. Drive FORCEON high to override AutoShutdown Plus, keeping transmitters on ($\overline{\text{FORCEOFF}}$ must be high) (Table 1).
13, 14	R_IN	RS-232 Receiver Inputs (R2IN and R1IN)
15, 16	T_OUT	RS-232 Transmitter Outputs (T2OUT and T1OUT)
17	GND	Ground
18	C1-	Negative terminal of voltage-doubler charge-pump capacitor
19	V_{CC}	+3V to +5.5V Supply Voltage
20	C1+	Positive terminal of voltage-doubler charge-pump capacitor

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

Table 1. MAX3320 Output Control Truth Table

FORCEON	$\overline{\text{FORCEOFF}}$	AUTOSHUTDOWN PLUS*	OPERATION STATUS	T_OUT	R_OUT
X	0	X	Shutdown (forced off)	High-Z	Active
1	1	X	Normal operation (forced on)	Active	Active
0	1	<30sec*	Normal operation (AutoShutdown Plus)	Active	Active
0	1	>30sec*	Shutdown (AutoShutdown Plus)	High-Z	Active

X = Don't Care
**Time since last receiver or transmitter input activity*

Detailed Description

Dual Charge-Pump Voltage Converter

The MAX3320's internal power supply consists of a regulated dual charge pump that provides output voltages of +5.5V (doubling charge pump) and -5.5V (inverting charge pump) while V_{CC} remains in the 3V to 5.5V range. The charge pumps operate in discontinuous mode; they are enabled if the output voltages are less than 5.5V, and disabled if output voltages exceed 5.5V. Each charge pump requires a flying capacitor (C1, C2) and a reservoir capacitor (C3, C4) to generate the V+ and V- supplies.

RS-232 Transmitters

The transmitters are inverting level translators that convert CMOS-logic levels to 5V EIA/TIA-232 levels. The MAX3320 transmitters guarantee a 250kbps data rate with worst-case loads of 3kΩ in parallel with 1000pF, providing compatibility with PC-to-PC communication software (such as LapLink™). Transmitters can be paralleled to drive multiple receivers. Figure 1 shows a complete system connection.

When $\overline{\text{FORCEOFF}}$ is driven to ground, the transmitter's outputs become high impedance. When the AutoShutdown Plus circuitry senses that all receiver and transmitter inputs are inactive for more than 30sec, the transmitters turn off and the outputs go into a high-impedance state, but the receivers remain active. When the power is off or the MAX3320 is shut down, outputs may be driven up to ±12V.

The transmitter inputs do not have pull-up resistors. Connect unused inputs to GND or V_{CC}.

Laplink is a trademark of Traveling Software.

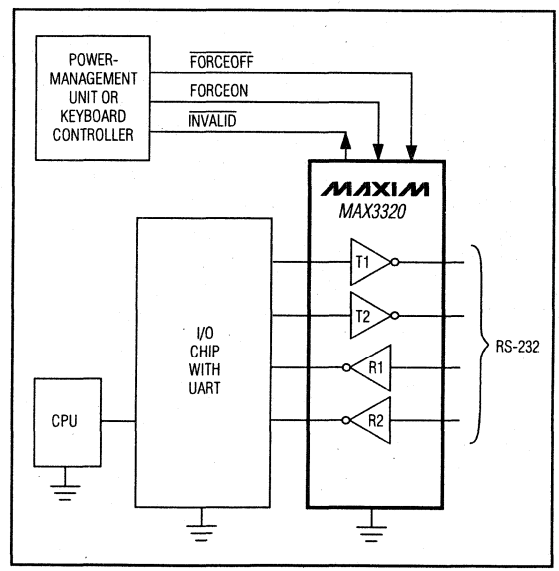


Figure 1. Interface Under Control of PMU

RS-232 Receivers

The receivers convert RS-232 signals to CMOS-logic output levels. All receivers have inverting outputs and are active in shutdown $\overline{\text{FORCEOFF}}$ (Table 1).

AutoShutdown Plus Mode

Maxim's AutoShutdown Plus feature, which operates when $\overline{\text{FORCEOFF}}$ is high and FORCEON is low, achieves a 4µA supply current. When the MAX3320 senses no valid signal levels on all receiver and transmitter inputs for 30sec, the on-board power supply and drivers shut off,

reducing supply current to 4µA. This occurs if the RS-232 cable is disconnected or the connected peripheral transmitters turn off. The system turns on again when a valid transition occurs at any RS-232 receiver or transmitter input. As a result, the system saves power without changes to the existing BIOS or operating system. The $\overline{\text{INVALID}}$ output is high when the receivers are active. Since $\overline{\text{INVALID}}$ indicates the receiver inputs' condition, it can be used in any mode (Figure 2).

Tables 1 and 2 and Figure 2 summarize the MAX3320's operating modes. FORCEON and $\overline{\text{FORCEOFF}}$ override the automatic circuitry and force the transceiver into its normal operating state or into its low-power standby state. When neither control is asserted, the IC enters AutoShutdown Plus mode and selects between these states automatically, based on the last receiver or transmitter input edge received.

When shut down, the device's charge pumps turn off, V+ decays to V_{CC}, V- decays to ground, and the transmitter outputs turn off (high impedance). The time required to exit shutdown is typically 25µs (Figure 3a).

Software-Controlled Shutdown

If direct software control is desired, use $\overline{\text{INVALID}}$ to indicate DTR or Ring Indicator signal. Connect $\overline{\text{FORCEOFF}}$ and FORCEON together to bypass the AutoShutdown Plus feature so the line acts like a $\overline{\text{SHDN}}$ input.

Power-On Reset

In addition to issuing a reset to the microprocessor (µP) during power-up, power-down, and brownout conditions, the MAX3320 is relatively immune to short-duration, negative-going V_{CC} transitions (glitches). Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts 20µs or less does not cause a reset pulse (see *Typical Operating Characteristics*). Additional bypass capacitance mounted as close as possible to the V_{CC} pin provides additional transient immunity.

Table 2. $\overline{\text{INVALID}}$ Truth Table

RS-232 SIGNAL PRESENT AT RECEIVER INPUT	$\overline{\text{INVALID}}$ OUTPUT
Yes	H
No	L

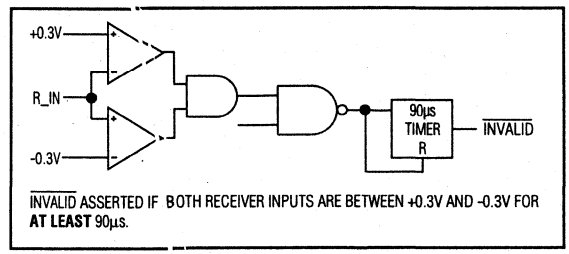


Figure 2a. INVALID Functional Diagram, $\overline{\text{INVALID}}$ Low

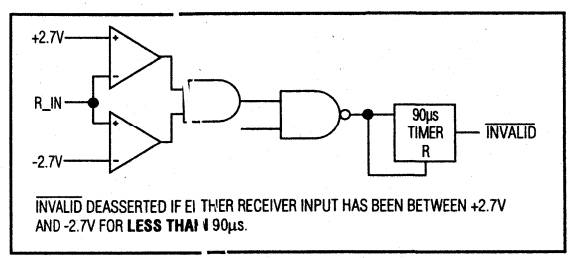


Figure 2b. $\overline{\text{INVALID}}$ Functional Diagram, $\overline{\text{INVALID}}$ High

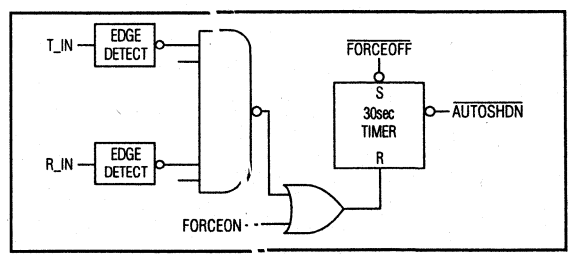


Figure 2c. AutoShutdown Plus Logic

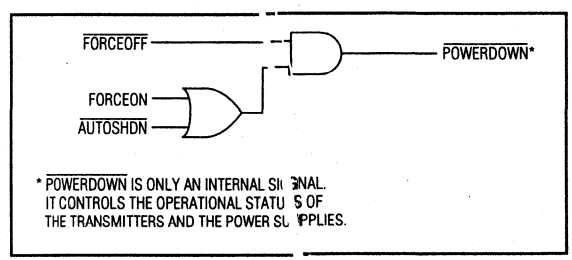


Figure 2d. Power-Down Logic

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

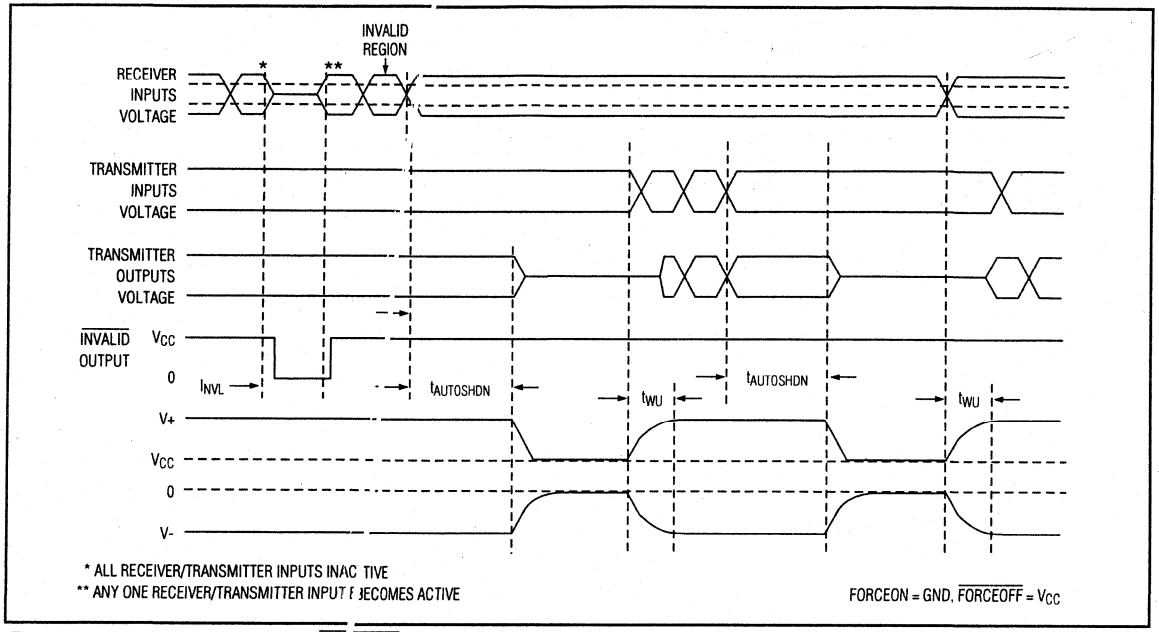


Figure 3a. AutoShutdown Plus and INVALID Timing Diagram

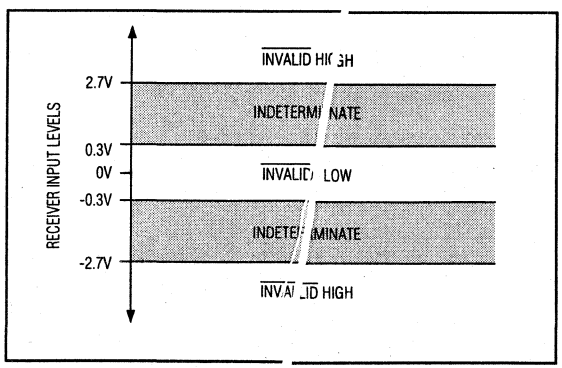


Figure 3b. Receiver Positive/Negative Thresholds for INVALID

Applications Information

Ensuring a Valid Reset Output Down to VCC = 0V

When VCC falls below 1V, RESET no longer sinks current: it becomes an open circuit. Therefore, high-impedance CMOS logic inputs connected to RESET can drift to undefined voltages. This presents no problem in most applications, since most µPs and other circuitry is inoperative with VCC below 1V. However, in applications where RESET must be valid down to 0V, add a pull-down resistor to ground, holding RESET low (Figure 4). R1's value is not critical; 100kΩ is large enough not to load RESET, and small enough to pull it to ground.

Capacitor Selection

The capacitor type used for C1–C4 is not critical for proper operation; use either polarized or nonpolarized capacitors. The charge pump requires 0.1µF capacitors for 3.3V operation. For other supply voltages, refer to Table 3 for required capacitor values. Do not use values smaller than those listed in Table 3. Increasing the capacitor values (e.g., by a factor of 2) reduces ripple on the transmitter outputs and slightly reduces power consumption. C2, C3, and C4 can be increased without changing C1's value. **However, do not increase C1 without also increasing the values of C2, C3, C4, and CBYPASS, to maintain the proper ratios (C1 to the other capacitors).**

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

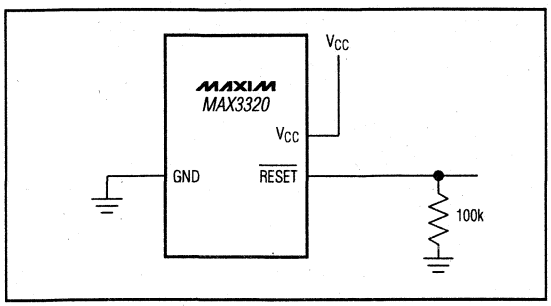


Figure 4. Ensuring $\overline{RESET}$ Valid to V_{CC} = 0V

When using the minimum required capacitor values, make sure the capacitor value does not degrade excessively with temperatures outside the 0°C to +70°C range. If in doubt, use capacitors with a larger nominal value. The capacitor's equivalent series resistance (ESR), which usually rises at low temperatures, influences the amount of ripple on V+ and V-.

Transmitter Outputs when Exiting Shutdown

Figure 5 shows two transmitter outputs when exiting shutdown mode. As they become active, the two transmitter outputs go to opposite RS-232 levels (one transmitter input is high; the other is low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they exit shutdown. Note that the transmitters are enabled only when the magnitude of V- exceeds approximately 3V.

High Data Rates

The MAX3320 maintains the RS-232 ±5V minimum transmitter output voltage even at high data rates. Figure 6 shows a transmitter loop-back test circuit. Figure 7 shows a loop-back test result at 120kbps, and Figure 8 shows the same test at 250kbps. For Figure 7, both transmitters were driven simultaneously at 120kbps into RS-232 loads in parallel with 1000pF. For Figure 8, a single transmitter was driven at 250kbps, and both transmitters were loaded with an RS-232 receiver in parallel with 1000pF.

Interconnection with 3V and 5V Logic

The MAX3320 can directly interface with various 5V logic families, including ACT and HCT CMOS. See Table 4 for more information on possible combinations of interconnections.

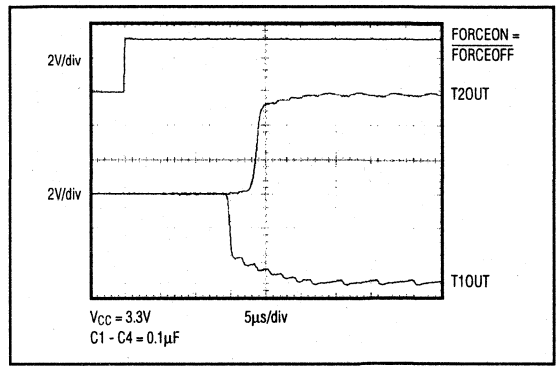


Figure 5. Transmitter Outputs when Exiting Shutdown or Powering Up

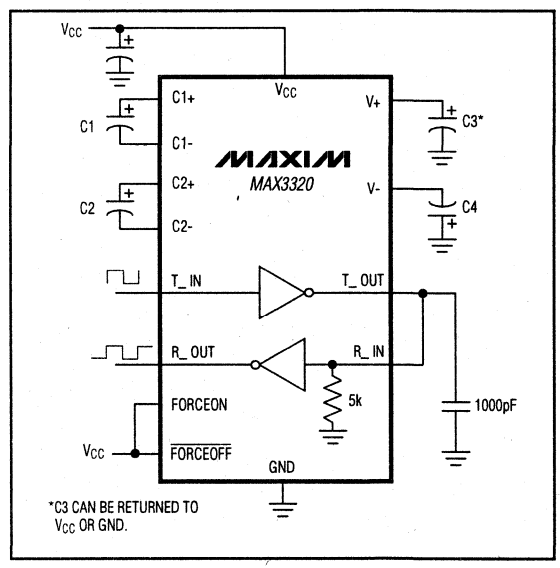


Figure 6. Loop-Back Test Circuit

Table 3. Required Minimum Capacitance Values

V_{CC} (V)	C1 (µF)	C2, C3, C4, C_{BYPASS} (µF)
3 to 3.6	0.1	0.1
4.5 to 5.5	0.047	0.33
3 to 5.5	0.1	0.47

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

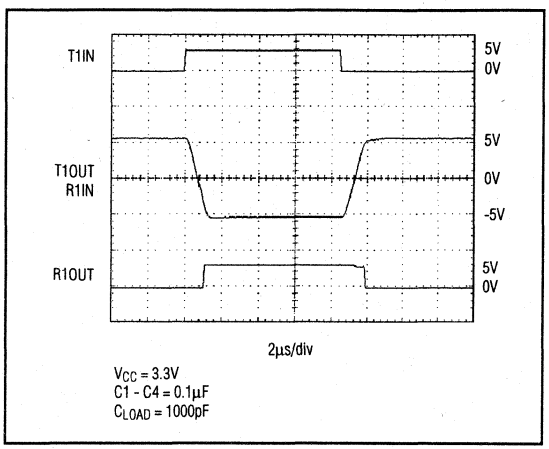


Figure 7. Loop-Back Test Result at 120kbps

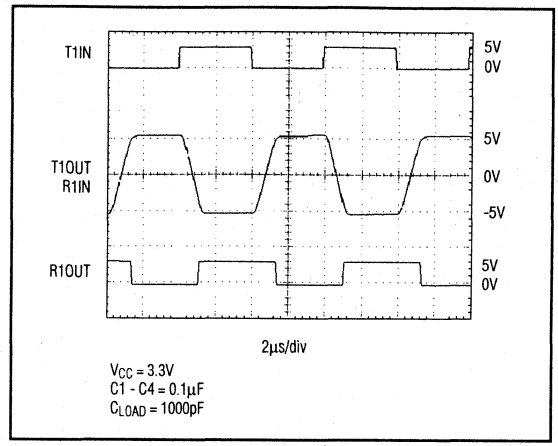


Figure 8. Loop-Back Test Result at 250kbps

Table 4. Logic-Family Compatibility with Various Supply Voltages

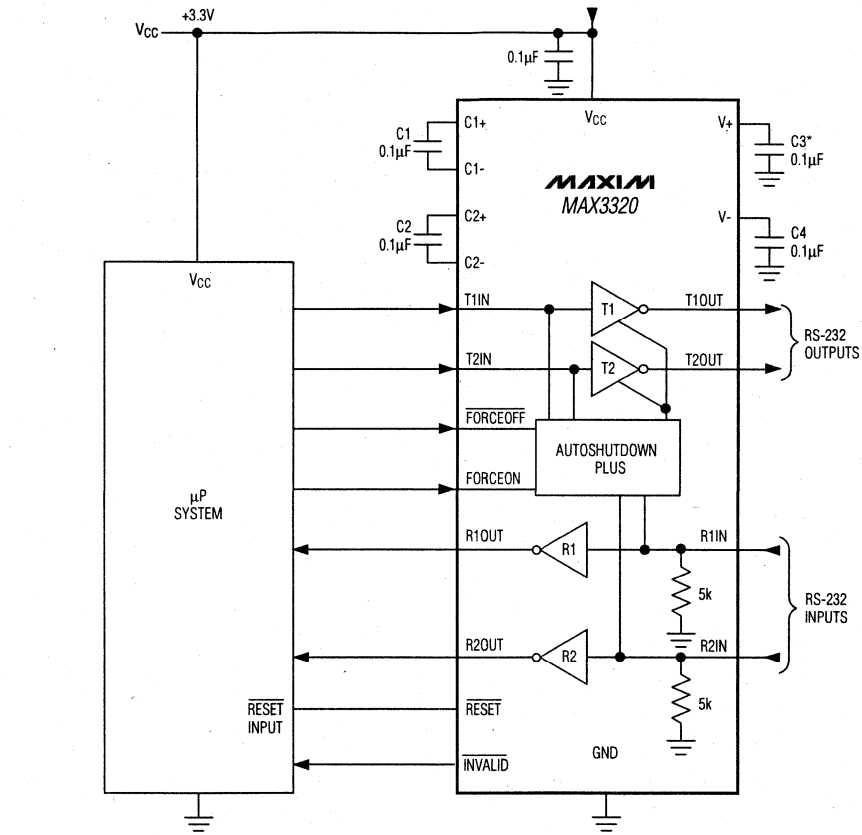
SYSTEM POWER-SUPPLY VOLTAGE (V)	VCC SUPPLY VOLTAGE (V)	COMPATIBILITY
3.3	3.3	Compatible with all CMOS families
5	5	Compatible with all TTL and CMOS families
5	3.3	Compatible with ACT and HCT CMOS, and with AC, HC, or CD4000 CMOS

Chip Information

TRANSISTOR COUNT: 1577

3V to 5.5V, up to 250kbps True RS-232 Transceiver with 4µA AutoShutdown Plus and Power-On Reset

Typical Operating Circuit



*C3 MAY BE RETURNED TO EITHER VCC OR GND.

MAXIM

Op Amps/Comparators

Op Amps/Comparators, Product Tables and Trees 3-3

MAX961 Single, High-Speed, 3V/5V, Rail-to-Rail Comparator 3-11
MAX962 Dual, High-Speed, 3V/5V, Rail-to-Rail, Single-Supply Comparator 3-11
MAX963 Ultra-High Speed, 3V/5V, Rail-to-Rail, Single-Supply Dual Comparator with Complementary Outputs, Shutdown, and Latch Enable 3-11
MAX964 Ultra-High Speed, 3V/5V, Rail-to-Rail, Single-Supply Quad Comparator with Shutdown 3-11
MAX965 Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference 3-21
MAX966 Dual, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator 3-21
MAX967 Dual, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference 3-21
MAX968 Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator with Internal Reference 3-21
MAX969 Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator 3-21
MAX970 Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparator 3-21
MAX976 Dual, High-Speed, Low-Power, 3V/5V Rail-to-Rail Comparator in 8-Pin µMAX 3-33*
MAX978 Quad, High-Speed, Low-Power, 3V/5V Rail-to-Rail Comparator 3-33*
MAX985 Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparator with Push/Pull Outputs 3-35
MAX986 Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparator with Open-Drain Outputs 3-35
MAX987 High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparator 3-45
MAX988 High-Speed, MIcropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparator with Open-Drain Output Stage 3-45
MAX989 Dual, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Push/Pull Output Stage 3-35
MAX990 Dual, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output Stage 3-35
MAX991 Dual, High-Speed, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator 3-45
MAX992 Dual, High-Speed, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output Stage 3-45
MAX993 Quad, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Push/Pull Output Stage 3-35
MAX994 Quad, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output Stage 3-35
MAX995 Quad, High-Speed, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator 3-45
MAX996 Quad, High-Speed, Micropower, Low-Voltage, Rail-to-Rail I/O Comparator with Open-Drain Output Stage 3-45
MAX997 3V/5V, High-Speed, Rail-to-Rail, 6-Pin SOT23 Comparator with Shutdown 3-57*
MAX998 High-Speed, Low-Power, 3V/5V, Rail-to-Rail Comparator with Shutdown 3-33*
MAX999 3V/5V, High-Speed, Rail-to-Rail, 5-Pin SOT23 Comparator 3-57*
MAX4162 SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp 3-59
MAX4163 Dual, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp in µMAX 3-59
MAX4164 Quad, Micropower, Single-Supply, Rail-to-Rail I/O Op Amp in µMAX 3-59
MAX4165 High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp 3-71
MAX4166 High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown 3-71
MAX4167 High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Dual Op Amp 3-71
MAX4168 High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Dual Op Amp with Shutdown 3-71

*Advance Information–first page of a data sheet in preparation.

Op Amps/Comparators (continued)

MAX4169	High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Quad Op Amp	3-71
MAX4172	Low-Cost, Precision, High-Side, Current-Sense Amplifier	3-87
MAX4230	Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp in 5-Pin SOT23	3-95*
MAX4231	Dual, Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp in 8-Pin µMAX	3-95*
MAX4232	Quad, Ultra-Low-Power, +1V/V Gain, Rail-to-Rail I/O Op Amp	3-95*
MAX4233	Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp in 5-Pin SOT23	3-95*
MAX4234	Dual, Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp in 8-Pin µMAX	3-95*
MAX4235	Quad, Ultra-Low-Power, +10V/V Gain, Rail-to-Rail I/O Op Amp	3-95*
MAX4240	1.8V Micropower, SOT23, Rail-to-Rail I/O Op Amp	3-97*
MAX4241	1.8V Micropower, 8-Pin µMAX, Rail-to-Rail I/O Op Amp with Shutdown	3-97*
MAX4242	Dual, 1.8V Micropower, 8-Pin, µMAX, Rail-to-Rail I/O Op Amp	3-97*
MAX4243	Dual, 1.8V Micropower, 10-Pin, µMAX, Rail-to-Rail I/O Op Amp with Shutdown	3-97*
MAX4244	Quad, 1.8V Micropower, Rail-to-Rail I/O Op Amp	3-97*
MAX4249	Dual, Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)	3-99*
MAX4250	Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp	3-99*
MAX4251	Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp	3-99*
MAX4252	Dual, Low-Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amp	3-99*
MAX4253	Dual, Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp with Shutdown	3-99*
MAX4254	Quad, Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp	3-99*
MAX4255	Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)	3-99*
MAX4256	Low-Noise/Distortion, Low-Power, Rail-to-Rail Op Amp with Shutdown (A_V > +10V/V)	3-99*
MAX4257	Dual, Low Noise/Distortion, Low-Power, Rail-to-Rail Op Amp (A_V > +10V/V)	3-99*
MAX4330	Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp	3-101
MAX4331	Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown	3-101
MAX4332	Dual, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp	3-101
MAX4333	Dual, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp with Shutdown	3-101
MAX4334	Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amp	3-101
MAX9000	Low-Power, High-Speed Op Amp + Comparator + Reference IC in 8-Pin µMAX	3-117*
MAX9001	Low-Power, High-Speed Op Amp + Comparator + Reference IC with Shutdown	3-117*
MAX9002	Low-Power, High-Speed Op Amp + Comparator IC in 8-Pin µMAX	3-117*
MAX9003	Low-Power, High-Speed, Single-Supply Op Amp + Comparator + Reference IC	3-117*
MAX9004	Low-Power, High-Speed Op Amp + Comparator + Reference IC with Shutdown	3-117*
MAX9005	Low-Power, High-Speed Op Amp + Comparator IC in 8-Pin µMAX	3-117*

*Advance Information–first page of a data sheet in preparation.

Op Amps

Precision

Low V_{OS}

Bipolar

MAX400
MAX427/437
MAX478/479 (dual/quad, 17µA)
MAX480
MAX492/494/495 (single/dual/quad)

MXL1001
MXL1007
MXL1013/1014
MXL1178/1179
OP07/27/37
OP90

Choppers

MAX420–423
MAX430/432 (internal caps)
ICL765x

★ New product
† Future product

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Low I_{BIAS}

MAX406/407/418 (single/dual/quad, <1pA)
MAX409/417/419 (single/dual/quad, <1pA, 150kHz, GBW)
MAX420–423
MAX430/432 (internal caps)
★ MAX4162/63/64 (single/dual/quad, 1pA, 25µA, 200kHz, rail-to-rail I/O)
ICL761x–765x

Low Noise

MAX400
MAX410/12/14 (single/dual/quad, <2.4nV/√Hz)
MAX427/437
MXL1001
MXL1007
OP07/27/37
† MAX4249/52/53/57 (dual, 2.7V, low noise/distortion)
† MAX4250/4255 (SOT23, 2.7V, low noise/distortion)
† MAX4251/4256 (single, 2.7V, low noise/distortion)
† MAX4254 (quad, 2.7V, low noise/distortion)

Special

MAX471/472 (current-sense amp)
MAX951 (7µA, 20kHz op amp + comparator + reference)
MAX952 (7µA, 125kHz op amp + comparator + reference)
→ cont.

MAX953 (5µA, 20kHz op amp + comparator)
MAX954 (5µA, 125kHz op amp + comparator)
★ MAX4172 (low-cost current-sense amp)
→ cont.

† MAX9000/9001 (1MHz op amp + comparator + reference)
† MAX9002 (1MHz op amp + comparator)
† MAX9003/9004 (8MHz op amp + comparator + reference)
† MAX9005 (8MHz op amp + comparator)

Low Power

Single Supply

MAX406/407/418 (single/dual/quad, 1.2µA, rail-to-rail output)
MAX409/417/419 (single/dual/quad, 1.2µA, 150kHz GBW, rail-to-rail output)
MAX478/479 (dual/quad, 17µA)
MAX480
★ MAX4162/63/64 (single/dual/quad, 1pA, 25µA, 200kHz, rail-to-rail I/O)
† MAX4230–4235 (single/dual/quad, 5µA, rail-to-rail I/O)
† MAX4240/4241 (SOT23, 1.8V, 10µA, rail-to-rail I/O)
† MAX4242/4243 (dual, 1.8V, 10µA, rail-to-rail I/O)
† MAX4244 (quad, 1.8V, 10µA, rail-to-rail I/O)
† MAX4249/52/53/57 (dual, 2.4V, low noise/distortion)
† MAX4250/4255 (SOT23, 2.4V, low noise/distortion)
† MAX4251/4256 (single, 2.4V, low noise/distortion)
† MAX4254 (quad, 2.4V, low noise/distortion)
cont. →

Single Supply & High Speed

MAX473/474/475 (single/dual/quad, 10MHz, 15V/µs)
MAX492/494/495 (dual/quad/single, 500kHz, rail-to-rail I/O)
MAX4122/4123 (5MHz, rail-to-rail I/O)
MAX4124/4125 (26MHz, rail-to-rail I/O)
MAX4126/4127 (dual, 5MHz, rail-to-rail I/O)
MAX4128 (dual, 26MHz, rail-to-rail I/O)
MAX4129 (quad, 5MHz, rail-to-rail I/O)
MAX4130/4131 (10MHz, rail-to-rail I/O)
★ MAX4132/4133 (dual, 10MHz, rail-to-rail I/O)
★ MAX4134 (quad, 10MHz, rail-to-rail I/O)
★ MAX4165/4166 (SOT23-5, 5MHz, 80mA, output drive, rail-to-rail I/O)
★ MAX4167/4168 (dual, 5MHz, 80mA output drive, rail-to-rail I/O)
→ cont.

ICL761x–765x
MXL1013/1014
MXL1178/1179

High Speed

MAX402 (2MHz, 75µA)
MAX403 (10MHz, 375µA)
MAX410/412/414 (single/dual/quad, 28MHz, 2.5mA)

★ MAX4169 (quad, 5MHz, 80mA output drive, rail-to-rail I/O)
★ MAX4330/4331 (SOT23-5, 3MHz, 245µA, rail-to-rail I/O)
★ MAX4332/4333 (dual, 3MHz, 245µA, rail-to-rail I/O)
★ MAX4334 (quad, 3MHz, 245µA, rail-to-rail I/O)

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC-}_V) to (V_{EE+}_V)	V_{OUT} Swing/Load (V_{CC-}_V) to (V_{EE+}_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
MAX400	10 to 15µV	2	0.4	1 to 1	3 to 3/1k	±3 to ±18	4	Ultra-low V_{OS} & drift, non-chopper stabilized	5.16
MAX402	2	5	2	1.2 to 1.2	1.1 to 1.1/20k	±3 to ±5	75µA	High speed, micropower	1.98
MAX403	2	25	10	1.2 to 1.2	1.4 to 1.4/4k	±3 to ±5	375µA	High speed, micropower	2.75
MAX406/407/418	10	10pA	8 to 40kHz	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, single supply, rail-to-rail outputs, unity-gain stable	1.38/1.95/3.40
MAX409/417/419	10	10pA	150kHz (A_V ≥ 10V/V)	1.1 to 0	0.01 to 0.01/1M	+2.5 to +10	1.2µA	Single/dual/quad, lowest power, decompensated (A_V ≥ 10V/V)	1.38/1.95/3.40
MAX410/412/414	1 typ (320µV MAX414)	150	28	1.3 to 1.2	1.3 to 1.2/2k	±2.4 to ±5.25	2.7	Single/dual/quad, high speed, low noise, <2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	1.50/2.45/4.50
MAX420/422	5 to 10µV	0.03 to 0.10	0.125 to 0.5	3.5 to -0.1	0.5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 to 10µV	0.03 to 0.10	0.125 to 0.5	3.5 to -0.1	0.5 to 0.5/10k 0.4 to 0.4/100k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX427/437	15µV	35	8/60	2.5 to 2.5	1.2 to 1.2/2k	±15	4	High speed, low noise 3.8nV/√Hz precision	1.83
MAX430/432	5µV	0.1	0.125 to 0.5	2.5 to -0.1	0.5 to 0.5/10k	±2.5 to ±16.5	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX471	–	–	–	0 to 3 amps*	1.5 to 0/no load	+3 to +36	100µA (5µA SHDN)	Precision, high-side current-sense amplifier with internal sense resistor, measures charge and discharge	2.50
MAX472	60µV	–	–	–	1.5 to 0/no load	+3 to +36	100µA (5µA SHDN)	Precision, high-side current-sense amplifier	2.05
MAX473/474/475	1 to 1.5	150	10	1.7 to -0.1	0.05 to 0.05/no load	+2.7 to +6	3	Single/dual/quad, single or dual supply, wide output swing, 15V/µs min slew rate	1.45/2.25/3.60
MAX478/479	70 to 250µV	6	60kHz	1.1 to -0.3	1.2 to 0.2/2k	+2.2 to +36, ±1.1 to ±18	17µA	Micropower, precision dual 8-pin SO and quad 14-pin narrow SO, 3V, 5V, and ±15V specs	2.58/3.35
MAX480	70µV	3	20kHz	1 to 0	0.8 to 0/2k	+1.6 to +36, ±0.8 to ±18	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	2.59
MAX492/494/495	500µV	60	500kHz	0 to 0	0.15 to 0.15/1k	+2.7 to +6	150µA	Dual/quad/single, precision, rail-to-rail I/O	2.25/3.60/1.45
MAX4122/4123	0.6 to 1.0	150	5	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	0.75	Single, rail-to-rail I/O, MAX4122 in SOT23-5, shutdown (MAX4123)	0.85/0.98
MAX4124/4125	0.6 to 1.0	150	25 (A_V ≥ 10V/V)	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	0.75	Single, rail-to-rail I/O, decompensated, shutdown (MAX4125)	0.85/0.98
MAX4126/4127	0.75 to 1.5	150	5	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.75	Dual, rail-to-rail I/O, unity-gain stable, shutdown (MAX4127)	1.40/1.67
MAX4128	0.75 to 1.5	150	25 (A_V ≥ 10V/V)	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.75	Dual, rail-to-rail I/O, decompensated	1.40
MAX4129	1.5	150	5	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	0.75	Quad, rail-to-rail I/O, unity-gain stable	2.40
MAX4130/4131	0.6 to 1.0	150	10	-0.25 to -0.25	0.24 to 0.125/250	+2.7 to +6.5	1.05	Single, rail-to-rail I/O, MAX4330 in SOT23-5, shutdown (MAX4131)	0.85/0.98
MAX4132/4133	0.6	150	10	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	1.05	Dual, rail-to-rail I/O, unity-gain stable, shutdown (MAX4133)	1.40/1.67
MAX4134	0.6	150	10	-0.25 to -0.25	0.28 to 0.18/250	+2.7 to +6.5	1.05	Quad, rail-to-rail I/O, unity-gain stable	2.40
MAX4162	4	100pA	200kHz	-0.25 to -0.25	0.04 to 0.025/10k	+2.7 to +10	40µA	Single, rail-to-rail I/O, ultra-low power, available in SOT23-5	0.75
MAX4163/4164	4	100pA	200kHz	-0.25 to -0.25	0.04 to 0.025/10k	+2.7 to +10	40µA	Dual/quad, rail-to-rail I/O, ultra-low power	1.20/2.10
MAX4165/4166	1.5	150	5	-0.25 to -0.25	0.34 to 0.16/25	+2.7 to +6.5	1.4	Single, 80mA output current drive, rail-to-rail I/O, MAX4165 in SOT23-5, shutdown (MAX4166)	0.80
MAX4167/4168	0.85	150	5	-0.25 to -0.25	0.34 to 0.16/25	+2.7 to +6.5	1.4	Dual, 80mA output current drive, rail-to-rail I/O, shutdown (MAX4168)	1.10/1.25
MAX4169	0.85	150	5	-0.25 to -0.25	0.34 to 0.16/25	+2.7 to +6.5	1.4	Quad, 80mA output current drive, rail-to-rail I/O	1.65
MAX4172	0.75	—	—	—	1.2 to 0/I_{OUT} ≤ 1.5mA	+3 to +32	1.6	Low-cost, precision, high-side current-sense amplifier	1.45
MAX4230/4233	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Single, ultra-low power, rail-to-rail I/O, available in SOT23	††
MAX4231/4234	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Dual, ultra-low power, rail-to-rail I/O, available in 8-pin µMAX	††
MAX4232/4235	1.3	0.75	40kHz	-0.1 to -0.1	0.2 to 0.2/5k	+2.7 to +5.5	5µA	Quad, ultra-low power, rail-to-rail I/O, available in 16-pin QSOP	††
MAX4240/4241	0.75	3.0	100kHz	-0.2 to -0.2	0.25 to 0.25/10k	+1.8 to +5.5	15µA	Single, 1.8V, micropower, rail-to-rail I/O, MAX4240 in SOT23-5, shutdown (MAX4241)	††
MAX4242/4243	0.75	3.0	100kHz	-0.2 to -0.2	0.25 to 0.25/10k	+1.8 to +5.5	15µA	Dual, 1.8V, micropower, rail-to-rail I/O, MAX4242 in 8-pin µMAX, shutdown (MAX4243)	††

* Sense resistor current range

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Part Number	V_{OS} (mV max)	I_{BIAS} (nA max)	Unity GBW (MHz)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	V_{OUT} Swing/Load (V_{CC}-_V) to (V_{EE}+_V)/(Ω)	Supply Voltage (V)	Supply Current/ Op Amp (mA max)	Features	Price† 1000-up ($)
MAX4244	0.75	3.0	100kHz	-0.2 to -0.2	0.25 to 0.25/10k	+1.8 to +5.5	15µA	Dual, 1.8V, micropower, rail-to-rail I/O	††
MAX4249/4247	1.5	150pA	22 ($A_V \geq 10V/V$)	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Dual, 2.4V, low noise, low distortion, rail-to-rail outputs, MAX4249 with shutdown ($A_V \geq 10V/V$)	††
MAX4250	1.5	150pA	3	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in SOT23	††
MAX4251	1.5	150pA	3	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in 8-pin µMAX with shutdown	††
MAX4252/4253	1.5	150pA	3	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Dual, 2.4V, low noise, low distortion, rail-to-rail outputs	††
MAX4254	1.5	150pA	3	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Quad, 2.4V, low-noise, low distortion, rail-to-rail outputs	††
MAX4255	1.5	150pA	22 ($A_V \geq 10V/V$)	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in SOT23 ($A_V \geq 10V/V$)	††
MAX4256	1.5	150pA	22 ($A_V \geq 10V/V$)	-0.1 to 1.5	0.15 to 0.25/5k	+2.4 to +5.5	575µA	Single, 2.4V, low noise, low distortion, rail-to-rail outputs in 8-pin µMAX with shutdown, ($A_V \geq 10V/V$)	††
MAX4330/4331	0.60	65	3	-0.25 to -0.25	0.175 to 0.15/2k	+2.3 to +6.5	290µA	Single, rail-to-rail I/O, MAX4330 in SOT23-5, shutdown (MAX4331)	0.78/0.85
MAX4332/4333	0.90	65	3	-0.25 to -0.25	0.175 to 0.15/2k	+2.3 to +6.5	290µA	Dual, rail-to-rail I/O, MAX4332 in 8-pin µMAX, shutdown (MAX4333)	1.25/1.40
MAX4334	0.10	65	3	-0.25 to -0.25	0.175 to 0.15/2k	+2.3 to +6.5	290µA	Quad, rail-to-rail I/O	2.15
ICL7611	2 to 15	0.05	0.044 to 1.4	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current	1.35
ICL7612	5 to 15	0.05	0.044 to 1.4	-0.3 to -0.1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current, rail-to-rail I/O	1.29
ICL7614	2 to 15	0.05	0.48**	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.25	External compensation	0.95
ICL7616	2 to 15	0.05	0.044 to 1.4	2 to -0.1	0.1 to 0.1/100k	±1 to ±8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	0.05	0.48	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.25	Dual, low I_{BIAS} and I_{OS}	1.06/1.48
ICL7631/7632	5 to 20	0.05	0.044 to 1.4	0.8 to 1	0.1 to 0.1/100k	±1 to ±8	0.022 to 2.5	Triple op amp, programmable quiescent current, ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 to 25	0.05	0.044 to 1.4	1.3 to 1.3, 0.6 to 1	0.5 to 0.5/10k 0.1 to 0.1/1M	±1 to ±8	0.015 to 2.5	Quad, low power, CMOS	1.41/1.56
ICL7650	5 to 10µV	0.01 to 0.02	2	3 to -0.2	0.05 to 0.05/100k	±5	2	Industry standard, chopper stabilized	2.16
ICL7652	5 to 10µV	0.03	0.45	1 to 0.2	0.05 to 0.05/100k	±5	2	Low noise, industry standard, chopper stabilized	3.24
MXL1001	15 to 60µV	2 to 4	0.8	1 to 1	1.5 to 1.5/1k	±3 to ±18	2	Precision LT1001 second source	1.73
MXL1007	25 to 60µV	35 to 55	8	2.5 to 2.5	2.5 to 2.5/600	±15	4 to 4.7	Low noise, precision LT1007 second source	1.85
MXL1013/1014	150 to 800µV	20 to 30	0.6	1.2 to -0.3	1 to 5mV/600	+4 to +36, ±2 to ±18	0.50 to 0.55	Dual/quad, precision LT1013/1014 second source	1.57/3.06
MXL1178/1179	70 to 600µV	5 to 6	60kHz	1.1 to -0.3	1.2 to 0.2mV/2k	+2.2 to +36, ±1.1 to ±18	17 to 21µA	Dual/quad, precision, micropower LT1178/1179 second source	2.50/3.35
OP07	25 to 150µV	2 to 12	0.6	1 to 1	3 to 3/1k	±3 to ±18	4	Industry standard, precision	1.58
OP27	25 to 100µV	40 to 80	8	2.7 to 2.7	3.5 to 3.5/600	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP37	25 to 100µV	40 to 80	63 ($A_V \geq 5$)	2.7 to 2.7	3.5 to 3.5/600	±3 to ±18	4.6 to 5.6	Industry standard, low noise	2.06
OP90	150 to 450µV	15 to 25	0.020	1 to 0	0.8 to 0.1mV/10k	±0.8 to ±18, +1.6 to +36	15 to 20µA	Industry standard, micropower	1.60

** External 39pF compensation capacitor added.
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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Op Amp + Comparator + Reference ICs

Part Number	Op Amp Compensation	Op Amp GBW (kHz)	Comparator Propagation Delay (µs)	Reference (1.2V ±1%)	Supply Voltage (V min)	Supply Current (µA max)	Features	Price† 1000-up ($)
MAX951	Unity-gain stable	20	4	Yes	2.7	10	Single-supply, rail-to-rail outputs, 8-pin package, low-cost op amp drives capacitive loads	1.60
MAX952	Decompensated ($A_V \geq 10V/V$)	125	4	Yes	2.7	10	MAX951 with decompensated op amp for $A_V \geq 10V/V$	1.60
MAX953	Unity-gain stable	20	4	—	2.4	8	MAX951 without the reference	1.30
MAX954	Decompensated ($A_V \geq 10V/V$)	125	4	—	2.4	8	MAX953 with decompensated op amp for $A_V \geq 10V/V$	1.30
MAX9000/9001	Unity-gain stable	1MHz	0.10	Yes	2.5	450	Low power, single supply, rail-to-rail outputs, shutdown (MAX9001)	††
MAX9002	Unity-gain stable	1MHz	0.10	Yes	2.5	450	MAX9000 without the reference	††
MAX9003/9004	Decompensated	8MHz	0.10	Yes	2.5	400	MAX9000 with decompensated op amp for $A_V \geq 10V/V$	††
MAX9005	Decompensated	8MHz	0.10	Yes	2.5	400	MAX9003 without the reference	††

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†† Future [illegible] contact factory for pricing and availability. Specifications are preliminary.

Comparators

Special

MAX516
(quad, programmable input threshold voltage)

MAX910
(8ns, programmable input threshold voltage)

† MAX9000/9001
(1MHz op amp + comparator + reference)

† MAX9002
(1MHz op amp + comparator)

† MAX9003/9004
(8MHz op amp + comparator + reference)

† MAX9005
(8MHz op amp + comparator)

MAX962
(dual, 4.5ns, single supply)

★ MAX963
(dual, 4.5ns, single supply)

★ MAX964
(quad, 4.5ns, single supply)

† MAX997
(SOT23, 4.5ns, single supply)

MAX9686
(6ns, industry standard)

MAX9698
(6ns, industry standard)

MXL1016

MXL1116

High-Speed Comparators

TTL Output Single/Dual Supply

<10ns

MAX900
(quad, 8ns, single/dual supply)

MAX901
(quad, 8ns, single/dual supply)

MAX902
(dual, 8ns, single/dual supply)

MAX903
(8ns, single/dual supply)

MAX910
(8ns, programmable input threshold)

MAX912
(dual, 10ns, single/dual supply)

MAX913
(10ns, single/dual supply)

MAX915
(6ns, master/slave, clocked)

MAX961
(single, 4.5ns, single supply)

← cont.

<50ns

MAX907
(dual, 40ns, single supply)

MAX908
(quad, 40ns, single supply)

MAX909
(40ns, single/dual supply)

† MAX976
(320µA, 20ns)

† MAX978
(320µA, 20ns)

† MAX998
(SOT23, 320µA, 20ns)

MAX975
(dual-speed comparator)

MAX977
(dual-speed comparator)

3V, High Speed

MAX941
(350µA, 80ns, rail-to-rail inputs)

MAX942
(dual MAX941)

MAX944
(quad MAX941)

† MAX976
(320µA, 20ns)

† MAX978
(320µA, 20ns)

MAX961
(single, 4.5ns, single supply)

MAX962
(dual, 4.5ns, single supply)

★ MAX963
(dual, 4.5ns, single supply)

★ MAX964
(quad, 4.5ns, single supply)

cont.→

ECL Output

MAX905
(master/slave, clocked)

MAX906
(dual, master/slave, clocked)

MAX9685
(industry standard)

MAX9687
(industry standard, dual)

MAX9690 (8-pin SO)

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† MAX997
(SOT23, 4.5ns, single supply)

† MAX998
(SOT23, 320µA, 20ns)

Micropower Special

MAX951
(7µA, 20kHz op amp + comparator + reference)

MAX952
(7µA, 125kHz op amp + comparator + reference)

MAX953
(5µA, 20kHz op amp + comparator)

MAX954
(5µA, 125kHz op amp + comparator)

← cont.

★ MAX987/988
(SOT23, 120ns, 60µA)

★ MAX989/990
(dual, 300ns, 13µA)

★ MAX991/992
(dual, 120ns, 60µA)

★ MAX993/994
(quad, 300ns, 13µA)

★ MAX995/996
(quad, 120ns, 60µA)

Micropower

MAX921/971
(3.2µA comparator + 1% reference)

MAX922/972
(dual, 3.2µA max supply current)

MAX923/973
(dual, 4.5µA comparator + 1% reference)

MAX924/974
(quad, 6.5µA comparator + 1% reference)

MAX931/981
(3.2µA comparator + 2% reference)

MAX932/982
(dual, 4.5µA comparator + 2% reference)

MAX933/983
(dual, 4.5µA comparator + 2% reference, window comparator)

MAX934/984
(quad, 6.5µA comparator + 2% reference)

★ MAX965
(single, 1.6V, 7µA comparator + 1.5% reference)

★ MAX966
(dual, 1.6V, 6µA)

★ MAX967/968
(dual, 1.6V, 10µA comparator + 1.5% reference)

★ MAX969
(quad, 1.6V, 14µA)

★ MAX970
(quad, 1.6V, 11µA)

★ MAX985/986
(SOT23, 300ns, 13µA)

← cont.

★ New product
† Future product

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
HIGH SPEED											
MAX900	4	0.5	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	0.5	2.25 to -0.1	TTL	No	No	+5 to +10, ±5	4 (I_{CC})	8	MAX900 without output latch	5.23
MAX902	2	1	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Dual MAX900	4.01
MAX903	1	1	2.25 to -0.1	TTL	Yes	No	+5 to +10, ±5	4 (I_{CC})	8	Single MAX900	3.15
MAX905	1	0.5	2.2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1.8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages, also operates with -5.2V or +5V, -5.2V ECL supplies	3.54
MAX906	2	0.5	2.2 to -0.1	ECL	Yes	Yes	-5 or ±5	24 (I_{EE})	1.8	Dual MAX905, also operates with -5.2V or +5V, -5.2V ECL supplies	5.23
MAX907	2	0.5	1.5 to -0.2	TTL	No	No	+4.5 to +5.5	1	30	High speed, ultra-low power, single +5V, 8-pin DIP/SO, built-in hysteresis	1.70
MAX908	4	0.5	1.5 to -0.2	TTL	No	No	+4.5 to +5.5	1	30	High speed, ultra-low power, single +5V, 14-pin DIP/SO, built-in hysteresis	2.95
MAX909	1	0.5	1.5 to -0.2	TTL	Yes	Yes	+4.5 to +5.5, ±5	1.8	30	High speed, low power, single or dual supply, input range includes ground, complementary outputs	1.50
MAX910	1	1	2 to 2	TTL	Yes	No	±5 or +5, -5.2	30 (I_{CC})	8	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX912	2	0.8	1.5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Dual MAX913	3.90
MAX913	1	0.8	1.5 to -0.2	TTL	Yes	Yes	+5 or ±5	10	10	Lowest power 10ns comparator with complementary outputs single/dual supply, CMVR extends below ground to V+ - 1.5V	2.55
MAX915	1	0.5	2.2 to -0.1	TTL	Yes	Yes	+5 or ±5	18 (I_{CC})	6	No oscillations, master/slave, clocked	2.55
MAX941	1	1	-0.2 to -0.2	TTL/CMOS	Yes	No	+2.7 to +6	600µA	75	Low power, 3V or 5V single supply, rail-to-rail inputs (5µA SHDN)	1.40
MAX942	2	1	-0.2 to -0.2	TTL/CMOS	No	No	+2.7 to +6	600µA	75	Dual MAX941, 8-pin DIP/SO	1.50
MAX944	4	1	-0.2 to -0.2	TTL/CMOS	No	No	+2.7 to +6	600µA	75	Quad MAX941	2.50
MAX961	1	0.5	-0.1 to -0.1	TTL/CMOS	Yes	Yes	+2.7 to +5.5	11	4.5	High speed, internal hysteresis, rail-to-rail inputs, shutdown mode	2.50
MAX962	2	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +5.5	8	4.5	Dual, internal hysteresis, rail-to-rail inputs	3.35
MAX963	2	0.5	-0.1 to -0.1	TTL/CMOS	Yes	Yes	+2.7 to +5.5	11	4.5	Dual, internal hysteresis, rail-to-rail inputs, shutdown mode	3.35
MAX964	4	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +5.5	8	4.5	Quad, internal hysteresis, rail-to-rail inputs, shutdown mode	5.50
MAX976	2	3	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	500µA	20	Dual, high speed, 3V/5V	††
MAX978	4	3	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	500µA	20	Quad, high speed, 3V/5V	††
MAX997	1	0.5	-0.1 to -0.1	TTL/CMOS	No	No	+2.7 to +5.5	5	4.5	SOT23, high speed, internal hysteresis, rail-to-rail inputs	††
MAX998	1	3	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	500µA	20	Single, high speed, 3V/5V, available in SOT23-6 with shutdown	††
MAX999	1	0.5	-0.1 to -0.2	TTL/CMOS	No	No	+2.7 to +5.5	5	4.5	Single, high speed, 3V/5V, available in SOT23-5	††
MAX9685	1	5	2.5 to 2.7	ECL	Yes	Yes	±5 or +5, -5.2	32 (I_{EE})	1.3	Higher speed industry standard	3.38
MAX9686	1	5	2 to 2	TTL	Yes	Yes	±5 or +5, -5.2	25 (I_{CC})	6	Higher speed industry standard	2.31
MAX9687	2	5	2.5 to 2.5	ECL	Yes	Yes	±5 or +5, -5.2	68 (I_{EE})	1.4	Higher speed industry standard	5.12
MAX9690	1	5	2.5 to 2.5	ECL	No	Yes	±5 or +5, -5.2	32 (I_{EE})	1.3	8-pin DIP/SO package	3.29
MAX9698	2	5	2 to 2	TTL	Yes	Yes	±5 or +5, -5.2	50 (I_{CC})	6	Higher speed industry standard	3.92
MXL1016	1	0.8	1.5 to 1.25	TTL	Yes	Yes	+5 or ±5	35 (I_{CC})	10	High speed, complementary outputs, LT1016 second source	1.92
MXL1116	1	1	2.5 to 0	TTL	Yes	Yes	+5 or ±5	38 (I_{CC})	12	High speed, single supply, complementary outputs, LT1116 second source	1.92
MICROPOWER											
MAX921/971	1 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2µA (total pkg.)	12µs	Micropower comparator + 1% reference & hysteresis, single-supply capability, CMVR extends to GND	1.50/1.50
MAX922/972	2	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2µA (total pkg.)	12µs	Dual, single-supply micropower comparator in 8-pin DIP/SO	0.98/0.98
MAX923/973	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5µA (total pkg.)	12µs	Dual, single-supply comparator with 1% voltage reference in 8-pin DIP/SO	1.95/1.95
MAX924/974	4 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5µA (total pkg.)	12µs	Quad, micropower comparator with 1% voltage reference	2.25/2.25
MAX931/981	1 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	3.2µA (total pkg.)	12µs	Low-cost comparator + 2% reference & hysteresis, single-supply, CMVR extends to GND	0.98/0.98
MAX932/982	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5µA (total pkg.)	12µs	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO	1.26/1.26
MAX933/983	2 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	4.5µA (total pkg.)	12µs	Dual, low-cost, single-supply comparator + 2% reference & hysteresis in 8-pin DIP/SO (window comparator input configuration)	1.26/1.26
MAX934/984	4 + ref	10	1.3 to 0	TTL/CMOS/ open drain	No	No	+2.5 to +11, ±1.25 to ±5	6.5µA (total pkg.)	12µs	Quad, low-cost comparator + 2%-accurate reference, single/dual supply	1.31/1.31

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

Part Number	Comps. per Pkg.	Input Offset Voltage (mV max)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
MICROPOWER (continued)											
MAX965	1 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	12µA	10µs	Single, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.05
MAX966	2	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	5µA	10µs	Dual, rail-to-rail I/O, operates down to 1.6V	1.05
MAX967/968	2 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	8µA	10µs	Dual, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.30
MAX969	4 + ref	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	5.5µA	10µs	Quad, rail-to-rail I/O, operates down to 1.6V, has 1.22V internal ref.	1.95
MAX970	4	3	-0.25 to -0.25	Open drain	No	No	+1.6 to +5.5	4.5µA	10µs	Quad, rail-to-rail I/O, operates down to 1.6V	1.60
MAX985/986	1	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20µA	300	Single, rail-to-rail I/O, single-supply operation, available in SOT23-5	0.66
MAX987/988	1	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	80µA	120	Single, rail-to-rail I/O, single-supply operation, available in SOT23-5	0.66
MAX989/990	2	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20µA	300	Dual, rail-to-rail I/O, single-supply operation	1.05
MAX991/992	2	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	80µA	120	Dual, rail-to-rail I/O, single-supply operation	1.05
MAX993/994	4	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	20µA	300	Quad, rail-to-rail I/O, single-supply operation	1.58
MAX995/996	4	5	-0.25 to -0.25	TTL/CMOS/ open drain	No	No	+2.5 to +5.5	80µA	120	Quad, rail-to-rail I/O, single-supply operation	1.58

Part Number	Comps. per Pkg.	Input Offset Voltage (mV)	V_{IN} Range (V_{CC}-_V) to (V_{EE}+_V)	Logic	Latched Outputs	Complementary Outputs	Supply Voltage (V)	Supply Current per Comp. (mA max)	t_{PD} (ns)	Features	Price† 1000-up ($)
SPECIAL											
MAX516	4	4.9‡	0 to 0	TTL/CMOS	No	No	+4.75 to +16.5	10.01 (total pkg.)	800	Quad comparator + quad 8-bit DAC for independent threshold setting, single-supply capability, rail-to-rail input voltage ranges	3.00
MAX910	1	1	2 to 2	TTL	Yes	No	±5 or +5, -5.2	30 (I_{CC})	8	TTL-compatible, 8-bit digitally programmable input tvoltage hreshold, on-board reference	5.20
MAX951–954		(See Op Amp + Comparator + Reference IC section for tables)									—
MAX975	1	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed), 0.003 (low power)	28 (high speed), 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	1.95
MAX977	2	0.2	1.2 to -0.2	TTL/CMOS	No	No	+2.7 to +5.25	0.300 (high speed), 0.003 (low power)	28 (high speed), 480 (low power)	Dual speed, automatically switches from high-speed comparator to low-power comparator	3.50
MAX9000–9005		(See Op Amp + Comparator + Reference IC section for tables)									—

‡ Total unadjusted error equals ±1LSB (max).
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-1129; Rev 2; 7/97

MAXIM

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

General Description

The MAX961–MAX964 are ultra-high-speed, single/dual/quad comparators with internal hysteresis. These devices are optimized for single +3V or +5V operation. The input common-mode range extends 100mV beyond both supply rails, and the outputs can sink or source 4mA to within 0.52V of GND and V_{CC}. Propagation delay is under 7ns (5mV overdrive), while supply current is 5.5mA per comparator.

The MAX961/MAX963 feature complementary outputs, a low-power shutdown mode, and a latch-enable function. The latch function enables the user to hold a valid comparator output. In shutdown mode, the MAX961/MAX963/MAX964 consume only 270µA supply current per comparator. The single MAX961 and dual MAX962 are available in space-saving 8-pin µMAX packages.

Features

- **Ultra-Fast, 4.5ns Propagation Delay**
- **Ideal for +3V and +5V Single-Supply Applications**
- **Rail-to-Rail® Input Voltage Range**
- **3.5mV Internal Hysteresis for Clean Switching**
- **Output Latch (MAX961/MAX963)**
- **TTL/CMOS-Compatible Complementary Outputs (MAX961/MAX963)**
- **270µA Shutdown Current per Comparator (MAX961/MAX963/MAX964)**
- **Available in Space-Saving Packages:**
  8-Pin µMAX (MAX961/MAX962)
  16-Pin QSOP (MAX964)

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

High-Speed Sampling Circuits

Ordering Information

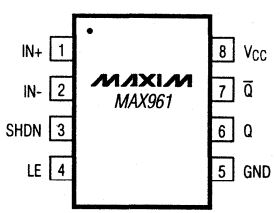
PART	TEMP. RANGE	PIN-PACKAGE
MAX961ESA	-40°C to +85°C	8 SO
MAX961EUA	-40°C to +85°C	8 µMAX
MAX962ESA	-40°C to +85°C	8 SO
MAX962EUA	-40°C to +85°C	8 µMAX
MAX963ESD	-40°C to +85°C	14 SO
MAX964ESE	-40°C to +85°C	16 Narrow SO
MAX964EEE	-40°C to +85°C	16 QSOP

Selector Guide

PART	NO. OF COMPARATORS	COMPLEMENTARY OUTPUT	SHUTDOWN	LATCH ENABLE	PACKAGE
MAX961	1	Yes	Yes	Yes	8 SO/µMAX
MAX962	2	No	No	No	8 SO/µMAX
MAX963	2	Yes	Yes	Yes	14 SO
MAX964	4	No	Yes	No	16 SO/QSOP

Pin Configurations

TOP VIEW



SO/µMAX

Pin Configurations continued at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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For small orders, phone 408-737-7600 ext. 3468.

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to GND.....+6V to -0.3V
All Other Pins.....-0.3V to (V_{CC} + 0.3V)
Duration of Output Short Circuit to GND or V_{CC} .....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW/°C
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW/°C
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW/°C
16-Pin SO (derate 8.70mW/°C above +70°C).....696mW/°C
16-Pin QSOP (derate 8.33mW/°C above +70°C)....667mW/°C
Operating Temperature Range
MAX96_E .....-40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
				MIN	TYP	MAX	MIN	MAX	
Supply Voltage	V_{CC}	Inferred by PSRR		2.7		5.5	2.7	5.5	V
Input Common-Mode Voltage Range	V_{CMR}	(Note 2)		-0.1		V_{CC} + 0.1	-0.1	V_{CC} + 0.1	V
Input-Referred Trip Points	V_{TRIP}	V_{CM} = - 0.1V or 5.1V, V_{CC} = 5V (Note 3)	MAX96_UA		±2.0	±3.5		±5.2	mV
			All other packages		±2.0	±3.5		±4.0	
Input-Referred Hysteresis					3.5				mV
Input Offset Voltage	V_{OS}	V_{CM} = - 0.1V or 5.1V, V_{CC} = 5V (Note 4)	MAX96_UA		±0.5	±1.5		±3.5	mV
			All other packages		±0.5	±1.5		±2.0	
Input Bias Current	I_B	V_{IN+} = V_{IN-} = 0V or V_{CC}, V_{CC} = 5V	MAX96_UA			±15		±30	µA
			All other packages			±15		±15	
Differential Input Clamp Voltage		V_{CC} = 5.5V, V_{IN-} = 0V, I_{IN+} = 100µA			2.1				V
Input Capacitance					3				pF
Differential Input Impedance	R_{IND}	V_{CC} = 5V			8				kΩ
Common-Mode Input Impedance	R_{INCM}	V_{CC} = 5V			130				kΩ
Common-Mode Rejection Ratio	CMRR	V_{CC} = 5V, V_{CM} = -0.1V to 5.1V (Note 5)			0.1	0.3		0.5	mV/V
Power-Supply Rejection Ratio	PSRR	V_{CM} = 0V (Note 6)			0.05	0.3		0.3	mV/V
Output High Voltage	V_{OH}	I_{SOURCE} = 4mA		V_{CC} - 0.52			V_{CC} - 0.52		V
Output Low Voltage	V_{OL}	I_{SINK} = 4mA				0.52		0.52	V
Capacitive Slew Current		V_{OUT} = 1.4V, V_{CC} = 2.7V		30	60				mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, V_{CM} = 0V, C_{OUT} = 5pF, V_{SHDN} = 0V, V_{LE} = 0V, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			T_{MIN} to T_{MAX}		UNITS
			MIN	TYP	MAX	MIN	MAX	
Output Capacitance				4				pF
Supply Current per Comparator	I_{CC}	MAX961/MAX963, V_{CC} = 5V		8.5	11		11	mA
		MAX962/MAX964, V_{CC} = 5V		5.5	8		9	
Shutdown Supply Current per Comparator	I_{SHDN}	MAX961/MAX963/MAX964, V_{CC} = 5V		0.27	0.5		0.5	mA
Shutdown Output Leakage Current		MAX961/MAX963/MAX964, V_{OUT} = 0.5V and V_{CC} - 0.5V			1		20	µA
Rise/Fall Time	t_R, t_F	V_{CC} = 5V		2.3				ns
Logic Input High	V_{IH}		(V_{CC} / 2) + 0.4			(V_{CC} / 2) + 0.4		V
Logic Input Low	V_{IL}				(V_{CC} / 2) - 0.4		(V_{CC} / 2) - 0.4	V
Logic Input Current	I_{IL}, I_{IH}	V_{LOGIC} = 0V or V_{CC}			±15		±30	µA
Propagation Delay	t_{PD}	5mV overdrive (Note 7)		4.5	7		8.5	ns
Differential Propagation Delay	t_{PD}	Between any two channels or outputs (Q/$\overline{Q}$)		0.3				ns
Propagation-Delay Skew	t_{SKEW}	Between t_{PD-} and t_{PD+}		0.3				ns
Data-to-Latch Setup Time	t_{SU}	(Note 8)			5		5	ns
Latch-to-Data Hold Time	t_H	(Note 8)			5		5	ns
Latch Pulse Width	t_{LPW}	(Note 8)			5		5	ns
Latch Propagation Delay	t_{LPD}	(Note 8)			10		10	ns
Shutdown Time	t_{OFF}	Delay until output is high-Z (>10kΩ)		150				ns
Shutdown Disable Time	t_{ON}	Delay until output is valid		250				ns

Note 1: The MAX961EUA/MAX962EUA are 100% production tested at T_A = +25°C; all temperature specifications are guaranteed by design.

Note 2: Inferred by CMRR. Either input can be driven to the absolute maximum limit without false output inversion, provided that the other input is within the input voltage range.

Note 3: The input-referred trip points are the extremities of the differential input voltage required to make the comparator output change state. The difference between the upper and lower trip points is equal to the width of the input-referred hysteresis zone. (See Figure 1.)

Note 4: Input offset voltage is defined as the mean of the trip points.

Note 5: CMRR = (V_{OSL} - V_{OSH}) / 5.2V, where V_{OSL} is the offset at V_{CM} = -0.1V and V_{OSH} is the offset at V_{CM} = 5.1V.

Note 6: PSRR = ($V_{OS}2.7$ - $V_{OS}5.5$) / 2.8V, where $V_{OS}2.7$ is the offset voltage at V_{CC} = 2.7V, and $V_{OS}5.5$ is the offset voltage at V_{CC} = 5.5V.

Note 7: Propagation delay cannot be measured in automatic test equipment with low input overdrive values. The MAX96_ES_ devices are sample tested to 0.1% AQL, with a 200mV step and 100mV overdrive at T_A = +25°C. Correlation tests show that t_{PD} can be guaranteed with this test, since additional DC tests are performed that guarantee that all internal bias conditions are correct. Propagation delay on the µMAX and QSOP packages is guaranteed by design. For low-overdrive conditions, V_{OS} is added to the overdrive.

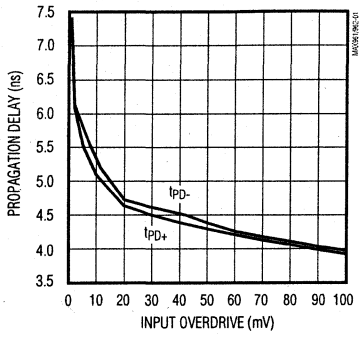
Note 8: Guaranteed by design.

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

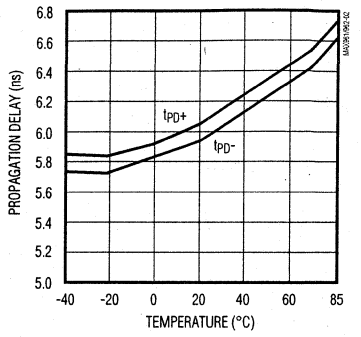
Typical Operating Characteristics

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

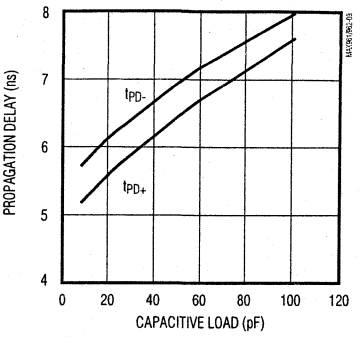
PROPAGATION DELAY vs. INPUT OVERDRIVE



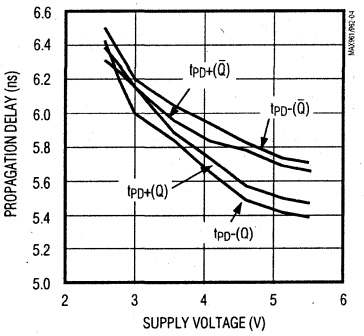
PROPAGATION DELAY vs. TEMPERATURE



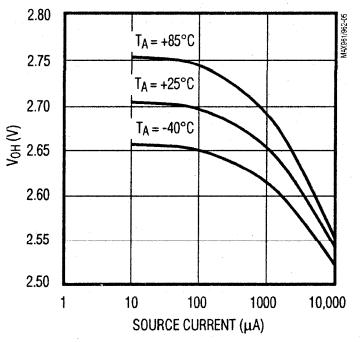
PROPAGATION DELAY vs. CAPACITIVE LOAD



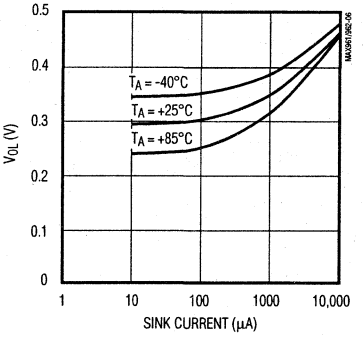
PROPAGATION DELAY vs. SUPPLY VOLTAGE



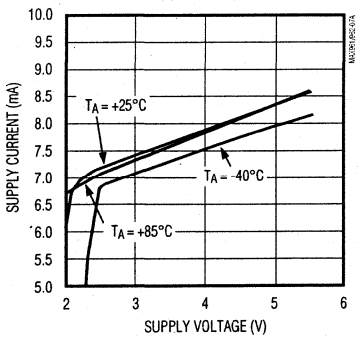
OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



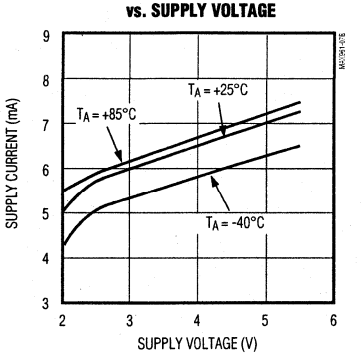
OUTPUT LOW VOLTAGE vs. SINK CURRENT



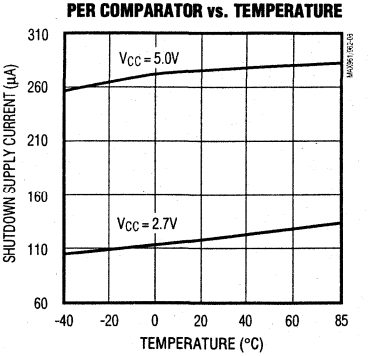
MAX961/MAX963 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



MAX962/MAX964 SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE



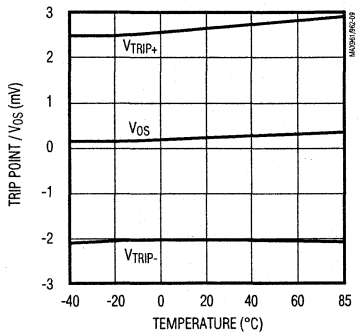
MAX961/MAX963/MAX964 SHUTDOWN SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



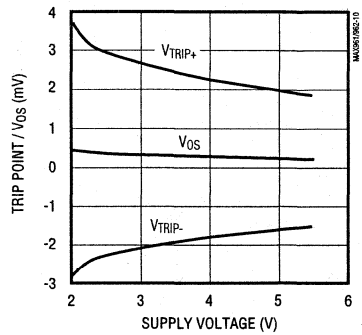
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

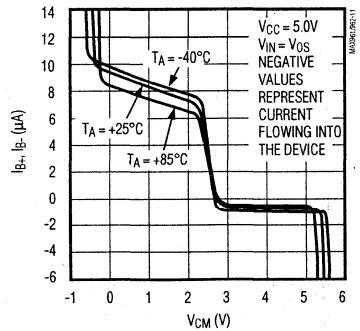
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. TEMPERATURE



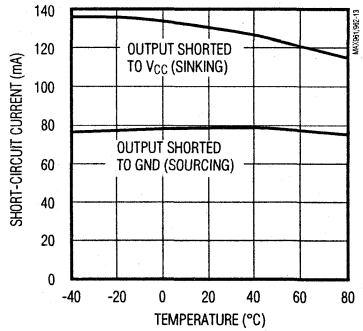
VOLTAGE TRIP POINT/INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE



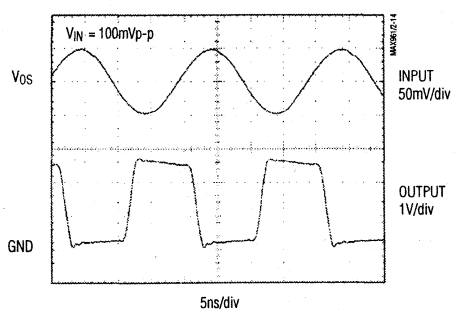
INPUT BIAS CURRENT (I_{B+}, I_{B-}) vs. COMMON-MODE VOLTAGE



SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



50MHz RESPONSE

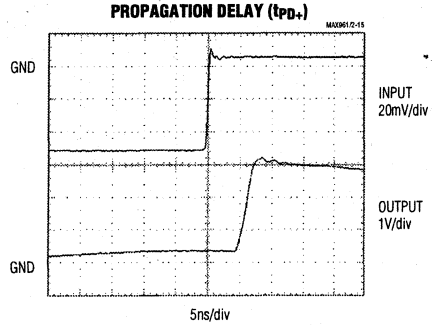


Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

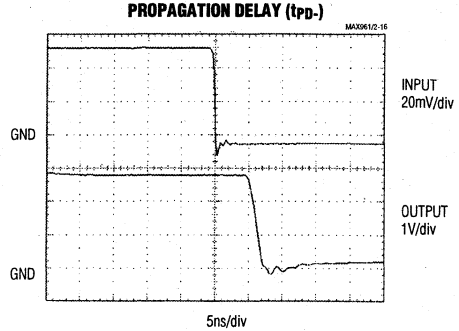
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, 5mV of overdrive, T_A = +25°C, unless otherwise noted.)

PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



Pin Description

PIN				NAME	FUNCTION
MAX961	MAX962	MAX963	MAX964		
2	2	1	1	INA-	Comparator A Inverting Input
1	1	2	2	INA+	Comparator A Noninverting Input
4	—	3, 5	—	LE, LEA, LEB	Latch-Enable Input. The output latches when LE_ is high. The latch is transparent when LE_ is low.
5	5	4, 11	12	GND	Ground
—	—	—	16	N.C.	No Connect. Connect to GND to prevent parasitic feedback.
—	4	6	3	INB-	Comparator B Inverting Input
—	3	7	4	INB+	Comparator B Noninverting Input
—	—	—	5	INC-	Comparator C Inverting Input
—	—	—	6	INC+	Comparator C Noninverting Input
—	—	—	7	IND-	Comparator D Inverting Input
—	—	—	8	IND+	Comparator D Noninverting Input
3	—	8	9	SHDN	Shutdown Input. The device shuts down when SHDN is high.
—	6	9	14	QB	Comparator B Output
—	—	—	11	QC	Comparator C Output
—	—	—	10	QD	Comparator D Output
—	—	10	—	$\overline{QB}$	Comparator B Complementary Output
8	8	12	13	V_{CC}	Positive Supply Input (V_{CC} to GND must be ≤5.5V)
6	7	13	15	QA	Comparator A TTL Output
7	—	14	—	$\overline{QA}$	Comparator A Complementary Output

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

Detailed Description

The MAX961–MAX964 single-supply comparators feature internal hysteresis, ultra-high-speed operation, and low power consumption. Their outputs are guaranteed to pull within 0.52V of either rail without external pull-up or pull-down circuitry. Rail-to-Rail input voltage range and low-voltage, single-supply operation make these devices ideal for portable equipment. The MAX961–MAX964 all interface directly to CMOS logic.

Timing

Most high-speed comparators oscillate in the linear region because of noise or undesirable parasitic feedback. This can occur when the voltage on one input is close to or equal to the voltage on the other input. These devices have a small amount of internal hysteresis to counter parasitic effects and noise.

The added hysteresis of the MAX961–MAX964 creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 1). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs. Standard comparators require hysteresis to be added with external resistors. The MAX961–MAX964's fixed internal hysteresis eliminates these resistors.

Figure 1 illustrates the case where IN- is fixed and IN+ is varied. If the inputs were reversed, the figure would look the same, except for an inverted output.

The MAX961/MAX963 include internal latches that allow storage of comparison results. LE has a high input impedance. If LE is low, the latch is transparent (i.e., the comparator operates as though the latch is not present). The comparator's output state is stored when LE is pulled high. All timing constraints must be met when using the latch function (Figure 2).

Input Stage Circuitry

The MAX961–MAX964 include internal protection circuitry that prevents damage to the precision input stage from large differential input voltages. This protection circuitry consists of two groups of three front-to-back diodes between IN+ and IN-, as well as two 200Ω resistors (Figure 3). The diodes limit the differential voltage applied to the comparator's internal circuitry to no more than $3V_F$, where V_F is the diode's forward-voltage drop (about 0.7V at +25°C).

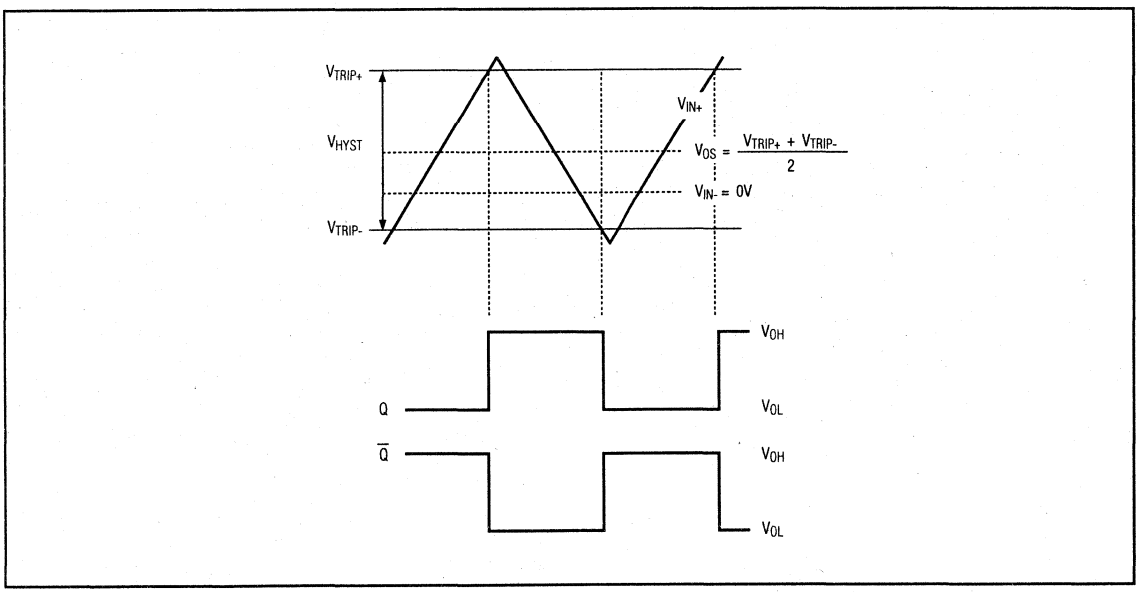


Figure 1. Input and Output Waveforms, Noninverting Input Varied

Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

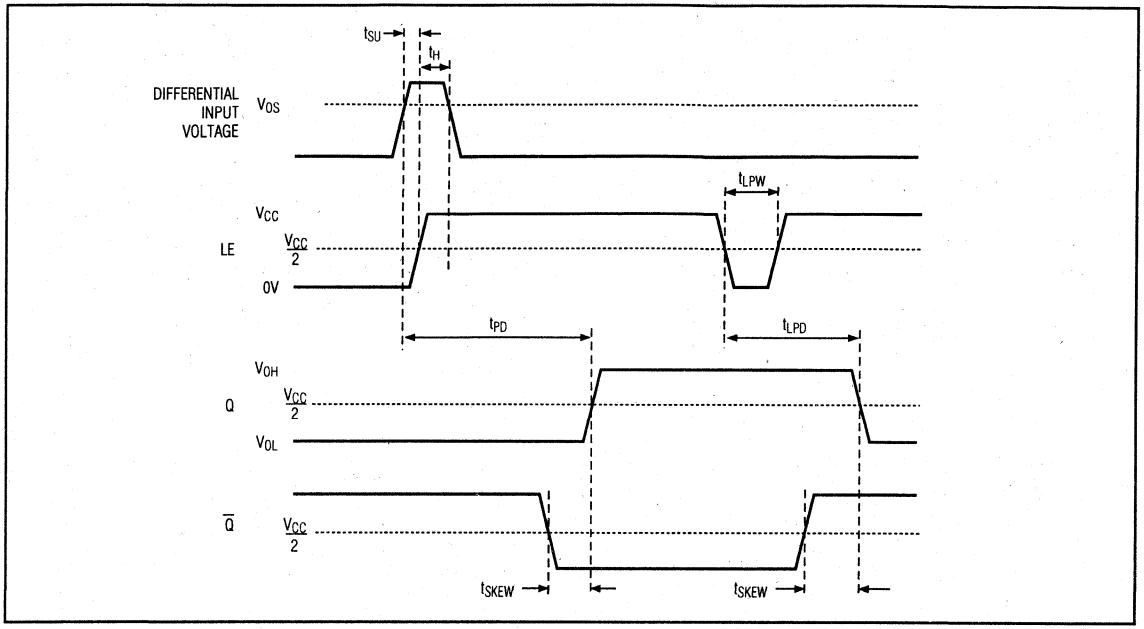


Figure 2. MAX961/MAX963 Timing Diagram

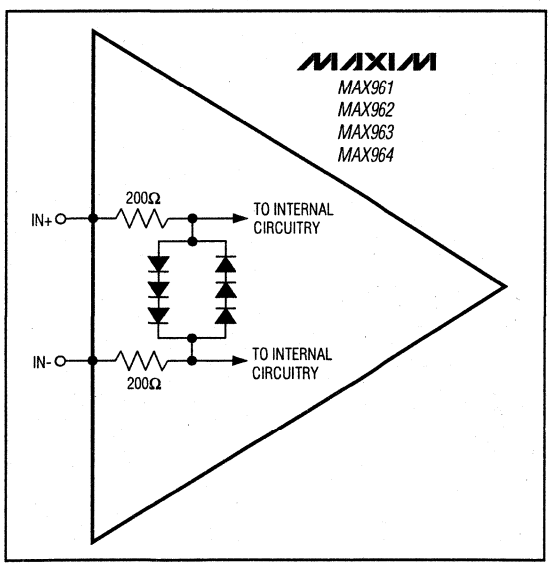


Figure 3. Input Stage Circuitry

For a large differential input voltage (exceeding $3V_F$), this protection circuitry increases the input bias current at IN+ (source) and IN- (sink).

$$\text{Input current} = \frac{(IN+ - IN-) - 3V_F}{2 \times 200}$$

Input currents with large differential input voltages should not be confused with input bias currents (I_B). As long as the differential input voltage is less than $3V_F$, this input current is less than $2I_B$. The protection circuitry also allows for the MAX961–MAX964's input common-mode range to extend beyond both power-supply rails. The output remains in the correct logic state if one or both inputs are within the common-mode range. Taking either input outside the common-mode range causes the input to saturate and the propagation delay to increase.

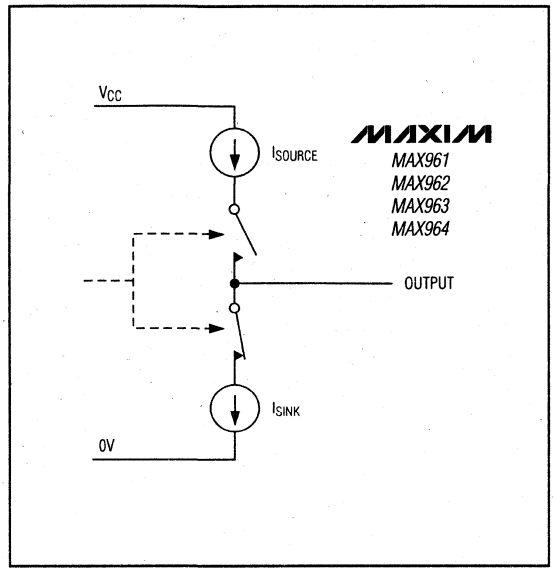


Figure 4. Output Stage Circuitry

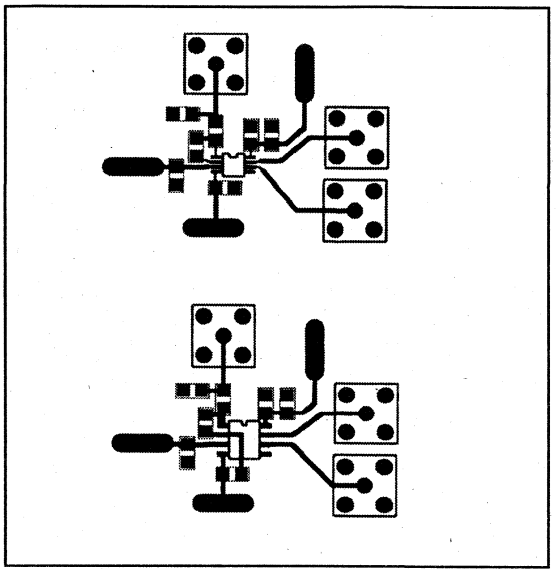


Figure 5. MAX961 PC Board Layout

Output Stage Circuitry

The MAX961–MAX964 contain a current-driven output stage, as shown in Figure 4. During an output transition, I_{SOURCE} or I_{SINK} is pushed or pulled to the output pin. The output source or sink current is high during the transition, creating a rapid slew rate. Once the output voltage reaches V_{OH} or V_{OL}, the source or sink current decreases to a small value, capable of maintaining the V_{OH} or V_{OL} in static condition. This decrease in current conserves power after an output transition has occurred.

One consequence of a current-driven output stage is a linear dependence between the slew rate and the load capacitance. A heavy capacitive load slows down the voltage output transition. This is useful in noise-sensitive applications, where fast edges may cause interference.

Shutdown Mode

When SHDN is high, the MAX961/MAX963/MAX964 shut down. When shut down, the supply current drops to 270µA per comparator, and the outputs become high impedance. SHDN has a high input impedance. Connect SHDN to GND for normal operation. Exit shutdown with LE low; otherwise, the output is indeterminate.

Applications Information

Circuit Layout and Bypassing

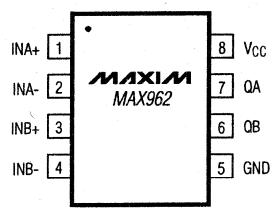
The MAX961–MAX964's high bandwidth requires a high-speed layout:

1) Use a printed circuit board with a good, unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic surface-mount capacitor is a good choice) as close to V_{CC} as possible.
3) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators. Keep inputs away from outputs. Keep impedance between the inputs low.
4) Solder the device directly to the printed circuit board rather than using a socket.
5) Figure 5 depicts the recommended circuit layout.
6) For slow-moving input signals, take care to prevent parasitic feedback. A small capacitor (1000pF or less) placed between the inputs can help eliminate oscillations in the transition region. This capacitor causes negligible degradation to t_{PD} when the source impedance is low.

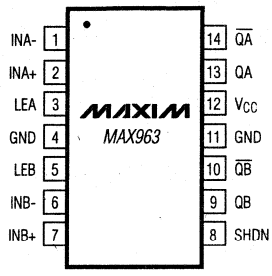
Ultra-High-Speed, +3V/+5V, Rail-to-Rail, Single-Supply Comparators

Pin Configurations

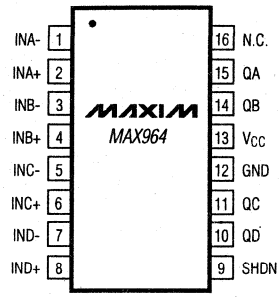
TOP VIEW



SO/µMAX



SO



SO/QSOP

Chip Information

TRANSISTOR COUNT:

MAX961/MAX962: 286

MAX963/MAX964: 607

19-1226; Rev 0; 4/97

MAXIM

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

General Description

The MAX965–MAX970 single/dual/quad micropower comparators feature Rail-to-Rail® inputs and outputs, and fully specified single-supply operation down to +1.6V. These devices draw less than 5µA per comparator and have open-drain outputs that can be pulled beyond V_{CC} to 6V (max) above ground. In addition, their rail-to-rail input common-mode voltage range makes these comparators suitable for ultra-low-voltage operation.

A +1.6V to +5.5V single-supply operating voltage range makes the MAX965 family of comparators ideal for 2-cell battery-powered applications. The MAX965/MAX967/MAX968/MAX969 offer programmable hysteresis and an internal 1.235V ±1.5% reference. All devices are available in either space-saving 8-pin µMAX or 16-pin QSOP packages.

Applications

2-Cell Battery-Powered/Portable Systems
Window Comparators
Threshold Detectors/Discriminators
Mobile Communications
Voltage-Level Translation
Ground/Supply-Sensing Applications

Selector Guide

PART	INTERNAL REFERENCE	COMPARATORS PER PACKAGE	PROGRAMMABLE HYSTERESIS
MAX965	Yes	1	Yes
MAX966	No	2	No
MAX967	Yes	2	Yes
MAX968	Yes	2	Yes
MAX969	Yes	4	Yes
MAX970	No	4	No

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Features

- ♦ **Ultra-Low Single-Supply Operation down to +1.6V**
- ♦ **Rail-to-Rail Common-Mode Input Voltage Range**
- ♦ **3µA Quiescent Supply Current per Comparator**
- ♦ **Open-Drain Outputs Swing Beyond V_{CC}**
- ♦ **1.235V ±1.5% Precision Internal Reference (MAX965/967/968/969)**
- ♦ **10µs Propagation Delay (50mV overdrive)**
- ♦ **Available in Space-Saving Packages:**
  8-Pin µMAX (MAX965–MAX968)
  16-Pin QSOP (MAX969/MAX970)

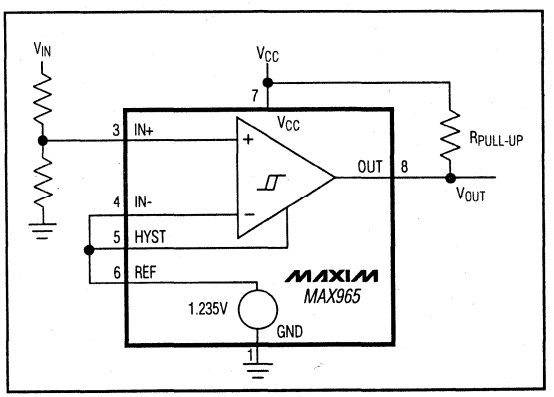
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX965ESA	-40°C to +85°C	8 SO
MAX965EUA	-40°C to +85°C	8 µMAX
MAX966ESA	-40°C to +85°C	8 SO
MAX966EUA	-40°C to +85°C	8 µMAX
MAX967ESA	-40°C to +85°C	8 SO
MAX967EUA	-40°C to +85°C	8 µMAX

Ordering Information continued on last page.

Pin Configurations appear at end of data sheet.

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....+6V
Voltages
  IN_-, IN_+, REF, HYST .....-0.3V to (V_{CC} + 0.3V)
  OUT_ .....-0.3V to +6.0V
Duration of OUT_ Short Circuit to GND or V_{CC} .....Continuous
Continuous Power Dissipation
  8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
  8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
  14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
  16-Pin SO (derate 8.70mW/°C above +70°C).....696mW
  16-Pin QSOP (derate 5.70mW/°C above +70°C).....457mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.6V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLIES								
Supply Voltage Range	V_{CC}	All packages, T_A = 0°C to +85°C			1.6		5.5	V
		SO/QSOP packages, T_A = -40°C to +85°C			1.7		5.5	
		µMAX package, T_A = -40°C to +85°C			1.8		5.5	
Comparator Minimum Operating Voltage						1.0		V
Supply Current	I_{CC}	MAX965				7.0	12	µA
		MAX966				6.0	10	
		MAX967/MAX968				10	16	
		MAX969				14	22	
		MAX970				11	18	
Power-Up Time (V_{CC} to output valid)		V_{CC} stepped 0V to 5V				20		µs
COMPARATOR								
Power-Supply Rejection Ratio	PSRR	1.7V ≤ V_{CC} ≤ 5.5V				0.1	1.0	mV/V
Common-Mode Voltage Range	V_{CMR}	T_A = +25°C			-0.25		V_{CC}	V
		T_A = -40°C to +85°C			-0.25		V_{CC} - 0.25	V
Input Offset Voltage	V_{OS}	Common-mode range = -0.25V to 1.3V, V_{CC} > 1.8V	SO package				3.0	mV
			QSOP package				4.0	
			µMAX package	0°C to +85°C			4.0	
				-40°C to +85°C			6.0	
		Full common-mode range	SO package				7.0	
			QSOP package				10.0	
			µMAX package	0°C to +85°C			10.0	
				-40°C to +85°C			15.0	
Input Hysteresis	V_{HYST}	HYST = REF				±1		mV
Input Bias Current	I_B	Common-mode range = -0.25V to (V_{CC} - 0.25V)				0.001	±5	nA
		Full common-mode range, T_A = +25°C				0.001	±50	
Input Offset Current	I_{OS}					0.2		pA
Input Capacitance	C_{IN}					7.0		pF

ELECTRICAL CHARACTERISTICS (continued)

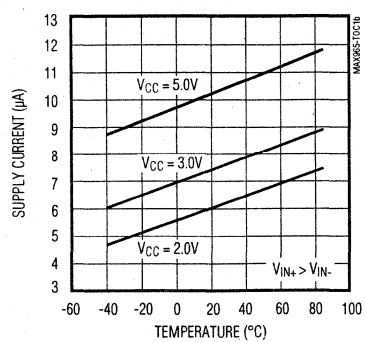
(V_{CC} = +1.6V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR				1.5	4.0	mV/V
HYST Input Voltage Range				V_{REF} - 0.05		V_{REF}	V
HYST Input Leakage	I_{HYST}					±5	nA
Hysteresis Gain					1.0		V/V
Input Voltage Noise	e_n	f = 100Hz to 100kHz, C_{REF} = 1000pF			10		μV_{RMS}
OUT Output Voltage Low	V_{OL}	I_{OUT} = 100µA, 1.6V < V_{CC} < 2.7V				0.2	V
		I_{OUT} = 500µA, 2.7V < V_{CC} < 5.5V				0.4	
Propagation Delay	t_{PD-}	$R_{PULL-UP}$ = 1MΩ, C_{LOAD} = 15pF, high to low	10mV overdrive		20		µs
			50mV overdrive		10		
REFERENCE							
Reference Voltage	V_{REF}	SO package		1.125	1.235	1.255	V
		QSOP package		1.205	1.235	1.265	
		µMAX package, T_A = 0°C to +85°C		1.205	1.235	1.265	
		µMAX package, T_A = -40°C to +85°C		1.185	1.235	1.285	
Source Current	I_{REF+}	HYST = REF		15	50		µA
Sink Current	I_{REF-}			200	400		nA
Output Voltage Noise		f = 100Hz to 100kHz, C_{REF} = 0.1µF			10		μV_{RMS}

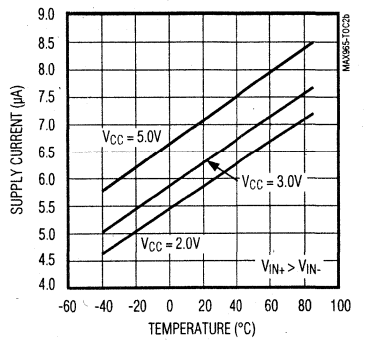
Typical Operating Characteristics

(V_{CC} = +3.0V, $R_{PULL-UP}$ = 100kΩ, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

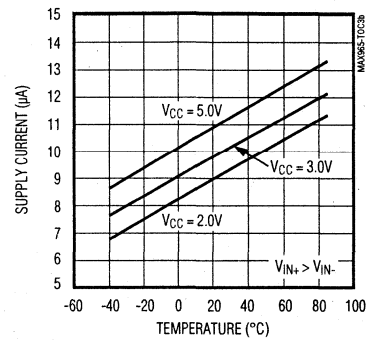
MAX965 SUPPLY CURRENT vs. TEMPERATURE



MAX966 SUPPLY CURRENT vs. TEMPERATURE



MAX967/MAX968 SUPPLY CURRENT vs. TEMPERATURE

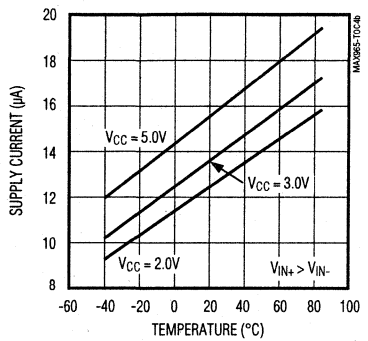


Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

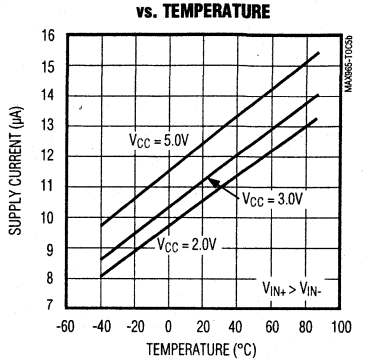
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, $R_{PULL-UP}$ = 100kΩ, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

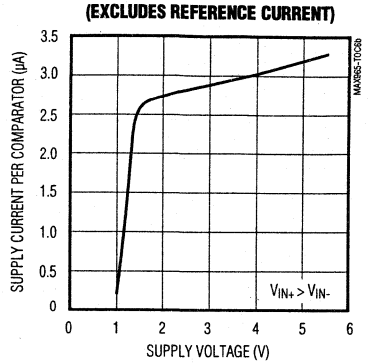
MAX969 SUPPLY CURRENT vs. TEMPERATURE



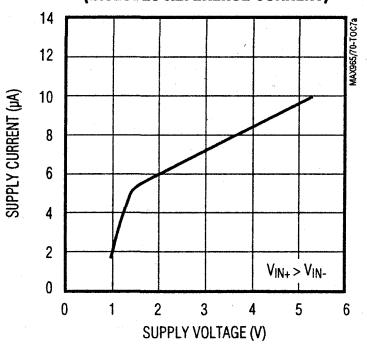
MAX970 SUPPLY CURRENT vs. TEMPERATURE



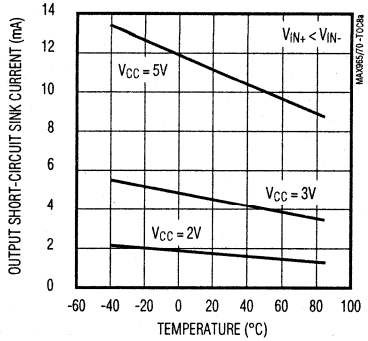
SUPPLY CURRENT PER COMPARATOR vs. SUPPLY VOLTAGE (EXCLUDES REFERENCE CURRENT)



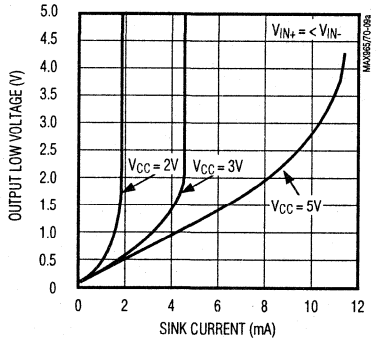
MAX965 SUPPLY CURRENT vs. SUPPLY VOLTAGE (INCLUDES REFERENCE CURRENT)



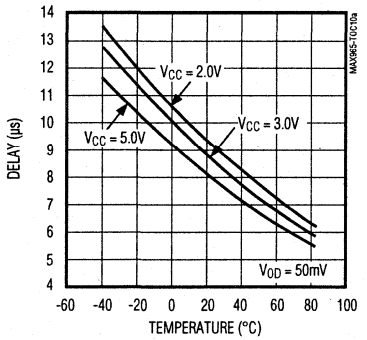
COMPARATOR OUTPUT SHORT-CIRCUIT SINK CURRENT vs. TEMPERATURE



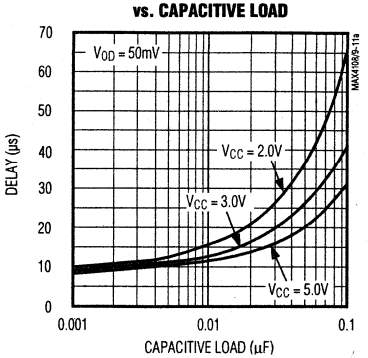
COMPARATOR OUTPUT LOW VOLTAGE vs. SINK CURRENT



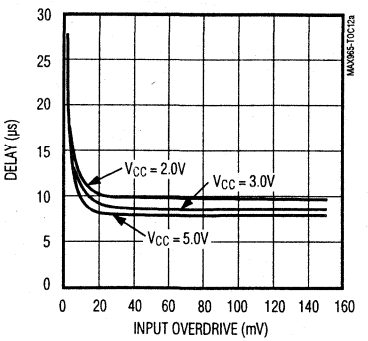
PROPAGATION DELAY (t_{PD-}) vs. TEMPERATURE



PROPAGATION DELAY (t_{PD-}) vs. CAPACITIVE LOAD



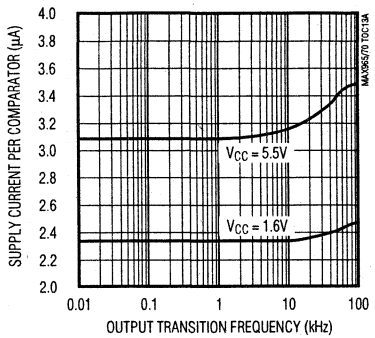
PROPAGATION DELAY (t_{PD-}) vs. INPUT OVERDRIVE



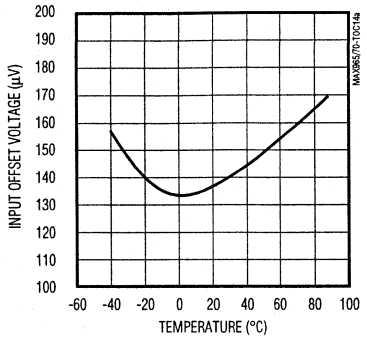
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, $R_{PULL-UP}$ = 100kΩ, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

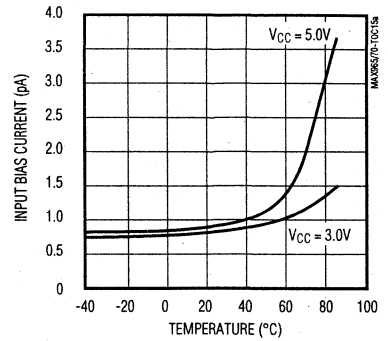
SUPPLY CURRENT PER COMPARATOR vs. OUTPUT TRANSITION FREQUENCY



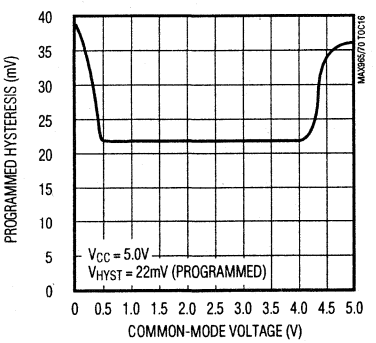
INPUT OFFSET VOLTAGE vs. TEMPERATURE



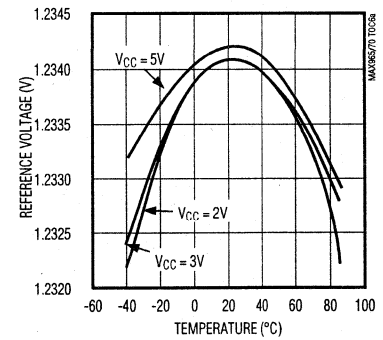
INPUT BIAS CURRENT vs. TEMPERATURE



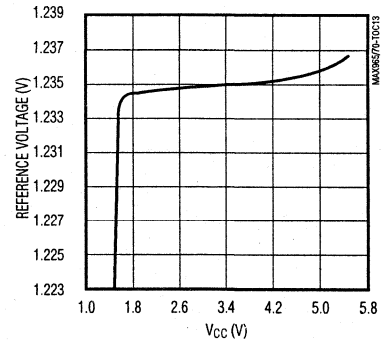
PROGRAMMED HYSTERESIS vs. COMMON-MODE VOLTAGE



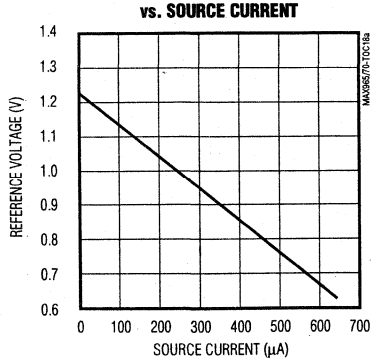
REFERENCE VOLTAGE vs. TEMPERATURE



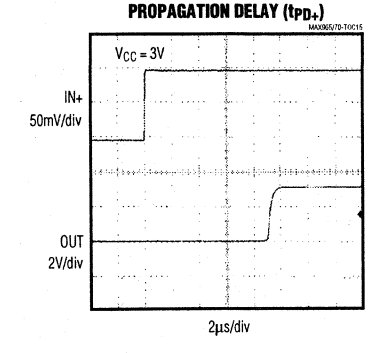
REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



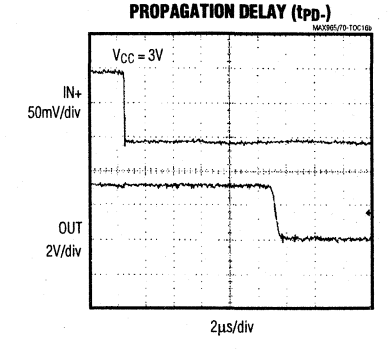
REFERENCE VOLTAGE vs. SOURCE CURRENT



PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})

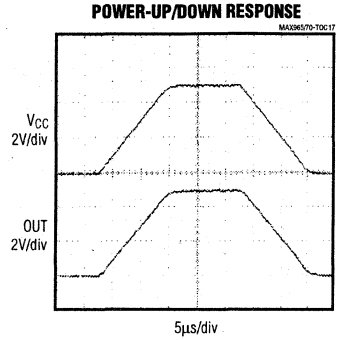


Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

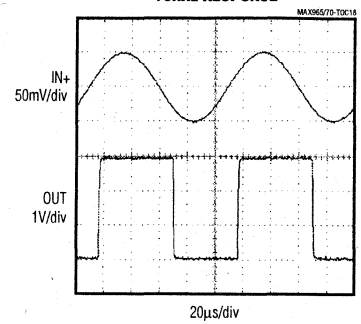
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V, $R_{PULL-UP}$ = 100kΩ, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

POWER-UP/DOWN RESPONSE



10kHz RESPONSE



Pin Descriptions

MAX965–MAX968

PIN				NAME	FUNCTION
MAX965	MAX966	MAX967	MAX968		
—	1	1	1	OUTA	Comparator A Open-Drain Output
1	2	2	2	GND	Ground
2	—	—	—	N.C.	No Connection. Not internally connected.
3	—	—	—	IN+	Comparator Noninverting Input
—	3	3	3	INA+	Comparator A Noninverting Input
4	—	—	—	IN-	Comparator Inverting Input
—	4	—	—	INA-	Comparator A Inverting Input
—	5	—	4	INB-	Comparator B Inverting Input
—	6	4	—	INB+	Comparator B Noninverting Input
5	—	5	5	HYST	Hysteresis Input. Connect HYST to REF if not used. Input voltage range is from V_{REF} to (V_{REF} - 50mV).
6	—	6	6	REF	Internal Reference Output. Typically 1.235V with respect to GND.
7	7	7	7	V_{CC}	Positive Supply Voltage, +1.6V to +5.5V
8	—	—	—	OUT	Comparator Open-Drain Output
—	8	8	8	OUTB	Comparator B Open-Drain Output

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

Pin Descriptions (continued)

MAX969/MAX970

PIN			NAME	FUNCTION
MAX969	MAX970			
	SO	QSOP		
1	1	1	OUTB	Comparator B Open-Drain Output
2	2	2	OUTA	Comparator A Open-Drain Output
3	3	3	VCC	Positive Supply Voltage, +1.6V to +5.5V
4	4	4	INA-	Comparator A Inverting Input
5	5	5	INA+	Comparator A Noninverting Input
6	6	6	INB-	Comparator B Inverting Input
7	7	7	INB+	Comparator B Noninverting Input
—	—	8, 9	N.C.	No Connection. Not internally connected.
8	—	—	REF	Internal Reference Output. Typically 1.235V with respect to GND.
9	—	—	HYST	Hysteresis Input. Connect to REF if not used. Input voltage range is from (V_{REF} - 50mV) to V_{REF}.
10	8	10	INC-	Comparator C Inverting Input
11	9	11	INC+	Comparator C Noninverting Input
12	10	12	IND-	Comparator D Inverting Input
13	11	13	IND+	Comparator D Noninverting Input
14	12	14	GND	Ground
15	13	15	OUTD	Comparator D Open-Drain Output
16	14	16	OUTC	Comparator C Open-Drain Output

Detailed Description

The MAX965–MAX970 single/dual/quad, micropower, ultra-low-voltage comparators feature Rail-to-Rail® inputs and outputs and an internal 1.235V ±1.5% bandgap reference. These devices operate from a single +1.6V to +5.5V supply voltage range, and consume less than 5µA supply current per comparator over the extended temperature range. Internal hysteresis is programmable up to ±50mV using two external resistors and the device's internal reference. The rail-to-rail input common-mode voltage range and the open-drain outputs allow easy voltage-level conversion for multivoltage systems. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail.

The MAX965 is a single comparator with adjustable hysteresis and a reference output pin. The MAX966 is a dual comparator without the reference and without adjustable hysteresis. The MAX967 is a dual comparator configured as a dual voltage monitor with common hysteresis adjustment and a reference output. The dual MAX968 is similar to the MAX967, but is configured as a window comparator. The MAX969 is a quad comparator with a common hysteresis adjustment and a reference output pin. The MAX970 is a quad comparator without a reference and without hysteresis adjustment. (See *Functional Diagrams* and *Selector Guide*.)

Comparator Input

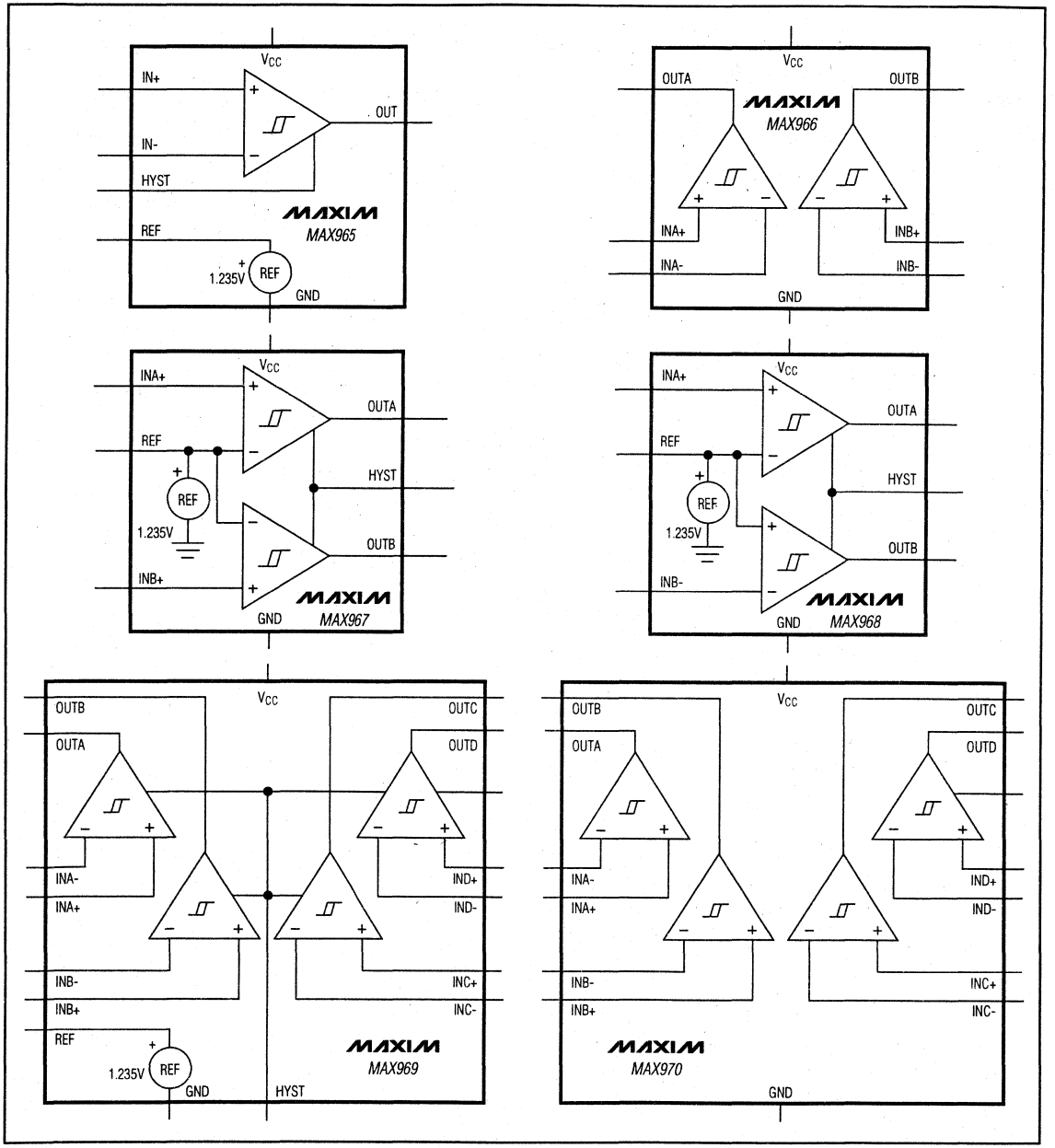
The MAX965–MAX970 have a -0.25V to V_{CC} input common-mode range. Both comparator inputs may operate at any differential voltage within the common-mode voltage range, and the comparator displays the correct output logic state.

Low-Voltage Operation: V_{CC} Down to 1V

The minimum operating voltage is 1.6V. As the supply voltage falls below 1.6V, performance degrades and supply current falls. The reference does not

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

Functional Diagrams



function below about 1.5V, although the comparators typically continue to operate with a supply voltage as low as 1V. At low supply voltages (<1.6V), the input common-mode range remains rail-to-rail, but the comparator's output sink capability is reduced and propagation delay increases (see *Typical Operating Characteristics*).

Figure 1 shows a typical comparator application that monitors V_{CC} at 1.6V. Resistor divider R1/R2 sets the voltage trip point (V_{TRIP}) at 1.6V. As V_{CC} drops below 1.6V and approaches 1V, the reference voltage typically falls below the divider voltage (V+). This causes the comparator output to change state. If OUT's state must be maintained under these conditions, a latching circuit is required.

Comparator Output

The MAX965–MAX970 contain a unique slew-rate-controlled output stage capable of rail-to-rail operation with an external pull-up resistor. Typical comparators consume orders of magnitude more current during switching than during steady-state operation. With the MAX965 family of comparators, during an output transition from high to low, the output slew rate is limited to minimize switching current.

Voltage Reference

With V_{CC} greater than 1.6V but less than 5.5V, the internal 1.235V bandgap reference is ±1.5% accurate over the commercial temperature range and ±2.5% accurate over the extended temperature range. The REF output is typically capable of sourcing 50µA. To reduce reference noise or to provide noise immunity, bypass REF with a capacitor (0.1nF to 0.1µF).

Noise Considerations

The comparator has an effective wideband peak-to-peak noise of around 10µV. The voltage reference has peak-to-peak noise approaching 1.0mV with a 0.1µF bypass capacitor. Thus, when a comparator is used with the reference, the combined peak-to-peak noise is about 1.0mV. This, of course, is much higher than the individual components' RMS noise. Avoid capacitive coupling from any output to the reference pin. Crosstalk can significantly increase the references' actual noise.

Applications Information

Hysteresis

Many comparators oscillate in the linear region of operation because of noise or undesired parasitic feedback. This tends to occur when the voltage on one input is equal or very close to the voltage on the other input. The MAX965–MAX970 have internal hysteresis to counter parasitic effects and noise. In addition, with the use of external resistor, the MAX965/MAX967/MAX968/MAX969's hysteresis can be programmed to as much as ±50mV (see the section *Adding Hysteresis to the MAX965/MAX967/MAX968/MAX969*).

The hysteresis in a comparator creates two trip points: one for the rising input voltage and one for the falling input voltage (Figure 2). The difference between the trip points is the hysteresis. When the comparator's input voltages are equal, the hysteresis effectively causes one comparator input voltage to move quickly past the other, thus taking the input out of the region where oscillation occurs.

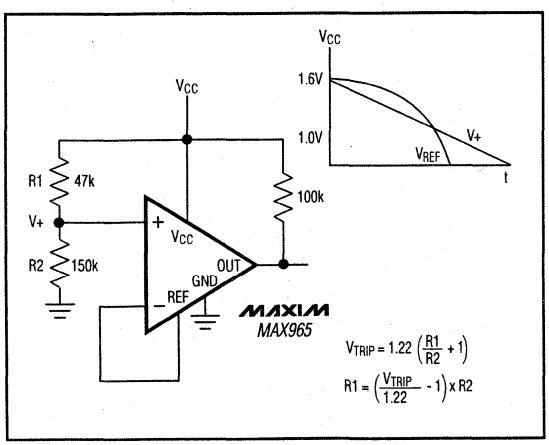


Figure 1. Operation below 1.6V

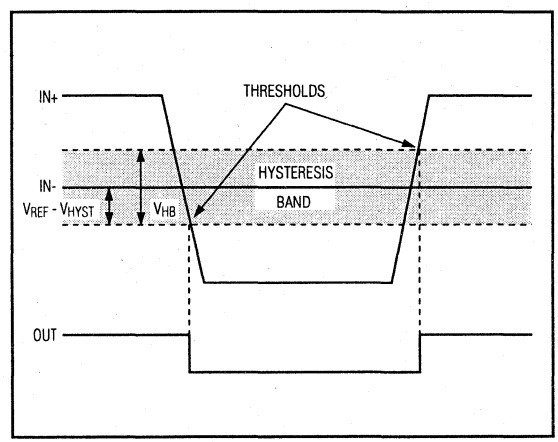


Figure 2. Threshold Hysteresis Band

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

Figure 2 illustrates the case in which IN- has a fixed voltage applied, and IN+ is varied. If the inputs were reversed, the figure would be the same, except with an inverted output.

Adding Hysteresis to the MAX965/MAX967/MAX968/MAX969

To add hysteresis to the MAX965/MAX967/MAX968/MAX969, connect resistor R1 between REF and HYST, and connect resistor R2 between HYST and GND (Figure 3). If additional hysteresis is not required, connect HYST to REF. When hysteresis is added, the upper and lower trip points change by the same amount in opposite directions. The hysteresis band (the difference between the upper and lower trip points, V_{HB}) is approximately twice the voltage between HYST and REF. The HYST input voltage range is from REF down to (REF - 50mV). This yields a hysteresis band from ±1mV to a maximum of ±50mV. Calculate the values of R1 and R2 for the desired hysteresis band with the following formulas:

$$R1 = V_{HB} / I_{REF}$$

$$R2 = (V_{REF} - V_{HB}) / I_{REF}$$

where I_{REF} (the current sourced by the reference) does not exceed the REF source capability (12µA typical), and is significantly larger than the HYST leakage current (5nA typical). I_{REF} values between 0.1µA and 4µA are good choices. If 2.4MΩ is chosen for R2 (I_{REF} = 0.5µA), the equation for R1 and V_{HB} can be approximated as:

$$R1(k\Omega) = 2 \times V_{HB}\ (mV)$$

In the MAX967/MAX968/MAX969, the HYST pin programs the same hysteresis for all comparators in the package.

Due to the internal structure of the input developed for ultra-low-voltage operation, the hysteresis band varies with common-mode voltage. The graph Programmed Hysteresis vs. Common-Mode Voltage in the *Typical Operating Characteristics* shows this variation. Notice that the hysteresis band increases to almost twice the calculated value toward the ends of the common-mode range. This is apparent only when programming additional hysteresis using the HYST pin. The hysteresis band is constant when HYST is connected to REF.

Adding Hysteresis to the MAX966/MAX970

The MAX966/MAX970 do not have a HYST pin for programming hysteresis. Hysteresis can be generated with three resistors using positive feedback (Figure 4). This method generally draws more current than the method using the HYST pin on the MAX965/MAX967/MAX968/MAX969. Also, the positive feedback method slows hysteresis response time. Use the following procedure to calculate the resistor values:

1) Select R3. The leakage current of IN+ is under 5nA, so the current through R3 should be at least 500nA to minimize errors caused by leakage current. The current through R3 at the trip point is (V_{REF} - V_{OUT}) / R3. Taking into consideration the two possible output states and solving for R3 yields two formulas:

   $$R3 = V_{REF} / 500nA$$

   and

   $$R3 = (V_{REF} - V_{CC}) / 500nA$$

   Use the smaller of the two resulting resistor values. For example, if V_{REF} = 1.2V and V_{CC} = 5.0V, then the two resistor values are 2.4MΩ and 7.6mΩ. For R3, choose the 2.2MΩ standard value.

2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.

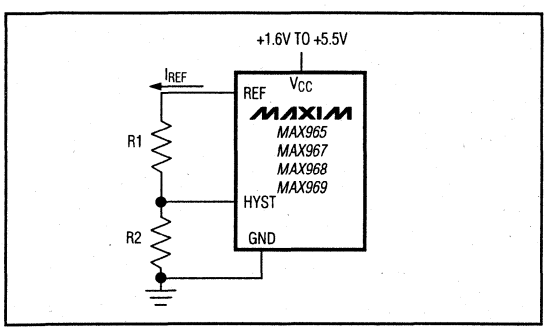


Figure 3. Programming the HYST Pin

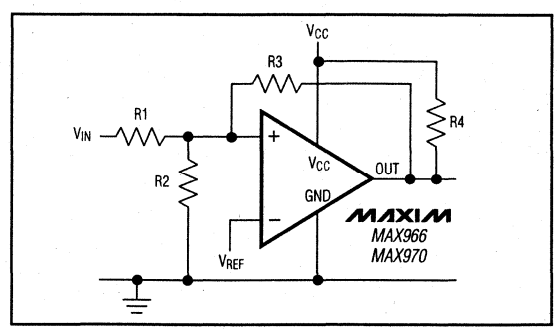


Figure 4. External Hysteresis

3) Calculate R1: R1 = (R3 + R4) x (V_{HB} / V_{CC}). Putting in the values for this example, R1 = (2.2MΩ + 10k) x (50mV / 5.0V) = 22.1kΩ.

4) Choose the trip point for V_{IN} rising. This is the threshold voltage where the comparator output transitions from low to high as V_{IN} rises above the trip point. For this example, choose 3.0V.

5) Calculate R2 as follows:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3 + R4}}$$

$$R2 = \frac{1}{\left(\frac{3.0V}{1.2 \times 22k}\right) - \frac{1}{22k} - \frac{1}{2.2M + 10k}} = 14.76k$$

where V_{THR} is the rising-voltage trip threshold. Choose a standard value of 15kΩ.

6) Verify trip voltages and hysteresis as follows:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3 + R4}\right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3 + R4}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

where V_{THR} is the rising-voltage trip point, and V_{THF} is the falling-voltage trip point.

Circuit Layout and Bypassing

Power-supply bypass capacitors are not needed if supply impedance is low, but 100nF bypass capacitors should be used when supply impedance is high or when supply leads are long. Minimize signal lead lengths to reduce stray capacitance between the input and output that might cause instability.

IR Receiver

Figure 5 shows an application using the MAX965 as an infrared receiver. The infrared photodiode creates a current relative to the amount of infrared light present. This current creates a voltage across R1. When this voltage level crosses the reference voltage applied to the inverting input, the output transitions. Optional R3 provides additional hysteresis for noise immunity.

2-Cell to TTL Logic-Level Shifter

Figure 6 shows an application using the MAX965 to convert a 2-cell voltage-level signal into a TTL-compatible signal. The supply voltage for the comparator comes from the 2-cell supply. The output is pulled up to a 5V supply.

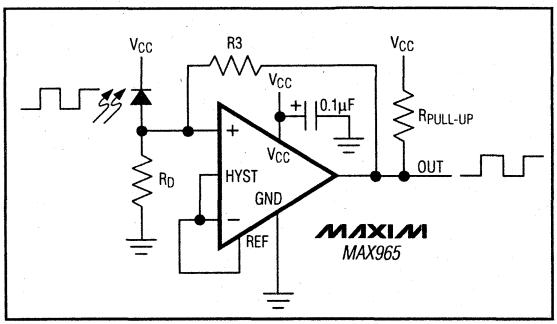


Figure 5. IR Receiver

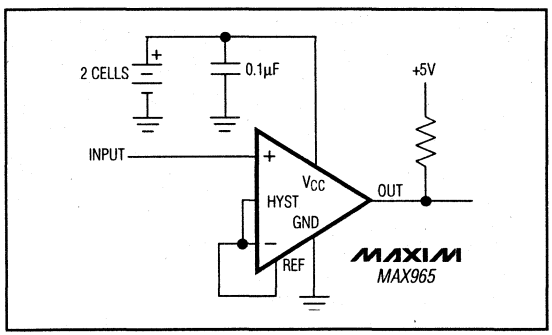


Figure 6. 2-Cell to TTL Logic-Level Translator

Single/Dual/Quad, Micropower, Ultra-Low-Voltage, Rail-to-Rail I/O Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....+6V
Voltages
  IN_-, IN_+, REF, HYST .....-0.3V to (V_{CC} + 0.3V)
  OUT_ .....-0.3V to +6.0V
Duration of OUT_ Short Circuit to GND or V_{CC}.....Continuous
Continuous Power Dissipation
  8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
  8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW
  14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
  16-Pin SO (derate 8.70mW/°C above +70°C).....696mW
  16-Pin QSOP (derate 5.70mW/°C above +70°C).....457mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +1.6V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = 3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER SUPPLIES								
Supply Voltage Range	V_{CC}	All packages, T_A = 0°C to +85°C			1.6		5.5	V
		SO/QSOP packages, T_A = -40°C to +85°C			1.7		5.5	
		µMAX package, T_A = -40°C to +85°C			1.8		5.5	
Comparator Minimum Operating Voltage						1.0		V
Supply Current	I_{CC}	MAX965				7.0	12	µA
		MAX966				6.0	10	
		MAX967/MAX968				10	16	
		MAX969				14	22	
		MAX970				11	18	
Power-Up Time (V_{CC} to output valid)		V_{CC} stepped 0V to 5V				20		µs
COMPARATOR								
Power-Supply Rejection Ratio	PSRR	1.7V ≤ V_{CC} ≤ 5.5V				0.1	1.0	mV/V
Common-Mode Voltage Range	V_{CMR}	T_A = +25°C			-0.25		V_{CC}	V
		T_A = -40°C to +85°C			-0.25		V_{CC} - 0.25	V
Input Offset Voltage	V_{OS}	Common-mode range = -0.25V to 1.3V, V_{CC} > 1.8V	SO package				3.0	mV
			QSOP package				4.0	
			µMAX package	0°C to +85°C			4.0	
				-40°C to +85°C			6.0	
		Full common-mode range	SO package				7.0	
			QSOP package				10.0	
			µMAX package	0°C to +85°C			10.0	
				-40°C to +85°C			15.0	
Input Hysteresis	V_{HYST}	HYST = REF				±1		mV
Input Bias Current	I_B	Common-mode range = -0.25V to (V_{CC} - 0.25V)				0.001	±5	nA
		Full common-mode range, T_A = +25°C				0.001	±50	
Input Offset Current	I_{OS}					0.2		pA
Input Capacitance	C_{IN}					7.0		pF

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Single/Dual/Quad, High-Speed, Low-Power, +3V/+5V Rail-to-Rail Comparators

General Description

The MAX976/MAX978/MAX998 dual/quad/single, high-speed comparators are optimized for +3V/+5V single-supply applications. These devices achieve a 20ns propagation delay while drawing only 300µA of supply current. They have a common-mode voltage range that extends 200mV beyond ground. The differential input voltage range extends Rail-to-Rail®. The outputs swing rail-to-rail without external pull-up circuitry, making these devices ideal for both CMOS and TTL logic. All inputs and outputs can tolerate a continuous short-circuit fault condition to either rail. The comparator's internal hysteresis ensures clean output switching, even with slow-moving input signals.

The MAX998 is available in a space-saving 6-pin SOT23 package. The dual MAX976 is available in 8-pin SO and µMAX packages, while the quad MAX978 is available in 16-pin SO and QSOP packages.

Applications

GPS Receivers
Battery-Powered Systems
Threshold Detectors/Discriminators
Single 3V/5V Systems
IR Receivers
Digital-Line Receivers
Zero-Crossing Detectors

Features

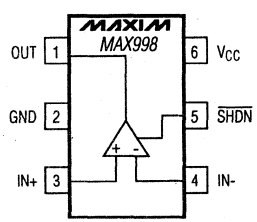
- ♦ **20ns Propagation Delay (5mV overdrive)**
- ♦ **300µA Supply Current**
- ♦ **+3V/+5V Single-Supply Operation**
- ♦ **Rail-to-Rail Outputs**
- ♦ **Input Common Mode Voltage Range Extends 200mV Below Ground**
- ♦ **<1µA Shutdown Supply Current (MAX998)**
- ♦ **Internal Hysteresis for Clean Switching**
- ♦ **Available in Space-Saving Packages:**
  6-pin SOT23-6 (MAX998)
  8-pin µMAX (MAX976)
  16-pin QSOP (MAX978)

Ordering Information

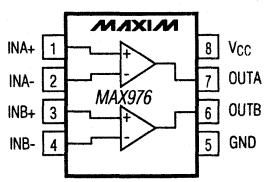
PART	TEMP. RANGE	PIN-PACKAGE
MAX976ESA	-40°C to +85°C	8 SO
MAX976EUA	-40°C to +85°C	8 µMAX
MAX978ESE	-40°C to +85°C	16 SO
MAX978EEE	-40°C to +85°C	16 QSOP
MAX998ESA	-40°C to +85°C	8 SO
MAX998EUT-T	-40°C to +85°C	6 SOT23-6

Pin Configurations

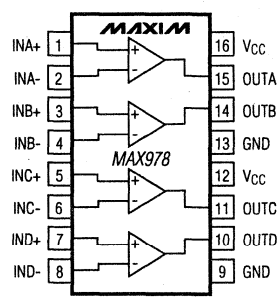
TOP VIEW



SOT23-6



SO/µMAX



SO/QSOP

Pin Configurations continued on next page.

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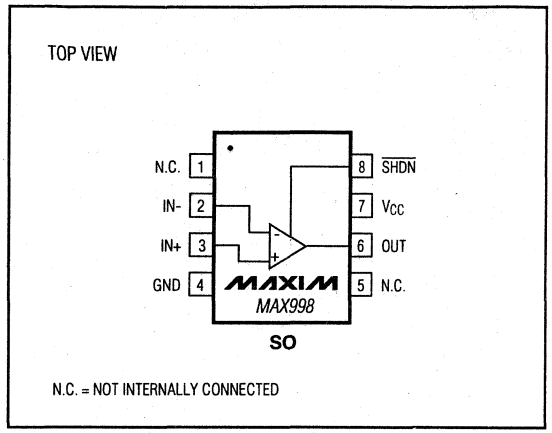
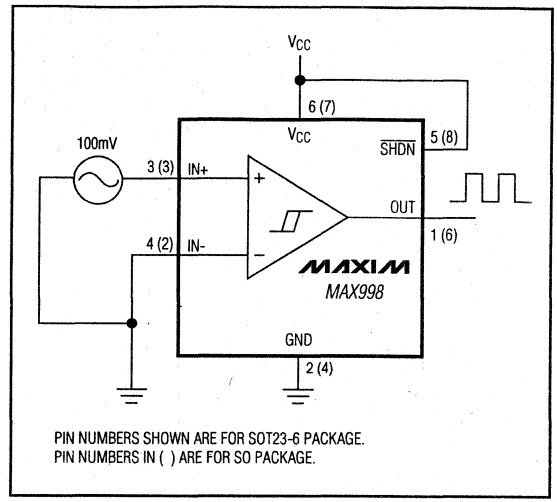
Single/Dual/Quad, High-Speed, Low-Power, +3V/+5V Rail-to-Rail Comparators

Pin Configurations (continued)



Typical Operating Circuit



19-1229; Rev 1; 7/97

MAXIM

Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

General Description

The MAX985/MAX986/MAX989/MAX990/MAX993/MAX994 single/dual/quad micropower comparators feature low-voltage operation and Rail-to-Rail® inputs and outputs. Their operating voltage ranges from +2.5V to +5.5V, making them ideal for both 3V and 5V systems. These comparators also operate with ±1.25V to ±2.75V dual supplies. They consume only 11µA of supply current while achieving a 300ns propagation delay.

The common-mode input voltage range extends 250mV beyond the supply rails. Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The output stage's unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX985/MAX989/MAX993 have a push/pull output stage that sinks as well as sources current. Large internal output drivers allow rail-to-rail output swing with loads up to 8mA. The MAX986/MAX990/MAX994 have an open-drain output stage that can be pulled beyond V_{CC} to 6V (max) above V_{EE}. These open-drain versions are ideal for level translators and bipolar to single-ended converters.

The single MAX985/MAX986 are available in tiny 5-pin SOT23 packages.

Selector Guide

PART	COMPARATORS PER PACKAGE	OUTPUT STAGE	PIN-PACKAGE
MAX985	1	Push/Pull	8 SO/ 5 SOT23-5
MAX986	1	Open-Drain	8 SO/ 5 SOT23-5
MAX989	2	Push/Pull	8 SO/µMAX
MAX990	2	Open-Drain	8 SO/µMAX
MAX993	4	Push/Pull	14 SO
MAX994	4	Open-Drain	14 SO

Applications

Portable/Battery-Powered Systems
Mobile Communications
Zero-Crossing Detectors
Window Comparators
Level Translators
Threshold Detectors/ Discriminators
Ground/Supply Sensing Applications
IR Receivers
Digital Line Receivers

Features

- ♦ **11µA Quiescent Supply Current**
- ♦ **+2.5V to +5.5V Single-Supply Operation**
- ♦ **Common-Mode Input Voltage Range Extends 250mV Beyond the Rails**
- ♦ **300ns Propagation Delay**
- ♦ **Push/Pull Output Stage Sinks and Sources 8mA Current (MAX985/MAX989/MAX993)**
- ♦ **Open-Drain Output Voltage Extends Beyond V_{CC} (MAX986/MAX990/MAX994)**
- ♦ **Unique Output Stage Reduces Output Switching Current, Minimizing Overall Power Consumption**
- ♦ **80µA Supply Current at 1MHz Switching Frequency**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Available in Space-Saving Packages:**
  SOT23 (MAX985/MAX986)
  µMAX (MAX989/MAX990)

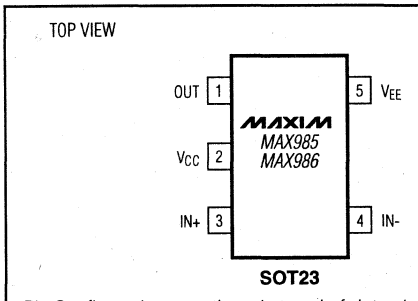
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX985EUK-T	-40°C to +85°C	5 SOT23-5	ABYZ
MAX985ESA	-40°C to +85°C	8 SO	—
MAX986EUK-T	-40°C to +85°C	5 SOT23-5	ABZA
MAX986ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

Typical Application Circuit appears at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

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Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 6V
IN_-, IN_+ to V_{EE} ..... -0.3V to (V_{CC} + 0.3V)
OUT_ to V_{EE}
MAX985/MAX989/MAX993 ..... -0.3V to (V_{CC} + 0.3V)
MAX986/MAX990/MAX994 ..... -0.3V to 6V
OUT_ Short-Circuit Duration to V_{EE} or V_{CC} 10sec

Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.10mW/°C above +70°C) 571mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
14-Pin SO (derate 8.33 mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Inferred from PSRR test			2.5		5.5	V
Supply Current per Comparator	I_{CC}	V_{CC} = 5V	T_A = +25°C			12	20	µA
			T_A = -40°C to +85°C				24	
		V_{CC} = 2.7V	T_A = +25°C			11	20	
			T_A = -40°C to +85°C				24	
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{CC} ≤ 5.5V			55	80		dB
Common-Mode Voltage Range (Note 2)	V_{CMR}	T_A = +25°C			V_{EE} - 0.25		V_{CC} + 0.25	V
		T_A = -40°C to +85°C			V_{EE}		V_{CC}	
Input Offset Voltage (Note 3)	V_{OS}	Full common-mode range	T_A = +25°C			±0.5	±5	mV
			T_A = -40°C to +85°C				±7	
Input Hysteresis	V_{HYST}					±3		mV
Input Bias Current (Note 4)	I_B					0.001	10	nA
Input Offset Current	I_{OS}					0.5		pA
Input Capacitance	C_{IN}					1.0		pF
Common-Mode Rejection Ratio	CMRR				52	80		dB
Output Leakage Current (MAX986/MAX990/ MAX994 only)	I_{LEAK}	V_{OUT} = high					1.0	µA
Output Short-Circuit Current	I_{SC}	Sourcing or sinking, V_{OUT} = V_{EE} or V_{CC}		V_{CC} = 5V		95		mA
				V_{CC} = 2.7V		35		
OUT Output Voltage Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 8mA	T_A = +25°C			0.2	0.4	V
			T_A = -40°C to +85°C				0.55	
		V_{CC} = 2.7V, I_{SINK} = 3.5mA	T_A = +25°C			0.15	0.3	
			T_A = -40°C to +85°C				0.4	
OUT Output Voltage High (MAX985/MAX989/ MAX993 only)	V_{OH}	V_{CC} = 5V, I_{SOURCE} = 8mA	T_A = +25°C		4.6	4.85		V
			T_A = -40°C to +85°C		4.45			
		V_{CC} = 2.7V, I_{SOURCE} = 3.5mA	T_A = +25°C		2.4	2.55		
			T_A = -40°C to +85°C		2.3			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
OUT Rise Time (MAX985/MAX989/ MAX993 only)	t_{RISE}	V_{CC} = 5.0V		C_L = 15pF		40		ns
				C_L = 50pF		50		
				C_L = 200pF		80		
OUT Fall Time	t_{FALL}	V_{CC} = 5.0V		C_L = 15pF		40		ns
				C_L = 50pF		50		
				C_L = 200pF		80		
Propagation Delay	t_{PD-}	C_L = 15pF	MAX985/MAX989/ MAX993 only	10mV overdrive		450		ns
				100mV overdrive		300		
			MAX986/MAX990/ MAX994 only, $R_{PULL-UP}$ = 5.1kΩ	10mV overdrive		450		
				100mV overdrive		300		
	t_{PD+}	MAX985/MAX989/ MAX993 only, C_L = 15pF		10mV overdrive		450		
				100mV overdrive		300		
Power-Up Time	t_{PU}					20		µs

Note 1: The MAX98 _EUK specifications are 100% tested at T_A = +25°C. Limits over the extended temperature range are guaranteed by design, not production tested.

Note 2: Inferred from the V_{OS} test. Either or both inputs can be driven 0.3V beyond either supply rail without output phase reversal.

Note 3: V_{OS} is defined as the center of the hysteresis band at the input.

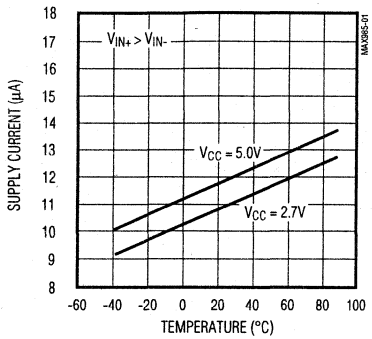
Note 4: I_B is defined as the average of the two input bias currents (I_{B-}, I_{B+}).

Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

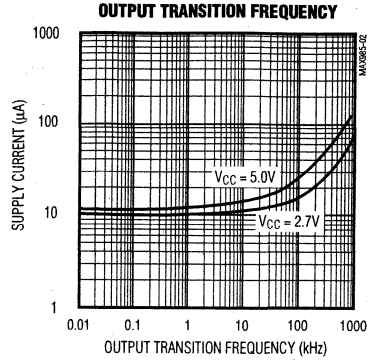
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

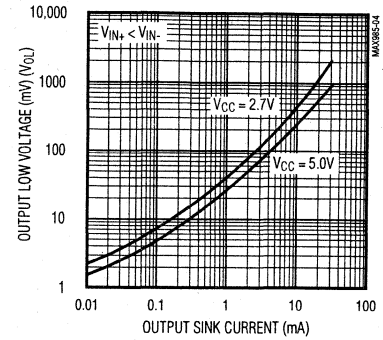
SUPPLY CURRENT vs. TEMPERATURE



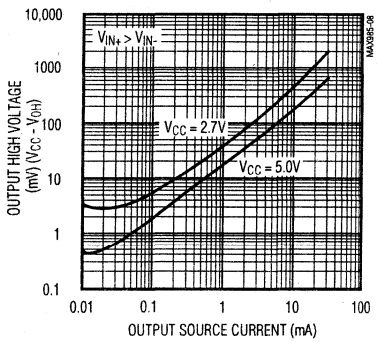
SUPPLY CURRENT vs. OUTPUT TRANSITION FREQUENCY



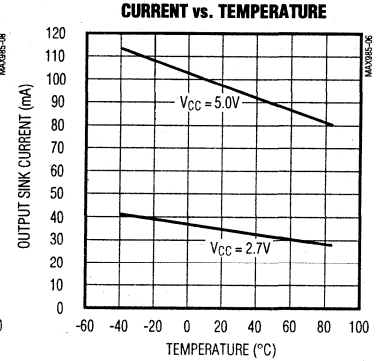
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



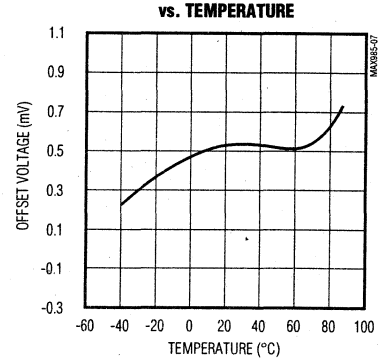
OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



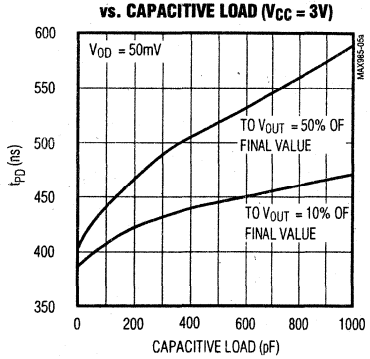
OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE



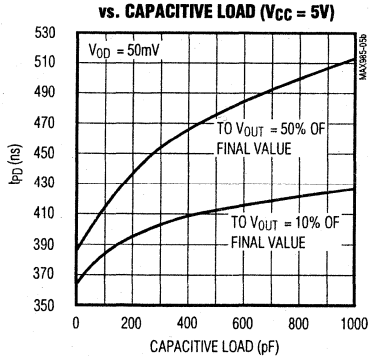
INPUT OFFSET VOLTAGE vs. TEMPERATURE



PROPAGATION DELAY vs. CAPACITIVE LOAD (V_{CC} = 3V)



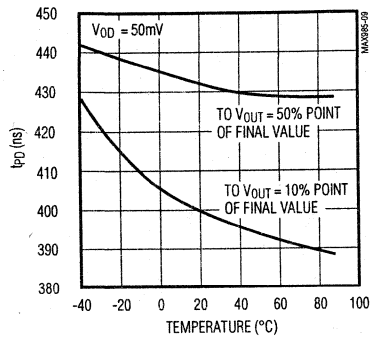
PROPAGATION DELAY vs. CAPACITIVE LOAD (V_{CC} = 5V)



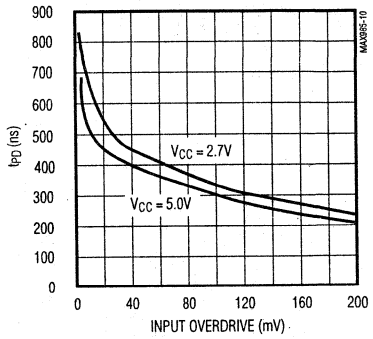
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

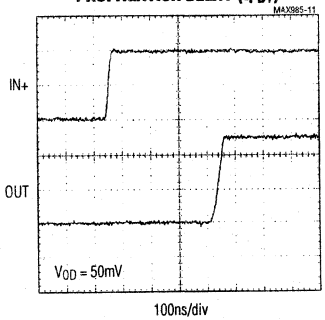
PROPAGATION DELAY vs. TEMPERATURE



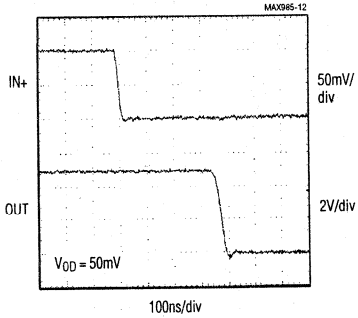
PROPAGATION DELAY vs. INPUT OVERDRIVE



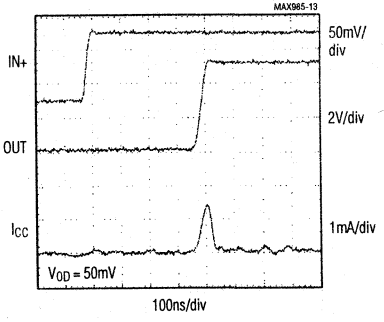
MAX985/MAX989/MAX993 PROPAGATION DELAY (t_{PD+})



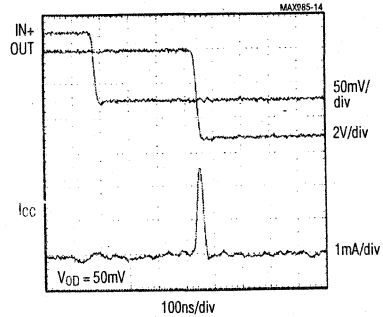
PROPAGATION DELAY (t_{PD-})



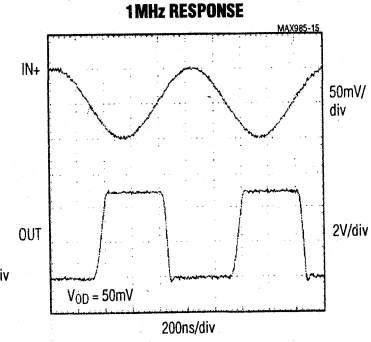
MAX985/MAX989/MAX993 SWITCHING CURRENT, OUT RISING



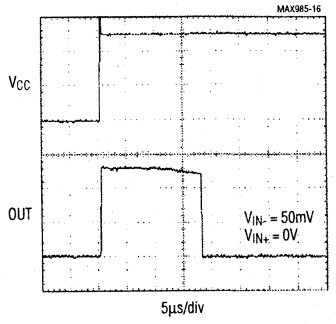
SWITCHING CURRENT, OUT FALLING



1MHz RESPONSE



POWER-UP DELAY



Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Pin Description

PIN				NAME	FUNCTION
MAX985 MAX986		MAX989 MAX990	MAX993 MAX994		
SOT23-5	SO	SO/µMAX	SO		
1	6	—	—	OUT	Comparator Output
2	7	8	4	V_{CC}	Positive Supply Voltage
3	3	—	—	IN+	Comparator Noninverting Input
4	2	—	—	IN-	Comparator Inverting Input
5	4	4	11	V_{EE}	Negative Supply Voltage
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output
—	1, 5, 8	—	—	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX985/MAX986/MAX989/MAX990/MAX993/MAX994 are single/dual/quad low-power, low-voltage comparators. They have an operating supply voltage range between +2.5V and +5.5V and consume only 11µA. Their common-mode input voltage range extends 0.25V beyond each rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals. Large internal output drivers allow rail-to-rail output swing with up to 8mA loads.

The output stage employs a unique design that minimizes supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. The MAX985/MAX989/MAX993 have a push/pull output structure that sinks as well as sources current. The MAX986/MAX990/MAX994 have an open-drain output stage that can be pulled beyond V_{CC} to an absolute maximum of 6V above V_{EE}.

Input Stage Circuitry

The devices' input common-mode range extends from -0.25V to (V_{CC} + 0.25V). These comparators may operate at any differential input voltage within these limits. Input bias current is typically 1.0pA if the input voltage is between the supply rails. Comparator inputs are protected from overvoltage by internal body diodes connected to the supply rails. As the input voltage exceeds the supply rails, these body diodes become forward biased and begin to conduct. Consequently, bias currents increase exponentially as the input voltage exceeds the supply rails.

Output Stage Circuitry

These comparators contain a unique output stage capable of rail-to-rail operation with up to 8mA loads. Many comparators consume orders of magnitude more current during switching than during steady-state operation. However, with this family of comparators, the supply-current change during an output transition is extremely small. The *Typical Operating Characteristics* graph Supply Current vs. Output Transition Frequency shows the minimal supply-current increase as the output switching frequency approaches 1MHz. This characteristic eliminates the need for power-supply filter capacitors to reduce glitches created by comparator switching currents. Another advantage realized in high-speed, battery-powered applications is a substantial increase in battery life.

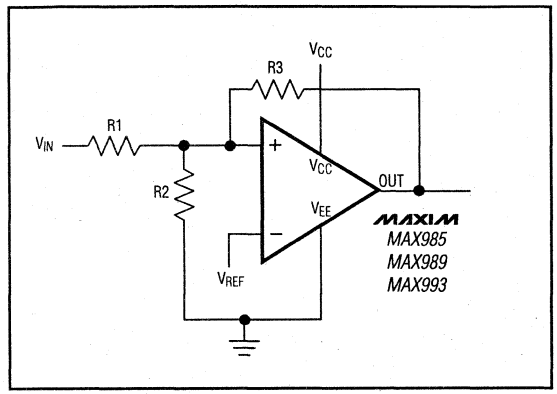


Figure1. Additional Hysteresis (MAX985/MAX989/MAX993)

Applications Information

Additional Hysteresis

MAX985/MAX989/MAX993

The MAX985/MAX989/MAX993 have ±3mV internal hysteresis. Additional hysteresis can be generated with three resistors using positive feedback (Figure 1). Unfortunately, this method also slows hysteresis response time. Use the following procedure to calculate resistor values for the MAX985/MAX989/MAX993.

1) Select R3. Leakage current at IN is under 10nA, so the current through R3 should be at least 1µA to minimize errors caused by leakage current. The current through R3 at the trip point is (V_{REF} - V_{OUT}) / R3. Considering the two possible output states in solving for R3 yields two formulas: R3 = V_{REF} / 1µA or R3 = (V_{REF} - V_{CC}) / 1µA. Use the smaller of the two resulting resistor values. For example, if V_{REF} = 1.2V and V_{CC} = 5V, then the two R3 resistor values are 1.2MΩ and 3.8MΩ. Choose a 1.2MΩ standard value for R3.

2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.

3) Calculate R1 according to the following equation:

$$R1 = R3 \times (V_{HB} / V_{CC})$$

For this example, insert the values R1 = 1.2MΩ x (50mV / 5V) = 12kΩ.

4) Choose the trip point for V_{IN} rising (V_{THR}; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. For this example, choose 3V.

Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

5) Calculate R2 as follows. For this example, choose an 8.2kΩ standard value:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3}}$$

$$R2 = \frac{1}{\left(\frac{3.0V}{1.2 \times 12k\Omega}\right) - \frac{1}{12k\Omega} - \frac{1}{2.2M\Omega}} = 8.03k\Omega$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

MAX986/MAX990/MAX994

The MAX986/MAX990/MAX994 have ±3mV internal hysteresis. They have open-drain outputs and require an external pull-up resistor (Figure 2). Additional hysteresis can be generated using positive feedback, but the formulas differ slightly from those of the MAX985/MAX989/MAX993.

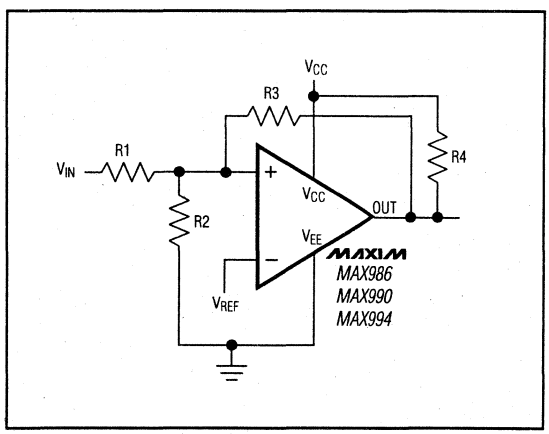


Figure 2. Additional Hysteresis (MAX986/MAX990/MAX994)

Use the following procedure to calculate resistor values:

1) Select R3 according to the formulas R3 = V_{REF} / 500µA or R3 = (V_{REF} - V_{CC}) / 500µA - R4. Use the smaller of the two resulting resistor values.
2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.
3) Calculate R1 according to the following equation:

$$R1 = (R3 + R4) \times (V_{HB} / V_{CC})$$

4) Choose the trip point for V_{IN} rising (V_{THR}; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point.
5) Calculate R2 as follows:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3 + R4}}$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3 + R4}\right)$$

$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3 + R4}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

Board Layout and Bypassing

Power-supply bypass capacitors are not typically needed, but use 100nF bypass capacitors when supply impedance is high, when supply leads are long, or when excessive noise is expected on the supply lines. Minimize signal trace lengths to reduce stray capacitance.

Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Zero-Crossing Detector

Figure 3 shows a zero-crossing detector application. The MAX985's inverting input is connected to ground, and its noninverting input is connected to a 100mVp-p signal source. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

Logic-Level Translator

Figure 4 shows an application that converts 5V logic levels to 3V logic levels. The MAX986 is powered by the +5V supply voltage, and the pull-up resistor for the MAX986's open-drain output is connected to the +3V supply voltage. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translation, simply connect the +3V supply to VCC and the +5V supply to the pull-up resistor.

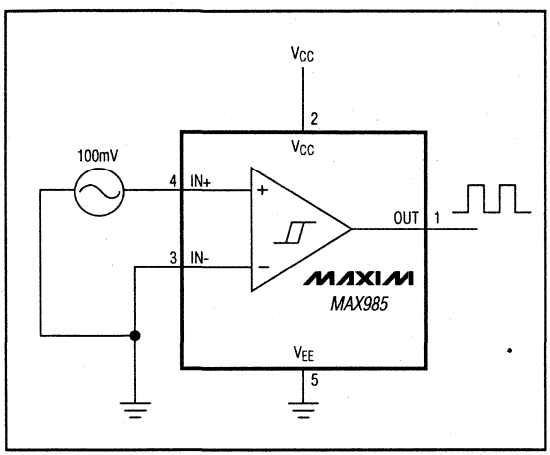


Figure 3. Zero-Crossing Detector

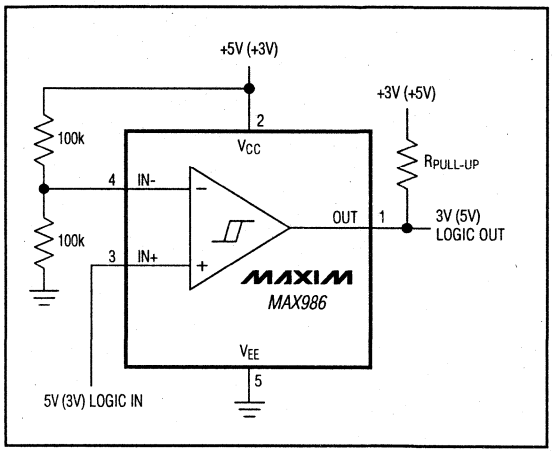
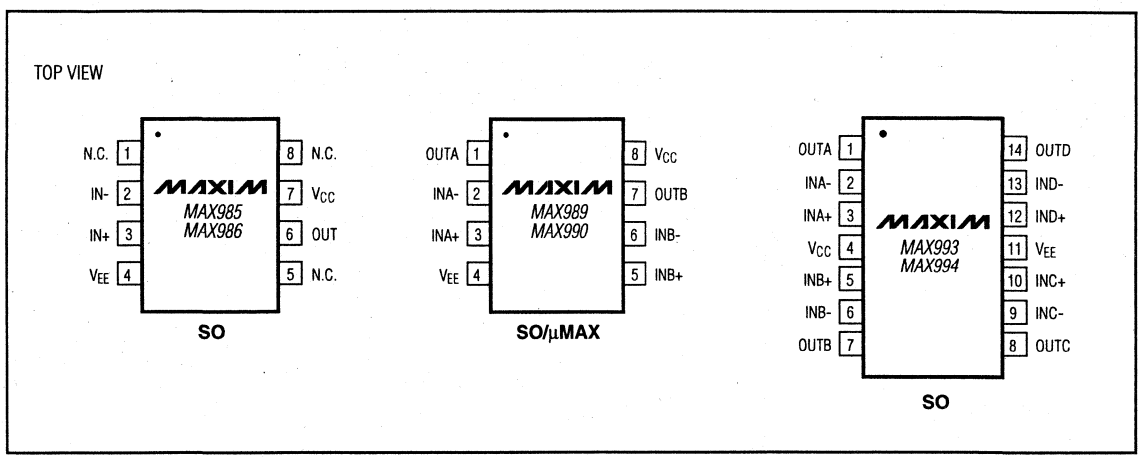


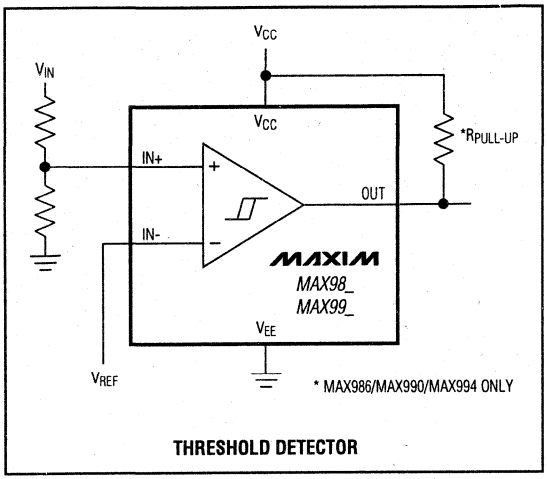
Figure 4. Logic-Level Translator

Pin Configurations (continued)



Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Typical Application Circuit



THRESHOLD DETECTOR

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX989ESA	-40°C to +85°C	8 SO	—
MAX989EUA	-40°C to +85°C	8 µMAX	—
MAX990ESA	-40°C to +85°C	8 SO	—
MAX990EUA	-40°C to +85°C	8 µMAX	—
MAX993ESD	-40°C to +85°C	14 SO	—
MAX994ESD	-40°C to +85°C	14 SO	—

19-1266; Rev 0b; 7/97

MAXIM

High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

General Description

The MAX987/MAX988/MAX991/MAX992/MAX995/MAX996 single/dual/quad micropower comparators feature low-voltage operation and Rail-to-Rail® inputs and outputs. Their operating voltage ranges from +2.5V to +5.5V, making them ideal for both 3V and 5V systems. These comparators also operate with ±1.25V to ±2.75V dual supplies. They consume only 48µA per comparator while achieving a 120ns propagation delay.

The common-mode input voltage range extends 250mV beyond the supply rails. Input bias current is typically 1.0pA, and input offset voltage is typically 0.5mV. Internal hysteresis ensures clean output switching, even with slow-moving input signals.

The output stage's unique design limits supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. This design also minimizes overall power consumption under dynamic conditions. The MAX987/MAX991/MAX995 have a push/pull output stage that sinks as well as sources current. Large internal output drivers allow rail-to-rail output swing with loads up to 8mA. The MAX988/MAX992/MAX996 have an open-drain output stage that can be pulled beyond V_{CC} to 6V (max) above V_{EE}. These open-drain versions are ideal for level translators and bipolar to single-ended converters.

The single MAX987/MAX988 are available in tiny 5-pin SOT23 packages.

Selector Guide

PART	COMPARATORS PER PACKAGE	OUTPUT STAGE	PIN-PACKAGE
MAX987	1	Push/Pull	8 SO/ 5 SOT23-5
MAX988	1	Open-Drain	8 SO/ 5 SOT23-5
MAX991	2	Push/Pull	8 SO/µMAX
MAX992	2	Open-Drain	8 SO/µMAX
MAX995	4	Push/Pull	14 SO
MAX996	4	Open-Drain	14 SO

Applications

Portable/Battery-Powered Systems
Mobile Communications
Zero-Crossing Detectors
Window Comparators
Level Translators
Threshold Detectors/ Discriminators
Ground/Supply Sensing
IR Receivers
Digital Line Receivers

Features

- ♦ **120ns Propagation Delay**
- ♦ **48µA Quiescent Supply Current**
- ♦ **+2.5V to +5.5V Single-Supply Operation**
- ♦ **Common-Mode Input Voltage Range Extends 250mV Beyond the Rails**
- ♦ **Push/Pull Output Stage Sinks and Sources 8mA Current (MAX987/MAX991/MAX995)**
- ♦ **Open-Drain Output Voltage Extends Beyond V_{CC} (MAX988/MAX992/MAX996)**
- ♦ **Unique Output Stage Reduces Output Switching Current, Minimizing Overall Power Consumption**
- ♦ **100µA Supply Current at 1MHz Switching Frequency**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Available in Space-Saving Packages:**
  5-Pin SOT23 (MAX987/MAX988)
  8-Pin µMAX (MAX991/MAX992)

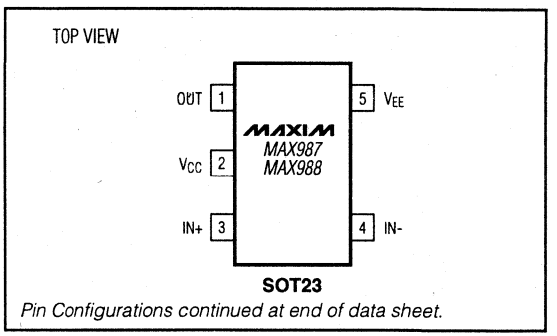
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX987EUK-T	-40°C to +85°C	5 SOT23-5	ABZB
MAX987ESA	-40°C to +85°C	8 SO	—
MAX988EUK-T	-40°C to +85°C	5 SOT23-5	ABZC
MAX988ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

Typical Application Circuit appears at end of data sheet.

Pin Configurations



SOT23

Pin Configurations continued at end of data sheet.

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High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 6V
IN_-, IN_+ to V_{EE} .....-0.3V to (V_{CC} + 0.3V)
OUT_ to V_{EE}
MAX987/MAX991/MAX995 .....-0.3V to (V_{CC} + 0.3V)
MAX988/MAX992/MAX996.....-0.3V to 6V
OUT_ Short-Circuit Duration to V_{EE} or V_{CC} 10sec

Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.10mW/°C above +70°C).....571mW
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW
14-Pin SO (derate 8.33 mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 1)

(V_{CC} = +2.7V to +5.5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}	Inferred from PSRR test			2.5		5.5	V
Supply Current per Comparator	I_{CC}	V_{CC} = 5V	T_A = +25°C			53	80	µA
			T_A = -40°C to +85°C				96	
		V_{CC} = 2.7V	T_A = +25°C			48	80	
			T_A = -40°C to +85°C				96	
Power-Supply Rejection Ratio	PSRR	2.5V ≤ V_{CC} ≤ 5.5V			55	80		dB
Common-Mode Voltage Range (Note 2)	V_{CMR}	T_A = +25°C			V_{EE} - 0.25		V_{CC} + 0.25	V
		T_A = -40°C to +85°C			V_{EE}		V_{CC}	
Input Offset Voltage (Note 3)	V_{OS}	Full common-mode range	T_A = +25°C			±0.5	±5	mV
			T_A = -40°C to +85°C				±7	
Input Hysteresis	V_{HYST}					±2.5		mV
Input Bias Current (Note 4)	I_B					0.001	10	nA
Input Offset Current	I_{OS}					0.5		pA
Input Capacitance	C_{IN}					1.0		pF
Common-Mode Rejection Ratio	CMRR				50	80		dB
Output Leakage Current (MAX988/MAX992/ MAX996 only)	I_{LEAK}	V_{OUT} = high					1.0	µA
Output Short-Circuit Current	I_{SC}	Sourcing or sinking, V_{OUT} = V_{EE} or V_{CC}		V_{CC} = 5V		95		mA
				V_{CC} = 2.7V		35		
OUT Output Voltage Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 8mA	T_A = +25°C			0.2	0.4	V
			T_A = -40°C to +85°C				0.55	
		V_{CC} = 2.7V, I_{SINK} = 3.5mA	T_A = +25°C			0.15	0.3	
			T_A = -40°C to +85°C				0.4	
OUT Output Voltage High (MAX987/MAX991/ MAX995 only)	V_{OH}	V_{CC} = 5V, I_{SOURCE} = 8mA	T_A = +25°C		4.6	4.85		V
			T_A = -40°C to +85°C		4.45			
		V_{CC} = 2.7V, I_{SOURCE} = 3.5mA	T_A = +25°C		2.4	2.55		
			T_A = -40°C to +85°C		2.3			

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +5.5V, V_{EE} = 0V, V_{CM} = 0V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
OUT Rise Time (MAX987/MAX991/ MAX995 only)	t_{RISE}	V_{CC} = 5.0V		C_L = 15pF		15		ns
				C_L = 50pF		20		
				C_L = 200pF		40		
OUT Fall Time	t_{FALL}	V_{CC} = 5.0V		C_L = 15pF		15		ns
				C_L = 50pF		20		
				C_L = 200pF		40		
Propagation Delay	t_{PD-}	C_L = 15pF, V_{CC} = 5V	MAX987/MAX991/ MAX995 only	10mV overdrive		210		ns
				100mV overdrive		120		
			MAX988/MAX992/ MAX996 only, $R_{PULL-UP}$ = 5.1kΩ	10mV overdrive		210		
				100mV overdrive		120		
	t_{PD+}	MAX987/MAX991/MAX995 only, C_L = 15pF, V_{CC} = 5V		10mV overdrive		210		
				100mV overdrive		120		
Power-Up Time	t_{PU}					25		µs

Note 1: The MAX98 _EUK specifications are 100% tested at T_A = +25°C. Limits over the extended temperature range are guaranteed by design, not production tested.

Note 2: Inferred from the V_{OS} test. Either or both inputs can be driven 0.3V beyond either supply rail without output phase reversal.

Note 3: V_{OS} is defined as the center of the hysteresis band at the input.

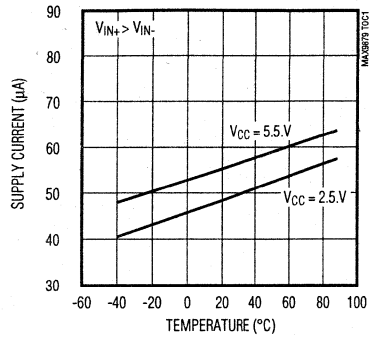
Note 4: I_B is defined as the average of the two input bias currents (I_{B-}, I_{B+}).

High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

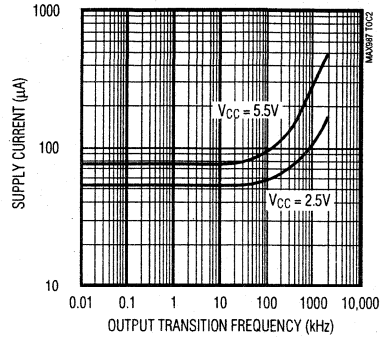
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

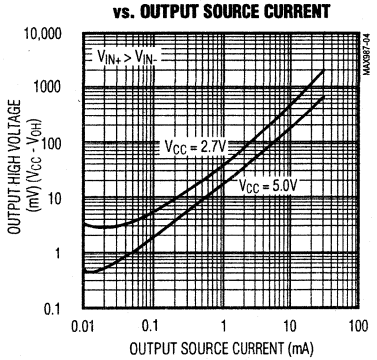
SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



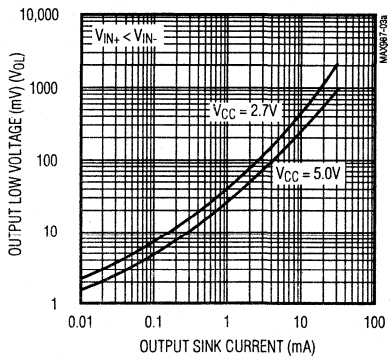
SUPPLY CURRENT PER COMPARATOR vs. OUTPUT TRANSITION FREQUENCY



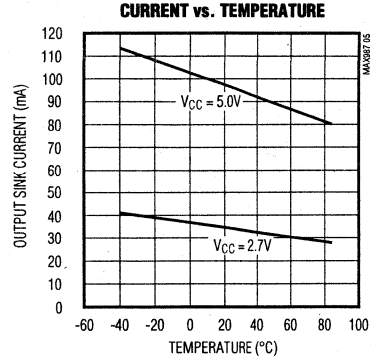
OUTPUT HIGH VOLTAGE vs. OUTPUT SOURCE CURRENT



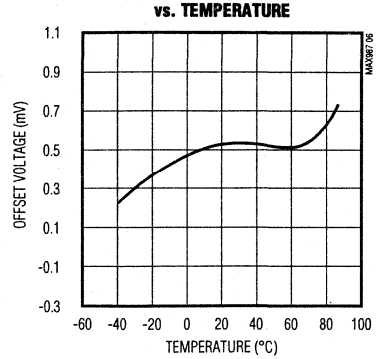
OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT



OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE



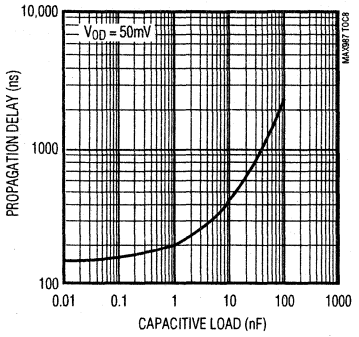
INPUT OFFSET VOLTAGE vs. TEMPERATURE



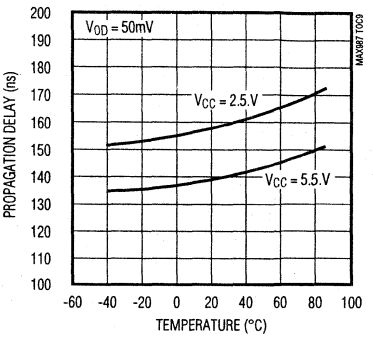
Typical Operating Characteristics

(V_{CC} = 5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

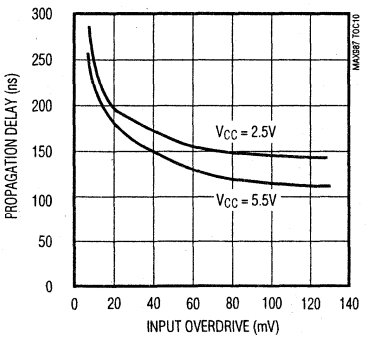
PROPAGATION DELAY vs. CAPACITIVE LOAD



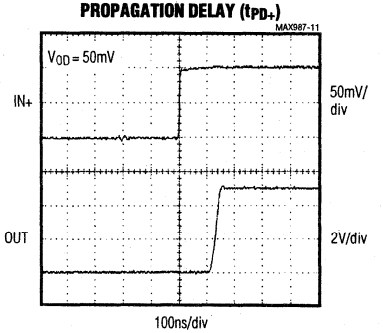
PROPAGATION DELAY vs. TEMPERATURE



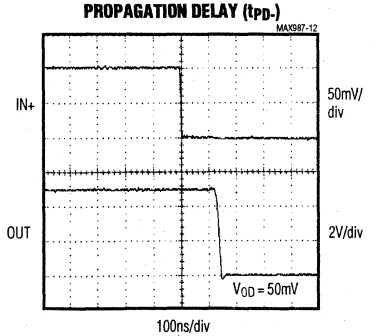
PROPAGATION DELAY vs. INPUT OVERDRIVE



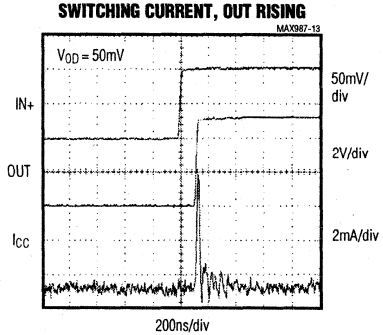
MAX987/MAX991/MAX995 PROPAGATION DELAY (t_{PD+})



PROPAGATION DELAY (t_{PD-})



MAX987/MAX991/MAX995 SWITCHING CURRENT, OUT RISING

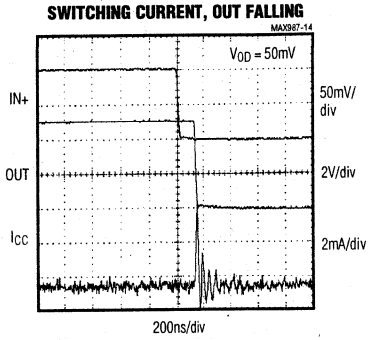


High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

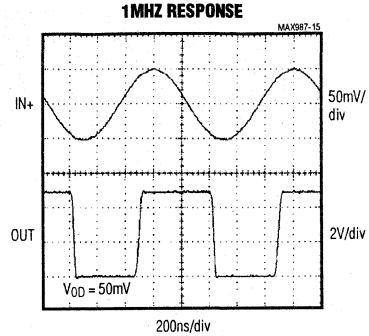
Typical Operating Characteristics (continued)

(V_{CC} = 5V, V_{CM} = 0V, T_A = +25°C, unless otherwise noted.)

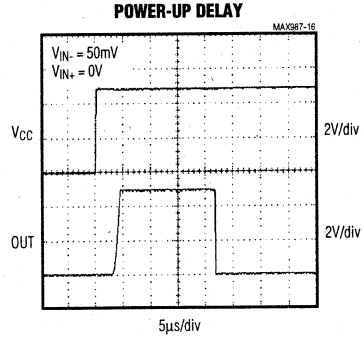
SWITCHING CURRENT, OUT FALLING



1MHZ RESPONSE



POWER-UP DELAY



Pin Description

PIN				NAME	FUNCTION
MAX987 MAX988		MAX991 MAX996	MAX995 MAX996		
SOT23-5	SO	SO/μMAX	SO		
1	6	—	—	OUT	Comparator Output
2	7	8	4	V_{CC}	Positive Supply Voltage
3	3	—	—	IN+	Comparator Noninverting Input
4	2	—	—	IN-	Comparator Inverting Input
5	4	4	11	V_{EE}	Negative Supply Voltage
—	—	1	1	OUTA	Comparator A Output
—	—	2	2	INA-	Comparator A Inverting Input
—	—	3	3	INA+	Comparator A Noninverting Input
—	—	5	5	INB+	Comparator B Noninverting Input
—	—	6	6	INB-	Comparator B Inverting Input
—	—	7	7	OUTB	Comparator B Output
—	—	—	8	OUTC	Comparator C Output
—	—	—	9	INC-	Comparator C Inverting Input
—	—	—	10	INC+	Comparator C Noninverting Input
—	—	—	12	IND+	Comparator D Noninverting Input
—	—	—	13	IND-	Comparator D Inverting Input
—	—	—	14	OUTD	Comparator D Output
—	1, 5, 8	—	—	N.C.	No Connection. Not internally connected.

High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Detailed Description

The MAX987/MAX988/MAX991/MAX992/MAX995/MAX996 are single/dual/quad low-power, low-voltage comparators. They have an operating supply voltage range between +2.5V and +5.5V and consume only 48µA per comparator, while achieving 120ns propagation delay. Their common-mode input voltage range extends 0.25V beyond each rail. Internal hysteresis ensures clean output switching, even with slow-moving input signals. Large internal output drivers allow rail-to-rail output swing with up to 8mA loads.

The output stage employs a unique design that minimizes supply-current surges while switching, virtually eliminating the supply glitches typical of many other comparators. The MAX987/MAX991/MAX995 have a push/pull output structure that sinks as well as sources current. The MAX988/MAX992/MAX996 have an open-drain output stage that can be pulled beyond V_{CC} to an absolute maximum of 6V above V_{EE}.

Input Stage Circuitry

The devices' input common-mode range extends from -0.25V to (V_{CC} + 0.25V). These comparators may operate at any differential input voltage within these limits. Input bias current is typically 1.0pA if the input voltage is between the supply rails. Comparator inputs are protected from overvoltage by internal body diodes connected to the supply rails. As the input voltage exceeds the supply rails, these body diodes become forward biased and begin to conduct. Consequently, bias currents increase exponentially as the input voltage exceeds the supply rails.

Output Stage Circuitry

These comparators contain a unique output stage capable of rail-to-rail operation with up to 8mA loads. Many comparators consume orders of magnitude more current during switching than during steady-state operation. However, with this family of comparators, the supply-current change during an output transition is extremely small. The *Typical Operating Characteristics* graph Supply Current vs. Output Transition Frequency shows the minimal supply-current increase as the output switching frequency approaches 1MHz. This characteristic eliminates the need for power-supply filter capacitors to reduce glitches created by comparator switching currents. Battery life increases substantially in high-speed, battery-powered applications.

Applications Information

Additional Hysteresis

MAX987/MAX991/MAX995

The MAX987/MAX991/MAX995 have ±2.5mV internal hysteresis. Additional hysteresis can be generated with three resistors using positive feedback (Figure 1). Unfortunately, this method also slows hysteresis response time. Use the following procedure to calculate resistor values for the MAX987/MAX991/MAX995.

1) Select R3. Leakage current at IN is under 10nA; therefore, the current through R3 should be at least 1µA to minimize errors caused by leakage current. The current through R3 at the trip point is (V_{REF} - V_{OUT}) / R3. Considering the two possible output states and solving for R3 yields two formulas: R3 = V_{REF} / 1µA or R3 = (V_{REF} - V_{CC}) / 1µA. Use the smaller of the two resulting resistor values. For example, if V_{REF} = 1.2V and V_{CC} = 5V, then the two R3 resistor values are 1.2MΩ and 3.8MΩ. Choose a 1.2MΩ standard value for R3.
2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.
3) Calculate R1 according to the following equation:

   $$R1 = R3 \times (V_{HB} / V_{CC})$$

   For this example, insert the values R1 = 1.2MΩ x (50mV / 5V) = 12kΩ.
4) Choose the trip point for V_{IN} rising (V_{THR}; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point. For this example, choose 3V.

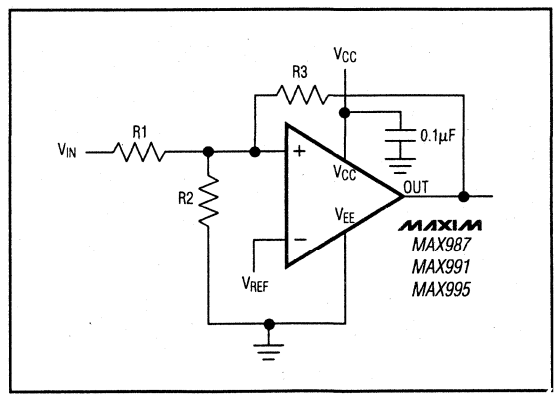


Figure 1. Additional Hysteresis (MAX987/MAX991/MAX995)

5) Calculate R2 as shown. For this example, choose an 8.2kΩ standard value:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3}}$$

$$R2 = \frac{1}{\left(\frac{3.0V}{1.2 \times 12k\Omega}\right) - \frac{1}{12k\Omega} - \frac{1}{2.2M\Omega}} = 8.03k\Omega$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

MAX988/MAX992/MAX996

The MAX988/MAX992/MAX996 have ±2.5mV internal hysteresis. They have open-drain outputs and require an external pull-up resistor (Figure 2). Additional hysteresis can be generated using positive feedback, but the formulas differ slightly from those of the MAX987/MAX991/MAX995.

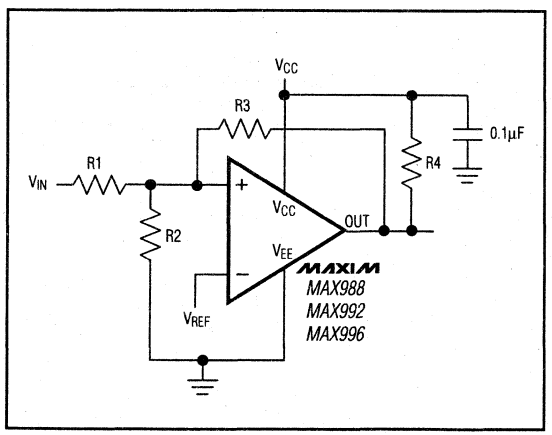


Figure 2. Additional Hysteresis (MAX988/MAX992/MAX996)

Use the following procedure to calculate resistor values:

1) Select R3 according to the formulas R3 = V_{REF} / 1µA or R3 = (V_{REF} - V_{CC}) / 1µA - R4. Use the smaller of the two resulting resistor values.
2) Choose the hysteresis band required (V_{HB}). For this example, choose 50mV.
3) Calculate R1 according to the following equation:

$$R1 = (R3 + R4) \times (V_{HB} / V_{CC})$$

4) Choose the trip point for V_{IN} rising (V_{THR}; V_{THF} is the trip point for V_{IN} falling). This is the threshold voltage at which the comparator switches its output from low to high as V_{IN} rises above the trip point.
5) Calculate R2 as follows:

$$R2 = \frac{1}{\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3 + R4}}$$

6) Verify trip voltages and hysteresis as follows:

$$V_{IN} \text{ rising: } V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3 + R4}\right)$$

$$V_{IN} \text{ falling: } V_{THF} = V_{THR} - \left(\frac{R1 \times V_{CC}}{R3 + R4}\right)$$

$$\text{Hysteresis} = V_{THR} - V_{THF}$$

Circuit Layout and Bypassing

These comparators' high-gain bandwidth requires design precautions to maximize their high-speed capability. The recommended precautions are:

1) Use a printed circuit board with an unbroken, low-inductance ground plane.
2) Place a decoupling capacitor (a 0.1µF ceramic capacitor is a good choice) as close to V_{CC} as possible.
3) On the inputs and outputs, keep lead lengths short to avoid unwanted parasitic feedback around the comparators.
4) Solder the devices directly to the printed circuit board instead of using a socket.

High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Zero-Crossing Detector

Figure 3 shows a zero-crossing detector application. The MAX987's inverting input is connected to ground, and its noninverting input is connected to a 100mVp-p signal source. As the signal at the noninverting input crosses 0V, the comparator's output changes state.

Logic-Level Translator

Figure 4 shows an application that converts 5V logic levels to 3V logic levels. The MAX988 is powered by the +5V supply voltage, and the pull-up resistor for the MAX988's open-drain output is connected to the +3V supply voltage. This configuration allows the full 5V logic swing without creating overvoltage on the 3V logic inputs. For 3V to 5V logic-level translation, simply connect the +3V supply to VCC and the +5V supply to the pull-up resistor.

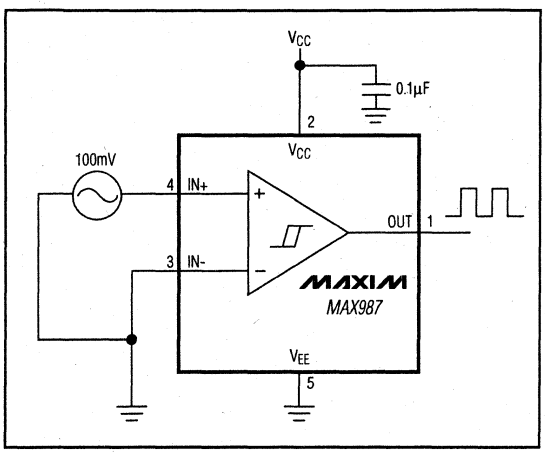


Figure 3. Zero-Crossing Detector

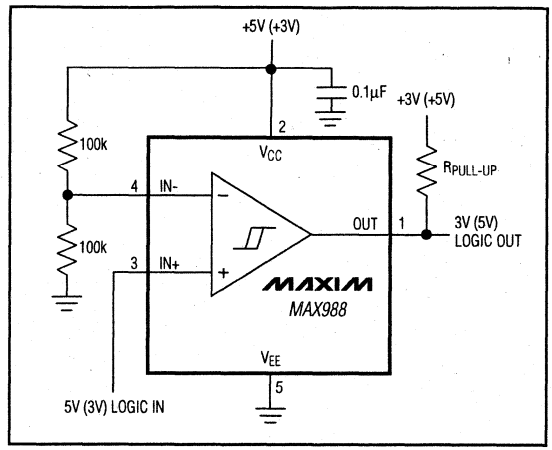
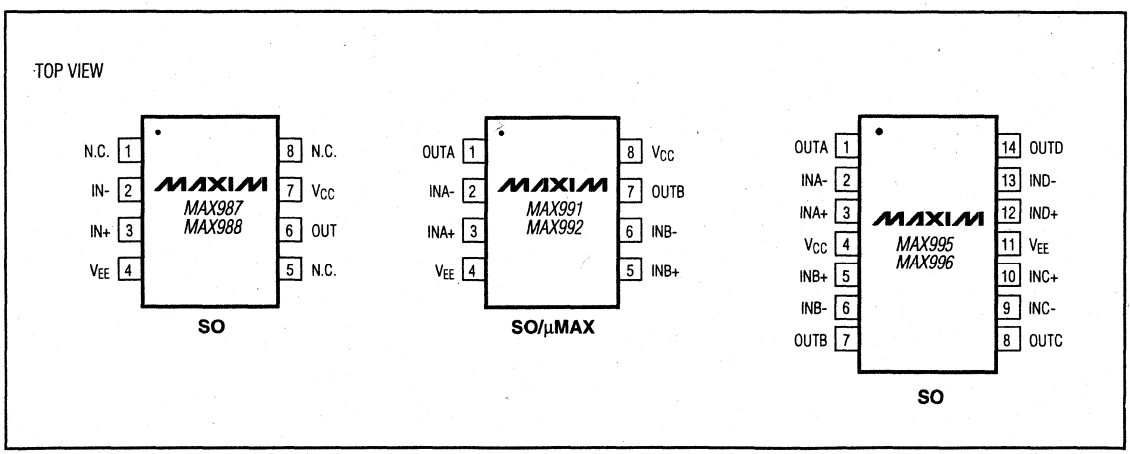


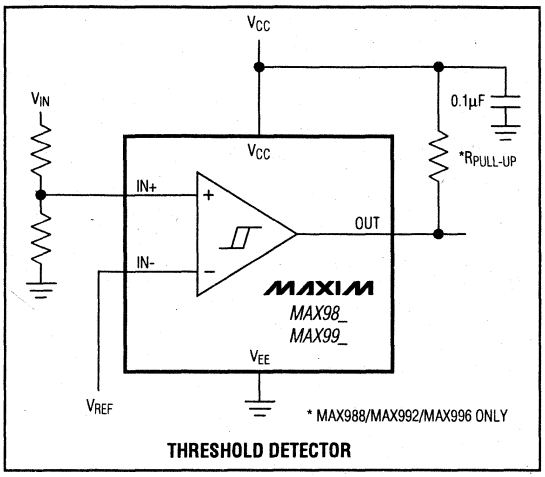
Figure 4. Logic-Level Translator

Pin Configurations (continued)



High-Speed, Micropower, Low-Voltage, SOT23, Rail-to-Rail I/O Comparators

Typical Application Circuit

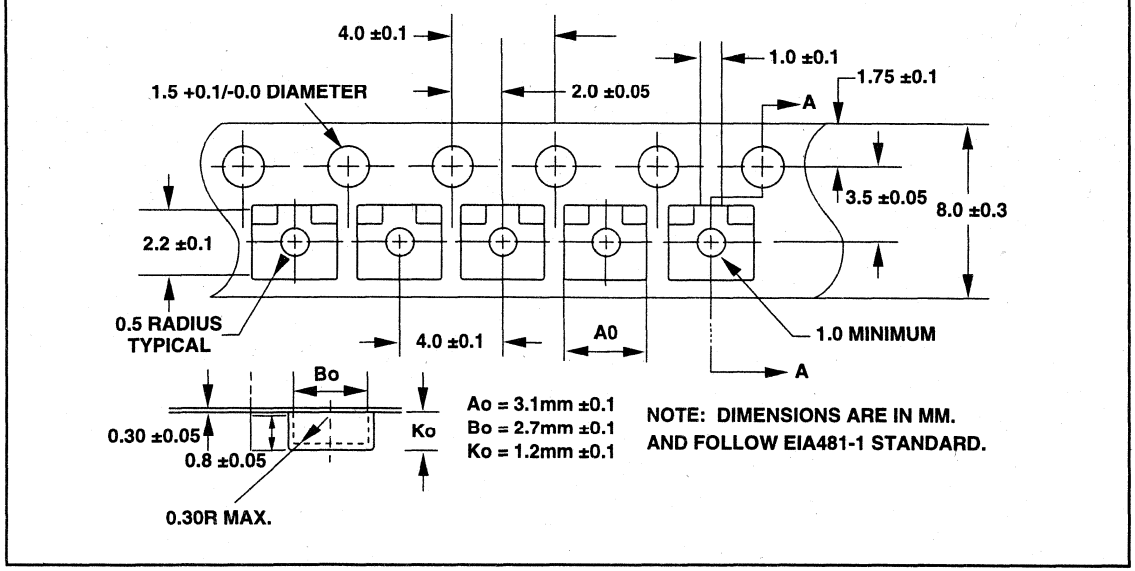


THRESHOLD DETECTOR

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX991ESA	-40°C to +85°C	8 SO	—
MAX991EUA	-40°C to +85°C	8 µMAX	—
MAX992ESA	-40°C to +85°C	8 SO	—
MAX992EUA	-40°C to +85°C	8 µMAX	—
MAX995ESD	-40°C to +85°C	14 SO	—
MAX996ESD	-40°C to +85°C	14 SO	—

Tape-and-Reel Information



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

+3V/+5V, High-Speed, Rail-to-Rail, SOT23 Comparators with Shutdown

General Description

The MAX997/MAX999 are high-speed, low-power voltage comparators available in tiny SOT23 and 8-pin SO packages. They have a 5ns propagation delay and consume only 5mA of supply current when operating from a single +2.7V to +5.5V supply. The input common-mode range extends from below ground to above the supply rail, and the output can pull to within 0.5V of the supply rail or GND.

The MAX997/MAX999 have internal hysteresis to minimize output indecision and oscillation during transitions, simplifying use without input resolution degradation. In addition, large input voltage overdrive causes no output phase reversal.

The MAX997/MAX999 consume less than 500µA supply current during shutdown. They are specified and guaranteed over the -40°C to +85°C extended temperature range.

Features

- **Ultra-Fast 5ns Propagation Delay (5mV overdrive)**
- **5mA Supply Current**
- **500µA (max) Shutdown Current**
- **Single-Supply Operation down to 2.7V**
- **Rail-to-Rail® Input Voltage Range**
- **Output Drive to Within 0.5V of Supply Rails**
- **CMOS/TTL-Compatible Logic Output**
- **No Output Phase Reversal for Overdriven Inputs**
- **Internal Hysteresis for Clean Switching**
- **Available in Tiny SOT23 Packages**

Applications

3V/5V Systems

Battery-Powered Systems

Threshold Detectors/Discriminators

Line Receivers

Zero-Crossing Detectors

Digital Network Line Receivers

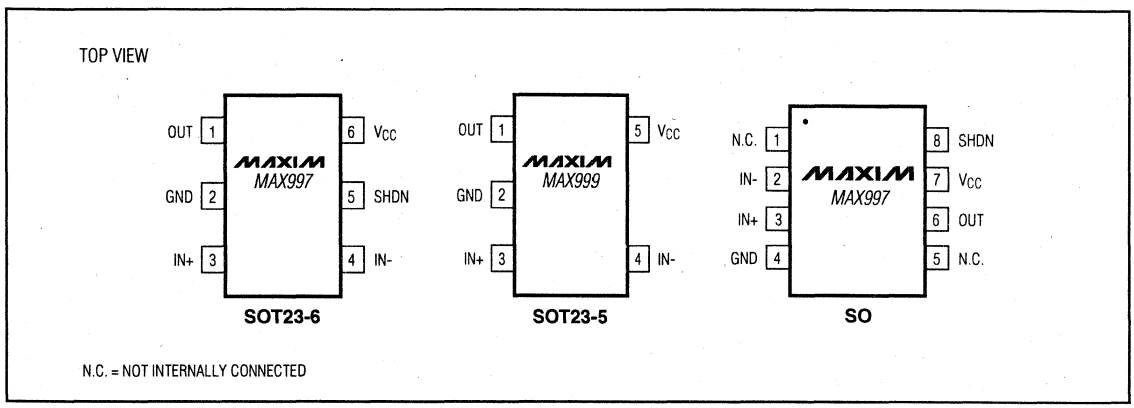
High-Speed Sampling Circuits

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX997ESA	-40°C to +85°C	8 SO
MAX997EUT-T	-40°C to +85°C	SOT23-6
MAX999EUK-T	-40°C to +85°C	SOT23-5

Ordering Information continued on next page.

Pin Configurations



Rail-to-Rail is a trademark of Nippon Motorola Ltd.

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19-1195; Rev 0; 4/97

MAXIM

SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

General Description

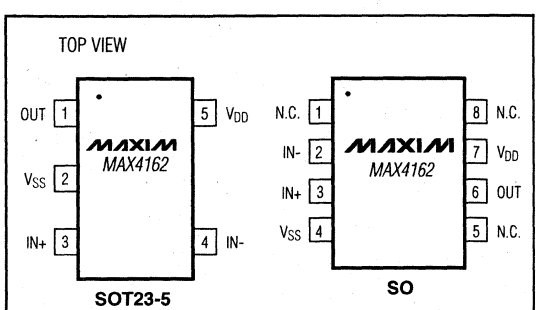
The MAX4162/MAX4163/MAX4164 are single/dual/quad, micropower operational amplifiers that combine an exceptional bandwidth to power consumption ratio with true rail-to-rail inputs and outputs. They consume a mere 25µA quiescent current per amplifier, yet achieve 200kHz gain-bandwidth product and are unity-gain stable while driving any capacitive load. The MAX4162/MAX4163/MAX4164 operate from either a single supply (+2.7V to +10V) or dual supplies (±1.35V to ±5V), with an input common-mode voltage range that extends 250mV *beyond* either supply rail. These amplifiers use a proprietary architecture to achieve a very high input common-mode rejection ratio without the mid-swing nonlinearities present in other Rail-to-Rail® op amps. This architecture also maintains high open-loop gain and output swing while driving substantial loads.

The combination of excellent bandwidth/power performance, single-supply operation, and miniature footprint makes these op amps ideal for portable equipment and other low-power, single-supply applications. The single MAX4162 is available in 8-pin SO and space-saving 5-pin SOT23 packages. The MAX4163 is available in an 8-pin µMAX or SO, while the MAX4164 comes in a 14-pin SO.

Applications

Battery-Powered Devices
pH Probes
Portable Equipment
Low-Power, Low-Voltage Equipment
Medical Instruments
Ionization Detectors
Cellular Phones

Pin Configurations



Pin Configurations continued at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon-Motorola, Ltd.

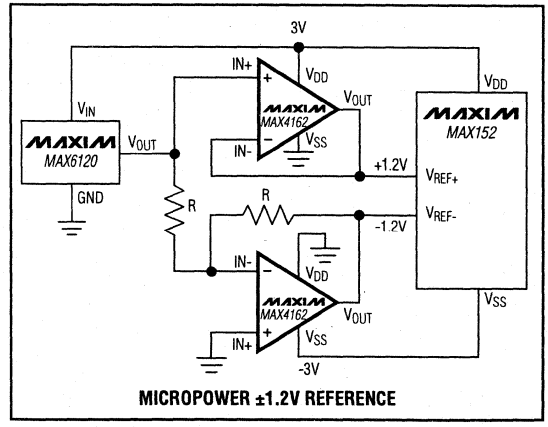
Features

- ♦ **5-Pin SOT23 Package (MAX4162)**
- ♦ **1.0pA Typical Input Bias Current**
- ♦ **Fully Specified Single-Supply Operation at 3V and 5V**
- ♦ **Input Common-Mode Voltage Range Extends 250mV Beyond Either Supply Rail**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **200kHz Gain-Bandwidth Product**
- ♦ **25µA Quiescent Current per Amplifier**
- ♦ **Excellent CMRR, PSRR, and Gain Linearity**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Unity-Gain Stable**
- ♦ **Stable with Any Capacitive Load**
- ♦ **Internally Short-Circuit Protected to Either Rail**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4162ESA	-40°C to +85°C	8 SO	—
MAX4162EUK	-40°C to +85°C	5 SOT23-5	AABX
MAX4163ESA	-40°C to +85°C	8 SO	—
MAX4163EUA	-40°C to +85°C	8 µMAX	—
MAX4164ESD	-40°C to +85°C	14 SO	—

Typical Application Circuit



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SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{DD} to V_{SS}) ..... +11V
IN+, IN-, OUT Voltage ..... (V_{DD} + 0.3V) to (V_{SS} - 0.3V)
Short-Circuit Duration (to either rail) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin µMAX (derate 4.1mW/°C above +70°C) 330mW
14-Pin SO (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: +3V Operation

(V_{DD} =+3V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, V_{OUT} = V_{DD} / 2, R_L tied to V_{DD} / 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	Inferred from PSRR test		2.7		10.0	V
Supply Current (per amplifier)				25	40	µA
Input Bias Current (Note 1)				1.0	100	pA
Input Offset Voltage	MAX4162	T_A = +25°C		±0.5	±3	mV
		T_A = -40°C to +85°C			±4	
	MAX4163	T_A = +25°C		±0.5	±4	
		T_A = -40°C to +85°C			±5	
	MAX4164	T_A = +25°C		±0.5	±5	
		T_A = -40°C to +85°C			±6	
Input Offset Voltage Tempco				2		µV/°C
Differential Input Resistance				>10		TΩ
Input Common-Mode Voltage Range	Inferred from CMRR test		V_{SS} - 0.25		V_{DD} + 0.25	V
Common-Mode Rejection Ratio	V_{CM} = (V_{SS} - 0.25V) to (V_{DD} + 0.25V)		70	100		dB
Large-Signal Voltage Gain	R_L = 10kΩ		85	120		dB
Output Voltage Swing	R_L = 10kΩ	V_{DD} - V_{OH}		30	180	mV
		V_{OL} - V_{SS}		30	180	
	R_L = 100kΩ	V_{DD} - V_{OH}		3	25	
		V_{OL} - V_{SS}		3	25	
Output Short-Circuit Current	To either supply rail			15		mA
Closed-Loop Output Resistance	A_V = +1V/V			0.1		Ω
Power-Supply Rejection Ratio	V_{DD} = 2.7V to 10V		80	110		dB
Gain-Bandwidth Product				200		kHz
Phase Margin				60		degrees
Gain Margin				12		dB
Total Harmonic Distortion	f = 1kHz, V_{OUT} = 2Vp-p, R_L = 100kΩ, A_V = +1V/V			0.02		%
Slew Rate				115		V/ms
Settling Time to 0.1%	V_{OUT} = 1V to 2V step			50		µs
Turn-On Time	V_{DD} = 0V to 3V step, V_{IN} = V_{DD} / 2, A_V = +1V/V			20		µs

ELECTRICAL CHARACTERISTICS: +3V Operation (continued)

(V_{DD} =+3V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, V_{OUT} = V_{DD} / 2, R_L tied to V_{DD} / 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Noise Voltage Density	f = 1kHz		80		nV/√Hz
Differential Input Capacitance			0.7		pF
Input Common-Mode Capacitance			1.5		pF
Internal Charge-Pump Frequency			700		kHz
Charge-Pump Output Feedthrough			100		µVp-p

ELECTRICAL CHARACTERISTICS: +5V Operation

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, V_{OUT} = V_{DD} / 2, R_L tied to V_{DD} / 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	Inferred from PSRR test		2.7		10.0	V
Supply Current (per amplifier)				27	45	µA
Input Bias Current (Note 1)				1.0	100	pA
Input Offset Voltage	MAX4162	T_A = +25°C		±0.5	±3	mV
		T_A = -40°C to +85°C			±4	
	MAX4163	T_A = +25°C		±0.5	±4	
		T_A = -40°C to +85°C			±5	
	MAX4164	T_A = +25°C		±0.5	±5	
		T_A = -40°C to +85°C			±6	
Input Offset Voltage Tempco				2		µV/°C
Differential Input Resistance				>10		TΩ
Input Common-Mode Voltage Range	Inferred from CMRR test		V_{SS} - 0.25		V_{DD} + 0.25	V
Common-Mode Rejection Ratio	V_{CM} = (V_{SS} - 0.25V) to (V_{DD} + 0.25V)		70	100		dB
Large-Signal Voltage Gain			85	120		dB
Output Voltage Swing	R_L = 10kΩ	V_{DD} - V_{OH}		50	300	mV
		V_{OL} - V_{SS}		50	300	
	R_L = 100kΩ	V_{DD} - V_{OH}		5	40	
		V_{OL} - V_{SS}		5	40	
Output Short-Circuit Current	To either supply rail			15		mA
Closed-Loop Output Resistance	A_V = +1V/V			0.1		Ω
Power-Supply Rejection Ratio	V_{DD} = 4.5V to 10V		80	110		dB
Gain-Bandwidth Product				200		kHz
Phase Margin				60		degrees
Gain Margin				12		dB

SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

ELECTRICAL CHARACTERISTICS: +5V Operation (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, V_{OUT} = V_{DD} / 2, R_L tied to V_{DD} / 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion	f = 1kHz, V_{OUT} = 2Vp-p, R_L = 100kΩ, A_V = +1V/V		0.02		%
Slew Rate			115		V/ms
Settling Time to 0.1%	V_{OUT} = 1V to 4V step		70		µs
Turn-On Time	V_{DD} = 0V to 5V step, V_{IN} = V_{DD} / 2, A_V = +1V/V		40		µs
Input Noise Voltage Density	f = 1kHz		80		nV/√Hz
Differential Input Capacitance			0.7		pF
Input Common-Mode Capacitance			1.5		pF
Internal Charge-Pump Frequency			700		MHz
Charge-Pump Output Feedthrough			100		µVp-p

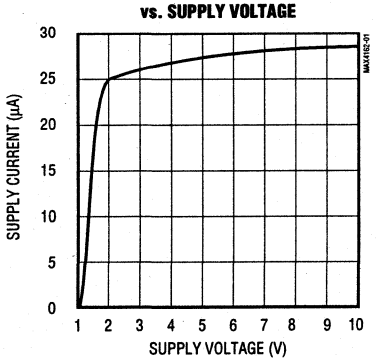
Note 1: Input bias current guaranteed by design, not production tested.

Note 2: The MAX4162EUK specifications are 100% tested at T_A = +25°C. Limits over the extended temperature range are guaranteed by design, not production tested.

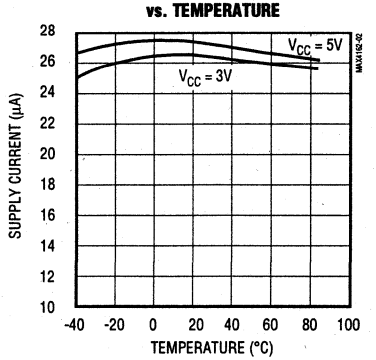
Typical Operating Characteristics

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

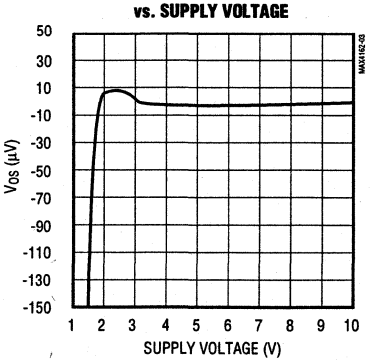
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



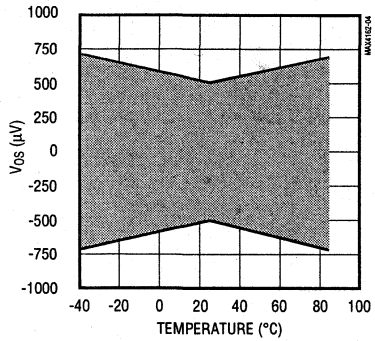
INPUT OFFSET VOLTAGE VARIATION vs. SUPPLY VOLTAGE



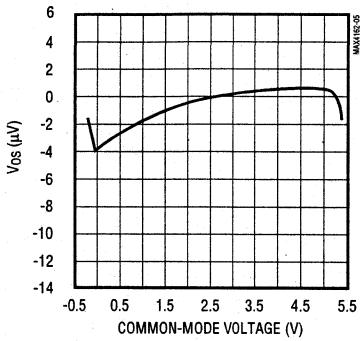
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

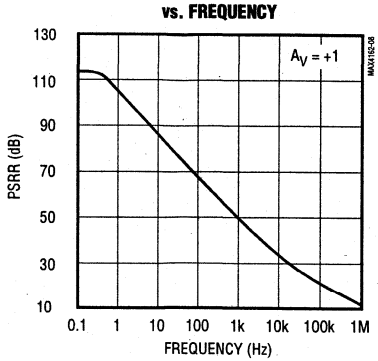
INPUT OFFSET VOLTAGE vs. TEMPERATURE



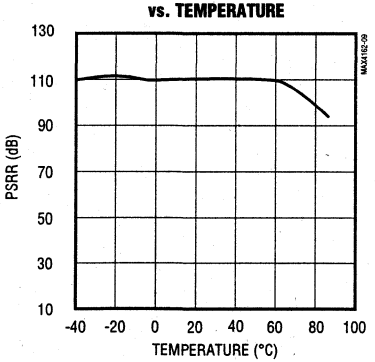
INPUT OFFSET VOLTAGE VARIATION vs. COMMON-MODE VOLTAGE



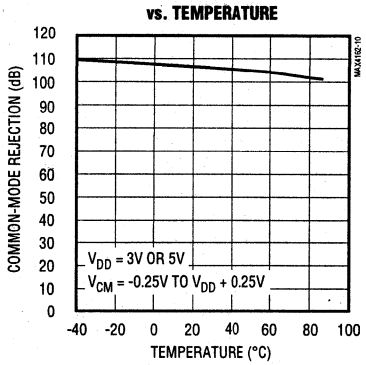
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



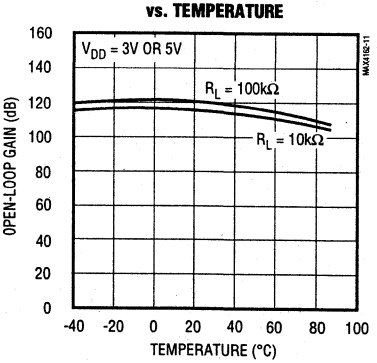
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



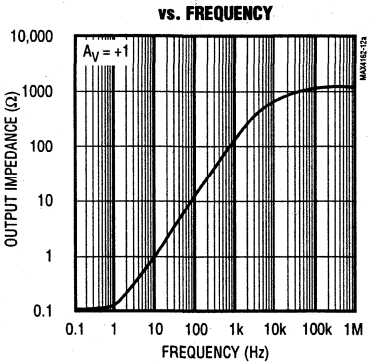
COMMON-MODE REJECTION vs. TEMPERATURE



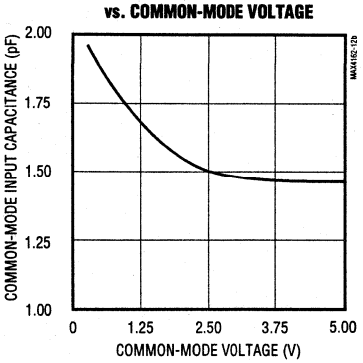
OPEN-LOOP GAIN vs. TEMPERATURE



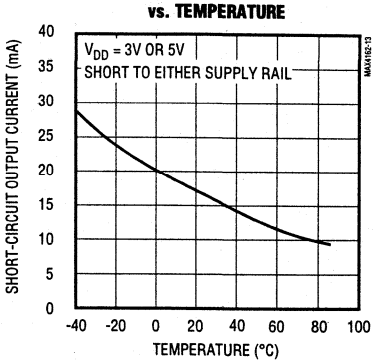
OUTPUT IMPEDANCE vs. FREQUENCY



COMMON-MODE INPUT CAPACITANCE vs. COMMON-MODE VOLTAGE



SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE

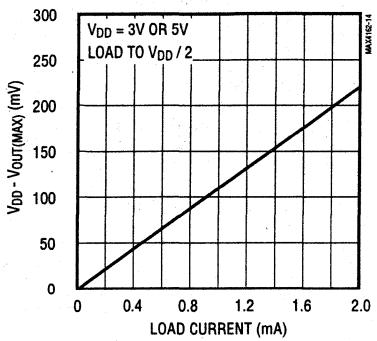


SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

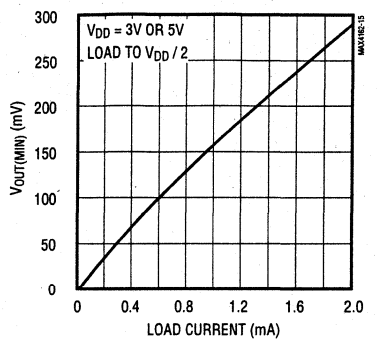
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

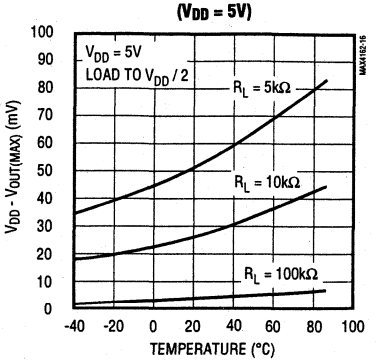
MAXIMUM OUTPUT VOLTAGE vs. LOAD CURRENT



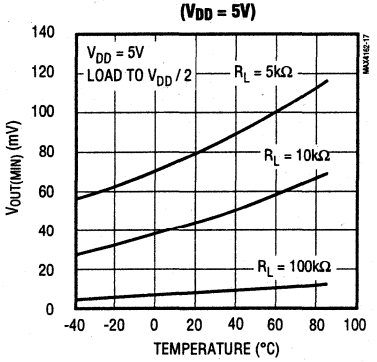
MINIMUM OUTPUT VOLTAGE vs. LOAD CURRENT



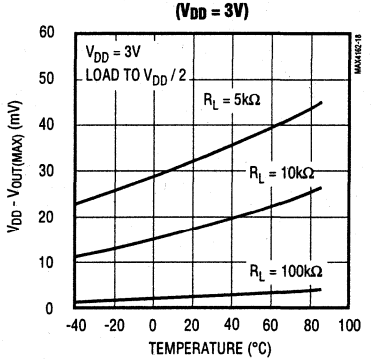
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE (V_{DD} = 5V)



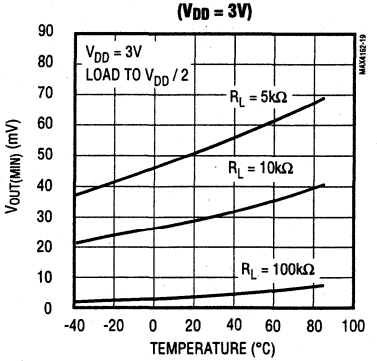
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE (V_{DD} = 5V)



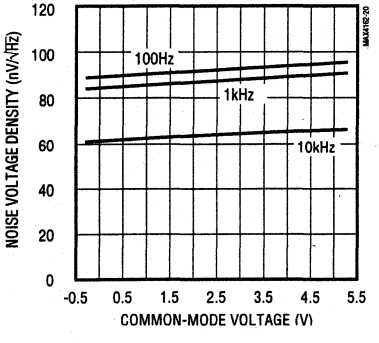
MAXIMUM OUTPUT VOLTAGE vs. TEMPERATURE (V_{DD} = 3V)



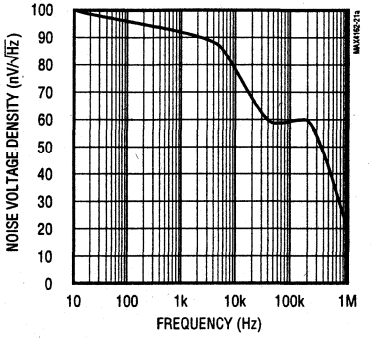
MINIMUM OUTPUT VOLTAGE vs. TEMPERATURE (V_{DD} = 3V)



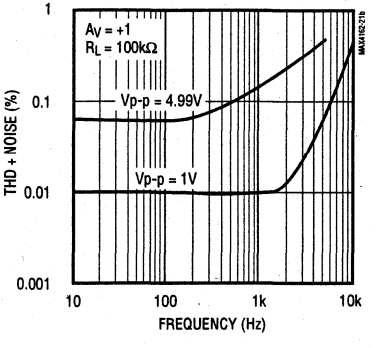
NOISE VOLTAGE DENSITY vs. COMMON-MODE VOLTAGE



NOISE VOLTAGE DENSITY vs. FREQUENCY



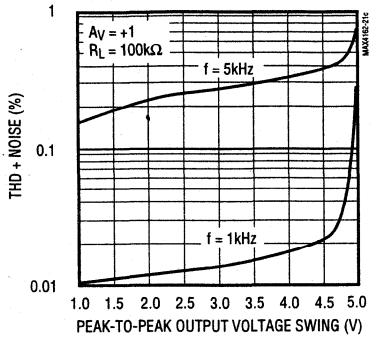
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



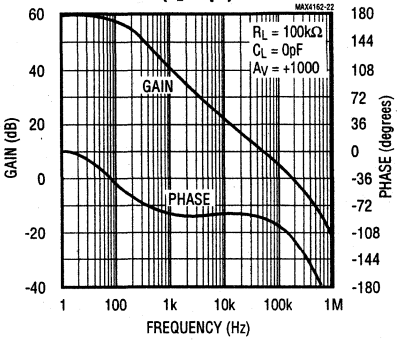
Typical Operating Characteristics (continued)

(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

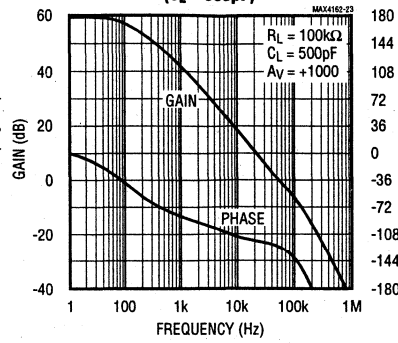
TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE SWING



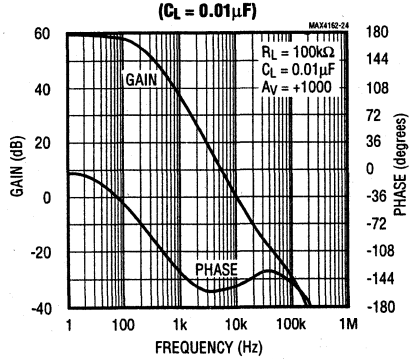
GAIN AND PHASE vs. FREQUENCY (C_L = 0pF)



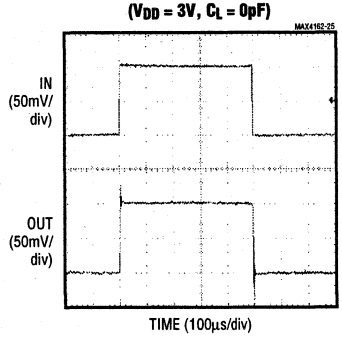
GAIN AND PHASE vs. FREQUENCY (C_L = 500pF)



GAIN AND PHASE vs. FREQUENCY (C_L = 0.01µF)

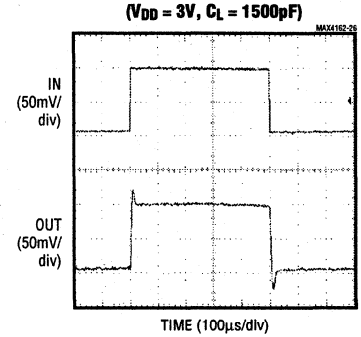


NONINVERTING SMALL-SIGNAL PULSE RESPONSE (V_{DD} = 3V, C_L = 0pF)



V_{DD} = 3V, V_{IN} = 100mV, R_L = 100kΩ to V_{DD} / 2, C_L = 0pF

NONINVERTING SMALL-SIGNAL PULSE RESPONSE (V_{DD} = 3V, C_L = 1500pF)



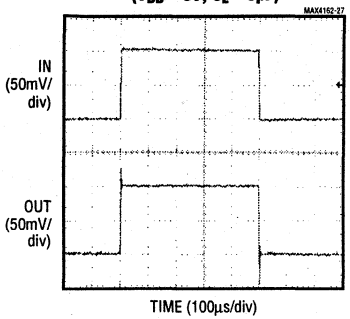
V_{DD} = 3V, V_{IN} = 100mV, R_L = 100kΩ to V_{DD} / 2, C_L = 1500pF

SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

Typical Operating Characteristics (continued)

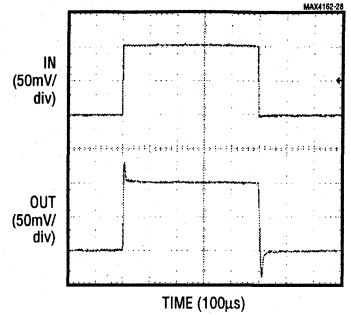
(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

NONINVERTING SMALL-SIGNAL PULSE RESPONSE (V_{DD} = 5V, C_L = 0pF)



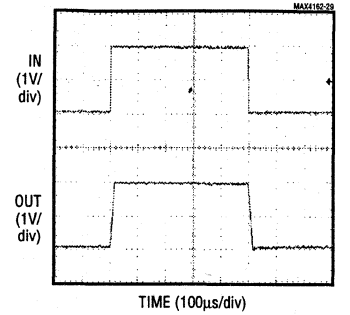
V_{DD} = 5V, V_{IN} = 100mV, R_L = 100kΩ to V_{DD} / 2, C_L = 0pF

NONINVERTING SMALL-SIGNAL PULSE RESPONSE (V_{DD} = 5V, C_L = 1500pF)



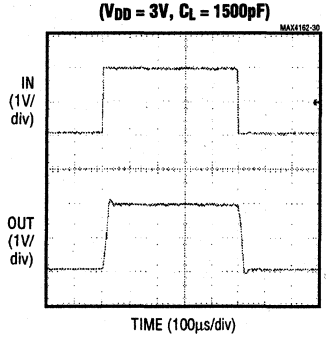
V_{DD} = 5V, V_{IN} = 100mV, R_L = 100kΩ to V_{DD} / 2, C_L = 1500pF

NONINVERTING LARGE-SIGNAL PULSE RESPONSE (V_{DD} = 3V, C_L = 0pF)



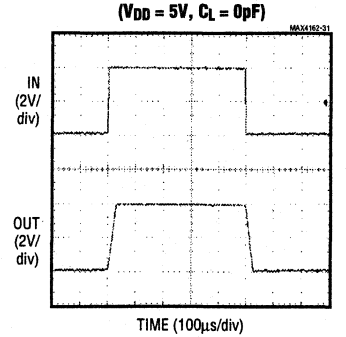
V_{DD} = 3V, V_{IN} = 2V, R_L = 100kΩ to V_{DD} / 2, C_L = 0pF

NONINVERTING LARGE-SIGNAL PULSE RESPONSE (V_{DD} = 3V, C_L = 1500pF)



V_{DD} = 3V, V_{IN} = 2V, R_L = 100kΩ to V_{DD} / 2, C_L = 1500pF

NONINVERTING LARGE-SIGNAL PULSE RESPONSE (V_{DD} = 5V, C_L = 0pF)



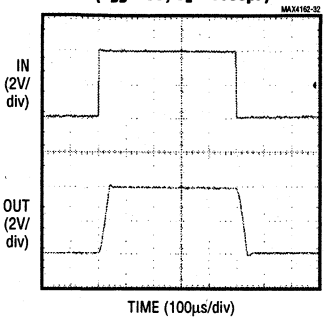
V_{DD} = 5V, V_{IN} = 4V, R_L = 100kΩ to V_{DD} / 2, C_L = 0pF

SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

Typical Operating Characteristics (continued)

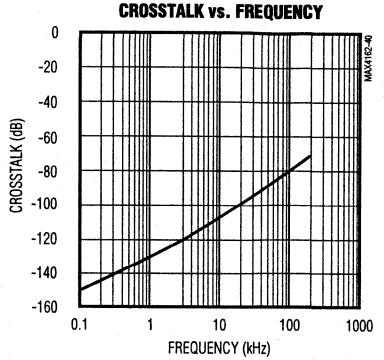
(V_{DD} = +5V, V_{SS} = 0V, V_{CM} = V_{DD} / 2, T_A = +25°C, unless otherwise noted.)

NONINVERTING LARGE-SIGNAL PULSE RESPONSE (V_{DD} = 5V, C_L = 1500pF)



V_{DD} = 5V, V_{IN} = 4V, R_L = 100kΩ to V_{DD} / 2, C_L = 1500pF

MAX4163/MAX4164 CROSSTALK vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX4162		MAX4163 SO/µMAX	MAX4164 SO		
SO	SOT23-5				
1, 5, 8	—	—	—	N.C.	No Connection. Not internally connected.
2	4	—	—	IN-	Amplifier Inverting Input
3	3	—	—	IN+	Amplifier Noninverting Input
4	2	4	11	V_{SS}	Negative Power Supply
6	1	—	—	OUT	Amplifier Output
7	5	8	4	V_{DD}	Positive Power Supply
—	—	1	1	OUTA	Amplifier A Output
—	—	2	2	INA-	Amplifier A Inverting Input
—	—	3	3	INA+	Amplifier A Noninverting Input
—	—	5	5	INB+	Amplifier B Noninverting Input
—	—	6	6	INB-	Amplifier B Inverting Input
—	—	7	7	OUTB	Amplifier B Output
—	—	—	8	OUTC	Amplifier C Output
—	—	—	9	INC-	Amplifier C Inverting Input
—	—	—	10	INC+	Amplifier C Noninverting Input
—	—	—	12	IND+	Amplifier D Noninverting Input
—	—	—	13	IND-	Amplifier D Inverting Input
—	—	—	14	OUTD	Amplifier D Output

SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

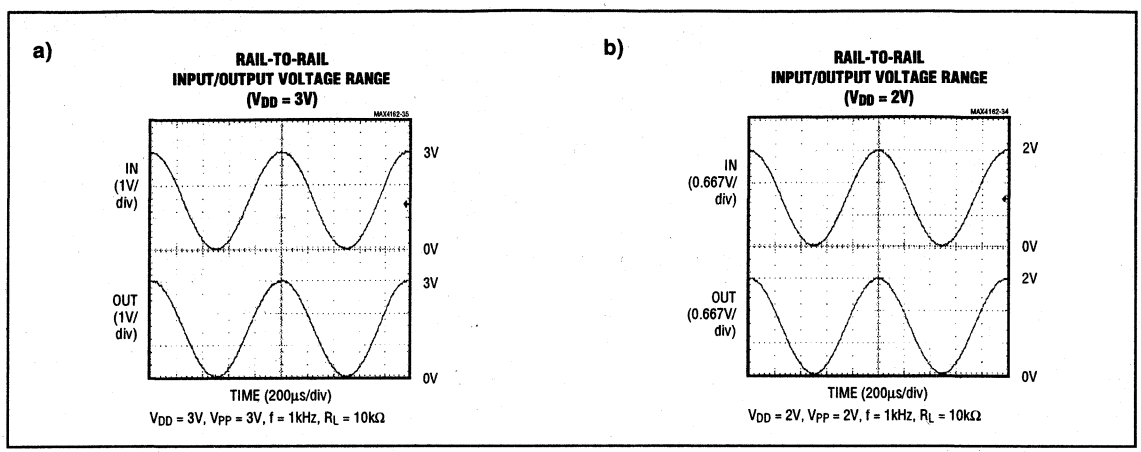


Figure 1. Rail-to-Rail I/O: a) V_{DD} = 3V; b) V_{DD} = 2V

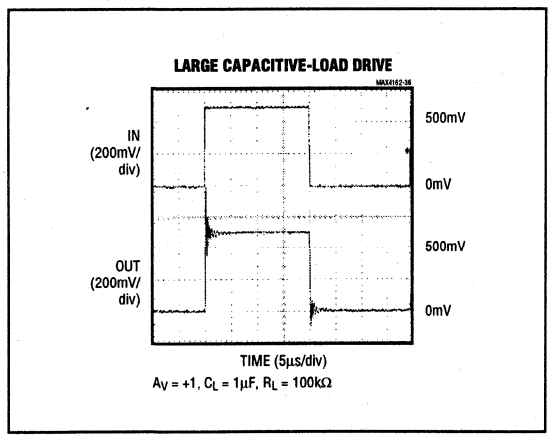


Figure 2. Large Capacitive-Load Drive

Applications Information

Rail-to-Rail Inputs and Outputs

The MAX4162/MAX4163/MAX4164 input common-mode range extends 250mV *beyond* each of the supply rails, providing a substantial increase in dynamic range over other op amps (even many of those referred to as rail-to-rail). Although the minimum operating voltage is specified at 2.7V, the devices typically provide full rail-to-rail operation below 2.0V (Figure 1). These amplifiers do not suffer from midswing common-mode-rejection degradation or crossover nonlinearity often encountered in other rail-to-rail op amps. Extremely low, 1.0pA input bias current makes these devices ideal for applications such as pH probes, electrometers, and ionization detectors. They are also protected against phase reversal (inferred from CMRR test) and latchup for input signals extending beyond the supply rails. The output stage achieves a lower output impedance than traditional rail-to-rail output stages, providing an output voltage range that typically swings within 150mV of the supply rails for 1mA loads. This architecture also maintains high open-loop gain and output swing while driving substantial loads.

Output Loading and Stability

These devices drive 1mA loads to within 150mV of the supply rails while consuming only 25µA of quiescent current. Internal compensation allows these amplifiers to remain unity-gain stable while driving any capacitive load (Figure 2).

Internal Charge Pump

An internal charge pump provides two internal supplies typically 2V beyond each rail. These internal rails allow the MAX4162/MAX4163/MAX4164 to achieve true rail-to-rail inputs and outputs, while providing excellent common-mode rejection, power-supply rejection ratios, and gain linearity.

These charge pumps require no external components, and in most applications are entirely transparent to the user. Two characteristics may be visible to the user, depending on the application:

1) The on-board charge pumps generate a small amount of 700kHz switching noise at the op amp's output. The amplitude of this noise is typically 100µVp-p. The noise is **not** referred to the input, and is independent of amplifier gain. The charge-pump switching frequency is well beyond the amplifier's 200kHz bandwidth, and is therefore unnoticeable in most applications.
2) The charge pumps typically require up to 20µs on power-up to fully energize the internal supply rails (Figure 3).

Power Supplies and Layout

The MAX4162/MAX4163/MAX4164 are guaranteed to operate from a single +2.7V to +10.0V power supply, but full rail-to-rail operation typically extends below 2V. For single-supply operation, bypass the power supply with a 1µF capacitor in parallel with a 0.1µF ceramic capacitor. If operating from dual supplies, bypass each supply to ground.

Good layout improves performance by decreasing the amount of stray capacitance at the op amp's inputs and output. To decrease stray capacitance, minimize both trace and external component lead lengths, and place external components close to the op amp's pins.

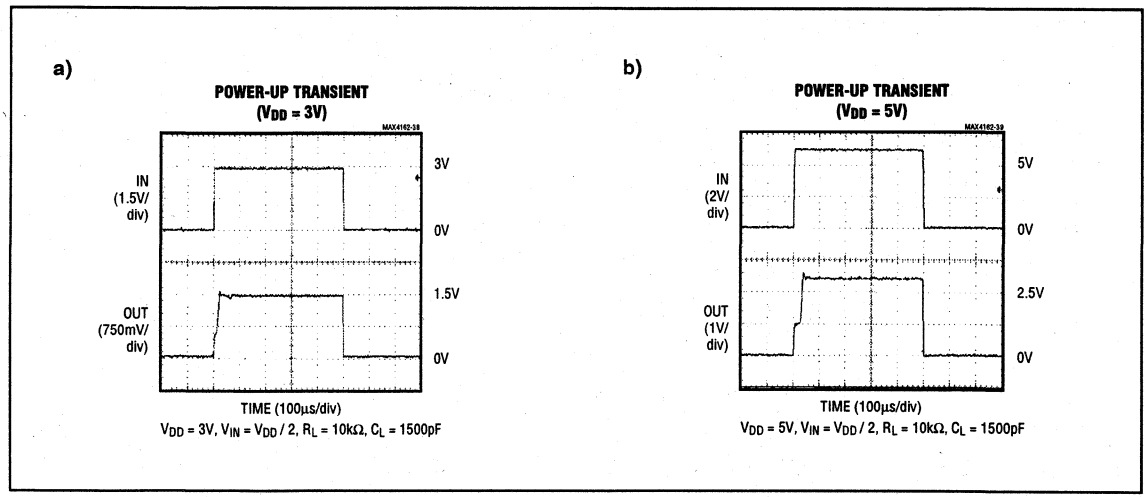
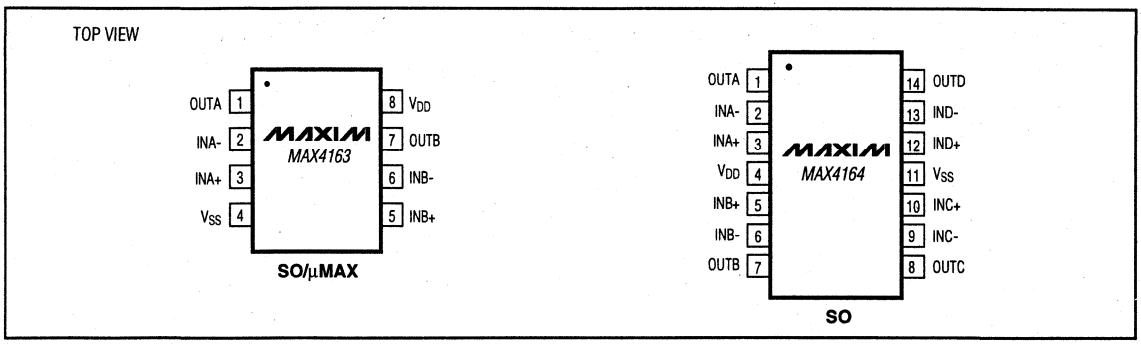


Figure 3. Power-Up Transient: a) V_{DD} = 3V; b) V_{DD} = 5V

Pin Configurations (continued)

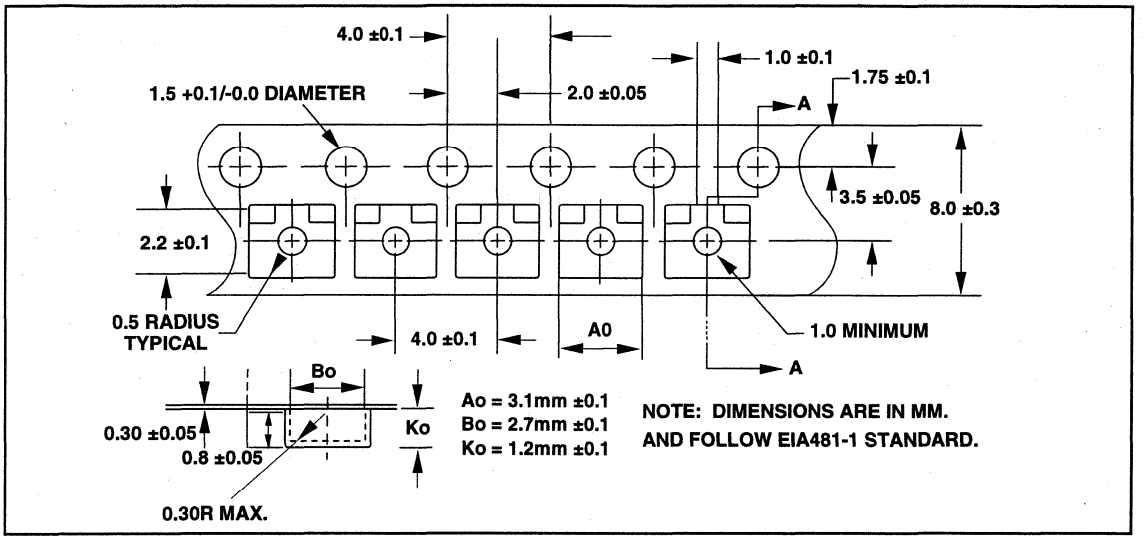


SOT23, Micropower, Single-Supply, Rail-to-Rail I/O Op Amps

Chip Information

MAX4162 TRANSISTOR COUNT: 291
MAX4163 TRANSISTOR COUNT: 496
MAX4164 TRANSISTOR COUNT: 992

Tape-and-Reel Information



19-1224; Rev 0; 4/97

MAXIM

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

General Description

The MAX4165–MAX4169 family of operational amplifiers combines excellent DC accuracy with high output current drive, single-supply operation, and Rail-to-Rail® inputs and outputs. These devices operate from a single +2.7V to +6.5V supply, or from dual ±1.35V to ±3.25V supplies. They typically draw 1.2mA supply current, and are guaranteed to deliver 80mA output current.

The MAX4166/MAX4168 have a shutdown mode that reduces supply current to 38µA per amplifier and places the outputs into a high-impedance state. The MAX4165–MAX4169's precision performance combined with high output current, wide input/output dynamic range, single-supply operation, and low power consumption makes them ideal for portable audio applications and other low-voltage, battery-powered systems. The MAX4165 is available in the space-saving 5-pin SOT23 package.

Selector Guide

PART	AMPS PER PACKAGE	SHUTDOWN MODE
MAX4165	Single	—
MAX4166	Single	Yes
MAX4167	Dual	—
MAX4168	Dual	Yes
MAX4169	Quad	—

Applications

Portable/Battery-Powered Audio Applications
Portable Head-Phone Speaker Drivers
Laptop/Notebook Computers
Sound Ports/Cards
Set-Top Boxes
Cell Phones
Hands-Free Car Phones (kits)
Signal Conditioning
Digital-to-Analog Converter Buffers
Transformer/Line Drivers
Motor Drivers

Typical Operating Circuit appears at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Features

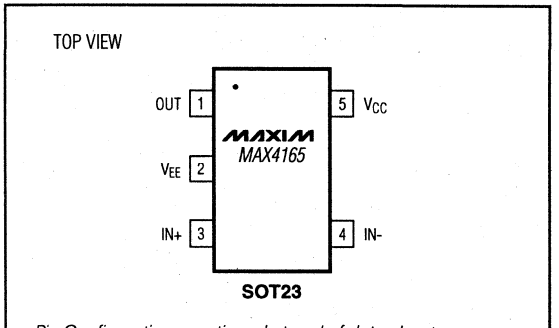
- ♦ **80mA (min) Output Drive Capability**
- ♦ **Rail-to-Rail Input Common-Mode Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Swing**
- ♦ **1.2mA Supply Current per Amplifier**
- ♦ **+2.7V to +6.5V Single-Supply Operation**
- ♦ **5MHz Gain-Bandwidth Product**
- ♦ **250µV Offset Voltage**
- ♦ **120dB Voltage Gain (R_L = 100kΩ)**
- ♦ **88dB Power-Supply Rejection Ratio**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Unity-Gain Stable for Capacitive Loads to 250pF**
- ♦ **Low-Power Shutdown Mode:**
  Reduces Supply Current to 38µA
  Places Outputs in High-Impedance State
- ♦ **Available in 5-Pin SOT23 Package (MAX4165)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4165EUK-T	-40°C to +85°C	5 SOT23-5	AABY
MAX4166EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4166ESA	-40°C to +85°C	8 SO	—
MAX4166EUA	-40°C to +85°C	8 µMAX	—

Ordering Information continued at end of data sheet.

Pin Configurations



Pin Configurations continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 7V
IN_+, IN_-, $\overline{SHDN}$_ ..... (V_{EE} - 0.3V) + (V_{CC} + 0.3V)
OUT_ (shutdown mode) ..... (V_{EE} - 0.3V) + (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE} (Note 1) .... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.10mW/°C above +70°C) 571mW
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C) 330mW
10-Pin µMAX (derate 5.60mW/°C above +70°C) 444mW
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) ... 800mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Continuous power dissipation should also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 100kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}	MAX416_EPA/EPD		0.25	0.85	mV
			MAX416_ESA/ESD		0.25	0.85	
			MAX416_EUA		0.35	1.7	
			MAX416_EUK		0.35	1.5	
			MAX4169E_D		0.25	1.0	
Input Bias Current	I_B	V_{CM} = V_{EE} to V_{CC}			±50	±150	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} to V_{CC}			±1	±15	nA
Differential Input Resistance	$R_{IN(DIFF)}$	$\lvert V_{IN+} - V_{IN-} \rvert \leq 1.8V$			500		kΩ
		$\lvert V_{IN+} - V_{IN-} \rvert > 1.8V$			2		
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		V_{EE} - 0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	CMRR	V_{EE} - 0.25V < V_{CM} < (V_{CC} + 0.25V)	MAX416_EPA/EPD	72	93		dB
			MAX416_ESA/ESD	72	93		
			MAX416_EUA	62	89		
			MAX416_EUK	63	90		
			MAX4169E_D	71	93		
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.5V	MAX416_EPA/EPD	72	88		dB
			MAX416_ESA/ESD	72	88		
			MAX416_EUA	72	86		
			MAX416_EUK	72	86		
			MAX4169E_D	70	88		
Output Resistance	R_{OUT}	A_{VCL} = +1V/V			0.1		Ω
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V, V_{OUT} = 0V to V_{CC}			±0.001	±2	µA
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ	95	120		dB
			V_{OUT} = 0.6V to 4.4V, R_L = 25Ω	71	83		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 100kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OUT}	V_{CC} = 5V	R_L = 100kΩ	V_{CC} - V_{OH}		15	30	mV
				V_{OL} - V_{EE}		10	25	
			R_L = 25Ω	V_{CC} - V_{OH}		340	430	
				V_{OL} - V_{EE}		160	350	
Output Source/Sink Current (Note 2)		V_{OUT} = 0.6V to (V_{CC} - 0.6V)			±80	±125		mA
$\overline{SHDN}$ Logic Threshold (Note 3)	V_{IL}	Shutdown mode					0.8	V
	V_{IH}	Normal mode			2.0			
$\overline{SHDN}$ Input Bias Current		$V_{EE} < V_{\overline{SHDN}} < V_{CC}$					±3.0	µA
Operating Supply-Voltage Range	V_{CC}	Inferred from PSRR test			2.7		6.5	V
Quiescent Supply Current (per Amplifier)	I_{CC}	V_{CC} = 5V				1.3	1.5	mA
		V_{CC} = 3V				1.2	1.4	
Shutdown Supply Current (per Amplifier)	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V		V_{CC} = 5V		58	75	µA
				V_{CC} = 3V		38	49	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 100kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = -40°C to +85°C,** unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}	MAX416_EPA/EPD			1.0	mV
			MAX416_ESA/ESD			1.0	
			MAX416_EUA			4.9	
			MAX416_EUK			4.3	
			MAX4169E_D			1.2	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$				±3		µV/°C
Input Bias Current	I_B	V_{CM} = V_{EE} to V_{CC}				±225	nA
Input Offset Current	I_{OS}	V_{CM} = V_{EE} to V_{CC}				±21	nA
Common-Mode Input Voltage Range	V_{CM}	Inferred from CMRR test		V_{EE} - 0.15		V_{CC} + 0.15	V
Common-Mode Rejection Ratio	CMRR	V_{EE} - 0.15V < V_{CM} < (V_{CC} + 0.15V)	MAX416_EPA/EPD			71	dB
			MAX416_ESA/ESD			71	
			MAX416_EUA			56	
			MAX416_EUK			57	
			MAX4169E_D			69	
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.7V to 6.5V	MAX416_EPA/EPD			67	dB
			MAX416_ESA/ESD			67	
			MAX416_EUA			65	
			MAX416_EUK			65	
			MAX4169E_D			66	

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 100kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V, V_{OUT} = 0V to V_{CC}					±5	µA
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ		90			dB
			V_{OUT} = 0.6V to 4.4V, R_L = 25Ω		66			
Output Voltage Swing	V_{OUT}	V_{CC} = 5V	R_L = 100kΩ	V_{CC} - V_{OH}			40	mV
				V_{OL} - V_{EE}			30	
			R_L = 25Ω	V_{CC} - V_{OH}			490	
				V_{OL} - V_{EE}			400	
Output Source/Sink Current (Note 2)		V_{OUT} = 0.6V to (V_{CC} - 0.6V)			±80			mA
$\overline{SHDN}$ Logic Threshold (Note 3)	V_{IL}	Shutdown mode					0.8	V
	V_{IH}	Normal mode			2.0			
$\overline{SHDN}$ Input Bias Current		V_{EE} < $V_{\overline{SHDN}}$ < V_{CC}					±3.5	µA
Operating Supply-Voltage Range	V_{CC}	Inferred from PSRR test			2.7		6.5	V
Quiescent Supply Current (per Amplifier)	I_{CC}	V_{CC} = 5V					1.7	mA
		V_{CC} = 3V					1.6	
Shutdown Supply Current (per Amplifier)	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V		V_{CC} = 5V			82	µA
				V_{CC} = 3V			54	

Note 2: Although the minimum output current is guaranteed to be ±80mA, exercise caution to ensure that the absolute maximum power-dissipation rating of the package is not exceeded.

Note 3: $\overline{SHDN}$ logic thresholds are referenced to V_{EE}.

Note 4: The MAX4165EUK is 100% tested at +25°C. All temperature limits are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 2.5kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, C_L = 15pF, **T_A = +25°C,** unless otherwise noted.)

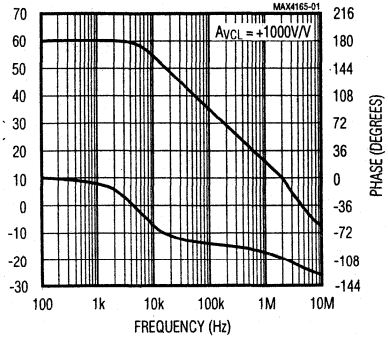
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP			5		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 4Vp-p, V_{CC} = 5V		260		kHz
Slew Rate	SR			2		V/µs
Phase Margin	PM			68		degrees
Gain Margin	GM			21		dB
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = 2Vp-p, A_{VCL} = +1V/V		0.005		%
Settling Time to 0.01%	t_S	A_{VCL} = +1V/V, 2V step		2.1		µs
Input Capacitance	C_{IN}			3		pF
Input Voltage Noise Density	e_n	f = 1kHz		26		nV/√Hz
Input Current Noise Density	i_n	f = 1kHz		0.4		pA/√Hz
Channel-to-Channel Isolation		f = 1kHz, R_L = 100kΩ (MAX4167–MAX4169)		125		dB
Capacitive Load Stability		A_{VCL} = +1V/V, no sustained oscillations		250		pF
Shutdown Time	$t_{\overline{SHDN}}$			1		µs
Enable Time from Shutdown	t_{ENABLE}			1		µs
Power-Up Time	t_{ON}			5		µs

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

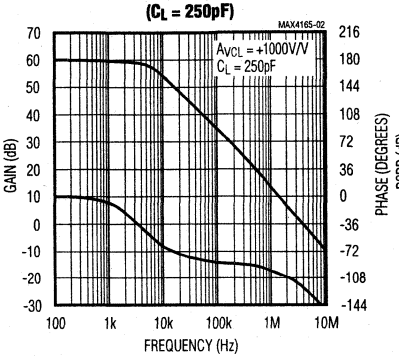
Typical Operating Characteristics

(V_{CC} = +5.0V, V_{EE} = 0V, R_L = 100kΩ, T_A = +25°C, unless otherwise noted.)

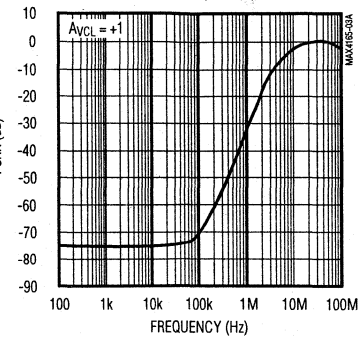
GAIN AND PHASE vs. FREQUENCY



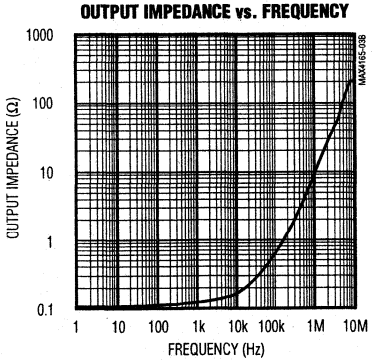
GAIN AND PHASE vs. FREQUENCY (C_L = 250pF)



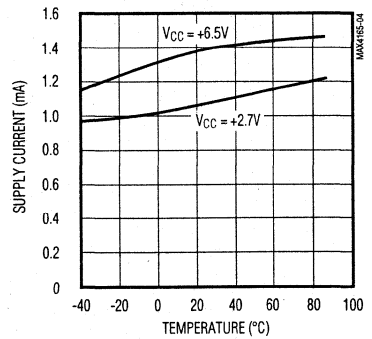
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



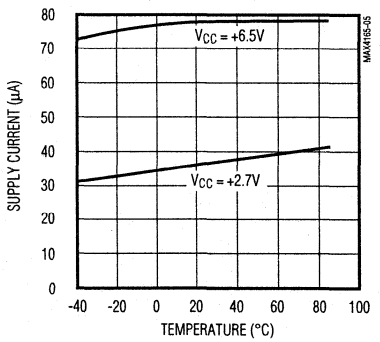
OUTPUT IMPEDANCE vs. FREQUENCY



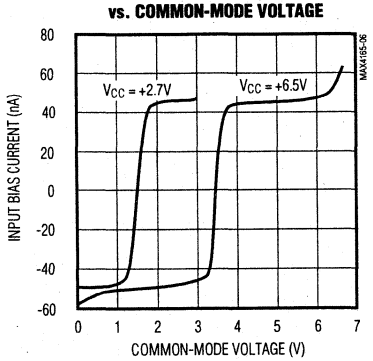
SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



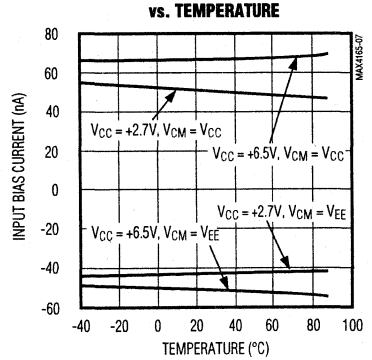
SHUTDOWN SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



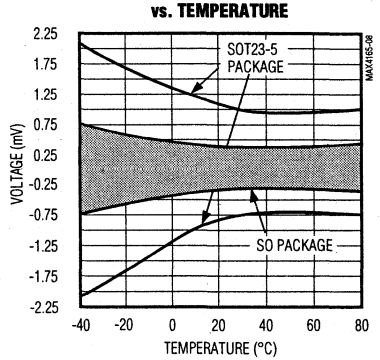
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



INPUT BIAS CURRENT vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE

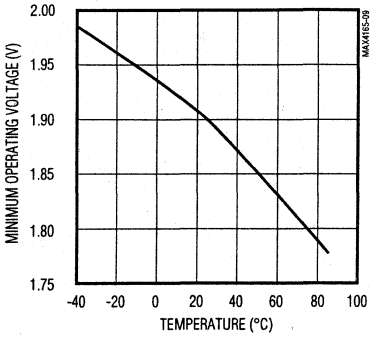


High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

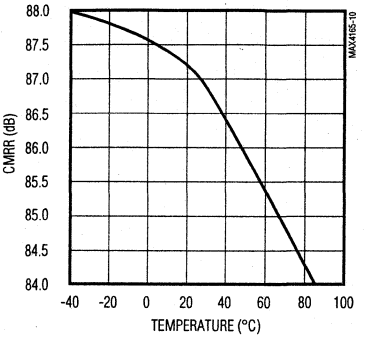
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, V_{EE} = 0V, R_L = 100kΩ, T_A = +25°C, unless otherwise noted.)

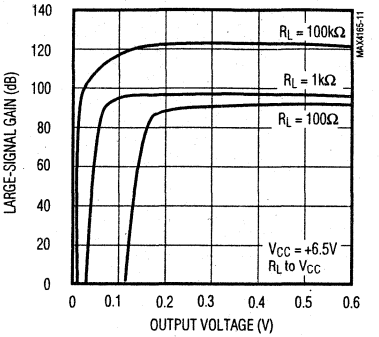
MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



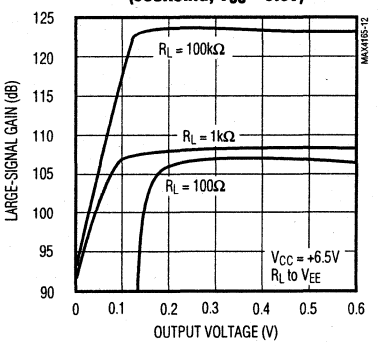
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



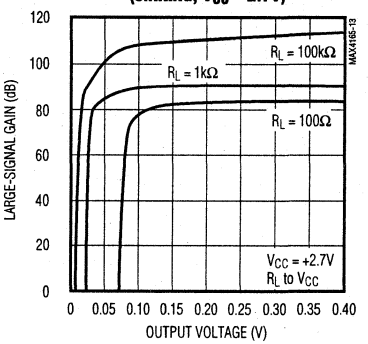
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (SINKING, V_{CC} = 6.5V)



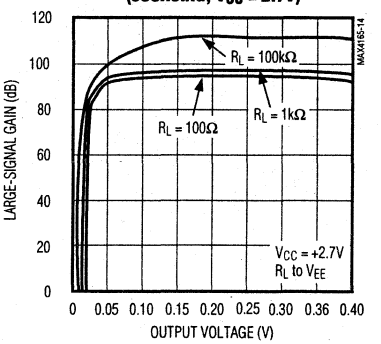
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (SOURCING, V_{CC} = 6.5V)



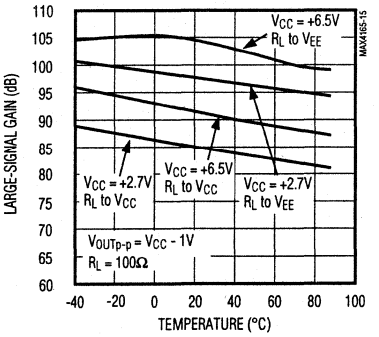
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (SINKING, V_{CC} = 2.7V)



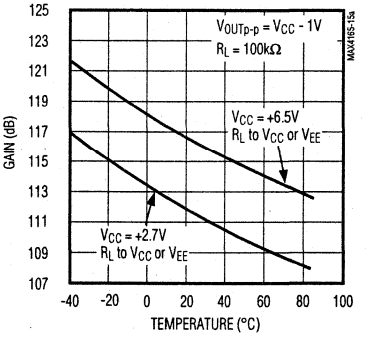
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (SOURCING, V_{CC} = 2.7V)



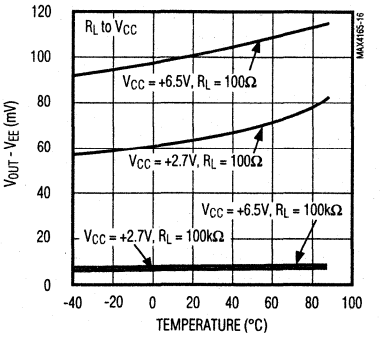
LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 100Ω)



LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 100kΩ)



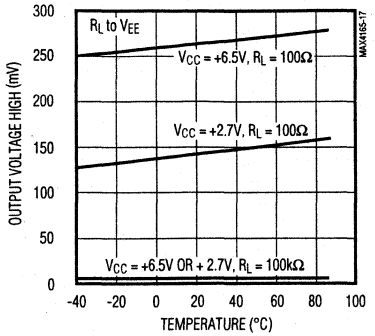
OUTPUT VOLTAGE LOW vs. TEMPERATURE



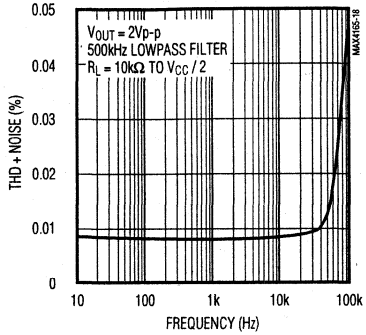
Typical Operating Characteristics (continued)

(V_{CC} = +5.0V, V_{EE} = 0V, R_L = 100kΩ, T_A = +25°C, unless otherwise noted.)

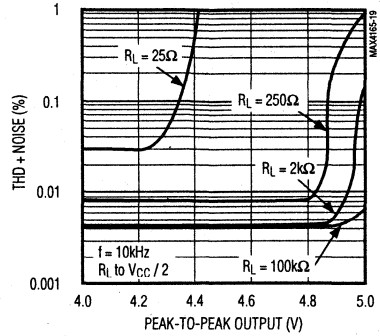
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



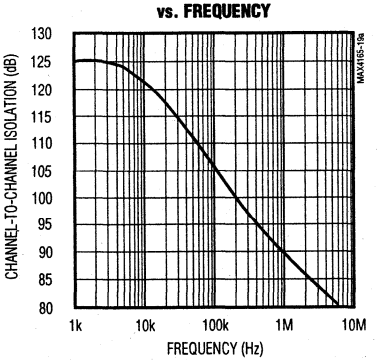
TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY



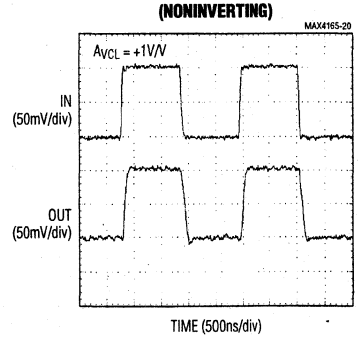
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK OUTPUT VOLTAGE



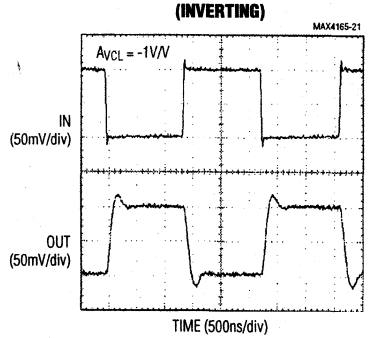
CHANNEL-TO-CHANNEL ISOLATION vs. FREQUENCY



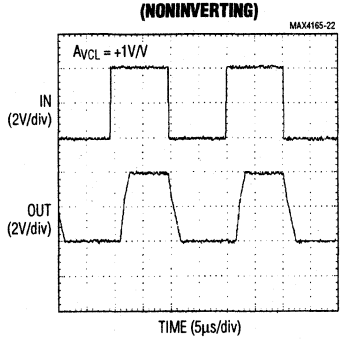
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



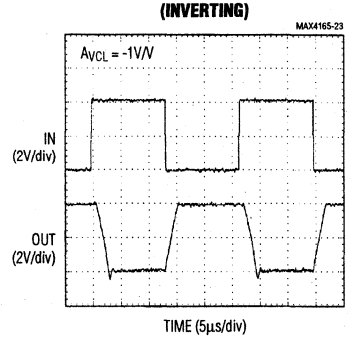
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Pin Description

PIN						NAME	FUNCTION
MAX4165	MAX4166	MAX4167	MAX4168		MAX4169		
			DIP/SO	µMAX			
1	6	—	—	—	—	OUT	Output
—	1, 5	—	5, 7, 8, 10	—	—	N.C.	No Connection. Not internally connected.
—	—	1, 7	1, 13	1, 9	1, 7	OUT1, OUT2	Outputs for Amplifiers 1 and 2
2	4	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	—	IN+	Noninverting Input
—		2, 6	2, 12	2, 8	2, 6	IN1-, IN2-	Inverting Inputs for Amplifiers 1 and 2
4	2	—	—	—	—	IN-	Inverting Input
—	—	3, 5	3, 11	3, 7	3, 5	IN1+, IN2+	Noninverting Inputs for Amplifiers 1 and 2
5	7	8	14	10	4	V_{CC}	Positive Supply
—	—	—	6, 9	5, 6	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Active-Low Shutdown Inputs for Amplifiers 1 and 2. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
—	8	—	—	—	—	$\overline{SHDN}$	Active-Low Shutdown Input. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amplifiers 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amplifiers 3 and 4
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amplifiers 3 and 4

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Applications Information

Package Power Dissipation

Warning: Due to the high output current drive, this op amp can exceed the absolute maximum power-dissipation rating. As a general rule, as long as the peak current is less than or equal to 80mA, the maximum package power dissipation will not be exceeded for any of the package types offered. There are some exceptions to this rule, however. The absolute maximum power-dissipation rating of each package should always be verified using the following equations. The following equation gives an approximation of the package power dissipation:

$$P_{IC(DISS)} \cong V_{RMS}\, I_{RMS} \cos\theta$$

where: V_{RMS} = the RMS voltage from V_{CC} to V_{OUT} when sourcing current

= the RMS voltage from V_{OUT} to V_{EE} when sinking current

I_{RMS} = the RMS current flowing out of or into the op amp and the load

θ = the phase difference between the voltage and the current. For resistive loads, $\cos\theta = 1$.

For example, the circuit in Figure 1 has a package power dissipation of 157mW.

$$V_{RMS} \cong (V_{CC} - V_{DC}) - \frac{V_{PEAK}}{\sqrt{2}}$$

$$= 6.5V - 3.25V - \frac{1.5V}{\sqrt{2}} = 2.189V_{RMS}$$

$$I_{RMS} \cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = \frac{3.25V}{60\Omega} + \frac{1.5V/60\Omega}{\sqrt{2}}$$

$$= 71.84mA_{RMS}$$

Therefore, $P_{IC(DISS)} = V_{RMS}\, I_{RMS} \cos\theta$

$= 157mW$

Adding a coupling capacitor improves the package power dissipation because there is no DC current to the load, as shown in Figure 2.

$$V_{RMS} \cong (V_{CC} - V_{DC}) - \frac{V_{PEAK}}{\sqrt{2}}$$

$$= 6.5V - 3.25V - \frac{1.5V}{\sqrt{2}} = 2.189V_{RMS}$$

$$I_{RMS} \cong I_{DC} + \frac{I_{PEAK}}{\sqrt{2}} = 0A + \frac{1.5V/60\Omega}{\sqrt{2}}$$

$$= 17.67mA_{RMS}$$

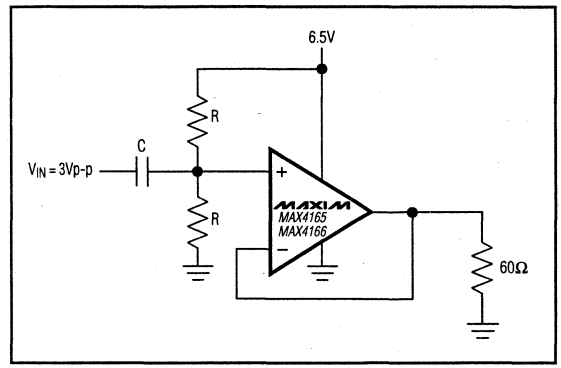


Figure 1. A Circuit Example where the MAX4165/MAX4166 is Being Used in Single-Supply Operation

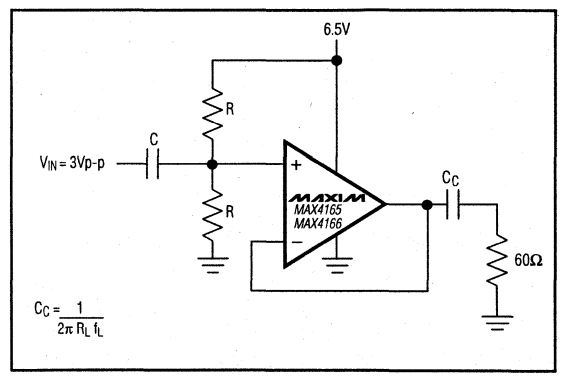


Figure 2. A Circuit Example where Adding a Coupling Capacitor Greatly Reduces the Power Dissipation of Its Package

Therefore, $P_{IC(DISS)} = V_{RMS}\, I_{RMS} \cos\theta$

$= 38.6mW$

The absolute maximum power-dissipation rating of this package would be exceeded if the configuration in Figure 1 were used with all four of the MAX4169ESD's amplifiers at a high ambient temperature of +75°C (157mW x 4 amplifiers = 628mW + a derating of 8.33mW/°C x 5°C = 669mW). Note that 669mW just exceeds the absolute maximum power dissipation of 667mW for the 14-pin SO package (see the *Absolute Maximum Ratings* section).

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

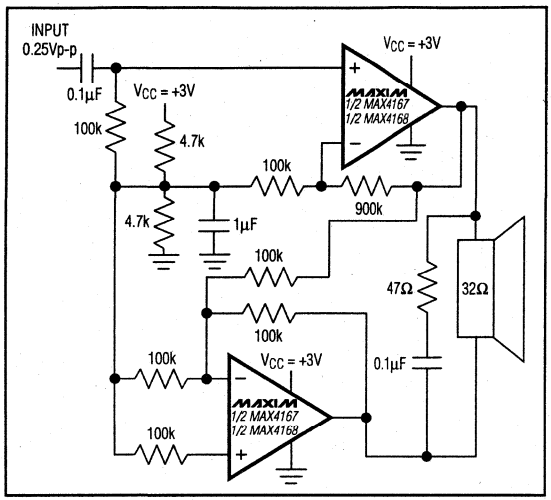


Figure 3. Dual MAX4167/MAX4168 Bridge Amplifier for 200mW at 3V

Single-Supply Speaker Driver

The MAX4165/MAX4166 can be used as a single-supply speaker driver, as shown in the *Typical Operating Circuit*. Capacitor C1 is used for blocking DC (a 0.1µF ceramic capacitor can be used). When choosing resistors R3 and R4, take into consideration the input bias current as well as how much supply current can be tolerated. Choose resistors R1 and R2 according to the amount of gain and current desired. Capacitor C3 ensures unity gain for DC. A 10µF electrolytic capacitor is suitable for most applications. The coupling capacitor C2 sets a low-frequency pole and is fairly large in value. For a 32Ω load, a 100µF coupling capacitor gives a low-frequency pole at 50Hz. The low-frequency pole can be set according to the following equation:

$$f = 1 / 2\pi (R_L C2)$$

Bridge Amplifier

The circuit shown in Figure 3 uses a dual MAX4167/MAX4168 to implement a 3V, 200mW amplifier suitable for use in size-constrained applications. This configuration eliminates the need for the large coupling capacitor required by the single op-amp speaker driver when single-supply operation is a must. Voltage gain is set to +10V/V; however, it can be changed by adjusting the 900kΩ resistor value. DC voltage at the speaker is limited to 10mV. The 47Ω and 0.1µF capacitors across the speaker maintain a low impedance at the load as frequency increases.

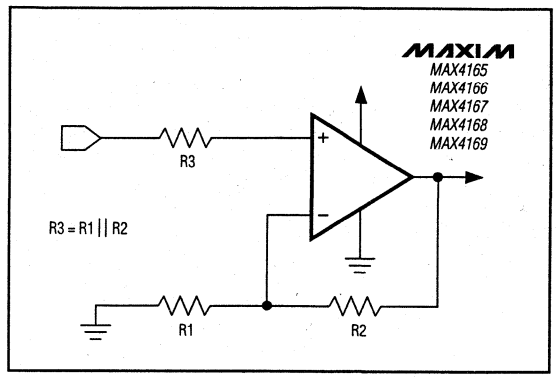


Figure 4. Reducing Offset Error Due to Bias Current (Noninverting)

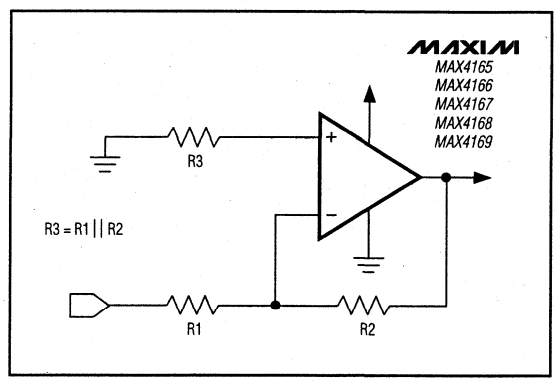


Figure 5. Reducing Offset Error Due to Bias Current (Inverting)

Rail-to-Rail Input Stage

Devices in the MAX4165–MAX4169 family of high-output-current amplifiers have rail-to-rail input and output stages designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages that combine to provide an input common-mode range that extends 0.25V beyond the supply rails. The PNP stage is active for input voltages close to the negative rail, and the NPN stage is active for input voltages near the positive rail. The switchover transition region, which occurs near V_{CC} / 2, has been extended to minimize the slight degradation in common-mode rejection ratio caused by mismatch of the input pairs.

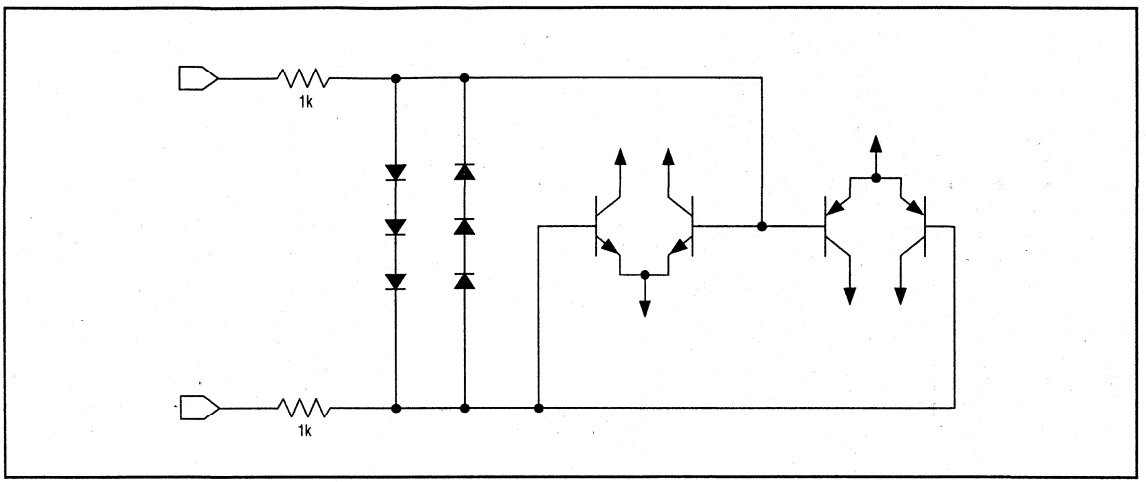


Figure 6. Input Protection Circuit

Since the input stage switches between the NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the transition region. Match the effective impedance seen by each input to reduce the offset error caused by input bias currents flowing through external source impedances (Figures 4 and 5).

High source impedances, together with input capacitance, can create a parasitic pole that produces an underdamped signal response. Reducing the input impedance or placing a small (2pF to 10pF) capacitor across the feedback resistor improves response.

The MAX4165–MAX4169's inputs are protected from large differential input voltages by 1kΩ series resistors and back-to-back triple diodes across the inputs (Figure 6).

For differential voltages less than 1.8V, input resistance is typically 500kΩ. For differential input voltages greater than 1.8V, input resistance is approximately 2kΩ. The input bias current is given by the following equation:

$$I_{BIAS} = (V_{DIFF} - 1.8V) / 2k\Omega$$

Rail-to-Rail Output Stage

The minimum output is within millivolts of ground for single-supply operation, where the load is referenced to ground (V_{EE}). Figure 7 shows the input voltage range and the output voltage swing of a MAX4165 connected as a voltage follower. The maximum output voltage swing is load dependent; however, it is guaranteed to be within 430mV of the positive rail (V_{CC} = 5V) even with maximum load (25Ω to ground).

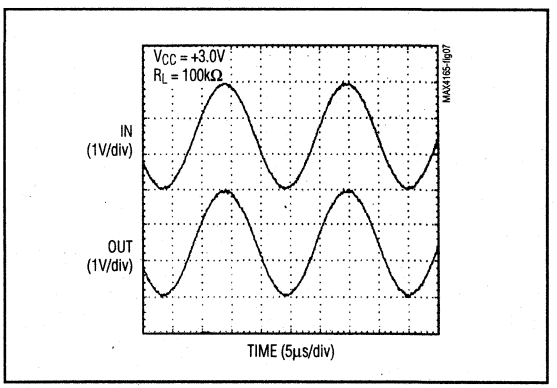


Figure 7. Rail-to-Rail Input/Output Range

Driving Capacitive Loads

The MAX4165–MAX4169 have a high tolerance for capacitive loads. They are stable with capacitive loads up to 250pF. Figure 8 is a graph of the stable operating region for various capacitive loads vs. resistive loads. Figures 9 and 10 show the transient response with excessive capacitive loads (1500pF), with and without the addition of an isolation resistor in series with the output. Figure 11 shows a typical noninverting capacitive-load-driving circuit in the unity-gain configuration. The resistor improves the circuit's phase margin by isolating the load capacitor from the op amp's output.

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

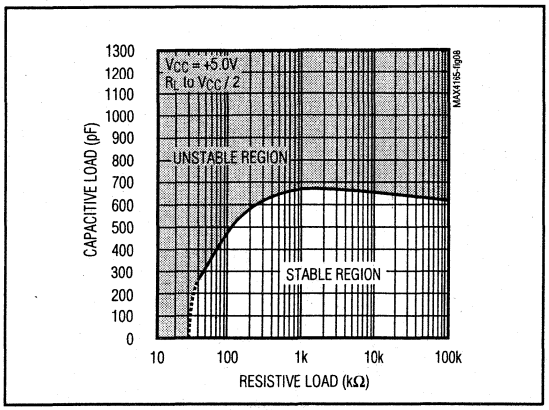


Figure 8. Capacitive Load Stability

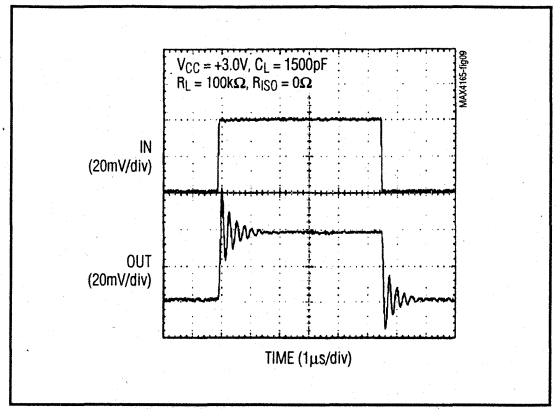


Figure 9. Small-Signal Transient Response with Excessive Capacitive Load

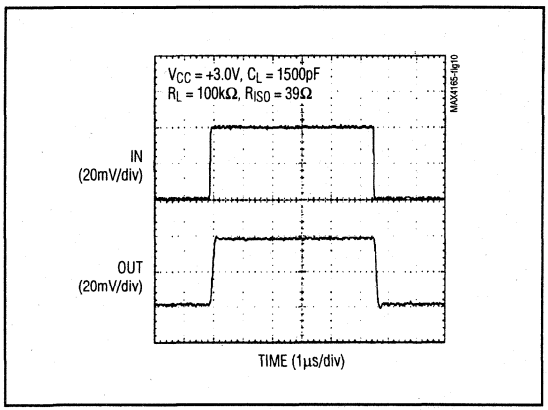


Figure 10. Small-Signal Transient Response with Excessive Capacitive Load with Isolation Resistor

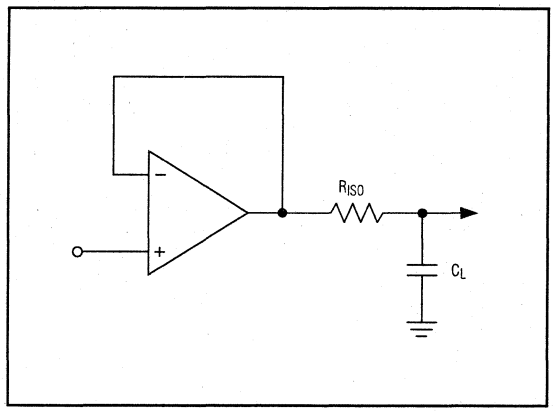


Figure 11. Capacitive-Load-Driving Circuit

Power-Up and Shutdown Modes

The MAX4166/MAX4168 have a shutdown option. When the shutdown pin ($\overline{SHDN}$) is pulled low, supply current drops to 58µA per amplifier (V_{CC} = +5V), the amplifiers are disabled, and their outputs are placed in a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. In the dual MAX4168, the two amplifiers shut down independently. Figures 12 and 13 show the MAX4166's output voltage and supply-current responses to a shutdown pulse. The MAX4166–MAX4169 typically settle within 5µs after power-up (Figure 14).

Power Supplies and Layout

The MAX4165–MAX4169 can operate from a single +2.7V to +6.5V supply, or from dual ±1.35V to ±3.25V supplies. For single-supply operation, bypass the power supply with a 0.1µF ceramic capacitor in parallel with at least 1µF. For dual-supply operation, bypass each supply to ground. Good layout improves performance by decreasing the amount of stray capacitance at the op amps' inputs and outputs. Decrease stray capacitance by placing external components close to the op amps' pins, minimizing trace and lead lengths.

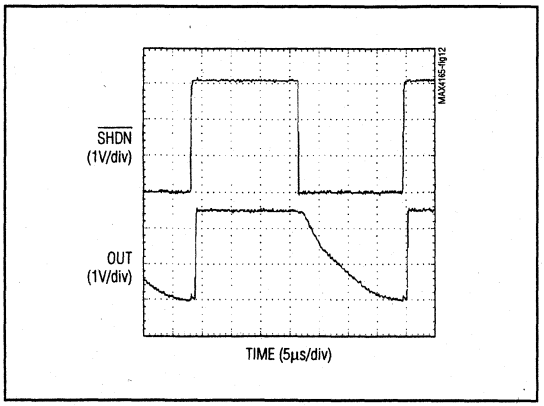


Figure 12. Shutdown Output Voltage Enable/Disable

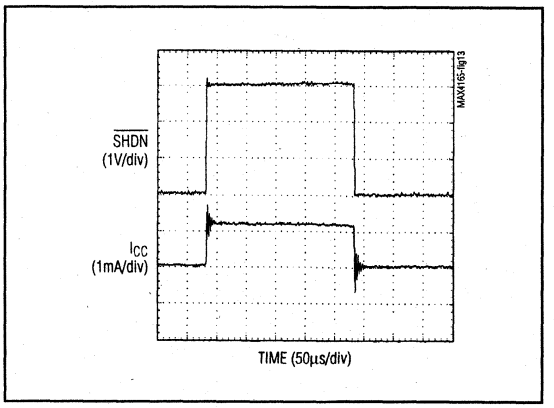


Figure 13. Shutdown Enable/Disable Supply Current

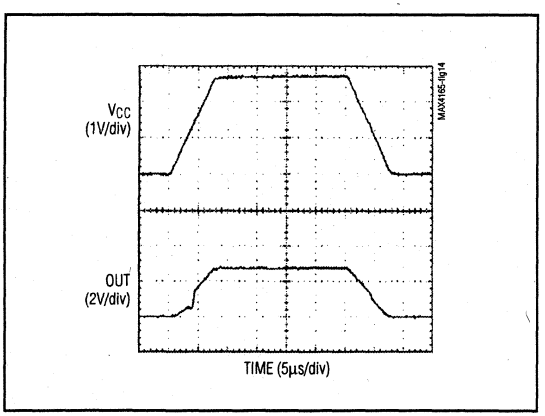


Figure 14. Power-Up/Down Output Voltage

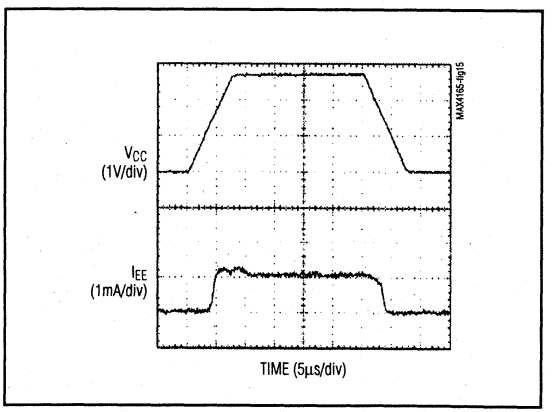
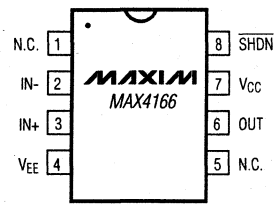


Figure 15. Power-Up/Down Supply Current

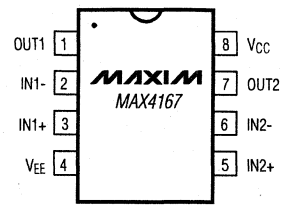
High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Pin Configurations (continued)

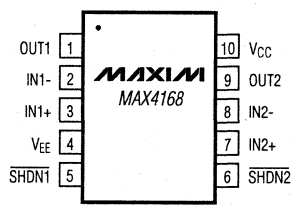
TOP VIEW



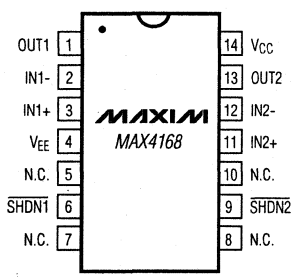
DIP/SO/μMAX



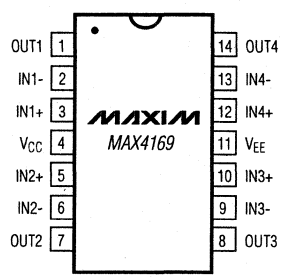
DIP/SO



μMAX



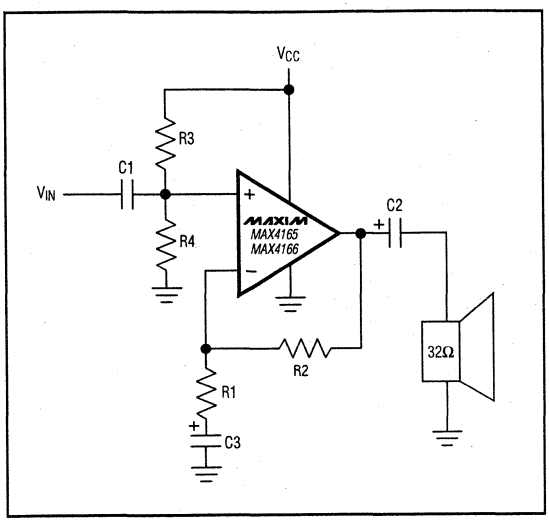
DIP/SO



DIP/SO

High-Output-Drive, Precision, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Typical Operating Circuit



Ordering Information (continued)

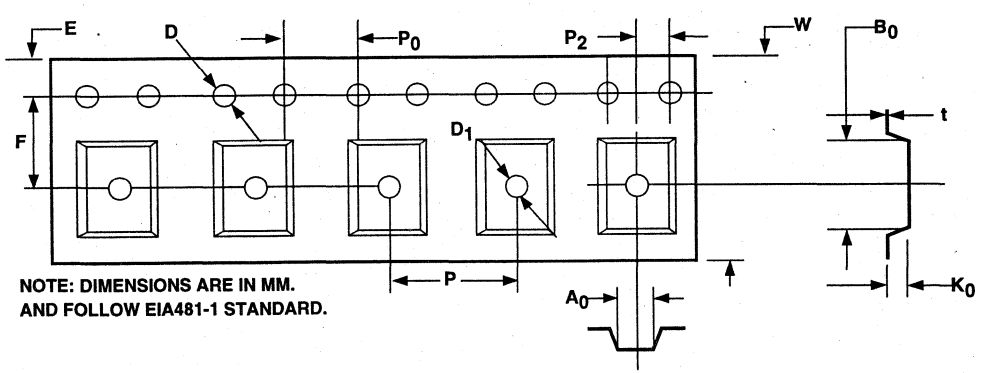
PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4167EPA	-40°C to +85°C	8 Plastic DIP	—
MAX4167ESA	-40°C to +85°C	8 SO	—
MAX4168EPD	-40°C to +85°C	14 Plastic DIP	—
MAX4168ESD	-40°C to +85°C	14 SO	—
MAX4168EUB	-40°C to +85°C	10 µMAX*	—
MAX4169EPD	-40°C to +85°C	14 Plastic DIP	—
MAX4169ESD	-40°C to +85°C	14 SO	—

**Contact factory for availability.*

Chip Information

MAX4165 TRANSISTOR COUNT: 230
MAX4166 TRANSISTOR COUNT: 230
MAX4167 TRANSISTOR COUNT: 462
MAX4168 TRANSISTOR COUNT: 462
MAX4169 TRANSISTOR COUNT: 924

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1184; Rev 0; 12/96

MAXIM

Low-Cost, Precision, High-Side Current-Sense Amplifier

General Description

The MAX4172 is a low-cost, precision, high-side current-sense amplifier for portable PCs, telephones, and other systems where battery/DC power-line monitoring is critical. High-side power-line monitoring is especially useful in battery-powered systems, since it does not interfere with the battery charger's ground path. Wide bandwidth and ground-sensing capability make the MAX4172 suitable for closed-loop battery-charger and general-purpose current-source applications. The 0V to 32V input common-mode range is independent of the supply voltage, which ensures that current-sense feedback remains viable, even when connected to a battery in deep discharge.

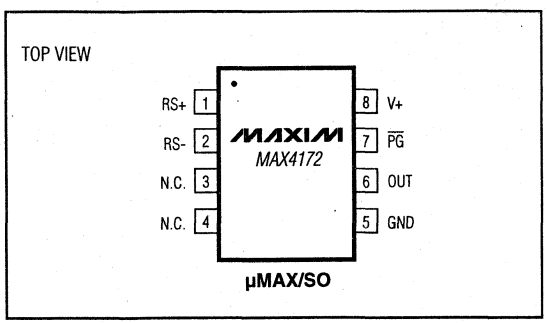
To provide a high level of flexibility, the MAX4172 functions with an external sense resistor to set the range of load current to be monitored. It has a current output that can be converted to a ground-referred voltage with a single resistor, accommodating a wide range of battery voltages and currents.

An open-collector power-good output ($\overline{PG}$) indicates when the supply voltage reaches an adequate level to guarantee proper operation of the current-sense amplifier. The MAX4172 operates with a 3.0V to 32V supply voltage, and is available in a space-saving, 8-pin µMAX or SO package.

Applications

Portable PCs: Notebooks/Subnotebooks/Palmtops
Battery-Powered/Portable Equipment
Closed-Loop Battery Chargers/Current Sources
Smart-Battery Packs
Portable/Cellular Phones
Portable Test/Measurement Systems
Energy Management Systems

Pin Configuration



µMAX/SO

Features

- ♦ **Low-Cost, High-Side Current-Sense Amplifier**
- ♦ **±0.5% Typical Full-Scale Accuracy Over Temperature**
- ♦ **3V to 32V Supply Operation**
- ♦ **0V to 32V Input Range—Independent of Supply Voltage**
- ♦ **800kHz Bandwidth [V_{SENSE} = 100mV (1C)]**
  200kHz Bandwidth [V_{SENSE} = 6.25mV (C/16)]
- ♦ **Available in Space-Saving µMAX and SO Packages**

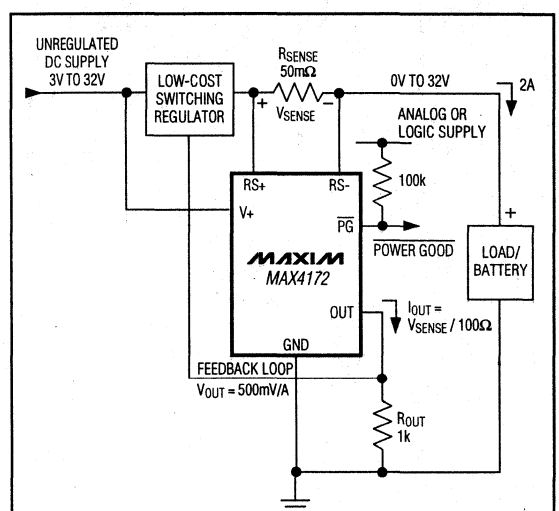
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4172ESA	-40°C to +85°C	8 SO
MAX4172EUA	-40°C to +85°C	8 µMAX*

Contact factory for availability.

3

Typical Operating Circuit



LOW-COST BATTERY CHARGER/CURRENT SOURCE

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Cost, Precision, High-Side Current-Sense Amplifier

ABSOLUTE MAXIMUM RATINGS

V+, RS+, RS-, $\overline{PG}$ ..... -0.3V to +36V
OUT ..... -0.3V to (V+ + 0.3V)
Differential Input Voltage, V_{RS+} - V_{RS-} ..... ±700mV
Current into Any Pin ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
Operating Temperature Range
MAX4172E_A ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +3V to +32V; RS+, RS- = 0V to 32V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at V+ = +12V, RS+ = 12V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V+			3		32	V
Input Voltage Range	V_{RS-}			0		32	V
Supply Current	I_{V+}	I_{OUT} = 0mA			0.8	1.6	mA
Input Offset Voltage	V_{OS}	V+ = 12V, V_{RS+} = 12V	MAX4172ESA		±0.1	±0.75	mV
			MAX4172EUA		±0.2	±1.6	
		V_{RS+} ≤ 2.0V			4		
Positive Input Bias Current	I_{RS+}	V_{RS+} > 2.0V, I_{OUT} = 0mA		0	27	42.5	µA
		V_{RS+} ≤ 2.0V, I_{OUT} = 0mA		-325		42.5	
Negative Input Bias Current	I_{RS-}	V_{RS+} > 2.0V		0	50	85	µA
		V_{RS+} ≤ 2.0V		-650		85	
Maximum V_{SENSE} Voltage				150	175		mV
Low-Level Current Error		V_{SENSE} = 6.25mV, V+ = 12V, V_{RS+} = 12V (Note 1)	MAX4172ESA			±8.0	µA
			MAX4172EUA			±15	
Output Current Error		V_{SENSE} = 100mV, V+ = 12V, V_{RS+} = 12V	MAX4172ESA, T_A = -40°C to 0°C			±20	µA
			MAX4172EUA, T_A = -40°C to 0°C			±50	
			MAX4172ESA, T_A = 0°C to +85°C			±10	
			MAX4172EUA, T_A = 0°C to +85°C			±15	
OUT Power-Supply Rejection Ratio	$\Delta I_{OUT} / \Delta V+$	3V ≤ V+ ≤ 32V, V_{RS+} > 2.0V			0.2		µA/V
OUT Common-Mode Rejection Ratio	$\Delta I_{OUT} / \Delta V_{RS+}$	2.0V < V_{RS+} < 32V			0.03		µA/V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +3V to +32V; RS+, RS- = 0V to 32V; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at V+ = +12V, RS+ = 12V, T_A = +25°C.)

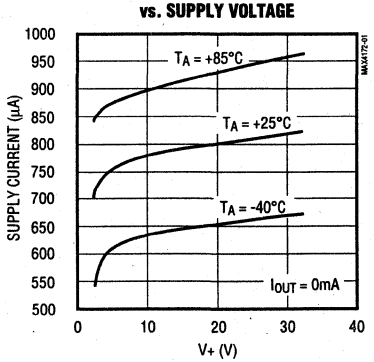
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Voltage (OUT)		I_{OUT} ≤ 1.5mA				V+ - 1.2	V
Bandwidth		V_{SENSE} = 100mV			800		kHz
		V_{SENSE} = 6.25mV (Note 1)			200		
Maximum Output Current	I_{OUT}			1.5	1.75		mA
Transconductance	G_m	G_m = I_{OUT} / (V_{RS+} - V_{RS-}), V_{SENSE} = 100mV, V_{RS+} > 2.0V	T_A = 0°C to +85°C	9.8	10	10.2	mA/V
			T_A = -40°C to 0°C	9.7	10	10.3	
V+ Threshold for $\overline{PG}$ Output Low (Note 2)		V+ rising			2.77		V
		V+ falling			2.67		
$\overline{PG}$ Output Low Voltage	V_{OL}	I_{SINK} = 1.2mA, V+ = 2.9V, T_A = +25°C				0.4	V
Leakage Current into $\overline{PG}$		V+ = 2.5V, T_A = +25°C				1	µA
Power-Off Input Leakage Current (RS+, RS-)		V+ = 0V, V_{RS+} = V_{RS-} = 32V			0.1	1	µA
OUT Rise Time		V_{SENSE} = 0mV to 100mV, 10% to 90%			400		ns
OUT Fall Time		V_{SENSE} = 100mV to 0mV, 90% to 10%			800		ns
OUT Settling Time to 1%		V_{SENSE} = 5mV to 100mV	Rising		1.3		µs
			Falling		6		
OUT Output Resistance		V_{SENSE} = 150mV			20		MΩ

Note 1: 6.25mV = 1/16 of typical full-scale sense voltage (C/16).
Note 2: Valid operation of the MAX4172 is guaranteed by design when $\overline{PG}$ is low.

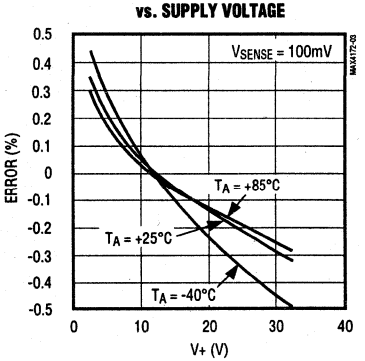
Typical Operating Characteristics

(V+ = +12V, V_{RS+} = 12V, R_{OUT} = 1kΩ, T_A = +25°C, unless otherwise noted.)

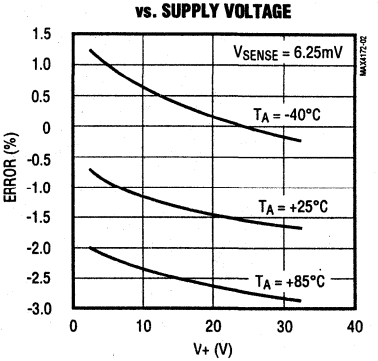
SUPPLY CURRENT vs. SUPPLY VOLTAGE



OUTPUT ERROR vs. SUPPLY VOLTAGE



C/16 LOAD OUTPUT ERROR vs. SUPPLY VOLTAGE

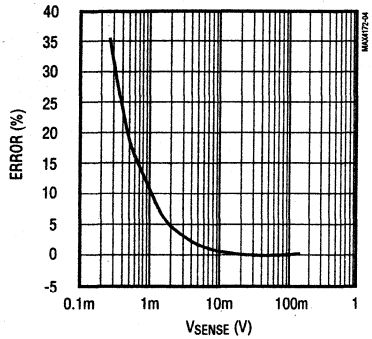


Low-Cost, Precision, High-Side Current-Sense Amplifier

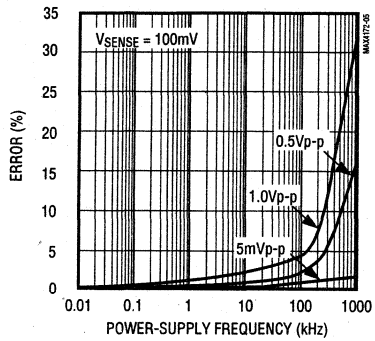
Typical Operating Characteristics (continued)

(V+ = +12V, V_{RS+} = 12V, R_{OUT} = 1kΩ, T_A = +25°C, unless otherwise noted.)

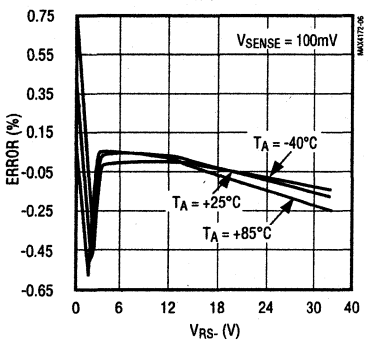
ERROR vs. SENSE VOLTAGE



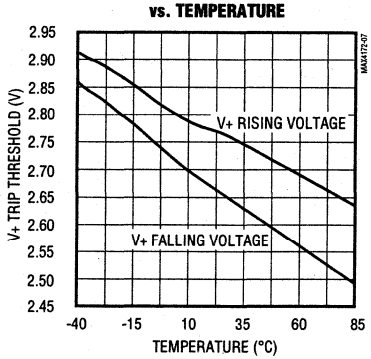
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



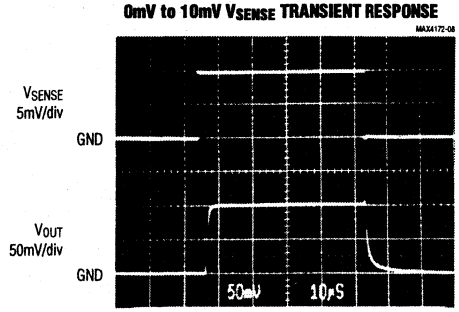
OUTPUT ERROR vs. COMMON-MODE VOLTAGE



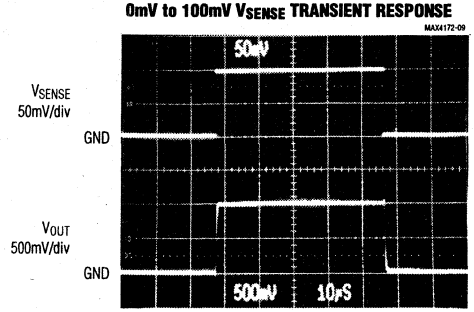
V+ THRESHOLD FOR $\overline{PG}$ OUTPUT LOW vs. TEMPERATURE



0mV to 10mV V_{SENSE} TRANSIENT RESPONSE



0mV to 100mV V_{SENSE} TRANSIENT RESPONSE

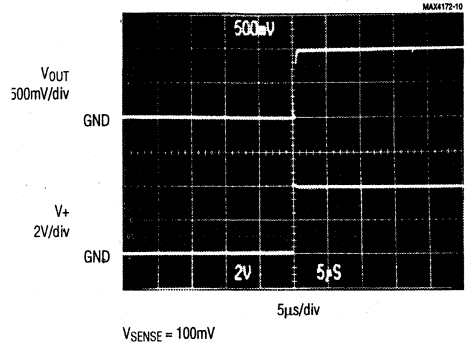


Low-Cost, Precision, High-Side Current-Sense Amplifier

Typical Operating Characteristics (continued)

(V+ = +12V, V_{RS+} = 12V, R_{OUT} = 1kΩ, T_A = +25°C, unless otherwise noted.)

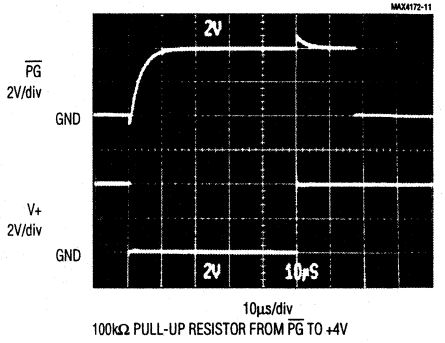
START-UP DELAY



5µs/div

V_{SENSE} = 100mV

V+ to $\overline{PG}$ POWER-UP DELAY



10µs/div

100kΩ PULL-UP RESISTOR FROM $\overline{PG}$ TO +4V

Pin Description

PIN	NAME	FUNCTION
1	RS+	Power connection to the external sense resistor. The "+" indicates the direction of current flow.
2	RS-	Load-side connection for the external sense resistor. The "-" indicates the direction of current flow.
3, 4	N.C.	No Connect. No internal connection. Leave open or connect to GND.
5	GND	Ground
6	OUT	Current Output. OUT is proportional to the magnitude of the sense voltage (V_{RS+} - V_{RS-}). A 1kΩ resistor from OUT to ground will result in a voltage equal to 10V/V of sense voltage.
7	$\overline{PG}$	Power Good Open-Collector Logic Output. A low level indicates that V+ is sufficient to power the MAX4172, and adequate time has passed for power-on transients to settle out.
8	V+	Supply Voltage Input for the MAX4172

Detailed Description

The MAX4172 is a unidirectional, high-side current-sense amplifier with an input common-mode range that is independent of supply voltage. This feature not only allows the monitoring of current flow into a battery in deep discharge, but also enables high-side current sensing at voltages far in excess of the supply voltage (V+).

The MAX4172 current-sense amplifier's unique topology simplifies current monitoring and control. The MAX4172's amplifier operates as shown in Figure 1. The battery/load current flows through the external sense resistor (R_{SENSE}), from the RS+ node to the RS- node. Current flows through R_{G1} and Q1, and into the current mirror, where it is multiplied by a factor of 50 before appearing at OUT.

To analyze the circuit of Figure 1, assume that current flows from RS+ to RS-, and that OUT is connected to GND through a resistor. Since A1's inverting input is high impedance, no current flows though R_{G2} (neglecting the input bias current), so A1's negative input is equal to V_{SOURCE} - (I_{LOAD} x R_{SENSE}). A1's open-loop gain forces its positive input to essentially the same voltage level as the negative input. Therefore, the drop across R_{G1} equals I_{LOAD} x R_{SENSE}. Then, since I_{RG1}

Low-Cost, Precision, High-Side Current-Sense Amplifier

flows through R_{G1}, $I_{RG1} \times R_{G1} = I_{LOAD} \times R_{SENSE}$. The internal current mirror multiplies I_{RG1} by a factor of 50 to give $I_{OUT} = 50 \times I_{RG1}$. Substituting $I_{OUT} / 50$ for I_{RG1}, $(I_{OUT} / 50) \times R_{G1} = I_{LOAD} \times R_{SENSE}$, or:

$$I_{OUT} = 50 \times I_{LOAD} \times (R_{SENSE} / R_{G1})$$

The internal current gain of 50 and the factory-trimmed resistor R_{G1} combine to result in the MAX4172 transconductance (G_m) of 10mA/V. G_m is defined as being equal to $I_{OUT} / (V_{RS+} - V_{RS-})$. Since $(V_{RS+} - V_{RS-}) = I_{LOAD} \times R_{SENSE}$, the output current ($I_{OUT}$) can be calculated with the following formula:

$$I_{OUT} = G_m \times (V_{RS+} - V_{RS-}) =$$
$$(10mA/V) \times (I_{LOAD} \times R_{SENSE})$$

Current Output

The output voltage equation for the MAX4172 is given below:

$$V_{OUT} = (G_m) \times (R_{SENSE} \times R_{OUT} \times I_{LOAD})$$

where V_{OUT} = the desired full-scale output voltage, I_{LOAD} = the full-scale current being sensed, R_{SENSE} = the current-sense resistor, R_{OUT} = the voltage-setting resistor, and G_m = MAX4172 transconductance (10mA/V).

The full-scale output voltage range can be set by changing the R_{OUT} resistor value, but the output voltage must be no greater than V+ - 1.2V. The above equation can be modified to determine the R_{OUT} required for a particular full-scale range:

$$R_{OUT} = (V_{OUT}) / (I_{LOAD} \times R_{SENSE} \times G_m)$$

OUT is a high-impedance current source that can be integrated by connecting it to a capacitive load.

$\overline{PG}$ Output

The $\overline{PG}$ output is an open-collector logic output that indicates the status of the MAX4172's V+ power supply. A logic low on the $\overline{PG}$ output indicates that V+ is sufficient to power the MAX4172. This level is temperature dependent (see *Typical Operating Characteristics* graphs), and is typically 2.7V at room temperature. The internal PG comparator has a 100mV (typical) hysteresis to prevent possible oscillations caused by repeated toggling of the $\overline{PG}$ output, making the device ideal for power-management systems lacking soft-start capability. An internal delay (15µs typical) in the $\overline{PG}$ comparator allows adequate time for power-on transients to settle out. The $\overline{PG}$ status indicator greatly simplifies the design of closed-loop systems by ensuring that the components in the control loop have sufficient voltage to operate correctly.

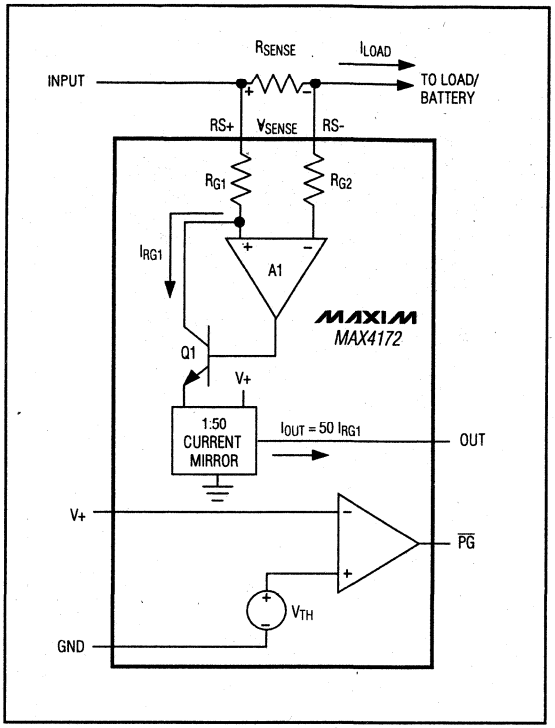


Figure 1. Functional Diagram

Applications Information

Suggested Component Values for Various Applications

The *Typical Operating Circuit* is useful in a wide variety of applications. Table 1 shows suggested component values and indicates the resulting scale factors for various applications required to sense currents from 100mA to 10A.

Adjust the R_{SENSE} value to monitor higher or lower current levels. Select R_{SENSE} using the guidelines and formulas in the following section.

Sense Resistor, R_{SENSE}

Choose R_{SENSE} based on the following criteria:

- **Voltage Loss:** A high R_{SENSE} value causes the power-source voltage to degrade through IR loss. For minimal voltage loss, use the lowest R_{SENSE} value.

Table 1. Suggested Component Values

FULL-SCALE LOAD CURRENT (A)	CURRENT-SENSE RESISTOR, R_{SENSE} (mΩ)	OUTPUT RESISTOR, R_{OUT} (kΩ)	FULL-SCALE OUTPUT VOLTAGE, V_{OUT} (V)	SCALE FACTOR, V_{OUT}/I_{SENSE} (V/A)
0.1	1000	3.48	3.48	34.8
1	100	3.48	3.48	3.48
5	20	3.48	3.48	0.696
10	10	3.48	3.48	0.348

- **Accuracy:** A high R_{SENSE} value allows lower currents to be measured more accurately. This is because offsets become less significant when the sense voltage is larger. For best performance, select R_{SENSE} to provide approximately 100mV of sense voltage for the full-scale current in each application.
- **Efficiency and Power Dissipation:** At high current levels, the I^2R losses in R_{SENSE} can be significant. Take this into consideration when choosing the resistor value and its power dissipation (wattage) rating. Also, the sense resistor's value might drift if it is allowed to heat up excessively.
- **Inductance:** Keep inductance low if I_{SENSE} has a large high-frequency component. Wire-wound resistors have the highest inductance, while metal film is somewhat better. Low-inductance metal-film resistors are also available. Instead of being spiral wrapped around a core, as in metal-film or wire-wound resistors, they are a straight band of metal and are available in values under 1Ω.
- **Cost:** If the cost of R_{SENSE} is an issue, you might want to use an alternative solution, as shown in Figure 2. This solution uses the PC board traces to create a sense resistor. Because of the inaccuracies of the copper resistor, the full-scale current value must be adjusted with a potentiometer. Also, copper's resistance temperature coefficient is fairly high (approximately 0.4%/°C).

In Figure 2, assume that the load current to be measured is 10A, and that you have determined a 0.3-inch-wide, 2-ounce copper to be appropriate. The resistivity of 0.1-inch-wide, 2-ounce (70µm thickness) copper is 30mΩ/ft. For 10A, you might want R_{SENSE} = 5mΩ for a 50mV drop at full scale. This resistor requires about 2 inches of 0.1-inch-wide copper trace.

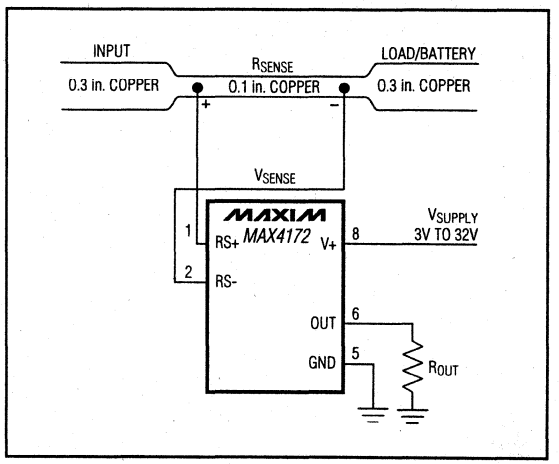


Figure 2. MAX4172 Connections Showing Use of PC Board

Current-Sense Adjustment (Resistor Range, Output Adjust)

Choose R_{OUT} after selecting R_{SENSE}. Choose R_{OUT} to obtain the full-scale voltage you require, given the full-scale I_{OUT} determined by R_{SENSE}. OUT's high impedance permits using R_{OUT} values up to 200kΩ with minimal error. OUT's load impedance (e.g., the input of an op amp or ADC) must be much greater than R_{OUT} (e.g., 100 x R_{OUT}) to avoid degrading measurement accuracy.

High-Current Measurement

The MAX4172 can achieve high-current measurements by using low-value sense resistors, which can be paralleled to further increase the current-sense limit. As an alternative, PC board traces can be adjusted over a wide range.

Low-Cost, Precision, High-Side Current-Sense Amplifier

Power-Supply Bypassing and Grounding

In most applications, grounding the MAX4172 requires no special precautions. However, in high-current systems, large voltage drops can develop across the ground plane, which can add to or subtract from V_{OUT}. Use a single-point star ground for the highest current-measurement accuracy.

The MAX4172 requires no special bypassing and responds quickly to transient changes in line current. If the noise at OUT caused by these transients is a problem, you can place a 1µF capacitor at the OUT pin to ground. You can also place a large capacitor at the RS terminal (or load side of the MAX4172) to decouple the load, reducing the current transients. These capacitors are not required for MAX4172 operation or stability. The RS+ and RS- inputs can be filtered by placing a capacitor (e.g., 1µF) between them to average the sensed current.

Chip Information

TRANSISTOR COUNT: 177

SUBSTRATE CONNECTED TO GND

MAXIM

Single/Dual/Quad, Ultra-Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

General Description

The MAX4230 family of amplifiers combines rail-to-rail inputs and outputs, low input bias current, and excellent capacitive-load driving capability with micropower operation in miniature packages. These devices operate from a single +2.7V to +5.5V supply or from dual ±1.35V to ±2.75V supplies. They require only 5.5µA of supply current per amplifier while delivering ±2.4mA of output current drive.

The MAX4230/MAX4231/MAX4232 are compensated for applications with a closed-loop gain of +1V/V (0dB) or greater and provide a gain-bandwidth product of 40kHz (G = +10V/V). The MAX4233/MAX4234/MAX4235 are compensated for applications with a closed-loop gain of +10V/V (20dB) or greater and provide a gain-bandwidth product of 379kHz (G = +100V/V).

Micropower operation combined with 100µV offset voltage, 250pA input bias current, and 120dB of open-loop gain makes these devices ideal for battery-powered remote sensing applications. The single MAX4230/MAX4233 are available in miniature 5-pin SOT23 packages. All devices are available for operation over the extended -40°C to +85°C operating temperature range.

Applications

Portable/Battery-Powered Systems

Remote Sensing

Medical Instrumentation

Electrometer Amplifiers

Photodiode Preamps

pH Meters

Smoke Detectors

Selector Guide

PART	NO. OF AMPLIFIERS	MINIMUM GAIN (V/V)	PIN-PACKAGE
MAX4230	1	1	5-pin SOT23 8-pin SO
MAX4231	2	1	8-pin SO/µMAX
MAX4232	4	1	14-pin SO 16-pin QSOP
MAX4233	1	10	5-pin SOT23 8-pin SO
MAX4234	2	10	8-pin SO/µMAX
MAX4235	4	10	14-pin SO 16-pin QSOP

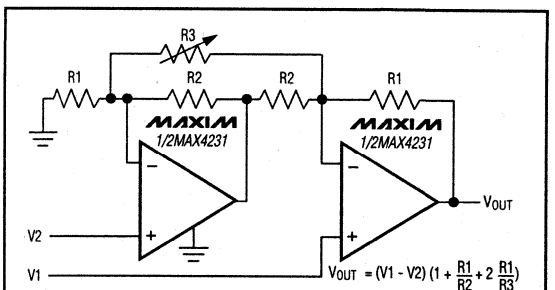
Features

- ♦ **Ultra-Low Supply Current: 5.5µA per Amplifier**
- ♦ **Operate from a Single Supply down to 2.7V**
- ♦ **Rail-to-Rail Common-Mode Input Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Swing**
- ♦ **40kHz Gain-Bandwidth Product (G = +10V/V)**
- ♦ **Available in Tiny Surface-Mount Packages:**
  - **5-pin SOT23 (MAX4230/MAX4233)**
  - **8-pin µMAX (MAX4231/MAX4234)**
  - **16-pin QSOP (MAX4232/MAX4235)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4230ESA	-40°C to +85°C	8 SO	—
MAX4230EUK-T	-40°C to +85°C	5 SOT23-5	ABZZ
MAX4231ESA	-40°C to +85°C	8 SO	—
MAX4231EUA	-40°C to +85°C	8 µMAX	—
MAX4232ESD	-40°C to +85°C	14 SO	—
MAX4232EEE	-40°C to +85°C	16 QSOP	—
MAX4233ESA	-40°C to +85°C	8 SO	—
MAX4233EUK-T	-40°C to +85°C	5 SOT23-5	ACAA
MAX4234ESA	-40°C to +85°C	8 SO	—
MAX4234EUA	-40°C to +85°C	8 µMAX	—
MAX4235ESD	-40°C to +85°C	14 SO	—
MAX4235EEE	-40°C to +85°C	16 QSOP	—

Typical Operating Circuit



MICROPOWER, HIGH-INPUT-IMPEDANCE DIFFERENTIAL AMPLIFIER WITH VARIABLE GAIN

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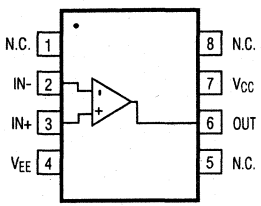
Single/Dual/Quad, Ultra-Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps

Pin Configurations/Functional Diagrams

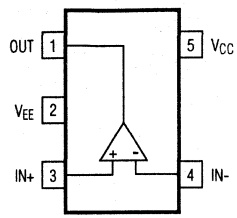
TOP VIEW

MAXIM
MAX4230
MAX4233



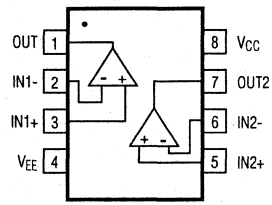
SO

MAXIM
MAX4230
MAX4233



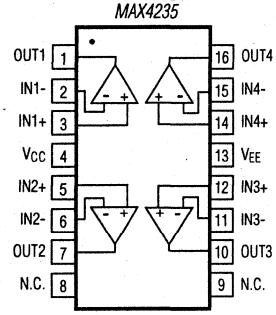
SOT23-5

MAXIM
MAX4231
MAX4234



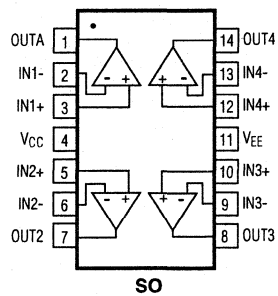
SO/μMAX

MAXIM
MAX4232
MAX4235



QSOP

MAXIM
MAX4232
MAX4235



SO

N.C. = NOT INTERNALLY CONNECTED

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Single/Dual/Quad, 1.8V Micropower, SOT23, Rail-to-Rail I/O Op Amps

General Description

The MAX4240–MAX4244 op amps operate from a +1.8V to +5.5V single supply and have Rail-to-Rail® input and output capabilities. These op amps have a 100kHz gain-bandwidth product while using only 10µA of supply current per amplifier in normal operation. The MAX4241/MAX4243 have a low-power shutdown mode that reduces supply current to less than 1µA and forces the output into a high-impedance state. The combination of ultra-low-voltage operation, rail-to-rail inputs and outputs, and low power consumption makes these devices ideal for any portable/two-cell battery-powered systems.

These devices have an input common-mode range that extends 200mV beyond each rail. Their output typically swings to within 30mV of the rails with a 10kΩ load. These rail-to-rail input and output characteristics allow full power-supply voltage to be used for signal range. The combination of low input offset voltage, low input bias current, and high open-loop gain makes them suitable for many low-power, precision applications.

The MAX4240 is offered in a space saving 5-pin SOT23 package. The MAX4240 family specifications are guaranteed over the -40°C to +85°C extended temperature range.

Applications

Two-Cell Battery-Powered Systems
Portable Electronic Equipment
Battery-Powered Instrumentation
Digital Scales
Strain Gauges
Sensor Amplifiers
Low-Power/Low-Voltage Equipment
Portable Medical Instruments
Cellular Phones

Selector Guide

PART	No. AMPLIFIERS	SHUT-DOWN	PIN-PACKAGE
MAX4240	1	—	5 SOT23
MAX4241	1	Yes	8 µMAX/8 SO
MAX4242	2	—	8 µMAX/8 SO
MAX4243	2	Yes	10 µMAX/14 SO
MAX4244	4	—	14 SO

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

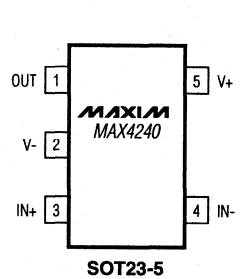
Features

- ♦ **Down to 1.8V Guaranteed Operation**
- ♦ **10µA (typ) Supply Current per Amplifier**
- ♦ **100kHz Gain-Bandwidth Product**
- ♦ **Output Swings Rail-to-Rail**
- ♦ **Input Common-Mode Range Extends 200mV Beyond the Rails**
- ♦ **1µA Shutdown Mode (MAX4241/MAX4243)**
- ♦ **Unity-Gain Stable For Capacitive Loads up to 100pF**
- ♦ **250µV Input Offset Voltage**
- ♦ **No Output Phase Reversal for Overdriven Inputs**
- ♦ **Available in Space-Saving 5-pin SOT23 and 8-pin µMAX Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4240EUK-T	-40°C to +85°C	5 SOT23-5
MAX4241ESA	-40°C to +85°C	8 SO
MAX4241EUA	-40°C to +85°C	8 µMAX
MAX4242ESA	-40°C to +85°C	8 SO
MAX4242EUA	-40°C to +85°C	8 µMAX
MAX4243ESD	-40°C to +85°C	14 SO
MAX4243EUB	-40°C to +85°C	10 µMAX
MAX4244ESD	-40°C to +85°C	14 SO

Pin Configurations



SOT23-5

Pin Configurations continued on next page.

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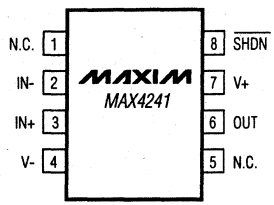
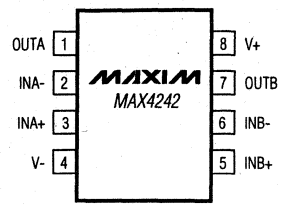
Single/Dual/Quad, 1.8V Micropower, SOT23, Rail-to-Rail I/O Op Amps

Pin Configurations (continued)

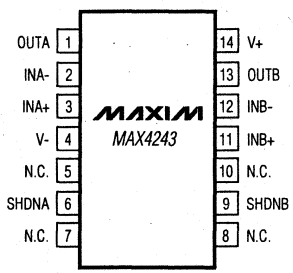
TOP VIEW



SO/μMAX



SO/μMAX



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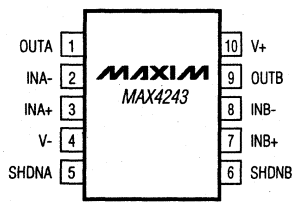
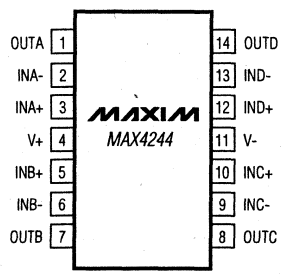


μMAX



SO

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ADVANCE INFORMATION

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8/97

MAXIM

Single/Dual/Quad, Low Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amps

General Description

The MAX4250 family of low-noise, low-distortion amplifiers offers rail-to-rail outputs and single-supply operation down to 2.4V. These op amps draw only 400µA of quiescent supply current per amplifier while featuring ultra-low distortion (0.0002%), low input voltage and current-noise density of only 7.9nV/√Hz and 0.5fA/√Hz, respectively. These features make these devices ideal choices for portable/battery-powered applications that require low distortion and/or low noise.

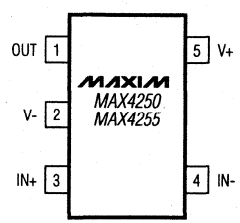
The MAX4249–MAX4257 outputs swing Rail-to-Rail®, and their input common-mode voltage range extends to ground. The MAX4249/MAX4251/MAX4253/MAX4256 have a low-power shutdown mode, which reduces supply current to 500nA and puts the amplifiers' outputs into a high-impedance state. The single MAX4250/MAX4255 are available in 5-pin SOT23-5 packages for space-critical applications.

Applications

Battery-Operated Systems
Medical Instrumentation
Analog-to-Digital Converter Buffers
Portable Electronic Equipment
Battery-Powered Instrumentation
Digital Scales
Strain Gauges
Sensor Amplifiers
Portable Communication Devices

Pin Configurations

TOP VIEW



SOT23

Pin Configurations continued on next page.

Features

- ♦ **Low Input Voltage Noise Density, Current-Noise Density: 7.9nV/√Hz, 0.5fA/√Hz**
- ♦ **0.0002% Total Harmonic Distortion (2Vp-p, 1kHz, 1kΩ load)**
- ♦ **400µA Quiescent Supply Current per Amplifier**
- ♦ **+2.4V to +5.5V Single-Supply Operation**
- ♦ **Input Common-Mode Voltage Range Includes Ground**
- ♦ **Outputs Swing Within 8mV of Rails with a 10kΩ Load**
- ♦ **3MHz Gain-Bandwidth Product (MAX4250–MAX4254)**
- ♦ **22MHz Gain-Bandwidth Product with $A_V \geq 10$ (MAX4249/MAX4255/MAX4256/MAX4257)**
- ♦ **Low-Power Shutdown Mode:**
  Reduces Supply Current to 500nA
  Outputs Placed in High-Impedance State
- ♦ **400pF Capacitive Load-Handling Capability**
- ♦ **<1pA Input Bias Current**
- ♦ **134dB Open-Loop Voltage Gain**
- ♦ **Available in Space-Saving SOT23/µMAX Packages**

Selector Guide

PART	GBW (MHz)	AMP/ PKG	SHDN MODE	PACKAGE
MAX4249	22	2	Yes	10-pin µMAX, 14-pin SO
MAX4250	3	1	—	5-pin SOT23
MAX4251	3	1	Yes	8-pin µMAX/SO
MAX4252	3	2	—	8-pin µMAX/SO
MAX4253	3	2	Yes	10-pin µMAX, 14-pin SO
MAX4254	3	4	—	14-pin SO
MAX4255	22	1	—	5-pin SOT23
MAX4256	22	1	Yes	8-pin µMAX/SO
MAX4257	22	2	—	8-pin µMAX/SO

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

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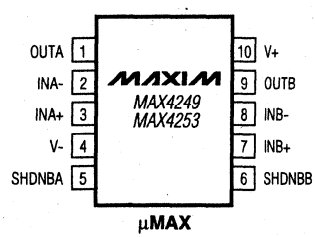
Single/Dual/Quad, Low Noise/Distortion, Single-Supply, Low-Power, Rail-to-Rail Op Amps

Ordering Information

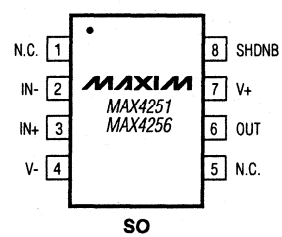
PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4249EUB	-40°C to +85°C	10 µMAX	—
MAX4249ESD	-40°C to +85°C	14 SO	—
MAX4250EUK-T	-40°C to +85°C	5 SOT23-5	ACCI
MAX4251ESA	-40°C to +85°C	8 SO	—
MAX4251EUA	-40°C to +85°C	8 µMAX	—
MAX4252ESA	-40°C to +85°C	8 SO	—
MAX4252EUA	-40°C to +85°C	8 µMAX	—
MAX4253ESD	-40°C to +85°C	14 SO	—
MAX4253EUB	-40°C to +85°C	10 µMAX	—
MAX4254ESD	-40°C to +85°C	14 SO	—
MAX4255EUK-T	-40°C to +85°C	5 SOT23-5	ACCJ
MAX4256ESA	-40°C to +85°C	8 SO	—
MAX4256EUA	-40°C to +85°C	8 µMAX	—
MAX4257ESA	-40°C to +85°C	8 SO	—
MAX4257EUA	-40°C to +85°C	8 µMAX	—

Pin Configurations (continued)

TOP VIEW



µMAX



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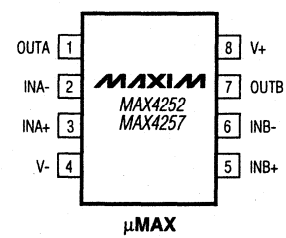
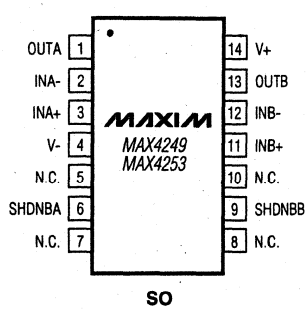


µMAX



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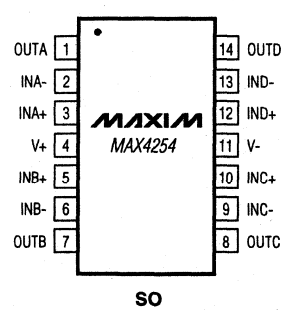


SO

N.C. = NOT INTERNALLY CONNECTED

19-1192; Rev 2; 8/97

MAXIM

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

General Description

The MAX4330–MAX4334 single/dual/quad op amps combine a wide 3MHz bandwidth, low-power operation, and excellent DC accuracy with Rail-to-Rail® inputs and outputs. These devices require only 245µA per amplifier, and operate from either a single +2.3V to +6.5V supply or dual ±1.15V to ±3.25V supplies. The input common-mode voltage range extends 250mV beyond V_{EE} and V_{CC}, and the outputs swing rail-to-rail. The MAX4331/MAX4333 feature a shutdown mode in which the output goes high impedance and the supply current decreases to 9µA per amplifier.

Low-power operation combined with rail-to-rail input common-mode range and output swing makes these amplifiers ideal for portable/battery-powered equipment and other low-voltage, single-supply applications. Although the minimum operating voltage is specified at 2.3V, these devices typically operate down to 2.0V. Low offset voltage and high speed make these amplifiers excellent choices for signal-conditioning stages in precision, low-voltage data-acquisition systems. The MAX4330 is available in the space-saving 5-pin SOT23 package, and the MAX4331/MAX4333 are offered in a µMAX package.

Applications

Portable/Battery-Powered Equipment

Data-Acquisition Systems

Signal Conditioning

Low-Power, Low-Voltage Applications

Selector Guide

PART	No. OF AMPS PER PACKAGE	SHUTDOWN MODE	PIN-PACKAGE
MAX4330	1	—	5 SOT23
MAX4331	1	Yes	8 SO/µMAX
MAX4332	2	—	8 SO
MAX4333	2	Yes	10 µMAX, 14 SO
MAX4334	4	—	14 SO

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

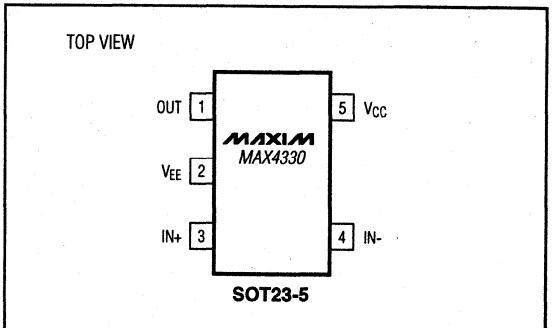
Features

- ♦ **3MHz Gain-Bandwidth Product**
- ♦ **245µA Quiescent Current per Amplifier**
- ♦ **Available in Space-Saving SOT23-5 Package (MAX4330)**
- ♦ **+2.3V to +6.5V Single-Supply Operation**
- ♦ **Rail-to-Rail Input Common-Mode Voltage Range**
- ♦ **Rail-to-Rail Output Voltage Swing**
- ♦ **250µV Offset Voltage**
- ♦ **Low-Power, 9µA (per amp) Shutdown Mode (MAX4331/MAX4333)**
- ♦ **No Phase Reversal for Overdriven Inputs**
- ♦ **Capable of Driving 2kΩ Loads**
- ♦ **Unity-Gain Stable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4330EUK	-40°C to +85°C	5 SOT23-5	ABAJ
MAX4331ESA	-40°C to +85°C	8 SO	—
MAX4331EUA	-40°C to +85°C	8 µMAX	—
MAX4332ESA	-40°C to +85°C	8 SO	—
MAX4333ESD	-40°C to +85°C	14 SO	—
MAX4333EUB	-40°C to +85°C	10 µMAX	—
MAX4334ESD	-40°C to +85°C	14 SO	—

Pin Configurations



Pin Configurations continued at end of data sheet.

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Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} to V_{EE} 7V
IN_+, IN_-, $\overline{SHDN}$ Voltage..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration..... Continuous
(short to either supply)
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C)..... 571mW
8-Pin SO (derate 5.88mW/°C above +70°C)..... 471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C)..... 330mW
10-Pin µMAX (derate 5.60mW/°C above +70°C)..... 444mW
14-Pin SO (derate 8.33mW/°C above +70°C)..... 667mW
Operating Temperature Ranges
MAX433_C/D ..... 0°C to +70°C
MAX433_E_ _..... -40°C to +85°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V\overline{SHDN} \geq$ 2V, **T_A = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}		MAX433_EUA/EUB		±0.65	±1.5	mV
				MAX4330EUK		±0.65	±1.5	
				MAX4331ESA		±0.25	±0.6	
				MAX4332ESA/MAX4333ESD		±0.25	±0.9	
				MAX4334ESD		±0.25	±1.0	
Input Bias Current	I_B					±25	±65	nA
Input Offset Current	I_{OS}					±1	±12	nA
Differential Input Resistance	$R_{IN(DIFF)}$	$\lvert V_{IN+} - V_{IN-} \rvert$ < 1.4V				2.3		MΩ
		$\lvert V_{IN+} - V_{IN-} \rvert$ > 2.5V				2		kΩ
Common-Mode Input Voltage Range	V_{CM}				-0.25		V_{CC} + 0.25	V
Common-Mode Rejection Ratio	CMRR	-0.25V < V_{CM} < (V_{CC} + 0.25V)	V_{CC} = 5V	MAX433_EUA/EUB	68	88		dB
				MAX4330EUK	67	87		
				MAX4331ESA	74	93		
				MAX4332ESA/ MAX4333ESD	71	93		
				MAX4334ESD	69	92		
			V_{CC} = 2.3V	MAX433_EUA/EUB	65	84		dB
				MAX4330EUK	64	82		
				MAX4331ESA	71	90		
				MAX4332ESA/ MAX4333ESD	69	90		
				MAX4334ESD	66	89		
Power-Supply Rejection Ratio	PSSR	V_{CC} = 2.3V to 6.5V		MAX433_EUA/EUB	76	88		dB
				MAX4330EUK	76	88		
				MAX4331ESA	79	92		
				MAX4332ESA/ MAX4333ESD	77	90		
				MAX4334ESD	75	90		
Output Resistance	R_{OUT}	A_V = 1				0.1		Ω
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V\overline{SHDN}$ < 0.8V, V_{OUT} = 0V to V_{CC}				±0.1	±2	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 2.3V	V_{OUT} = 0.2V to 2.1V, R_L = 100kΩ		93	112		dB
			V_{OUT} = 0.35V to 1.95V, R_L = 2kΩ		78	90		
		V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ		93	120		
			V_{OUT} = 0.35V to 4.65V, R_L = 2kΩ		83	95		
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{CC} - V_{OH}			8	30	mV
			V_{OL}			8	30	
		R_L = 2kΩ	V_{CC} - V_{OH}			100	175	
			V_{OL}			70	150	
Output Short-Circuit Current	I_{SC}					20		mA
$\overline{SHDN}$ Logic Threshold (Note 1)	V_{IL}	Low (shutdown mode)					0.8	V
	V_{IH}	High (normal mode)			2.0			
$\overline{SHDN}$ Input Current		$V_{EE} < V_{\overline{SHDN}} < V_{CC}$					±2	µA
Operating Supply-Voltage Range	V_{CC}				2.3		6.5	V
Quiescent Supply Current per Amplifier	I_{CC}	$V_{CM} = V_{OUT} = V_{CC} / 2$		V_{CC} = 5V		275	325	µA
				V_{CC} = 2.3V		245	290	
Shutdown Supply Current per Amplifier	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}} < 0.8V$		V_{CC} = 5V		17	25	µA
				V_{CC} = 2.3V		9	14	

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = V_{EE} to V_{CC}	MAX433_EUA			±3.2	mV
			MAX433_EUK/EUB			±3.8	
			MAX4331ESA			±0.7	
			MAX4332ESA/MAX4333ESD			±1	
			MAX4334ESD			±1	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$				±3		µV/°C
Input Bias Current	I_B					±115	nA
Input Offset Current	I_{OS}					±15	nA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.3V to 6.5V	MAX433_EUA	72			dB
			MAX433_EUK/EUB	71			
			MAX4331ESA	76			
			MAX4332ESA/ MAX4333ESD	73			
			MAX4334ESD	71			
Common-Mode Input Voltage Range	V_{CM}			-0.15		V_{CC} + 0.15	V

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.3V to +6.5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L tied to (V_{CC} / 2), $V_{\overline{SHDN}} \geq 2V$, **$T_A$ = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	-0.25V < V_{CM} < (V_{CC} + 0.25V)	V_{CC} = 5V	MAX433_EUA/EUB	63			dB
				MAX4330EUK	62			
				MAX4331ESA	72			
				MAX4332ESA/ MAX4333ESD	69			
				MAX4334ESD	67			
			V_{CC} = 2.3V	MAX433_EUA/EUB	58			
				MAX4330EUK	57			
				MAX4331ESA	68			
				MAX4332ESA/ MAX4333ESD	66			
				MAX4334ESD	65			
Off-Leakage Current in Shutdown	$I_{OUT(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V, V_{OUT} = 0V to V_{CC}					±5	µA
Large-Signal Voltage Gain	A_{VOL}	V_{CC} = 2.3V	V_{OUT} = 0.2V to 2.1V, R_L = 100kΩ		90			dB
			V_{OUT} = 0.35V to 1.95V, R_L = 2kΩ		70			
		V_{CC} = 5V	V_{OUT} = 0.2V to 4.8V, R_L = 100kΩ		90			
			V_{OUT} = 0.35V to 4.65V, R_L = 2kΩ		74			
Output Voltage Swing	V_{OUT}	R_L = 100kΩ	V_{CC} - V_{OH}				40	mV
			V_{OL}				40	
		R_L = 2kΩ	V_{CC} - V_{OH}				200	
			V_{OL}				180	
$\overline{SHDN}$ Logic Threshold (Note 1)	V_{IL}	Low (shutdown mode)					0.8	V
	V_{IH}	High (normal mode)			2.0			
$\overline{SHDN}$ Input Current		V_{EE} < $V_{\overline{SHDN}}$ < V_{CC}					±2	µA
Operating Supply-Voltage Range	V_{CC}	T_A = -40°C to +85°C			2.3		6.5	V
Quiescent Supply Current per Amplifier	I_{CC}	V_{CM} = V_{OUT} = V_{CC} / 2		V_{CC} = 5V			350	µA
				V_{CC} = 2.3V			330	
Shutdown Supply Current per Amplifier	$I_{CC(\overline{SHDN})}$	$V_{\overline{SHDN}}$ < 0.8V		V_{CC} = 5V			30	µA
				V_{CC} = 2.3V			17	

Note 1: $\overline{SHDN}$ logic thresholds are referenced to V_{EE}.
Note 2: The MAX4330EUK is 100% tested at T_A = +25°C. All temperature limits are guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

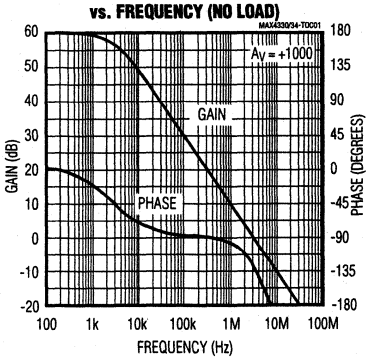
(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = 0V, V_{OUT} = (V_{CC} / 2), R_L = 10kΩ to (V_{CC} / 2), $V_{\overline{SHDN}} \geq$ 2V, C_L = 15pF, **T_A = +25°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBWP			3		MHz
Full-Power Bandwidth	FPBW	V_{OUT} = 4Vp-p		190		kHz
Slew Rate	SR			1.5		V/µs
Phase Margin	PM			55		degrees
Gain Margin	GM			10		dB
Total Harmonic Distortion	THD	f = 10kHz, V_{OUT} = 2Vp-p, A_{VCL} = +1V/V		0.012		%
Settling Time to 0.01%	t_S	A_V = +1V/V, 2V step		4		µs
Input Capacitance	C_{IN}			3		pF
Input Noise Voltage Density	V_{NOISE}	f = 10kHz		28		nV/√Hz
Input Current Noise Density	I_{NOISE}	f = 10kHz		0.26		pA/√Hz
Crosstalk		f = 10kHz, MAX4332/MAX4333/MAX4334		-124		dB
Capacitive Load Stability		A_V = 1, no sustained oscillations		150		pF
Shutdown Time	$t_{\overline{SHDN}}$			0.8		µs
Enable Time from Shutdown	t_{ENABLE}			1		µs
Power-Up Time	t_{ON}			5		µs

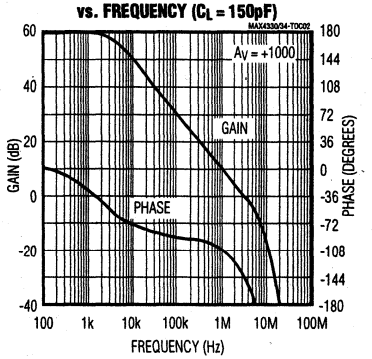
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

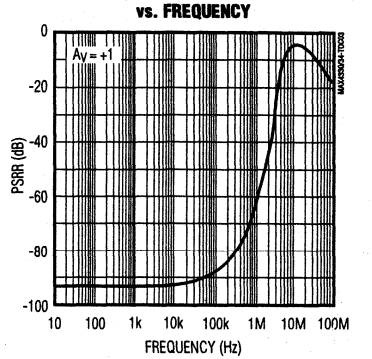
GAIN AND PHASE vs. FREQUENCY (NO LOAD)



GAIN AND PHASE vs. FREQUENCY (C_L = 150pF)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY

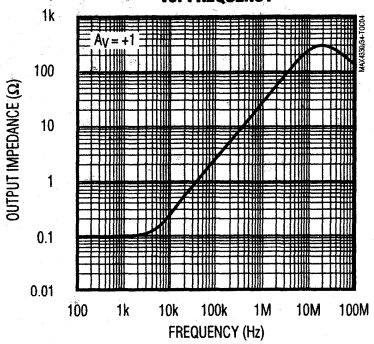


Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

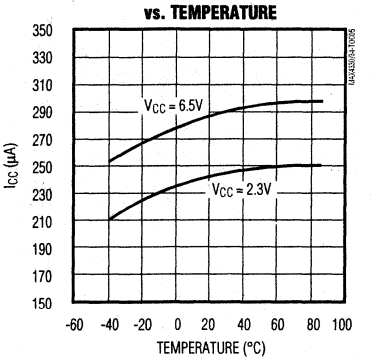
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

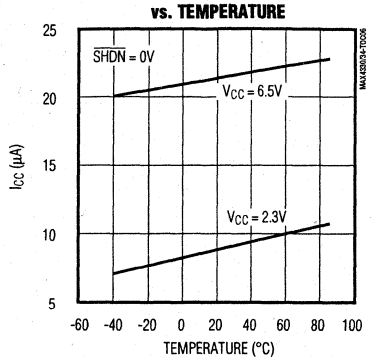
OUTPUT IMPEDANCE vs. FREQUENCY



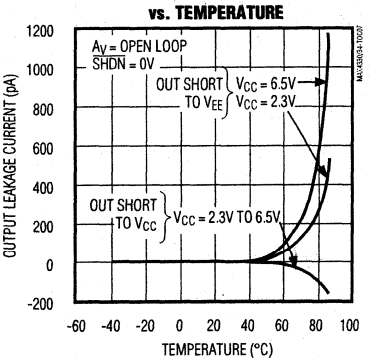
SUPPLY CURRENT vs. TEMPERATURE



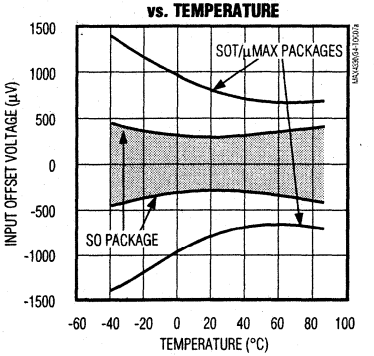
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



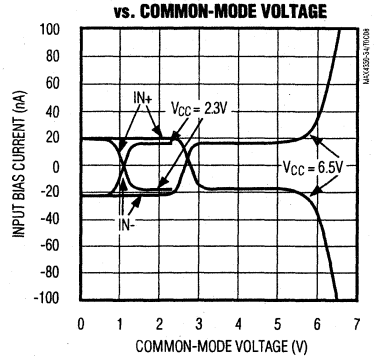
OUTPUT LEAKAGE CURRENT vs. TEMPERATURE



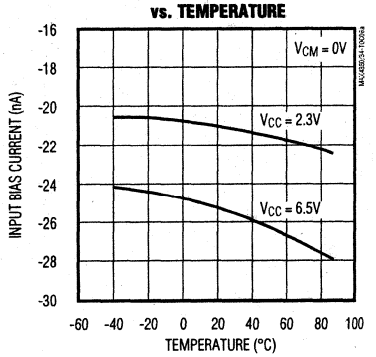
INPUT OFFSET VOLTAGE vs. TEMPERATURE



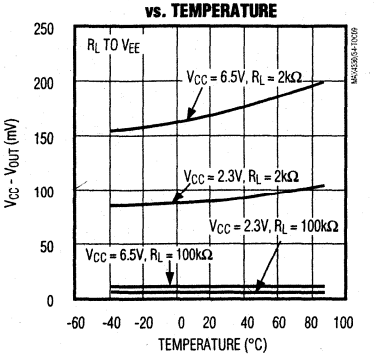
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



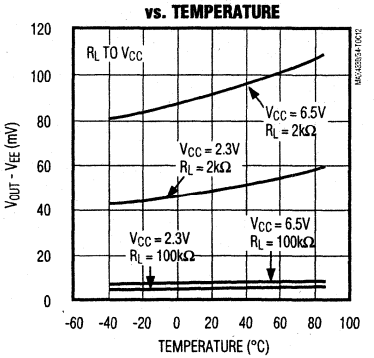
INPUT BIAS CURRENT vs. TEMPERATURE



OUTPUT SWING HIGH vs. TEMPERATURE



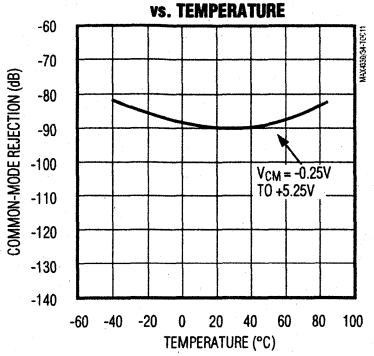
OUTPUT SWING LOW vs. TEMPERATURE



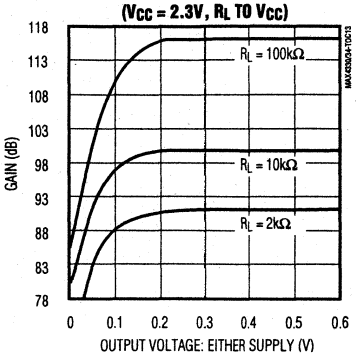
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

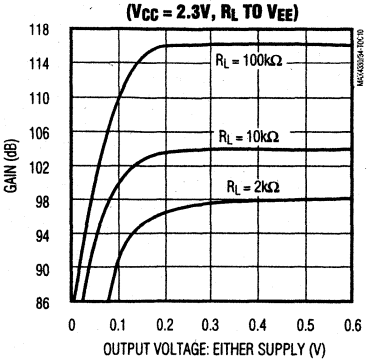
COMMON-MODE REJECTION vs. TEMPERATURE



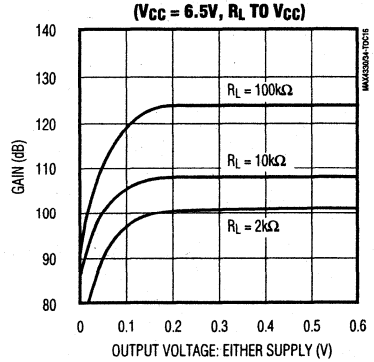
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 2.3V, R_L TO V_{CC})



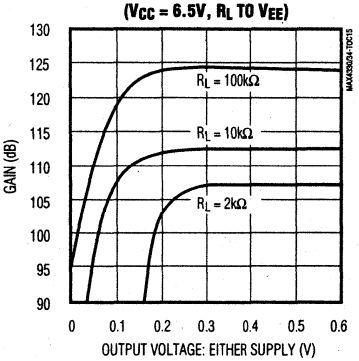
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 2.3V, R_L TO V_{EE})



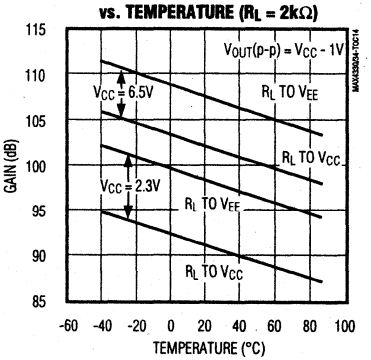
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 6.5V, R_L TO V_{CC})



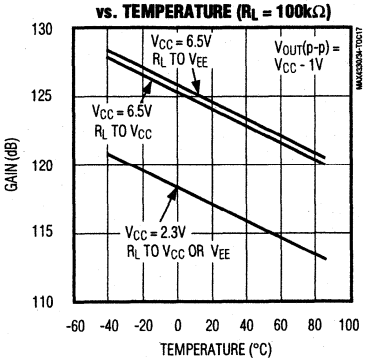
LARGE-SIGNAL GAIN vs. OUTPUT VOLTAGE (V_{CC} = 6.5V, R_L TO V_{EE})



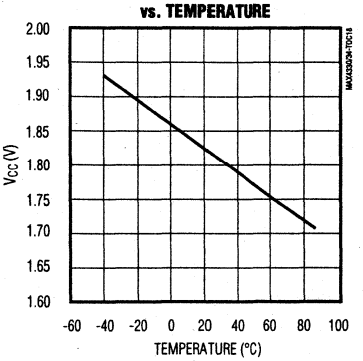
LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 2kΩ)



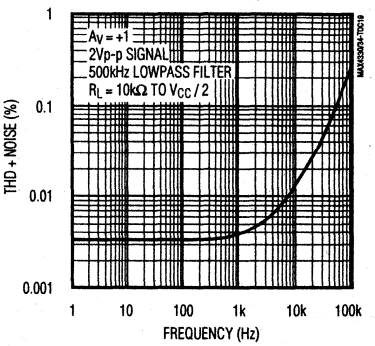
LARGE-SIGNAL GAIN vs. TEMPERATURE (R_L = 100kΩ)



MINIMUM OPERATING VOLTAGE vs. TEMPERATURE



TOTAL HARMONIC DISTORTION AND NOISE vs. FREQUENCY

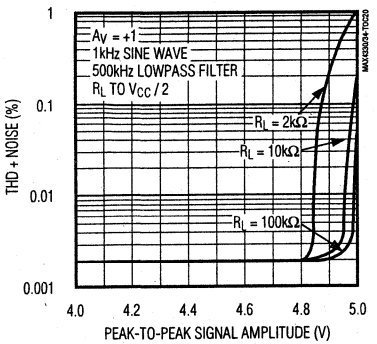


Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

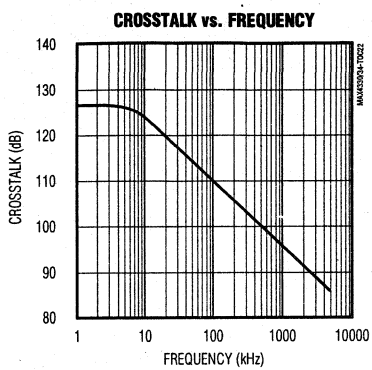
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = V_{CC} / 2, $V_{\overline{SHDN}}$ > 2V, T_A = +25°C, unless otherwise noted.)

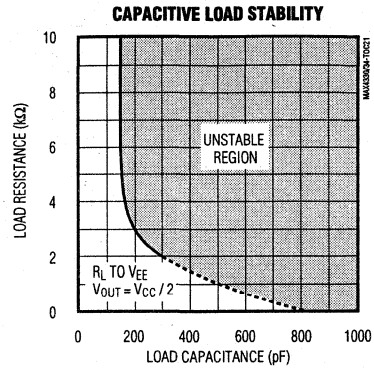
TOTAL HARMONIC DISTORTION AND NOISE vs. PEAK-TO-PEAK SIGNAL AMPLITUDE



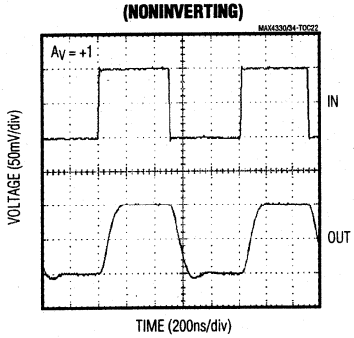
CROSSTALK vs. FREQUENCY



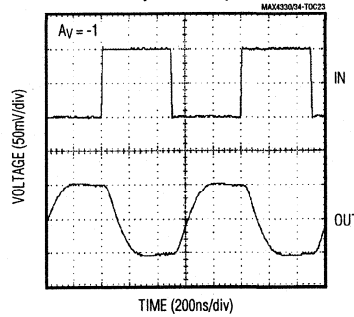
CAPACITIVE LOAD STABILITY



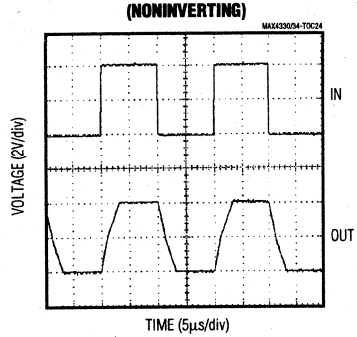
SMALL-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



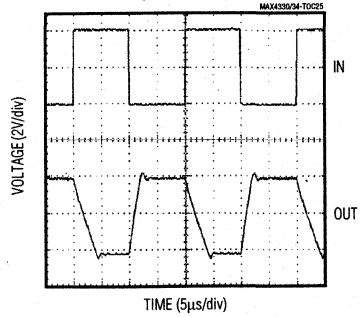
SMALL-SIGNAL TRANSIENT RESPONSE (INVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (NONINVERTING)



LARGE-SIGNAL TRANSIENT RESPONSE (INVERTING)



Pin Description

PIN						NAME	FUNCTION
MAX4330	MAX4331	MAX4332	MAX4333		MAX4334		
			10-Pin µMAX	14-Pin SO			
1	6	—	—	—	—	OUT	Output
2	4	4	4	4	11	V_{EE}	Negative Supply. Ground for single-supply operation.
3	3	—	—	—	—	IN+	Noninverting Input
4	2	—	—	—	—	IN-	Inverting Input
5	7	8	10	14	4	V_{CC}	Positive Supply
—	1, 5	—	—	5, 7, 8, 10	—	N.C.	No Connection. Not internally connected.
—	—	1, 7	1, 9	1, 13	1, 7	OUT1, OUT2	Outputs for Amplifiers 1 and 2
—	—	3, 5	3, 7	3, 11	3, 5	IN1+, IN2+	Noninverting Inputs to Amplifiers 1 and 2
—	—	2, 6	2, 8	2, 12	2, 6	IN1-, IN2-	Inverting Inputs to Amplifiers 1 and 2
—	8	—	—	—	—	$\overline{SHDN}$	Shutdown Input for Amplifier. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
--	—	—	5, 6	6, 9	—	$\overline{SHDN1}$, $\overline{SHDN2}$	Shutdown for Amplifiers 1 and 2. Drive low for shutdown mode. Drive high or connect to V_{CC} for normal operation.
—	—	—	—	—	8, 14	OUT3, OUT4	Outputs for Amplifiers 3 and 4
—	—	—	—	—	9, 13	IN3-, IN4-	Inverting Inputs for Amplifiers 3 and 4
—	—	—	—	—	10, 12	IN3+, IN4+	Noninverting Inputs for Amplifiers 3 and 4

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Detailed Description

Rail-to-Rail Input Stage

The MAX4330–MAX4334 have rail-to-rail input and output stages that are specifically designed for low-voltage, single-supply operation. The input stage consists of separate NPN and PNP differential stages, which operate together to provide a common-mode range extending to 0.25V beyond both supply rails. The crossover region, which occurs halfway between V_{CC} and V_{EE}, is extended to minimize degradation in CMRR caused by mismatched input pairs. The input offset voltage is typically 250µV. Low offset voltage, high bandwidth, rail-to-rail common-mode input range, and rail-to-rail outputs make this family of op amps an excellent choice for precision, low-voltage data-acquisition systems.

Since the input stage consists of NPN and PNP pairs, the input bias current changes polarity as the input voltage passes through the crossover region. Match the effective impedance seen by each input to reduce the offset error due to input bias currents flowing through external source impedances (Figures 1a and 1b). The combination of high source impedance with input capacitance (amplifier input capacitance plus stray capacitance) creates a parasitic pole that produces an underdamped signal response. Reducing input capacitance or placing a small capacitor across the feedback resistor improves response.

The MAX4330–MAX4334's inputs are protected from large differential input voltages by internal 1kΩ series resistors and back-to-back triple diode stacks across the inputs (Figure 2). For differential input voltages (much less than 1.8V), input resistance is typically 2.3MΩ. For differential input voltages greater than 1.8V, input resistance is around 2kΩ, and the input bias current can be approximated by the following equation:

$$I_{BIAS} = (V_{DIFF} - 1.8V) / 2k\Omega$$

In the region where the differential input voltage approaches 1.8V, input resistance decreases exponentially from 2.3MΩ to 2kΩ as the diode block begins conducting. Inversely, the bias current increases with the same curve.

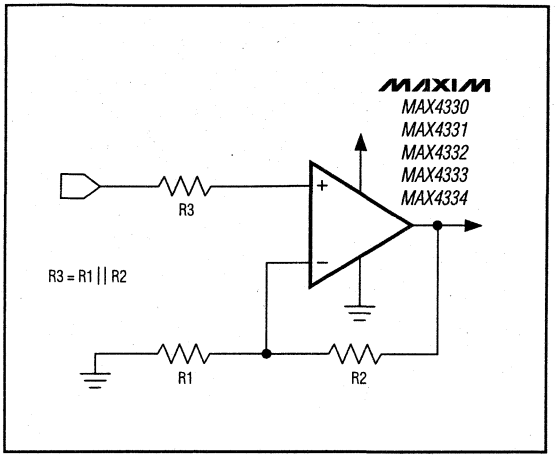


Figure 1a. Reducing Offset Error Due to Bias Current (Noninverting)

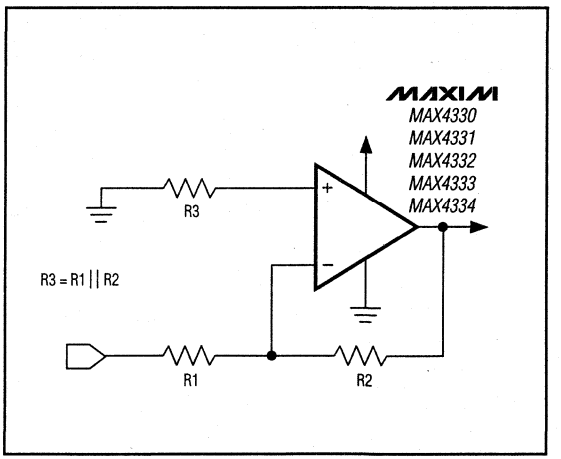


Figure 1b. Reducing Offset Error Due to Bias Current (Inverting)

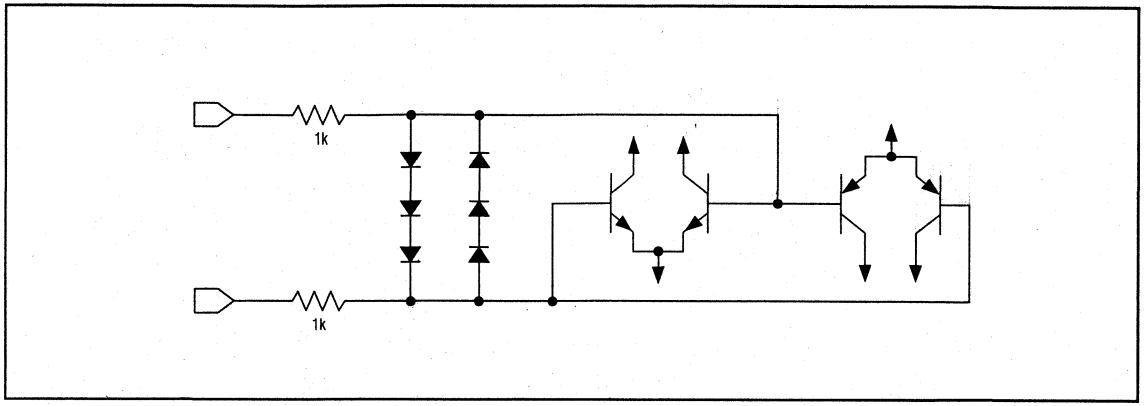


Figure 2. Input Protection Circuit

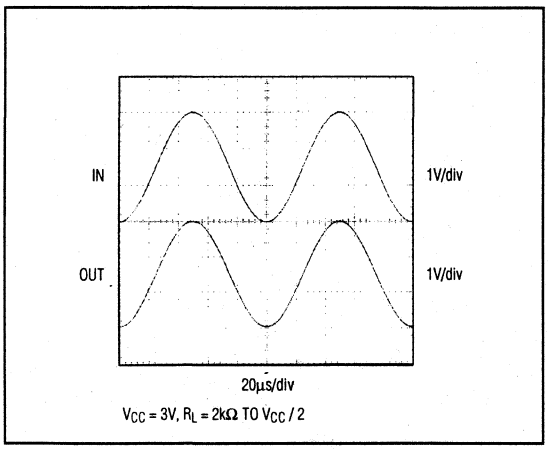


Figure 3. Rail-to-Rail Input/Output Voltage Range

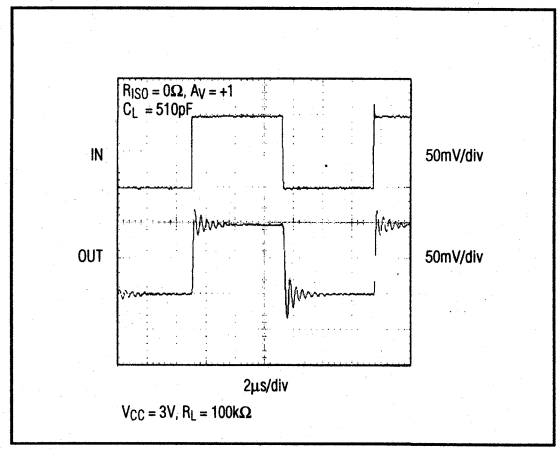


Figure 4. Small-Signal Transient Response with Excessive Capacitive Load

Rail-to-Rail Output Stage

The MAX4330–MAX4334 output stage can drive up to a 2kΩ load and still typically swing within 125mV of the rails. Figure 3 shows the output voltage swing of a MAX4331 configured as a unity-gain buffer. The operating voltage is a single +3V supply, and the input voltage is 3Vp-p. The output swings to within 70mV of V_{EE} and 100mV of V_{CC}, even with the maximum load applied (2kΩ to mid-supply).

Driving a capacitive load can cause instability in many op amps, especially those with low quiescent current. The MAX4330–MAX4334 are stable for capacitive loads up to 150pF. The Capacitive Load Stability graph in the *Typical Operating Characteristics* gives the stable operating region for capacitive vs. resistive loads. Figures 4 and 5 show the response of the MAX4331 with an excessive capacitive load, compared with the response when a series resistor is added between the output and the capacitive load. The resistor improves the circuit's response by isolating the load capacitance from the op amp's output (Figure 6).

Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

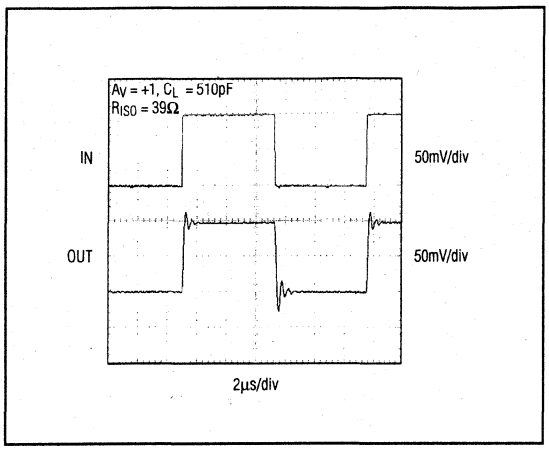


Figure 5. Small-Signal Transient Response with Excessive Capacitive Load and Isolation Resistor

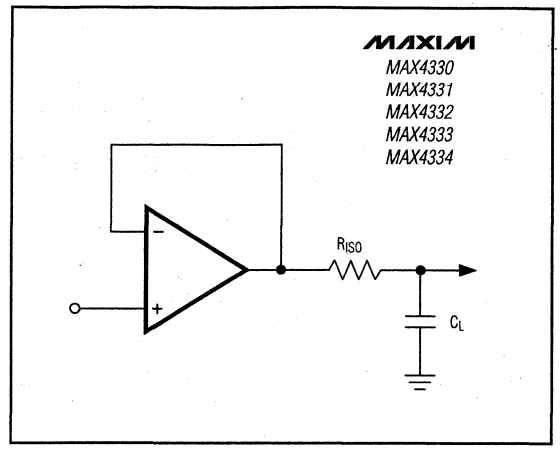


Figure 6. Capacitive-Load-Driving Circuit

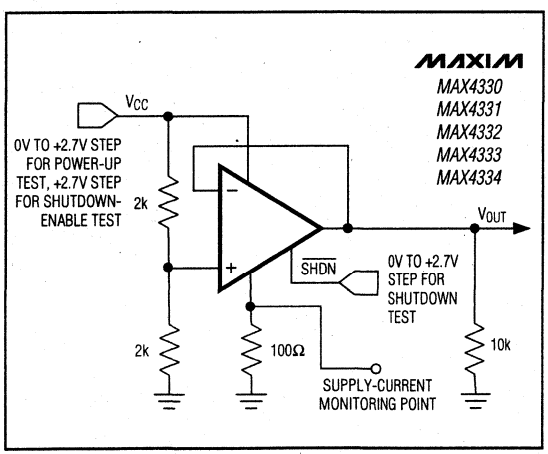


Figure 7. Power-Up/Shutdown Test Circuit

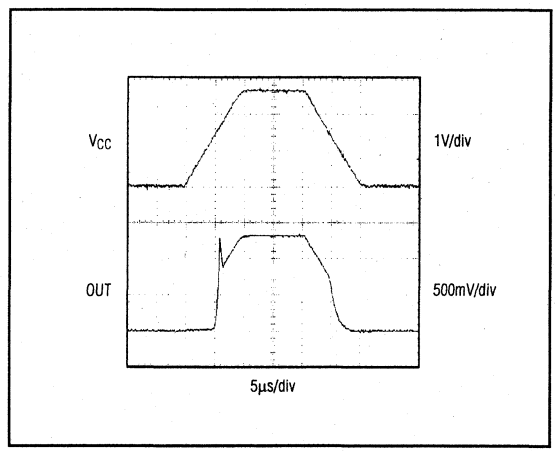


Figure 8. Power-Up/Down Output Voltage

Applications Information

Power-Up

The MAX4330–MAX4334 outputs typically settle within 5µs after power-up. Using the test circuit of Figure 7, Figures 8 and 9 show the output voltage and supply current on power-up and power-down.

Shutdown Mode

The MAX4331/MAX4333 feature a low-power shutdown mode. When the shutdown pin ($\overline{SHDN}$) is pulled low, the supply current drops to 9µA per amplifier (typical), the amplifier is disabled, and the outputs enter a high-impedance state. Pulling $\overline{SHDN}$ high or leaving it floating enables the amplifier. Figures 10 and 11 show the MAX4331/MAX4333's output voltage and supply-current responses to a shutdown pulse.

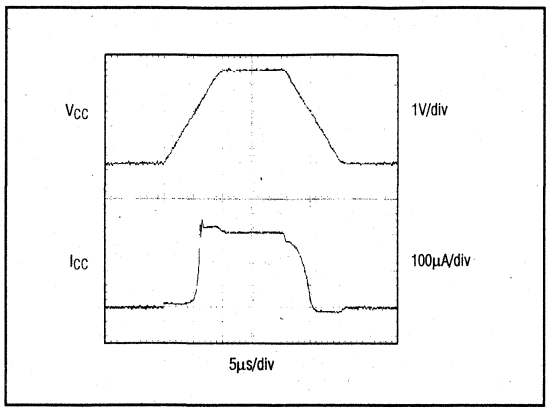


Figure 9. Power-Up/Down Supply Current

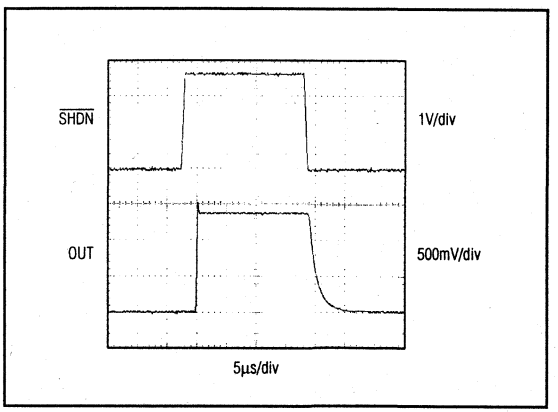


Figure 10. Shutdown Output Voltage Enable/Disable

Do not three-state $\overline{SHDN}$. Due to the output leakage currents of three-state devices and the small internal pull-up current for $\overline{SHDN}$, three-stating this pin could result in indeterminate logic levels, and could adversely affect op-amp operation.

The logic threshold for $\overline{SHDN}$ is always referred to V_{EE}, **not** GND. When using dual supplies, pull $\overline{SHDN}$ to V_{EE} to place the op amp in shutdown mode.

Power Supplies and Layout

The MAX4330–MAX4334 operate from a single +2.3V to +6.5V power supply, or from dual ±1.15V to ±3.25V supplies. For single-supply operation, bypass the power supply with a 0.1µF capacitor to ground (V_{EE}). For dual supplies, bypass both V_{CC} and V_{EE} with their own set of capacitors to ground.

Good layout technique helps optimize performance by decreasing the amount of stray capacitance at the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the op amp's pins.

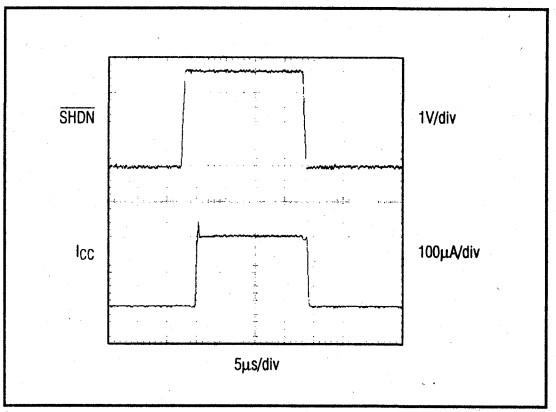
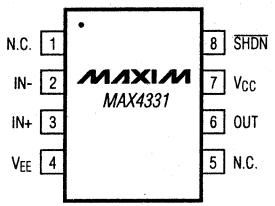


Figure 11. Shutdown Enable/Disable Supply Current

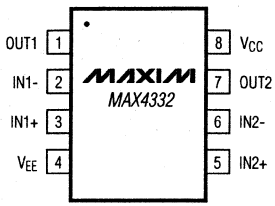
Single/Dual/Quad, Low-Power, Single-Supply, Rail-to-Rail I/O Op Amps with Shutdown

Pin Configurations (continued)

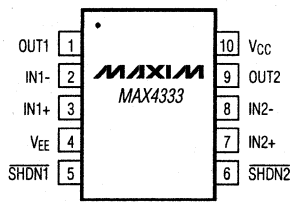
TOP VIEW



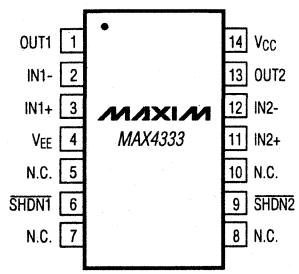
SO/μMAX



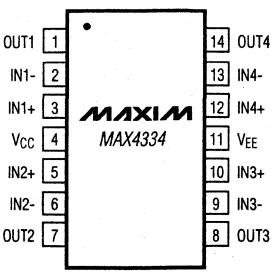
SO



μMAX



SO



SO

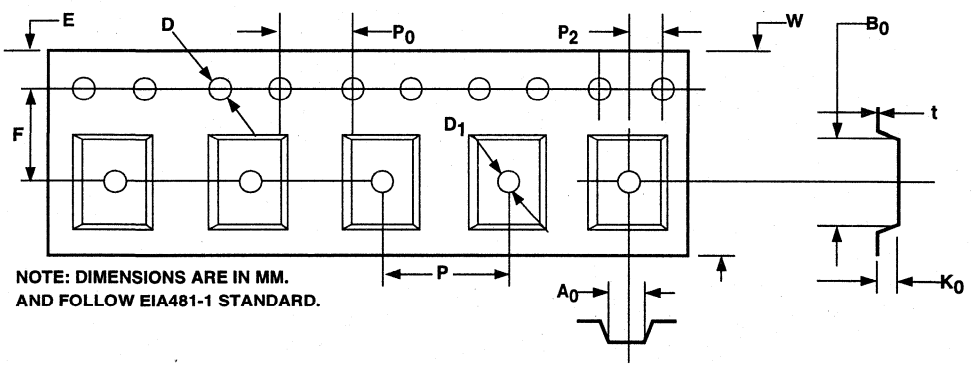
Chip Information

MAX4330/MAX4331
TRANSISTOR COUNT: 199
SUBSTRATE CONNECTED TO V_{EE}

MAX4332/MAX4333
TRANSISTOR COUNT: 398
SUBSTRATE CONNECTED TO V_{EE}

MAX4334
TRANSISTOR COUNT:
SUBSTRATE CONNECTED TO V_{EE}

Tape-and-Reel Information



NOTE: DIMENSIONS ARE IN MM.
AND FOLLOW EIA481-1 STANDARD.

A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

MAXIM

Low-Power, High-Speed, Single-Supply Op Amp + Comparator + Reference ICs

General Description

The MAX9000 family features combinations of micropower, high-speed operational amplifiers, a comparator, and an internal 1.233V reference. These devices operate from a +2.5V to +5.5V single supply. The MAX9000/MAX9001/MAX9003/MAX9004 typically draw 450µA of quiescent current, while the MAX9002/MAX9005 typically consume 375µA. The MAX9001/MAX9004 feature a low-power shutdown mode that reduces supply current to 2µA, making them ideal for portable/battery-powered applications.

The amplifiers in the MAX9000/MAX9001/MAX9002 are internally compensated to be unity-gain stable with a 1.25MHz gain-bandwidth product, while the amplifiers in the MAX9003/MAX9004/MAX9005 are stable for closed-loop gains of +10V/V or greater with an 8MHz gain-bandwidth product. Besides excellent DC accuracy, these amplifiers and comparators can swing Rail-to-Rail® and deliver 2.5mA and 4.0mA, respectively. The input common-mode range (CMR) extends from 150mV below the negative rail to within 1.2V of the positive rail for the amplifier, and to within 1.1V for the comparator.

The comparator's ±2mV of built-in hysteresis provides noise immunity, which allows glitch-free switching for slow-moving input signals. The MAX9000/MAX9001/MAX9003/MAX9004 have an internal, 1.233V ±1% precision reference with a low, 10ppm/°C temperature coefficient, and can sink or source an external load of up to 1mA.

Applications

Single-Supply Zero-Crossing Detector

Instruments, Terminals, and Bar-Code Readers

Automotive Keyless Entry

Local Area Alarms/Detectors

Photodiode Preamps

Smart Cards

Infrared Receivers for Remote Controls

Safety Sensors

GPS Receivers

Cellular Phones

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd

Features

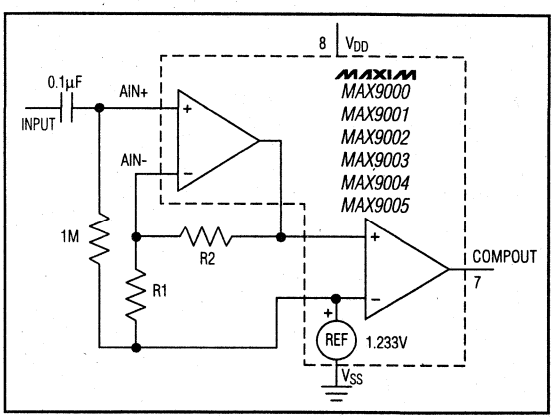
- **Op Amp + Comparator + Reference Available in Space-Saving, 8-Pin µMAX Package**
- **+2.5V to +5.5V Single-Supply Operation**
- **375µA Quiescent Supply Current (MAX9002/MAX9005)**
- **1.25MHz and 8MHz Gain-Bandwidth Options**
- **2µA Shutdown Current (MAX9001/MAX9004)**
- **Outputs Swing Rail-to-Rail**
- **Fast, 100ns Propagation-Delay Comparator**
- **Input CMR Includes Ground**
- **No Phase Reversal for Overdriven Inputs**
- **Internal Precision Reference:**
  - **±1% Initial Accuracy**
  - **Low, 10ppm/°C Temperature Drift**
  - **Sink or Source up to 1mA**
  - **Stable for Capacitive Loads up to 100nF**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX9000ESA	-40°C to +85°C	8 SO
MAX9000EUA	-40°C to +85°C	8 µMAX
MAX9001ESD	-40°C to +85°C	14 SO
MAX9001EUB	-40°C to +85°C	10 µMAX

Ordering Information continued on next page

Typical Operating Circuit



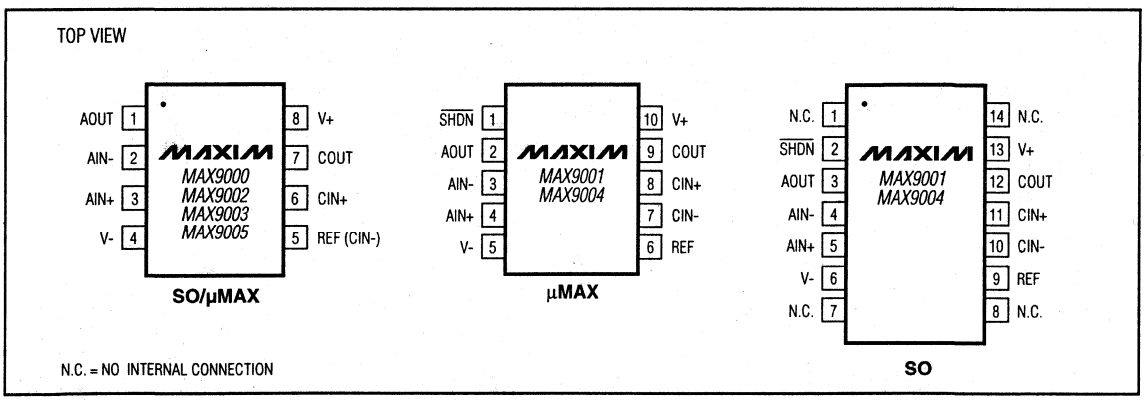
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Power, High-Speed, Single-Supply Op Amp + Comparator + Reference ICs

Selector Guide

PART	INTERNAL ±1% PRECISION REFERENCE	OP-AMP GAIN STABILITY (V/V)	SHUTDOWN	OP-AMP GAIN BANDWIDTH (MHz)	PIN-PACKAGE
MAX9000	Yes	1	No	1.25	8-pin SO/µMAX
MAX9001	Yes	1	Yes	1.25	14-pin SO, 10-pin µMAX
MAX9002	No	1	No	1.25	8-pin SO/µMAX
MAX9003	Yes	10	No	8	8-pin SO/µMAX
MAX9004	Yes	10	Yes	8	14-pin SO, 10-pin µMAX
MAX9005	No	10	No	8	8-pin SO/µMAX

Pin Configurations



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX9002ESA	-40°C to +85°C	8 SO
MAX9002EUA	-40°C to +85°C	8 µMAX
MAX9003ESA	-40°C to +85°C	8 SO
MAX9003EUA	-40°C to +85°C	8 µMAX
MAX9004ESD	-40°C to +85°C	14 SO
MAX9004EUB	-40°C to +85°C	10 µMAX
MAX9005ESA	-40°C to +85°C	8 SO
MAX9005EUA	-40°C to +85°C	8 µMAX

Power-Supply Circuits

Power-Supply Circuits, Product Tables and Trees 4-3

MAX629	28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter	4-13
MAX679	Regulated 3.3V Charge Pump	4-23
MAX682	3.3V to Regulated 5V Charge Pump with 50mA Output Current	4-29*
MAX683	3.3V to Regulated 5V Charge Pump with 100mA Output Current	4-29*
MAX684	3.3V to Regulated 5V Charge Pump with 200mA Output Current	4-29*
MAX685	Low-Noise, Dual-Output (Positive and Negative) DC-DC Converter for CCD and LCD	4-31*
MAX686	DAC-Controlled Boost or Inverter LCD Bias Supply with 28V Internal Switch	4-33*
MAX710	3.3V/5V, Step-Up/Down DC-DC Converter	4-35
MAX711	Adjustable, Step-Up/Down DC-DC Converter	4-35
MAX798	High-Accuracy Step-Down Controller with Synchronous Rectification for CPU Power	4-45
MAX847	1-Cell, Step-Up, Two-Way Pager System IC	4-55*
MAX863	Dual, High-Efficiency, PFM, Step-Up DC-DC Controller	4-57*
MAX868	Regulated, 30mA-Output Charge-Pump DC-DC Inverter	4-73*
MAX869L	2A, Current-Limited, High-Side, P-Channel Switch with Thermal Shutdown	4-75*
MAX870	125kHz Switched-Capacitor Voltage Inverter	4-77
MAX871	500kHz Switched-Capacitor Voltage Inverter	4-77
MAX881R	Low-Noise Bias Supply for GaAsFET PA with Power-OK in µMAX	4-85*
MAX891L	Current-Limited, 0.12Ω, High-Side P-Channel Switch with Thermal Shutdown	4-87
MAX892L	Current-Limited, 0.25Ω, High-Side P-Channel Switch with Thermal Shutdown	4-87
MAX1615	High-Voltage, Low-Power Linear Regulator for Notebook Computers	4-95
MAX1620	Digitally Adjustable LCD Bias Supply	4-101
MAX1621	Digitally Adjustable LCD Bias Supply with SMBus Serial Interface	4-101
MAX1624	High-Speed Step-Down Controller with Synchronous Rectification for CPU Power	4-119
MAX1625	High-Speed Step-Down Controller with Synchronous Rectification for CPU Power	4-119
MAX1636	Low-Voltage, Precision, Step-Down Controller for Portable CPU Power	4-143
MAX1637	Low-Voltage, Precision, Step-Down Controller for Portable CPU Power in QSOP Package	4-165*
MAX1638	Digitally Programmable, High-Speed, Step-Down Controller with Synchronous Rectification for CPU Power	4-167*
MAX1639	High-Speed, Step-Down Controller with Synchronous Rectification for CPU Power	4-167*
MAX1640	Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier and High-Side Current Sensing	4-169
MAX1641	Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier and Low-Side Current Sensing	4-169
MAX1642	High-Efficiency, Step-Up DC-DC Converter with Logic-Controlled Shutdown for 1V Inputs	4-181
MAX1643	High-Efficiency, Step-Up DC-DC Converter for 1V Inputs	4-181
MAX1647	Chemistry-Independent Battery Charger	4-191
MAX1648	Chemistry-Independent Battery Charger	4-191
MAX1652	High-Efficiency, PWM, Step-Down DC-DC Controller in QSOP Package	4-215*

*Advance Information–first page of a data sheet in preparation.

Power-Supply Circuits (continued)

MAX1653 High-Efficiency, PWM, Step-Down DC-DC Controller with PWM Override Feature 4-215*
MAX1654 4.5V to 28V Input, High-Efficiency, PWM, Step-Down DC-DC Controller in QSOP Package....4-215*
MAX1655 High-Efficiency, PWM, Step-Down DC-DC Controller with Down to 1V Output Range in QSOP Package....4-215*
MAX1658 3.3V-Output, 16.5V-Input, 350mA, Low-Dropout Linear Regulator 4-217
MAX1659 5V-Output, 16.5V-Input, 350mA, Low-Dropout Linear Regulator 4-217
MAX1660 Digitally Controlled Fuel-Gauge Interface....4-227*
MAX1661 Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for N-Channel MOSFETs....4-229*
MAX1662 Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for P-Channel MOSFETs 4-229*
MAX1663 Serial-to-Parallel/Parallel-to-Serial Converter and Load-Switch Controller with SMBus Interface for P-Channel MOSFETs 4-229*
MAX1672 Step-Up/Down DC-DC Converter in QSOP Package 4-231*
MAX1673 Regulated, 125mA-Output, Charge-Pump DC-DC Inverter....4-233*
MAX1680 125mA, 125kHz/250kHz, Switched-Capacitor Voltage Converter....4-235
MAX1681 125mA, 500kHz/1MHz, Switched-Capacitor Voltage Converter 4-235
MAX1700 1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converter....4-245*
MAX1701 1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converter with Power-Good Output....4-245*
MAX1703 1-Cell to 3-Cell, High-Power (2A), Low-Noise, Step-Up DC-DC Converter....4-247*
MAX1705 1-Cell to 3-Cell, 1A, Low-Noise, Step-Up DC-DC Converter with Linear Regulator 4-249
MAX1706 1-Cell to 3-Cell, 0.5A, Low-Noise, Step-Up DC-DC Converter with Linear Regulator 4-249
MAX8867 Low-Noise, Low-Dropout, 150mA Linear Regulator with Auto-Discharge Function in SOT23 Package 4-267*
MAX8868 Low-Noise, Low-Dropout, 150mA Linear Regulator in SOT23 Package 4-267*
MAX8873T/S/R Low-Dropout, 120mA Linear Regulator with CP2980 Pinout 4-269
MAX8874T/S/R Low-Dropout, 120mA Linear Regulator with LP2980 Pinout and C_{OUT} Auto-Discharge Function 4-269
MAX8877 Low-Noise, Low-Dropout, 150mA Linear Regulator with '2982 Pinout 4-277*
MAX8878 Low-Noise, Low-Dropout, 150mA Linear Regulator with '2982 Pinout and Auto-Discharge Function 4-277*

*Advance Information–first page of a data sheet in preparation.

Power Management

Multi-Function Supplies

1-Cell Portables & 2-Way Pagers

† MAX847
(multi-function supply with boost charger, drivers & A/D)

★☆ MAX848/849
(1V start-up, step-up, with A/D battery monitoring, 200mA)

★☆ MAX1705/1706
(1V start-up, step-up & linear reg. dual output, 200mA)

2- or 3-Cell Portables & 2-Way Pagers

☆ MAX717
(3.3V & 12V flash prog.)

☆ MAX718
(3.3V or 5V & 12V flash prog.)

☆ MAX719
(3V or 5V & 12V flash prog.)

MAX720
(3.3V or 5V & 12V flash prog.)

MAX721
(3V or 5V & 12V flash prog.)

☆ MAX722
(3.3V or 5V_{OUT}, neg. LCD)

☆ MAX723
(3V or 5V_{OUT}, neg. LCD)

† MAX769
(multi-function step-up/down with charger, drivers, & A/D)

★☆ MAX848
(500mA, step-up, ADC)

★☆ MAX849
(800mA, step-up, ADC)

★☆ MAX863
(dual PFM boost controller in small package)

5- to 12-Cell Portables/ Notebooks

MAX781
(3.3V, battery charger, PCMCIA)

☆ MAX782
(3.3V, 5V, PCMCIA)

☆ MAX783
(3.3V, 5V, PCMCIA, optimized for 6-cell inputs)

☆ MAX786
(3.3V, 5V)

★☆ MAX1630–1635
(3.3V, 5V, 12V)

3V & 5V PCMCIA Card & Hosts

MAX613
(PCMCIA controller, dual V_{PP})

MAX614
(PCMCIA controller, single V_{PP})

MAX624
(dual output (5V & adj.), 1MHz switcher)

MAX780
(PCMCIA controller, 4 level translators, dual V_{PP}, power ready)

MAX1600/1603
(dual card-slot power network with internal switches)

MAX1601/1604
(dual card-slot power network with internal switches & SMBus serial interface)

MAX1602
(single card-slot power network with internal switches)

Power-Plane Switches/ CardBus Switches

★ MAX1614
(N-channel drive for MOSFETs)

† MAX1661/1662
(serial-to-parallel/parallel-to-serial converter and load switch controller)

Isolated Power

☆ MAX845
(750mW isolated transformer driver)

High-Side MOSFET Drivers

MAX620 (quad driver)

MAX622
(V_{OUT} = V_{IN} + 11V)

USB Current-Limited Power Switches

★ MAX869L
(70mΩ, 2A, 16-QSOP)

MAX890L
(90mΩ, 1A, 8-SO)

★ MAX891L/892L
(150mΩ, 0.5A/ 300mΩ, 0.25A, 8-µMAX)

MAX894L/895L
(dual 150mΩ, 0.5A/ dual 300mΩ, 0.25A, 8-SO)

Battery Chargers/ Fuel Gauges

MAX471/472
(current-sense amp, fuel gauge)
(see Op Amp table)

☆ MAX712
(NiCd/NiMH, zero voltage-slope detection)

☆ MAX713
(NiCd/NiMH, negative voltage-slope detection)

★☆ MAX745
(high-efficiency, 0.75%-accurate 4Amp Li+ charger)

☆ MAX846A
(cost-saving 1% linear charger for Li+, NiMH, NiCd)

★☆ MAX1640/1641
(PWM current source)

★☆ MAX1647
(SBS level 2 smart charger: Li+, NiMH, NiCd)

★☆ MAX1648
(precision switch-mode universal charger: Li+, NiMH, NiCd)

☆ MAX2003
(NiCd/NiMH, temp. slope detection)

☆ MAX2003A
(improved MAX2003, includes pulse trickle)

† MAX1660
(±1%-accurate fuel gauge)

Low-Side MOSFET Drivers

MAX626
(2A, 4Ω, dual inverting)

MAX627
(2A, 4Ω, dual noninverting)

MAX628
(2A, 4Ω, dual mixed)

MAX4420
(6A, 1.5Ω, single noninverting)

MAX4426
(1.5A, 4Ω, dual inverting)

MAX4427
(1.5A, 4Ω, dual noninverting)

MAX4428
(1.5A, 4Ω, dual mixed)

MAX4429
(6A, 1.5Ω, single inverting)

ICL7667
(1.5A, 4Ω, dual inverting)

TSC426
(1.5A, 6Ω, dual inverting)

TSC427
(1.5A, 6Ω, dual noninverting)

TSC428
(1.5A, 6Ω, dual mixed)

★ New product
† Future product
☆ Evaluation kit available

DC-DC Converters

Low-Dropout Linear Regulators

Positive

MAX603/604
(5V/3.3V or adj., 500mA, 1.8W 8-pin SO)

MAX663
(5V or adj., I_Q = 6µA)

MAX666
(5V or adj., I_Q = 6µA, low-battery detect)

MAX667
(5V or adj., I_Q = 20µA, 120mV dropout, 200mA, low-battery detect)

MAX687
(3.3V ±3%, 0.073V dropout at 500mA, 0.80V dropout at 4A)

☆ MAX688/689
(3.3V/3V ±3%, 0.073V dropout at 500mA, 0.80V dropout at 4A)

MAX882
(3.3V or adj., P-Ch, 200mA, low-battery detector, 1.5W 8-pin SO)

MAX883/884
(5V/3.3V or adj., P-Ch, 200mA, low-battery detector, 1.5W 8-pin SO, 1mA off mode)

★ MAX1615
(3.3V/5V at 30mA, SOT23-5 ±4% output accuracy)

† MAX1616
(adj. at 30mA, SOT23-5)

★ MAX1658/1659
(16.5V_{IN}, 350mA)

MAX8862
(dual, 250mA/100mA low-noise LDO)

→ cont.

Negative

MAX664
(-5V or adj., I_Q = 6µA)

ICL7664A (±1%V_{OUT})

ICL7664B
(±5% V_{OUT})

★ New product
† Future product
☆ Evaluation kit available

Switching Regulators

Step-Up

PWM

☆ MAX731 (2V_{IN} to 5V_{OUT})

☆ MAX732/733/752 (12V/5V/adj.)

☆ MAX734 (12V, flash prog.)

★☆ MAX848 (1-3 cells to 2.7V–5V, 800mA)

☆ MAX849 (1-3 cells to 2.7V–5V, 500mA)

†☆ MAX1700/1701 (1V start-up, 800mA output, battery monitors)

†☆ MAX1703 (1V start-up, 1.5A output)

★☆ MAX1705/1706 (1V start-up, 800mA output, includes 200mA LDO)

PFM

☆ MAX606/607 (5V or 12V or adj., 8-pin µMAX, for PCMCIA, 1MHz)

☆ MAX608 (5V or adj. controller, 2V_{IN}, 300kHz)

★☆ MAX629 (28V int. switch)

MAX630 (adj.)

MAX631/632/633 (5V/12V/15V or adj.)

MAX641/642/643 (5V/12V/15V or adj. controller)

†☆ MAX686 (28V int. switch w/DAC control)

☆ MAX756/757 (3.3V or 5V/adj., 1.8V_{IN}, 250mA)

☆ MAX761 (12V, 120mA, flash prog.)

☆ MAX762 (15V or adj.)

☆ MAX770/771/772 (5V/12V/15V or adj., controller)

MAX773
(5V, 12V, 15V, or adj., controller)

☆ MAX777L/778L/779L
(5V/3.3V or 3V/adj., 1V start-up)

☆ MAX856/857 (3.3V or 5V/adj., 1.8V_{IN}, 150mA)

☆ MAX858/859 (3.3V or 5V/adj., 1.8V_{IN}, 35mA)

★☆ MAX863 (dual high-efficiency controllers, 1.8V_{IN})

☆ MAX866/867 (3.3V or 5V/adj., 0.9V_{IN}, 90mA)

★☆ MAX1642/1643 (0.85V_{IN} start-up with synchronous rectifier)

† MAX1674/5/6 (low noise, 1-3 cell input, µMAX)

☆ MAX1771 (12V or adj. controller)

MAX4193 (adj.)

MAX8863/8864
(100mA low-noise LDO in SOT23)

MAX8865/8866
(dual, 100mA low-noise LDO in µMAX)

† MAX8867/8868
(30µV_{RMS}, low-noise MAX8863/4)

★ MAX8873/8874
(LP2980 2nd source)

† MAX8877/8878
(LP2982 2nd source)

ICL7663A
(adj., 40mA)

Inverting

PWM

MAX735/755
(-5V/adj., max ΔV = 11.7V)

☆ MAX736/737/739/759
(-12V/-15V/-5V/adj., max ΔV = 22V)

PFM

MAX634 (adj.)

MAX635/636/637
(-5V/-12V/-15V or adj.)

☆ MAX749 (digital adj.)

☆ MAX764/765/766
(-5V/-12V/-15V or adj.)

☆ MAX774/775/776
(-5V/-12V/-15V or adj. controller)

Step-Down

PWM

MAX724 (adj., 5A)

MAX726/727/728/729
(adj./5V/3.3V/3V, 2A)

☆ MAX730A (5V)

☆ MAX738A (5V)

☆ MAX744A (5V, optimized for cellular comm.)

☆ MAX748A (3.3V)

☆ MAX750A (adj.)

☆ MAX758A (adj.)

☆ MAX763A (3.3V)

☆ MAX767 (3.3V)

☆ MAX781
(3.3V, battery charger, PCMCIA)

☆ MAX782
(3.3V & 5V, PCMCIA)

☆ MAX783
(3.3V & 5V, PCMCIA for 6-cell inputs)

☆ MAX786 (3.3V & 5V)

MAX787/788/789
(5V/3.3V/3V, 5A)

☆ MAX796/797/799
(5V, 3.3V, 2.9V, or adj. controllers)

★☆ MAX798
(adj. to 1.6V)

☆ MAX830/831
(adj./5V, 1A, 16-pin SOIC)

☆ MAX832/833
(3.3V/3V, 1A, 16-pin SOIC)

☆ MAX887
(3.3V/adj, 500mA, synchronous rectifier)

★☆ MAX1624
(2.1V–3.5V, Pentium Pro™ VID, adjustable synchronous rectifier)

★☆ MAX1625
(1.1V–3.5V, adjustable synchronous rectifier)

★☆ MAX1630-1635
(3.3V, 5V, 12V)

★☆ MAX1636
(1.1V to 5.5V adj.)

†☆ MAX1637
(1.1V to 5.5V adj.)

†☆ MAX1638/1639
(1.3V to 3.5V, Pentium II™, VID, adjustable synchronous rectifier)

★☆ MAX1640/1641
(current-source)

†☆ MAX1652/3/4
(improved MAX797 family)

†☆ MAX1655
(1V output version of MAX1653)

PFM

☆ MAX638 (5V or adj.)

☆ MAX639/640/653 (5V/3.3V/3V or adj., >90% efficiency)

MAX1626/1627 (3.3V or 5V/adj., 100% duty cycle)

☆ MAX1649/1651 (5V/3.3V or adj. controller)

Step-Up/Down

★☆ MAX710/711
(250mA, step-up + linear)

☆ MAX761 (200mA, SEPIC)

†☆ MAX1672
(150mA, step-up + linear)

Dual-Output PWM

†☆ MAX685 (±output for CCD)

☆ MAX742 (±12V or ±15V controller)

☆ MAX743 (±12V or ±15V)

★☆ MAX1705/1706
(800mA boost and 200mA LDO)

Display

★☆ MAX629 (28V int. switch)

†☆ MAX686 (28V int. switch w/DAC control)

☆ MAX749 (w/DAC control)

☆ MAX1610 (CCFL with digital adj.)

☆ MAX1611 (CCFL with SMBus digital adj.)

★☆ MAX1620 (LCD bias supply with digital adj.)

★☆ MAX1621 (LCD bias supply with SMBus digital adj.)

see next page for Charge Pumps

DC-DC Converters

see previous page for
Low-Dropout Linear Regulators
and Switching Regulators

Charge Pumps

-VIN or (2 x VIN)

MAX660
(100mA, V_{IN} up to 5V)

MAX665
(100mA, V_{IN} up to 8V)

MAX828/829
(25mA in SOT23)

MAX860/861
(50mA, V_{IN} up to 5.5V, 250kHz osc. freq.)

★ MAX870/871
(25mA in SOT23, 500kHz)

MAX1044
(60kHz osc. freq. boost)

★ MAX1680/1681
(up to 1MHz, 100mA)

ICL7660
(µMAX, V_{IN} up to 10V)

ICL7662
(V_{IN} up to 20V)

Si7661
(V_{IN} up to 20V)

-VIN and (2 x VIN)

MAX864
(5kHz to 200kHz, 1µF caps, shutdown)

MAX865
(30kHz, µMAX package)

Regulated

† MAX868
(10mA, doubler or inverter, 500kHz)

†☆ MAX1673
(125mA, doubler or inverter, 250kHz)

12V, 30mA

☆ MAX662A
(programs flash memories, "E" temp. range)

5V

☆ MAX619
(50mA, 1.8V_{IN})

†☆ MAX682
(250mA, 2.7V_{IN})

†☆ MAX683/684
(100mA/50mA, 2.7V_{IN})

3.3V

★☆ MAX679
(20mA, 1.8V_{IN})

Regulated GaAsFET Bias Supply

★ MAX768
(pos. and neg. output, up to ±2 x V_{IN}, neg. GaAsFET bias, pos. VCO/LCD supply, power-OK signal)

☆ MAX840/843/844
(2.5V_{IN}, -2V_{OUT} low-noise, neg. GaAsFET bias)

☆ MAX850/851/852/853
(4.5V_{IN}, -4.1V_{OUT} low-noise, neg. GaAsFET bias)

† MAX881R
(µMAX package, power-OK signal, like MAX840)

★ New product
† Future product
☆ Evaluation kit available

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
STEP-UP SWITCHING REGULATORS										
MAX606/607	3 to 5.5	5 or 12 or adj.	0.5(0.25)/0.3(0.15)	200	PFM	8-µMAX	E	Yes	1MHz switching frequency fits Type 1 PCMCIA cards	3.25
MAX608	1.8 to 16.5	5 or adj.	0.11(0.085)	1A	PFM	8-DIP, 8-SO	E	Yes	Same as MAX1771, but accepts low input voltages	1.89
MAX624	3 to 5.5	5 & 12 or adj.	0.6(0.3)	200 at 5V, 80 at 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type 1 PCMCIA cards	5.25
MAX629	2.7 to 28	V_{IN} to 28 or 0 to -28	0.100(0.080)	10 at 28V	PFM	8-SO	E	Yes	30V/0.5A internal switch, configure as +28V or -28V	2.85
MAX630	2 to 16.5	Adj.	0.125(0.070)	30mW	PFM	8-DIP, 8-SO	C,E,M		Improved RC4123 second source	2.88
MAX631/632/633	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	40/25/20	PFM	8-DIP, 8-SO	C,E,M		Only two external components	2.56
MAX641/642/643	1.5 to 5.6/ 12.6/15.6	5/12/15 or adj.	0.4(0.135)/ 2(0.5)/2.5(0.75)	300/550/ 325	PFM	8-DIP, 8-SO	C,E,M		PFM controller	2.87
MAX686	2.7 to 27.5	Up to 28	0.125(0.08)	10 at 28V	PFM	16-QSOP	E	Yes	30V/0.5A internal switch, DAC-controlled output, configure as +28V or -28V	††
MAX731	1.8 to 5.25	5	4(2)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX732	4 to 9.3	12	3(1.7)	200	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.76
MAX733	4 to 11	15	3(1.7)	125	PWM	8-DIP, 16-WSO	C,E,M	Yes		2.60
MAX734	1.9 to 12	12	2.5(1.2)	120	PWM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, hot insert	2.23
MAX752	1.8 to 16	Adj.	3(1.7)	2.4W	PWM	8-DIP, 8-SO	C,E,M	Yes		2.94
MAX756/757	1.1 to 5.5	(3.3 or 5)/adj.	0.060(0.045)	250	PFM	8-DIP, 8-SO	C,E	Yes	Best combination of low I_Q & high 86% efficiency	1.95
MAX761/762	2 to 16.5	12/15 or adj. to 16.5	0.1(0.080)	120	PFM	8-DIP, 8-SO	C,E,M	Yes	12V flash memory, lowest I_Q, 1.8V/3V/5V inputs	2.23
MAX770/771/772	2 to 16.5	5/12/15 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	1.80
MAX1771	2 to 16.5	12 or adj.	0.1(0.085)	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Same as MAX771, but with single 100mV current-sense limit	1.80
MAX773	3 to 16.5	Adj.	0.1(0.085)	1A	PFM	14-DIP, 14-NSO	C,E,M		Controller, high-voltage applications	1.80
MAX777L/778L/779L	1 to 4.5	5/(3 or 3.3)/adj.	0.310(0.220)	300	PFM	8-DIP, 8-SO	C,E,M	Yes	On-chip active diode, true turn-off in shutdown	2.65
MAX848/849	0.7 to 5.5	3.3 or 2.7 to 5	0.06	100 to 600	PWM	16-NSO	E	Yes	1-3 cell step-up, low-noise, fixed-frequency PWM	2.38/2.50
MAX856/857	0.5 to 6	(3.3 or 5)/adj.	0.060(0.025)	100	PFM	8-SO, 8-µMAX	C,E	Yes	Smallest, best combination of low I_Q & high 85% efficiency	1.72
MAX858/859	0.5 to 6	(3.3 or 5)/adj	0.060(0.025)	25	PFM	8-SO, 8-µMAX	C,E	Yes	Smallest, best combination of low I_Q & high efficiency	1.72
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A	PFM	16-QSOP	E	Yes	Dual output, lowest I_Q, high efficiency	2.80
MAX866/867	0.5 to 6	(3.3 or 5)/adj.	0.06(0.027)	90	PFM	8-SO	E	Yes	Guaranteed 0.9V start-up, low I_Q	1.76
MAX1642/1643	0.7 to 5.5	3.3 or adj.	16(10)	90	PFM	8-µMAX	E	Yes	High efficiency, synchronous rectifier, dual LBI/LBO	1.76
MAX1700/1701	0.7 to 5.5	2.5 to 5.5	0.100(0.060)	800	PWM/ PFM	8-SO/16-QSOP	E	Yes (1700)	1V guaranteed start-up, MAX1701 includes 2 battery monitors and op-amp block	††
MAX1703	0.8 to 5.5	3.3 or adj. (2.7 to 5.5)	0.140(0.100)	1.5A	PWM/ PFM	16-NSO	E	Yes	1.1V guaranteed start-up, 92% efficiency	††
MAX1705/1706	0.7 to 5.5	2.5 to 5.5 (dual)	0.190(0.100)	800/500	PWM/ PFM	16-QSOP	E	Yes	Dual output: step-up and 200mA linear regulator, 1V guaranteed start-up	3.15/2.96
STEP-UP/DOWN SWITCHING REGULATORS										
MAX710/711	1.8 to 11	3.3 or 5/adj.(2.7 to 5)	0.1(0.08)	250	PFM	16-NSO	E	Yes	No transformer, step-up and linear	2.95
MAX761	2.7 to 12	Adj. (1.5 to 6)	0.1(0.08)	200	PFM	8-DIP, 8-SO	C,E,M		No transformer, SEPIC	2.23
	4.5 to 30	Adj. (1.1 to 5.5)	0.3	50W	PWM	16-SO	E		High efficiency over I_{OUT} range, 1% V_{OUT} accuracy	††
MAX1672	1.8 to 11	5 or 3.3 or adj. (2.7 to 5.0)	0.125(0.100)	150	PFM	16-QSOP	E	Yes	Step-up followed by linear regulator, in/out disconnect in shutdown	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
STEP-DOWN SWITCHING REGULATORS										
MAX638	2.6 to 16.5	5, adj.	0.6(0.135)	75	PFM	8-DIP, 8-SO	C,E,M			2.56
MAX639/640/653	4 to 11.5	5/3.3/3 or adj.	0.02(0.01)	225	PFM	8-DIP, 8-SO	C,E,M	Yes	Ultra-low I_Q	2.96
MAX1649/1651	3 to 16	5/3.3 or adj.	0.1(0.080)	2A	PFM	8-DIP, 8-SO	C,E	Yes	Drives external P-channel FET, low I_Q, but with 96.5% duty cycle and single 100mV current-sense limit	1.60
MAX1626/1627	3 to 16.5	3.3 or 5/adj.	0.080(0.060)	2A	PFM	8-SO	E	Yes	Same as MAX1651, but with 100% duty cycle, high efficiency, and controller	1.88
MAX724	0 to 60	Adj.	11(8.5)	5A	PWM	7-TO220	C,E			4.52
MAX726	0 to 40	Adj.	11(8.5)	2A	PWM	7-TO220	C,E			3.00
MAX727/728/729	0 to 40	5/3.3/3	11(8.5)	2A	PWM	7-TO220	C,E			3.00
MAX730A	5.2 to 11	5	3(1.7)	300	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX738A	6 to 16	5	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX730A/50A/63A	Up to 11	5/adj./3.3	3(1.7)	500	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX738A/48A/58A	Up to 16	5/3.3/adj.	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX744A	4.75 to 16	5	2.5(1.2)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	Optimized for cellular communications, no subharmonic switching noise	2.90
MAX748A	3.3 to 16	3.3	3(1.7)	750	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX750A	4 to 11	Adj.	3(1.7)	1.5W	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX758A	4 to 16	Adj.	3(1.7)	3.75W	PWM	8-DIP, 16-WSO	C,E,M	Yes	No subharmonic switching noise	2.60
MAX763A	3.3 to 11	3.3	2.5(1.4)	500	PWM	8-DIP, 8-SO	C,E,M	Yes	No subharmonic switching noise	2.15
MAX1640/1641	5.5 to 30	6 to 30	4(2)	50W	PWM	16-QSOP	E	Yes	High-efficiency current-source, synchronous rectifier	2.75
MAX767	4.5 to 5.5	3.3, 3.45 (R), or 3.6 (S)	0.75	1.5A to 10A	PWM	20-SSOP	C,E	Yes	Dedicated 5V-to-3.3V, high efficiency, small size	3.40
MAX787/788/789	0 to 60	5/3.3/3	11(8.5)	5A	PWM	7-TO220	C,E			4.52
MAX796/797/799	4.5 to 30	5.05/3.3/2.9/adj.	1(0.7)	50W	PWM	16-DIP, 16-NSO	C,E,M	Yes	Synchronous rectifier, secondary output regulation, high efficiency over full I_{OUT} range	3.65
MAX798	4.5 to 30	1.6/adj.	1(0.7)	50W	PWM	16-NSO	E		Synchronous rectifier, secondary output regulation, high efficiency over full I_{OUT} range	4.93
MAX830/831	0 to 30	Adj./5	–	1A	PWM	16-SO	C	Yes	Small package	3.99
MAX832/833	0 to 30	3.3/3	–	3A	PWM	20-SSOP	E	Yes	Small package	3.99
MAX887	4 to 11	adj. (1.27 to 9)	0.5(0.2)	500mA	PFM/PWM	8-SO	E	Yes	Internal synchronous rectifier, high efficiency, synchronizable	2.44
MAX1624	4.5 to 5.5	1.1 to 3.5	0.3	to 20A	PWM	24-SSOP	E	Yes	High accuracy Pentium Pro™ V_{ID} programming, synchronous rectifier, power-good output	3.85
MAX1625	4.5 to 5.5	1.1 to 3.5	0.3	to 20A	PWM	16-SO	E	Yes	High accuracy, synchronous rectifier, power-good output	3.39
MAX1636	4.5 to 30	Adj. (1.1 to 5.5)	0.3	50W	PWM	20-SSOP	E	Yes	Synchronous rectifier, high efficiency over I_{OUT} range, 1% V_{OUT} accuracy, OVP, power-good output	3.95
MAX1637	4.5 to 30	Adj. (1.1 to 5.5)	0.3	50W	PWM	16-SO	E		High efficiency over I_{OUT} range, 1% V_{OUT} accuracy	††
MAX1638	4.5 to 5.5	Adj. (1.3 to 3.5)	0.3	to 20A	PWM	24-SSOP	E	Yes	Pentium II™ VID, high accuracy, adjustable synchronous rectifier	††
MAX1639	4.5 to 5.5	Adj. (1.3 to 3.5)	0.3	to 20A	PWM	16-SO	E		High accuracy, adjustable synchronous rectifier	††
MAX1652/53/54	4.5 to 30	2.6 to 5.5	0.440(0.320)	50W	PWM/PFM	16-QSOP	E	Yes	High-efficiency, synchronous rectified, all N-channel design	††
MAX1655	4.5 to 30	1 to 5.5	0.440(0.320)	50W	PWM/PFM	16-QSOP	E	Yes	Same as MAX1653 with low-voltage output range	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package, µMAX = Micro Max, TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchanges rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

DC-DC Switching Converters (continued)

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Control Scheme	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
INVERTING SWITCHING REGULATORS										
MAX735/755	4 to 6.2	-5/adj.	3(1.6)	275	PWM	8-DIP, 8-SO	C,E,M		>80% efficiencies	2.15
MAX736/37/39/59	4 to 8.6	-12/-15/-5/adj.	3(1.6)	500	PWM	14-DIP, 16-WSO	C,E,M	Yes	>80% efficiencies	2.75
MAX749	2 to 6	Digital adj.	0.06	5W	PFM	8-DIP, 8-SO	C,E,M	Yes	Digital adjust for negative LCD	2.49
MAX764/765/766	3 to 16.5	-5/-12/-15 or adj. to 21ΔV	0.1	200	PFM	8-DIP, 8-SO	C,E,M	Yes	Lowest I_Q	2.38
MAX774/775/776	3 to 16.5	-5/-12/-15 or adj.	0.1	1A	PFM	8-DIP, 8-SO	C,E,M	Yes	Controllers, high efficiency over wide I_{OUT} range	2.20
DUAL-OUTPUT SWITCHING REGULATORS										
MAX624	3 to 5.5	5 & 12 or adj.	0.6(0.3)	200 at 5V, 80 at 12V	PFM	16-NSO	I		1.2MHz switching frequency fits Type 1 PCMCIA cards	5.25
MAX685	2.7 to 5.5	Pos: 2.7 to 24 Neg: -1.3 to -9	2(1)	10/output	PWM	16-QSOP	E	Yes	CCD power supply, single inductor, internal switches	††
MAX742	4.2 to 10	±12, ±15	15(8)	±15W	PWM	20-DIP, 20-WSO	C,E,M	Yes	Drives external MOSFETs	3.91
MAX743	4.2 to 6	±12, ±15	30(20)	±1.5W	PWM	16-DIP, 16-WSO	C,E,M	Yes	Internal power MOSFETs	4.49
MAX863	1.5 to 11	2 pos. adj.	65(40)	1A each	PFM	16-QSOP	E	Yes	Lowest I_Q, high efficiency	2.80
MAX1705/1706	0.7 to 5.5	Switcher: 2.5 to 5.5 LDO: down to 2.5	0.190(0.100)	800/500	PWM/ PFM	16-QSOP	E	Yes	Step-up, LDO, 1V guaranteed start-up	3.15/2.96

DC-DC Charge-Pump Converters

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—UNREGULATED								
MAX660	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	8-DIP, 8-SO	C,E,M	8-pin SO	2.95
MAX665	1.5 to 8	$-V_{IN}$, $+2 \times V_{IN}$	0.5(0.12)	100	8-DIP, 16-WSO	C,E,M		3.96
MAX680	2 to 6	$\pm 2 \times V_{IN}$	2(1)	±10	8-DIP, 8-SO	C,E,M	Dual output	1.62
MAX828/829	1.25 to 5.5	$-V_{IN}$	0.09(0.06)	25	5-SOT23	E	Better than ICL7660, smaller capacitors, ultra-small, lower ROUT	1.30
MAX860/861	1.5 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	0.33(0.18)	50	8-SO, 8-μMAX	C,E,M	Up to 250kHz oscillation frequency	1.45
MAX864	1.5 to 6.2	$\pm 2 \times V_{IN}$	0.3(0.2)	±10	16-QSOP	E	5kHz to 200kHz frequency select, 1μA shutdown	1.50
MAX865	1.5 to 6.2	$\pm 2 \times V_{IN}$	1.0(0.6)	±10	8-μMAX	E	Ultra-small μMAX package	1.30
MAX870/871	1.25 to 5.5	$-V_{IN}$	1(0.7)	25	5-SOT23	E	Smallest inverter, 0.1μF capacitors, 500kHz switching	1.30
MAX1044	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.2(0.03)	20	8-DIP, 8-SO	C,E,M	60kHz oscillator boost mode	1.19
MAX1680/1681	2 to 5.5	$-V_{IN}$, $+2 \times V_{IN}$	2(1.2)	125	8-SO	E	125kHz to 1MHz operation, small capacitors, same pin-out as MAX660	2.05
ICL7660	1.5 to 10	$-V_{IN}$, $+2 \times V_{IN}$	0.175(0.110)	20	8-DIP, 8-SO, 8-TO99, 8-μMAX	C,E,M	μMAX package	1.09
ICL7662	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	0.6(0.25)	10	8-DIP, 8-SO, 8-TO99	C,I		1.86
Si7661	4.5 to 20	$-V_{IN}$, $+2 \times V_{IN}$	2(0.3)	10	8-DIP, 8-SO, 8-TO99	C,I		1.86

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), TO-__ = Can

** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C

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†† Future product—contact factory for availability. Specifications

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA), max(typ)	Output (mA)	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
CHARGE-PUMP CONVERTERS—REGULATED									
MAX619	2 to 3.6	5	0.15	60	8-DIP, 8-SO	C,E,M	Yes	No inductors, battery backup	1.60
MAX622	3.5 to 16.5	V_{IN} + 11	0.5(0.07)	500µA	8-DIP, 8-SO	C,E		High-side switching	1.86
MAX662A	4.5 to 5.5	12	0.5(0.19)	30mA, guaranteed over temp.	8-DIP, 8-SO	C,E,M	Yes	World's smallest 12V flash memory programmer	2.09
MAX679	1.8 to 4	3.3	0.050(0.035)	20	8-µMAX	E	Yes	Up to 1MHz f_{OSC}, small caps	1.55
MAX682	2.7 to 5.5	5	0.130(0.100)	250	8-SO	E	Yes	Low-noise or low-I_Q modes, small caps	††
MAX683/684	2.7 to 5.5	5	0.100(0.070)	100/50	8-µMAX	E	Yes	Low-noise or low-I_Q modes, small circuit and caps	††
MAX768	2.5 to 5.5	Dual ±5V or adj.	0.8(0.45)	2 x 10mA	16-QSOP	E		Performs 3 power functions for handsets: -2 x V_{IN} for GaAsFET bias, +2 x V_{IN} for VCO, negative power-ready signal	2.40
MAX840/843/844	2.5 to 10	-2 or adj.	1.1(0.75)	10	8-SO	I,E	Yes	Low-voltage negative GaAsFET bias, low noise, 1µA shutdown	1.75
MAX850-853	4.5 to 10	-4.1 or adj.	3(2)	5	8-SO	I,E	Yes	Negative GaAsFET bias, low noise, 1µA shutdown	1.65
MAX868	1.8 to 5.5	Adj., ($-V_{IN}$, -2 x V_{IN})	0.050(0.035)	10	10-µMAX	E		Supply current varies with load, uses 0.22µF caps	††
MAX881R	2.5 to 5.5	-2 or adj.	0.9(0.5)	5	10-µMAX	E	Yes	GaAsFET PA bias in 1.11mm-high package, includes power-OK output signal	††
MAX1673	2 to 5.5	Adj., ($-V_{IN}$, -2 x V_{IN})	0.200(0.150)	125	8-SO	E	Yes	Small caps, 2 regulation modes: linear or skipping, up to 250kHz	††

PCMCIA Switch Matrices

Part Number	Input Voltages (V)	Outputs	Controls	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX613	3.3/5/12	2 card slots	Std. PCMCIA	14-DIP, 14-SO	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.68
MAX614	3.3/5/12	1 card slot	Std. PCMCIA	8-DIP, 8-SO	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.48
MAX780A–C	3.3/5/12	2 card slots	Std. PCMCIA	24-DIP, 24-SSOP	C,E	Internal V_{PP} switches, external V_{CC} drivers, V_{PP} valid output	2.25/2.00/2.05
MAX780D	3.3/5/12	2 card slots	Std. PCMCIA	20-DIP, 20-SSOP	C,E	Internal V_{PP} switches, external V_{CC} drivers	1.80
MAX1600/1603	3.3/5/12	2 card slots	Std. PCMCIA	28-SSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	5.95/5.25
MAX1601/1604	3.3/5/12	2 card slots	SMBus	28-SSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	5.95/5.25
MAX1602	3.3/5/12	1 card slots	Std. PCMCIA	16-QSOP	E	Internal V_{CC} and V_{PP} switches, current limit, thermal protection	2.35
MAX1614	5 to 26	—	N-channel drive for MOSFETs	8-µMAX	E	High-side, N-channel MOSFET switch drivers	1.74

Load Switch Controllers

Part Number	Input Voltage Range (V)	Supply Current (µA)	Power-On Reset	Applications	Pins Package Options**	Temp. Ranges**	Features	Price† 1000-up ($)
MAX1661	2.7 to 5.5	3	Outputs low	N-channel MOSFETs	10-µMAX	E	Serial-to-parallel/parallel-to-serial	††
MAX1662	2.7 to 5.5	3	Outputs high	P-channel MOSFETs	10-µMAX	E	Load switch controller with SMBus interface	††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

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Linear Voltage Regulators

Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage (V)	Quiescent Current (µA), max(typ)	Output Voltage Accuracy (%)	Shutdown	Pins-Package Options*	EV Kit	Temp. Ranges**	Price† 1000-up ($)
DC LINEAR REGULATORS—POSITIVE OUTPUT										
MAX603/4	2.7 to 11.5	5/3.3 or adj. (1.3 to 11.5)	0.32 at 500mA	35(15)	±5	2µA off	8-DIP, 8-SO (P_{DISS} = 1.8W)		C,E,M	1.85
MAX663	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.75
MAX666	2 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.9 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.76
MAX667	3.5 to 16.5	Fixed 5 or adj.(1.3 to 15)	0.15 at 200mA	25(20)	±4	Yes	8-DIP, 8-SO		C,E,M	2.35
MAX687/8/9	2.7 to 11	Fixed 3.3/3.3/3.0	0.073 at 500mA, 0.80 at 4A	250(150)	±3	Yes 25µA, off 1µA	8-DIP, 8-SO, 8-µMAX	Yes	C,E	1.60
MAX882	2.7 to 11.5	3.3 or adj. (1.5 to 11.5)	0.32 at 200mA	15(10)	±5	15µA standby	8-DIP, 8-SO (P_{DISS} = 1.5W)		C,E,M	1.45
MAX883/4	2.7 to 11.5	5/3.3 or adj. (1.5 to 11.5)	0.22 at 200mA	15(10)	±5	1µA off	8-DIP, 8-SO (P_{DISS} = 1.5W)		C,E,M	1.45
MAX1615	4 to 28	3.3/5	0.35 at 30mA	6(8)	±4	Yes	5-SOT23		E	0.79
MAX1616	4 to 28	Adj.	0.35 at 30mA	6(8)	±4	Yes	5-SOT23		E	††
MAX1658/1659	2.7 to 16.5	3.3/5 or adj. (1.25 to 16)	0.49 at 350mA	60(30)	±3	Yes	8-SO (P_{DISS} = 1.8W)		E	1.95
MAX8862	2.5 to 11.5	2.85/3.18/4.9 or adj. (2 to 11)	0.20 at 250mA (dual)	330(200)	±3.5	10nA off	16-NSO		E	2.20
MAX8863/8864	2.5 to 6.5	1.25 to V_{IN}	0.11 at 100mA	170(70)	±3.5	Yes	5-SOT23		E	0.79
MAX8865/8866	2.5 to 6.5	2.8/2.84/3.15 or adj. (1.3 to 5.5)	0.11 at 100mA (dual)	270(105)	±2.5	2nA off	8-µMAX		E	1.46
MAX8867/8868	2.5 to 6.5	1.25 to V_{IN}	0.14 at 120mA	180(90)	±3	Yes	5-SOT23		E	††
MAX8873/8874	2.5 to 6.5	1.25 to V_{IN}	0.11 at 100mA	170(70)	±3.5	Yes	5-SOT23		E	0.79
MAX8877/8878	2.5 to 6.5	1.25 to V_{IN}	0.14 at 120mA	180(90)	±3	Yes	5-SOT23		E	††
ICL7663/A	1.5 to 16/2 to 16	Adj.(1.3 to 15)	0.9 at 40mA	10(3.5)	±8/±1.9	Yes	8-DIP, 8-SO, 8-TO99		C,E,I,M	1.81/1.99
DC LINEAR REGULATORS—NEGATIVE OUTPUT										
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.35 at 40mA	12(6)	±5	Yes	8-DIP, 8-SO		C,E,M	1.75
ICL7664A	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±1	Yes	8-DIP, 8-SO, 8-TO99		C,I,M	2.40
ICL7664B	-2 to -16	-1.3 to -15	0.4 at 30mA	10(3.5)	±5	Yes	8-DIP, 8-SO, 8-TO99		C,I,M	1.85

Battery Chargers/Fuel Gauges

Part Number	No. of Cells Charged	Cell Chemistry	Charge Rate	Charge Termination Method	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
MAX712/713	1 to 16	NiMH/NiCd	Fast, trickle	0ΔV, max V, max temp, max time (neg ΔV, MAX713)	16-DIP, 16-NSO	C,E,M	Yes	Linear or switcher, supplies load while charging, built-in termination algorithms	3.09
MAX745	1 to 4	Li+	Digital prog.	Voltage and current limit	20-SSOP	E	Yes	High-efficiency switch mode, 0.75% precision	4.50
MAX846A	1 to 10	Li+/NiCd/NiMH	Fast, trickle, top-off	Universal charger, user set	16-QSOP	E	Yes	Complete system, 1%-accurate V_{OUT} for Li+, built-in 1% LDO, drives PNP, cost-saving, independent V & I reg loops	3.25
MAX1640/1641	1 to 16	Universal	Fast, trickle, top-off	Voltage and current limit	16-QSOP	E	Yes	High-efficiency PWM current-source, synchronous rectifier	2.75
MAX1647/1648	1 to 8	Universal	Digitally programmed	Voltage and current limit, thermistor	20-SSOP/16-NSO	E	Yes	SBS level 2 smart-battery charger with SMBus interface (MAX1647)9	4.79/4.25
MAX1660	4 to 28	—	—	—	16-QSOP	E	Yes	Digitally controlled fuel-gauge interface with ±1% absolute accuracy	††
MAX2003/A	1 to 16	NiCd and/ or NiMH	Fast, trickle, top-off	Temp slope, neg. ΔV, max temp, max time	16-DIP, 16-WSO 16-NSO	C	Yes	Linear, built-in termination algorithms, discharge-before-charge, pulse trickle (A)	3.25/3.80

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Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Auxiliary Outputs (V)	Quiescent Supply Current, Over Temp. (µA)	Pins-Package Options*	Temp. Ranges**	EV Kit	Features	Price† 1000-up ($)
MAX717-721	0.9 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	3.3 (MAX717), 3.3 or 5 (MAX718/720), 3 or 5 (MAX719/721)	5 or 12 (all)	60, 40 shutdown	16-NSO	C,E	Yes (MAX717-MAX719)	Built-in switchover from main battery to plug-in adapter power, low-voltage warning, AC detect, clock & RAM keep-alive mini-switcher from backup battery	4.95
MAX722/723	0.85 to 5.5 (battery), 7 to 18 (plug-in adapter)	–	3.3 or 5 (MAX722), 3 or 5 (MAX723)	Neg. LCD (0 to -40)	60, 40 shutdown	16-NSO	C,E	Yes	Built-in switchover from main battery to plug-in adapter power, low-voltage warning	4.63
MAX769	1.5 to 5.5	3.0 @ 65mA, 2.85 @ 25mA, 1.0 @ 2mA	1.8 to 4.9 @ 80mA	Battery charger, 2 x 1.8Ω drivers	875 full-on, 15 coasting	28-QSOP	E		Step-up/down DC-DC intended for 3-cell, 2-way pagers; serial interface	††
MAX781	5 to 18	3.3 at 10mA, 5.0 at 25mA	3.3, 14, battery charger	Battery charger, current source, dual V_{PP} outputs	100 shutdown, 750 standby, 2mA operating	36-SSOP	C,E		High-power controller to 50W or more, dual PCMCIA V_{PP} outputs, analog mux, SPI interface	8.80
MAX782	5.5 to 30	3.3 at 5mA, 5 at 25mA	3.3‡, 5, 14	Dual V_{PP} outputs	70 standby, 750 per output enabled	36-SSOP	C,E	Yes	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors	5.95
MAX783	5.5 to 30	3.3 at 5mA, 5.0 at 25mA	3.3‡, 5, 14	Dual V_{PP} outputs	70 standby, 750 per output enabled	36-SSOP	C,E	Yes	High-power dual controller to 50W or more, dual PCMCIA V_{PP} outputs, three precision voltage monitors, optimized for 6-cell operation	5.95
MAX786	5.5 to 30	3.3 at 5mA, 5.0 at 25mA	3.3‡, 5	–	40 shutdown, 70 standby, 750 per output enabled	28-SSOP	C,E	Yes	High-power dual controller to 50W or more, two precision voltage monitors	4.15
MAX847	0.8 to 1.8	3.0 @ 65mA, 2.85 @ 25µA, 1.0 @ 2mA	1.8 to 4.9 @ 80mA	Battery charger, 2 x 1.8Ω drivers	875 full-on, 15 coasting	28-QSOP	E		Step-up DC-DC intended for 1-cell, 2-way pagers; serial interface	††
MAX863	1.5 to 11	–	Main = 3.3 or 5 or adj./1A, aux. = adj./1A	LBI/LBO low-battery detector	45 w/main on, 65 w/both on, 1 in shutdown	16-QSOP	E	Yes	Two high-efficiency boost controllers on one IC, for PDAs and organizers	2.80
MAX1630/ 1632/1633/ 1635	4.2 to 30	5.0 at 50mA	3.3 or adj./ 5.0 or adj.	12V at 120mA	10 shutdown, 30 standby (typ), 2.5mW (typ) both outputs enabled	28-SSOP	C,E	Yes	High-efficiency controller for notebook computers, include 12V Li+ and secondary winding controller, MAX1630/32 include OVP/VVP	5.45/4.50
MAX1631/ 1634	4.2 to 30	5.0 at 50mA	3.3 or adj./ 5.0 or adj.	Programmable secondary	10 shutdown, 30 standby, 1.5mW (typ) both outputs enabled	28-SSOP	C,E	Yes	High-efficiency controller for notebook computers, include secondary winding controller, MAX1631 includes OVP/VVP	5.22/4.27
BATTERY-CHARGING SYSTEM										
MAX846A	3.5 to 20	Up to 2A	N/A	1%, 3.3V, 20mA LDO	500 (on), 1 (off)	16-QSOP	E	Yes	Cost-saving universal charging system, 0.5% reference for Li+, drives low-cost PNP, independent I and V loops, 1% LDO is power to µC and reference for ADC	3.25

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

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LCD & CCFL Display Power Supplies

Part Number	Input Voltage Range (V)	DC-DC Output Voltages (V)	Quiescent Supply Current (µA)	Pins-Package Options*	EV Kit	Features	Price† 1000-up ($)
MAX629	2.7 to 28	V_{IN} to 28 or 0 to -28	80	8-SO	Yes	Internal 30V/0.5A switch	2.85
MAX686	2.7 to 27.5	Configure up to +28 or -28	80	16-QSOP	Yes	DAC-controlled output, internal 30V/0.5A switch	††
MAX749	2 to 6	Negative LCD	60	8-DIP, 8-SO	Yes	Digital LCD adjustment	2.49
MAX753	6 to 24	CCFL drive, configurable; negative LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX754	6 to 24	CCFL drive, configurable; positive LCD, configurable	100	16-DIP, 16-NSO		Digital CCFT and LCD adjustment	4.45
MAX759	4 to 15	Negative LCD, adjustable	1.2mA	14-DIP, 16-WSO	Yes	Internal MOSFET	2.75
MAX774/775/776	3 to 16.5	Negative LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	2.20
MAX828/829	1.25 to 5.5	$-V_{IN}$	60	5-SOT23		No inductors, low-cost compact pager supply, better than '7660	1.30
MAX860/861	1.5 to 5.5	$-V_{IN}$ or 2 x V_{IN}	180	8-SO, 8-µMAX		No inductors, up to 250kHz oscillator, 2.2µF caps, smallest pager LCD supply	1.45
MAX868	1.8 to 5.5	Adj.($-V_{IN}$ to -2 x V_{IN})	35	10-µMAX	Yes	Supply current varies with load, compact, low I_Q for pagers	††
MAX870/871	1.25 to 5.5	$-V_{IN}$	700	5-SOT23		Smallest inverter, uses 0.1µF capacitors, 500kHz switching	1.30
MAX1044	1.5 to 10	$-V_{IN}$ or 2 x V_{IN}	30	8-DIP, 8-SO		No inductors, 60kHz boost pin, pager LCD supply	1.19
MAX1610	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital adjust, open and shorted lamp protection	3.85
MAX1611	4.5 to 28	CCFL drive, configurable	2mA	16-SO	Yes	Internal MOSFET, digital SMBus adjust, open and shorted lamp protection	3.85
MAX1620	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		Digital adjust, 32 levels	1.99
MAX1621	4.5 to 24	Positive or negative LCD, configurable	500	16-QSOP		SMBus adjust, 32 levels	1.99
MAX1771	2 to 16.5	Positive LCD, adjustable	85	8-DIP, 8-SO	Yes	PFM controller, high efficiency, 5µA shutdown	1.80
ICL7660	1.5 to 10	$-V_{IN}$ or 2 x V_{IN}	110	8-DIP, 8-SO, 8-µMAX		No inductors, low-cost pager LCD supply, µMAX package	1.09

MOSFET Drivers

Part Number	Output Resistance (Ω) max(typ)	Rise/Fall, T_A = +25°C (ns max)	Rise/Fall, Over Temp. (ns max)	Peak Output Current (A)	Supply Voltage (V)	Pins-Package Options*	Temp. Ranges**	Features	Price† 1000-up ($)
MAX626/627/628	15(4)	30/30(1000pF)	40/40(1000pF)	2	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.49
MAX4420/4429	2.5(1.5)	30/30(2500pF)	60/60(2500pF)	6	4.5 to 18	8-DIP, 8-SO	C,E,M	Single noninverting/single inverting	1.71
MAX4426/4427/4428	10(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.61
ICL7667	12(4)	30/30(1000pF)	40/40(1000pF)	1.5	4.5 to 15	8-DIP, 8-SO	C,E,M	Dual inverting	1.12
TSC426/427/428	15(6)	30/30(1000pF)	60/40(1000pF)	1.5	4.5 to 18	8-DIP, 8-SO	C,E,M	Dual inverting/dual noninverting/dual mixed	1.06

Miscellaneous Power Supplies

Part Number	Description	Pins-Package Options*	Temp. Range**	EV Kit	Features	Price† 1000-up ($)
MAX845	Isolated transformer driver	8-SO, 8-µMAX	E	Yes	750mW output, thin transformer, fits PCMCIA cards	1.55
MAX869L	Current-limit power switch	16-QSOP	E		70mΩ/2A switch	2.15
MAX890L	Current-limited power switch	8-SO	E		90mΩ, 1A switch	1.25
MAX891L/892L	Current-limited power switches	8-µMAX	E		150mΩ/0.5A (MAX891L), 300mΩ/0.25A (MAX892L)	1.32
MAX894L/895L	Dual current-limited power switches	8-SO	E		Dual, 150mΩ/0.5A (MAX894L), 300mΩ/0.25A (MAX895L)	1.99
MAX1661/1662	Serial-to-parallel/parallel-to-serial converter and load switch controller with SMBus	10-µMAX	E			††

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline (N = Narrow, W = Wide), SSOP = Shrink Small-Outline Package

** Temperature Ranges: C = 0°C to +70°C, E = -40°C to +85°C, I = -25°C to +85°C, M = -55°C to +125°C

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-1219; Rev 1; 6/97

EVALUATION KIT AVAILABLE

MAXIM

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

General Description

The MAX629 low-power DC-DC converter features an internal N-channel MOSFET switch and programmable current limiting. It is designed to supply positive or negative bias voltages up to ±28V from input voltages in the 0.8V to V_{OUT} range, and can be configured for boost, flyback, and SEPIC topologies.

The MAX629's current-limited pulse-frequency-modulation (PFM) control scheme provides high efficiency over a wide range of load conditions. An internal, 0.5A N-channel MOSFET switch reduces the total part count, and a high switching frequency (up to 300kHz) allows for tiny surface-mount magnetics.

The MAX629's combination of low supply current, logic-controlled shutdown, small package, and tiny external components makes it an extremely compact and efficient high-voltage biasing solution that's ideal for battery-powered applications. The MAX629 is available in an 8-pin SO package.

Applications

Positive or Negative LCD Bias Generators

High-Efficiency DC-DC Boost Converters

Varactor Tuning Diode Bias

Palmtop Computers

2-Cell and 3-Cell Battery-Powered Applications

Features

- **Internal, 500mA, 28V N-Channel Switch (No External FET Required)**
- **Generates Positive or Negative Output Voltages**
- **80µA Supply Current**
- **1µA Max Shutdown Current**
- **Up to 300kHz Switching Frequency**
- **Adjustable Current Limit Allows Use of Small, Inexpensive Inductors**
- **8-Pin SO Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX629C/D	0°C to +70°C	Dice*
MAX629ESA	-40°C to +85°C	8 SO

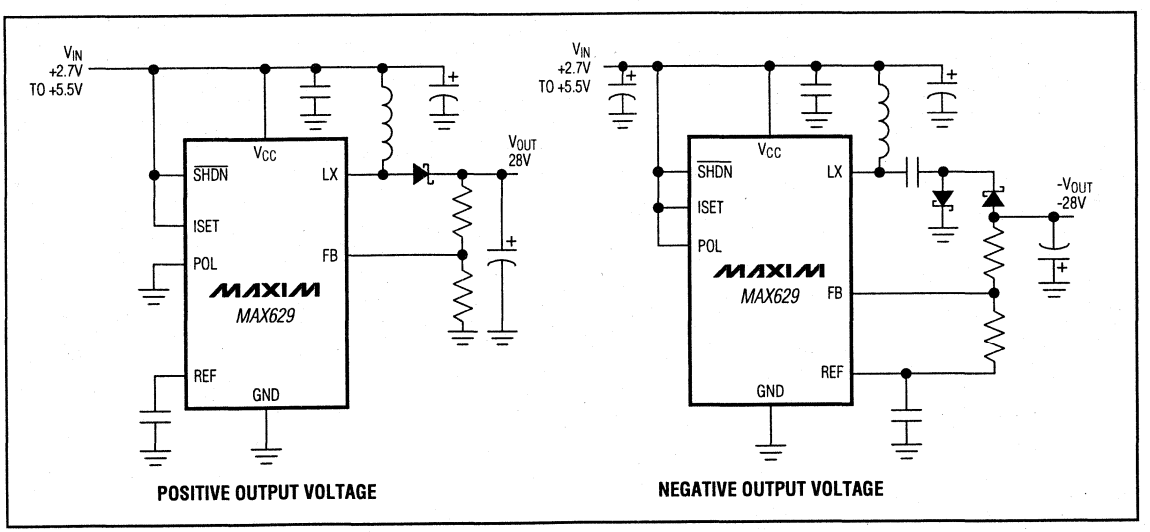
**Dice are tested at T_A = +25°C, DC parameters only.*

Note: To order tape-and-reel shipping, add "-T" to the end of the part number.

Pin Configuration appears at end of data sheet.

4

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to GND) ..... -0.3V to +6V
$\overline{SHDN}$ to GND ..... -0.3V to +6V
ISET, REF, FB, POL to GND ..... -0.3V to (V_{CC} + 0.3V)
LX to GND ..... -0.3V to +30V
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Input Voltage (Note 2)			2.7		5.5	V
V_{CC} Supply Current	V_{FB} = 1.3V			80	120	µA
V_{CC} Shutdown Current	$\overline{SHDN}$ = GND			0.04	1	µA
V_{CC} Undervoltage Lockout	100mV hysteresis		2.3	2.5	2.65	V
Input Supply Voltage (Note 2)	Voltage applied to L1 (V_{IN})		0.8		$\lvert V_{OUT} \rvert$	V
$\overline{SHDN}$, POL, ISET Logic Levels	V_{IH}		2.4			V
	V_{IL}				0.4	
Positive Output Voltage	Circuit of Figure 2				28	V
Negative Output Voltage	Circuit of Figure 3		$-\lvert V_{IN} \rvert$		-28	V
LX Switch-Current Limit	ISET = V_{CC}		0.39	0.45	0.51	A
	ISET = GND		0.20	0.25	0.33	
LX On-Resistance	V_{CC} = 5V			0.6	1.2	Ω
	V_{CC} = 3.3V			0.7	1.4	
LX Leakage Current	V_{LX} = 28V, T_A = +85°C			0.05	2.5	µA
Maximum LX On-Time			6.5	8.5	10.0	µs
Minimum LX Off-Time	POL = GND		0.7	1.0	1.3	µs
	POL = V_{CC}		2.0	3.2	3.8	
	POL = GND, V_{FB} < 1V		3.0	4.5	6.0	
	POL = V_{CC}, V_{FB} > 0.25V		3.0	4.5	6.0	
FB Set Point	POL = GND (positive output)	T_A = 0°C to +85°C	1.225	1.250	1.275	V
		T_A = -40°C to +85°C	1.218		1.282	
	POL = V_{CC} (negative output)	T_A = 0°C to +85°C	-15	0	15	mV
		T_A = -40°C to +85°C	-25		25	
FB Input Bias Current				5	50	nA
REF Output Voltage	V_{CC} = 2.7V to 5.5V, no load on REF	T_A = 0°C to +85°C	1.225	1.250	1.275	V
		T_A = -40°C to +85°C	1.218		1.282	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, C_{REF} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REF Load Regulation	I_{REF} = 0µA to 100µA, C_{REF} = 0.47µF (Note 3)		10	25	mV
Line Regulation	Circuit of Figure 2, V_{OUT} = 24V, V_{CC} = 3V to 5.5V, I_{LOAD} = 5mA		0.2		%/V
Load Regulation	Circuit of Figure 2, V_{OUT} = 24V, V_{CC} = 5V, I_{LOAD} = 0mA to 5mA		0.15		%
Thermal Shutdown Threshold	Die temperature		150		°C

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

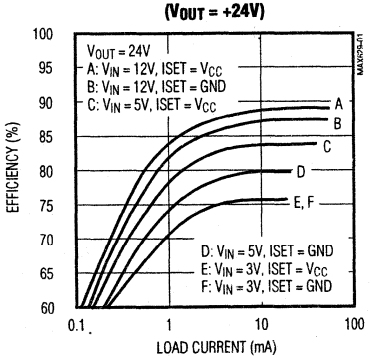
Note 2: The IC itself requires a supply voltage between +2.7V and +5.5V; however, the voltage that supplies power to the inductor can vary from 0.8V to 28V, depending on circuit operating conditions.

Note 3: For reference currents less than 10µA, a 0.1µF reference-bypass capacitor is adequate.

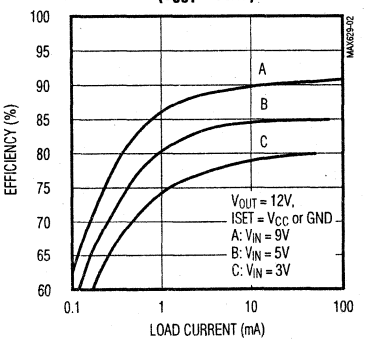
Typical Operating Characteristics

($\overline{SHDN}$ = V_{CC}, C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

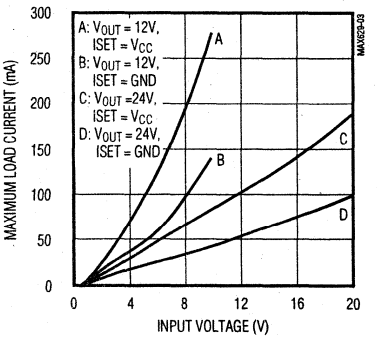
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +24V)



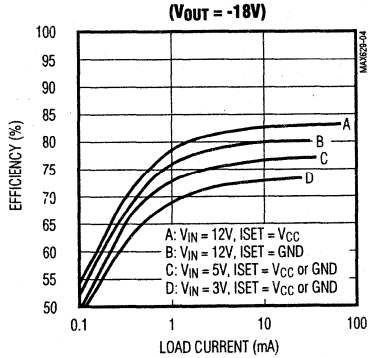
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = +12V)



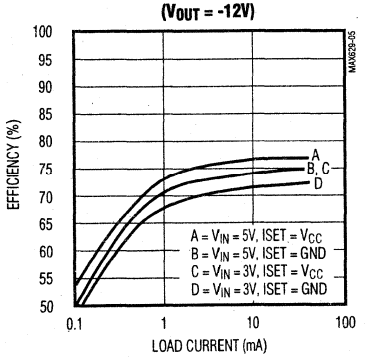
MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE (V_{OUT} = +24V, +12V)



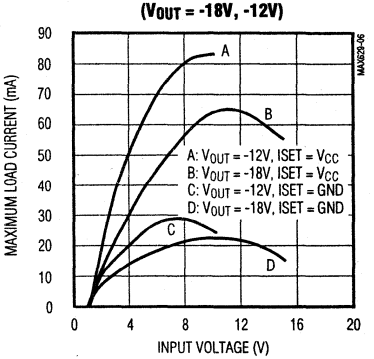
EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -18V)



EFFICIENCY vs. LOAD CURRENT (V_{OUT} = -12V)



MAXIMUM LOAD CURRENT vs. INPUT VOLTAGE (V_{OUT} = -18V, -12V)

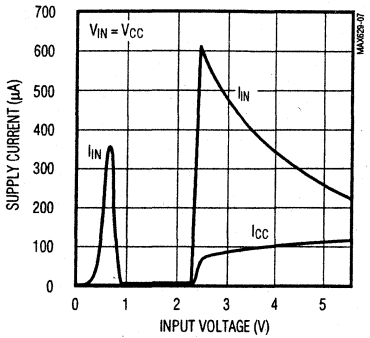


28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

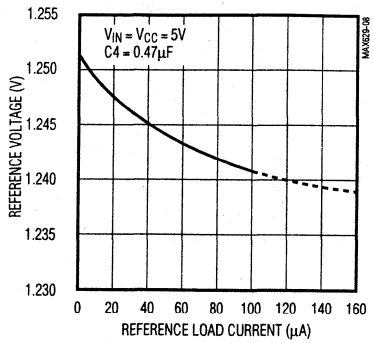
Typical Operating Characteristics (continued)

($\overline{SHDN}$ = V_{CC} , C_{REF} = 0.1µF, T_A = +25°C, unless otherwise noted.)

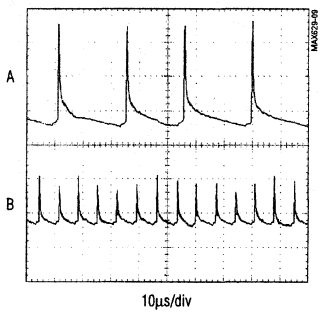
SUPPLY CURRENT vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT

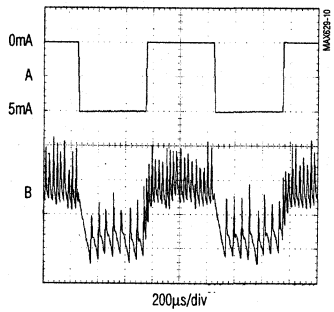


OUTPUT VOLTAGE RIPPLE



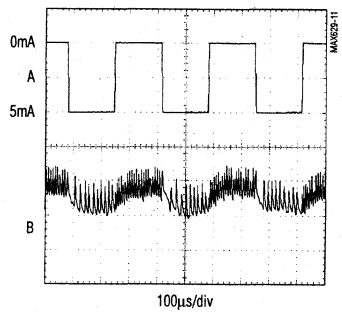
VOUT = +24V, ILOAD = 5mA
A: ISET = VCC, 20mV/div
B: ISET = GND, 20mV/div

LOAD-TRANSIENT RESPONSE (ISET = VCC, ILIM = 500mA)



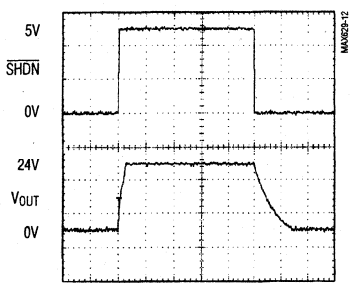
VOUT = +24V, ISET = VCC
A: LOAD CURRENT, 0mA TO 5mA, 2.5mA/div
B: VOUT, AC-COUPLED, 10mV/div

LOAD-TRANSIENT RESPONSE (ISET = GND, ILIM = 250mA)



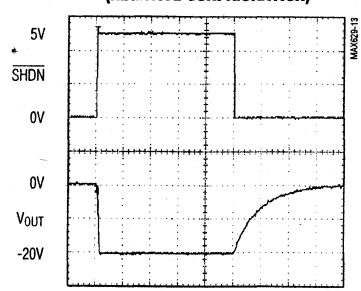
VOUT = +24V, ISET = GND
A: LOAD CURRENT, 0mA TO 5mA, 2.5mA/div
B: VOUT, AC-COUPLED, 10mV/div

SHUTDOWN TRANSIENT (POSITIVE CONFIGURATION)



VCC = VIN = 5V, RL = 4kΩ

SHUTDOWN TRANSIENT (NEGATIVE CONFIGURATION)



VCC = VIN = 5V, RL = 4kΩ

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low puts the MAX629 in shutdown mode and reduces supply current to 1µA.
2	POL	Polarity Input. Changes polarity and threshold of FB to allow regulation of either positive or negative output voltages. Set POL = GND for positive output voltage, or set POL = V_{CC} for negative output voltage.
3	REF	1.25V Reference Output. Bypass to GND with a 0.1µF capacitor for $I_{REF} \leq 10µA$. REF can source 100µA to drive external loads. For $10µA \leq I_{REF} \leq 100µA$, bypass REF with a 0.47µF capacitor.
4	FB	Feedback Input for setting output voltage. Connect to an external voltage divider. See *Setting the Output Voltage.*
5	ISET	Current-Limit Set Input. Connect to V_{CC} for a 500mA LX current limit, or connect to GND for a 250mA LX current limit. See *Setting the Current Limit.*
6	GND	Ground
7	LX	Internal N-Channel DMOS Switch Drain
8	V_{CC}	Power-Supply Input

Detailed Description

The MAX629 low-power, boost DC-DC converter provides either positive or negative output voltages up to ±28V from a wide range of input voltages. It is designed primarily for use in low-power, high-voltage applications such as LCD biasing and set-top box varactor tuning. The MAX629's unique control scheme provides high efficiency and a wide range of output voltages with only 80µA quiescent supply current, making it ideal for battery-powered applications. The internal N-channel DMOS switch has a pin-programmable current limit (250mA and 500mA), allowing optimization of output current and component size. Figure 1 shows the MAX629 functional diagram.

Control Scheme

A combination of peak-current limiting and a pair of one-shots controls the MAX629 switching, determining the maximum on-time and constant off-time. During the on-cycle, the internal switch closes, and current through the inductor ramps up until either the fixed 10µs maximum on-time expires (at low input voltages) or the switch's peak current limit is reached. The peak switch current limit is selectable to either 500mA (ISET = V_{CC}) or 250mA (ISET = GND) (see *Setting the Current Limit*). After the on-cycle terminates, the switch turns off, charging the output capacitor through the diode. In normal operation, the minimum off-time is set to 1µs for positive output voltages and 3.5µs for negative output voltages. When the output is well below regulation, however, the off-time is increased to 5µs to provide soft-start during start-up. The switching frequency, which depends upon the load, can be as high as 300kHz.

Shutdown Mode

When $\overline{SHDN}$ is low, the MAX629 enters shutdown mode. In this mode, the feedback and control circuit, reference, and internal biasing circuitry turn off. The shutdown current drops to less than 1µA. $\overline{SHDN}$ is a logic-level input; connect it to V_{CC} for normal operation.

The output voltage behavior in shutdown mode depends on the output voltage polarity. In the positive output voltage configuration (Figure 2), the output is directly connected to the input through the diode (D1) and the inductor (L1). When the device is in shutdown mode, the output voltage falls to one diode drop below the input voltage, and any load connected to the output may still conduct current. In the negative output voltage configuration (Figure 3), there is no DC connection between the input and the output, and in shutdown mode the output is pulled to GND.

Design Procedure

Setting the Output Voltage

For either positive or negative output voltage applications, set the MAX629's output voltage using two external resistors, R1 and R2, as shown in Figures 2 and 3. Since the input bias current at FB has a 50nA maximum value, large resistors can be used in the feedback loop

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

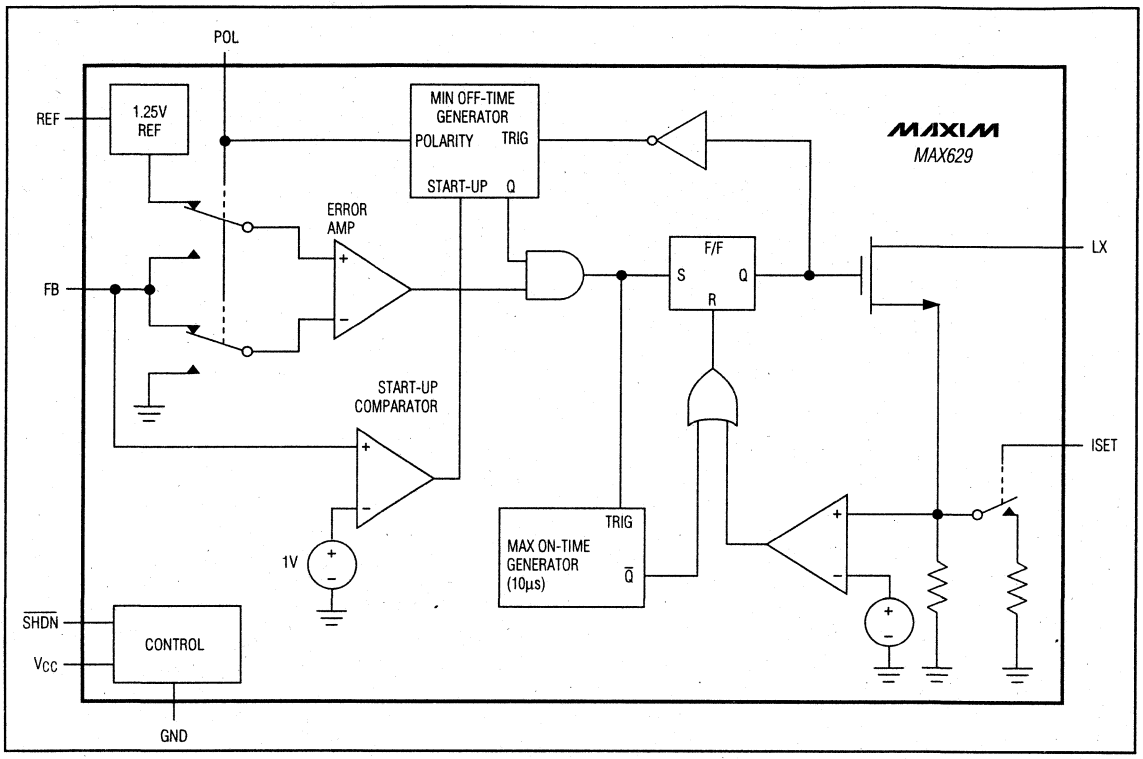


Figure 1. Functional Diagram

without a significant loss of accuracy. Begin by selecting R2 to be in the 10kΩ to 200kΩ range, and calculate R1 using the applicable equation from the following subsections.

Positive Output Voltages

For positive output voltages, use the typical boost configuration shown in Figure 2, connecting POL to GND. This sets the threshold voltage at FB to equal V_{REF}. Choose the value of R2 and calculate R1 as follows:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right)$$

where V_{REF} = 1.25V.

Negative Output Voltages

For negative output voltages, configure R1 and R2 as shown in Figure 3, connecting POL to V_{CC}. This sets the FB threshold voltage to GND so that negative voltages can be regulated. Choose R2 and calculate R1 as follows:

$$R1 = R2 \times \frac{|V_{OUT}|}{V_{REF}}$$

where V_{REF} = 1.25V.

Figure 3 demonstrates generation of a negative output voltage by following the MAX629 with an inverting charge pump. This configuration limits $|V_{OUT}|$ to values between $-|V_{IN}|$ and -28V. If smaller negative output voltages are required, D2's cathode can be connected to V_{IN}. This alternative configuration permits output voltages smaller than $-|V_{IN}|$, but cannot be used for output voltages more negative than $-|28V - V_{IN}|$. It produces roughly one-half the output current as the standard configuration and is typically 5% less efficient.

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

Setting the Current Limit

External current-limit selection provides added control over the MAX629's output performance. A higher current limit increases the amount of energy stored in the inductor during each cycle, which provides a higher output current capability. For higher output current applications, choose the 500mA current-limit option by connecting ISET to VCC. When lower output current is required, the 250mA current limit can provide several advantages. First, a smaller inductor can be used, which saves board area and cost. Second, the smaller energy transfer per cycle reduces output ripple for a given capacitor, providing design flexibility between board area, cost, and output ripple by allowing cheaper, higher-ESR capacitors. Connect ISET to GND to select the 250mA current-limit option.

Inductor Selection

The MAX629's high switching frequency allows for the use of a small inductor. The 47µH inductor shown in the *Typical Operating Circuit* is recommended for most applications. Larger inductances reduce the peak inductor current, but may limit output current capability at low input voltages and provide slower start-up times. Smaller inductances require less board space, but may cause greater peak current due to current-sense comparator propagation delay. If input voltages below 2V will be common, reducing the inductance to 22µH might improve performance; however, maximum load current and efficiency may decline. It is important to thoroughly test operation under all input and output conditions to ensure proper component selection.

Inductors with a ferrite core or equivalent are recommended; powder iron cores are not recommended for use with high switching frequencies. The inductor's incremental saturation rating must exceed the selected current limit. For highest efficiency, use an inductor with a low DC resistance (under 100mΩ). See Table 1 for a list of inductor suppliers.

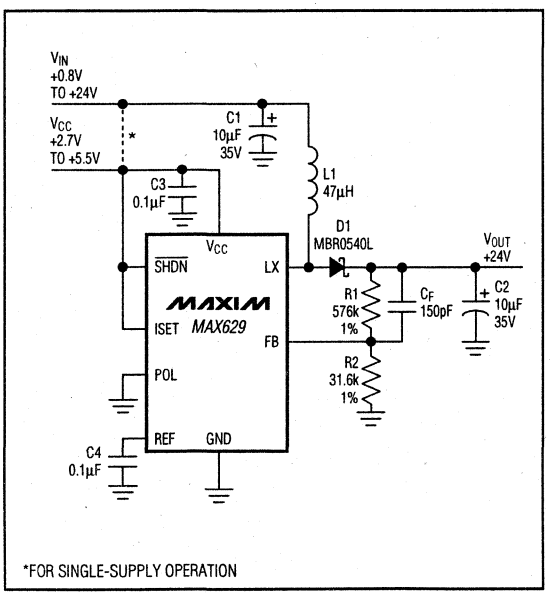


Figure 2. +24V for a Positive LCD Bias

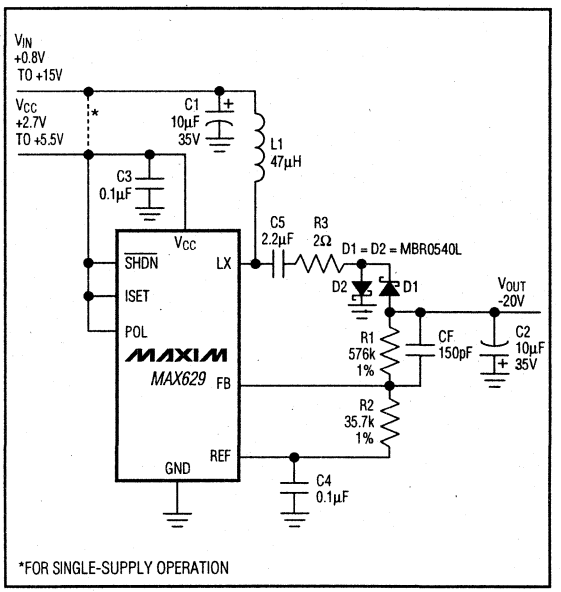


Figure 3. -20V for a Negative LCD Bias

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

Diode Selection

The MAX629's high switching frequency demands a high-speed rectifier. Schottky diodes, such as the 1N5819 or MBR0530L, are recommended. Make sure that the diode's peak current rating exceeds the peak current set by ISET, and that its breakdown voltage exceeds the output voltage. Schottky diodes are preferred due to their low forward voltage. However, ultra-high-speed silicon rectifiers are also acceptable. Table 1 lists Schottky diode suppliers.

Capacitor Selection

Output Filter Capacitor

The primary criterion for selecting the output filter capacitor is low effective series resistance (ESR). The product of the peak inductor current and the output filter capacitor's ESR determines the amplitude of the high-frequency ripple seen on the output voltage. These requirements can be balanced by appropriate selection of the current limit, as discussed in the *Setting the Current Limit* section. Table 1 lists some low-ESR capacitor suppliers. See the Output Voltage Ripple graph in the *Typical Operating Characteristics* section.

Input Bypass Capacitor

Although the output current of many MAX629 applications may be relatively small, the input must be designed to withstand current transients equal to the inductor current limit. The input bypass capacitor reduces the peak currents drawn from the voltage source, and reduces noise caused by the MAX629's switching action. The input source impedance determines the size of the capacitor required at the input (V_{IN}). As with the output filter capacitor, a low-ESR capacitor is recommended. A 10µF, low-ESR capacitor is adequate for most applications, although smaller bypass capacitors may also be acceptable. Bypass the IC separately with a 0.1µF ceramic capacitor placed as close as possible to the V_{CC} and GND pins.

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
CAPACITORS		
AVX: TPS series	(803) 946-0690	(803) 626-3123
Matsuo: 267 series	(714) 969-2491	(714) 960-6492
Sprague: 595D series	(603) 224-1961	(603) 224-1430
DIODES		
Motorola: MBR0530L	(602) 303-5454	(602) 994-6430
Nihon: EC11 FS1 series	(805) 867-2555	(805) 867-2698
INDUCTORS		
Coilcraft: DO1608 and DT1608 series	(847) 639-6400	(847) 639-1469
Murata-Erie: LQH4 series	(814) 237-1431	(814) 238-0490
Sumida: CD43, CD54, and CDRH62B series	(847) 956-0666	(847) 956-0702
TDK: NLC565050 series	(847) 390-4373	(847) 390-4428

Reference Capacitor

Bypass REF to GND with a 0.1µF ceramic capacitor for REF currents up to 10µA. REF can source up to 100µA of current for external loads. For $10\mu A \le I_{REF} \le 100\mu A$, bypass REF with a 0.47µF capacitor.

Feed-Forward Capacitor

Parallel a capacitor (C_F) across R1 to compensate the feedback loop and ensure stability (Figures 2 and 3). Values up to 270pF are recommended for most applications. Choose the lowest capacitor value that ensures stability; high capacitance values may degrade line regulation.

Applications Information

Adjusting the Output Voltage

Many biasing applications require an adjustable output voltage, which is easily obtained using the configuration in Figure 4. In this circuit, an external bias voltage (which may be generated by a potentiometer, a DAC, or other means) is coupled to FB through the resistor R_B. The output voltage of this circuit is given by:

$$V_{OUT} = V_{INIT} + \frac{R1}{R_B}(V_{FB} - V_{BIAS})$$

where V_{INIT} is the fixed output voltage as calculated in the section *Setting the Output Voltage*, and V_{FB} is equal to either V_{REF} (1.25V) for the positive configuration or 0V for the negative configuration. Proper choice of R_B provides a wide range of available output voltages using simple external components to generate V_{BIAS}.

Input Voltage Range

Although, in many cases, the MAX629 and the inductor are powered from the same source, it is often advantageous in battery-powered applications to power the device from an available regulated supply and to power the inductor directly from a battery. The MAX629 requires a +2.7V to +5.5V supply at V_{CC}, but the inductor can be powered from as low as +0.8V, significantly

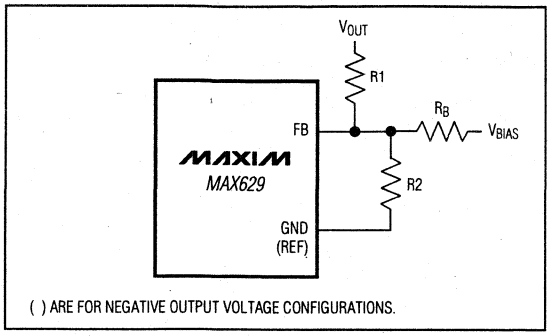


Figure 4. Adjustable Output Voltage

increasing usable battery life. Using separate supplies for V_{CC} and V_{IN} also reduces noise injection onto V_{CC} by isolating it from the switching transients, allowing a smaller, less-expensive input filter capacitor to be used in many applications. If input voltages below 2V will be common, reducing the inductor to 22µH may improve performance in this voltage range, at the potential cost of some decrease in maximum load current and efficiency.

In the negative configuration shown in Figure 3, the inverting charge pump injects current into LX with each cycle. The amount of charge injected increases at higher V_{IN}, and may prematurely trip the internal current-limit threshold. Resistor R3 increases the usable input voltage range by limiting the peak injected current. The 2Ω resistor shown provides a usable input voltage range beyond V_{IN} = 15V. In applications with a different input voltage range, R3 may be increased or decreased as necessary, with a resulting efficiency change of roughly 0.5%/Ω.

Layout Considerations

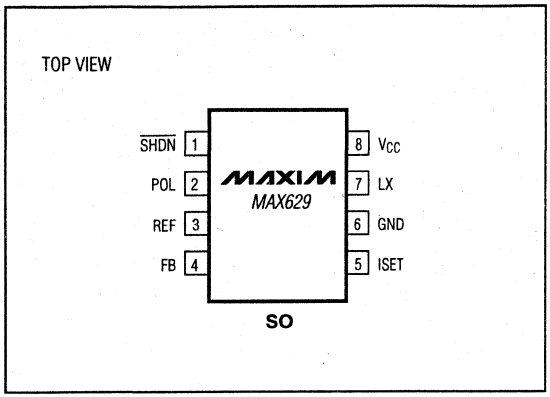
Proper PC board layout is essential due to high current levels and fast switching waveforms that radiate noise. It is recommended that initial prototyping be performed using the MAX629 evaluation kit or equivalent PC board-based design. Breadboards or proto-boards should never be used when prototyping switching regulators.

It is important to connect the GND pin, the input bypass-capacitor ground lead, and the output filter-capacitor ground lead to a single point (star ground configuration) to minimize ground noise and improve regulation. Also, minimize lead lengths to reduce stray capacitance, trace resistance, and radiated noise, with preference given to the feedback circuit, the ground circuit, and LX. Place R1 and R2 as close to the feedback pin as possible. Place the input bypass capacitor as close as possible to V_{CC} and GND.

Refer to the MAX629 evaluation kit data sheet for an example of proper board layout.

28V, Low-Power, High-Voltage, Boost or Inverting DC-DC Converter

Pin Configuration



Chip Information

TRANSISTOR COUNT: 653

SUBSTRATE CONNECTED TO GND

19-1217; Rev 0; 4/97

MAXIM

Regulated 3.3V Charge Pump

General Description

The MAX679 step-up, regulated charge pump generates a 3.3V ±4% output voltage from a 1.8V to 3.6V input voltage (two alkaline, NiCd, or NiMH; or one Lithium-Ion battery). Output current is 20mA (min) from a 2.0V input. Only three external capacitors are needed to build a complete DC-DC converter.

The MAX679's switching frequency is pin selectable at 330kHz or 1MHz to allow trade-offs between lowest supply current and smallest-size capacitors. The logic shutdown function reduces the supply current to 5µA (max) and disconnects the load from the input. Special soft-start circuitry prevents excessive current from being drawn from the battery during start-up. This DC-DC converter requires no inductors and has low EMI. It is available in the ultra-small µMAX package, which is only 1.11mm high and half the area of an 8-pin SO.

Features

- **Regulated 3.3V ±4% Output**
- **Ultra-Small: 1.1mm-High, 8-Pin µMAX Package**
- **No Inductors Required**
- **Up to 1MHz Operation (small external components)**
- **Fits into 0.05 in.²**
- **Up to 85% Efficiency**
- **1.8V to 3.6V Input Voltage Range**
- **50µA Quiescent Supply Current**
- **1µA Shutdown Current**

Applications

Battery-Powered Applications

Miniature Equipment

Backup-Battery Boost Converters

Translators

Two-Way Pagers

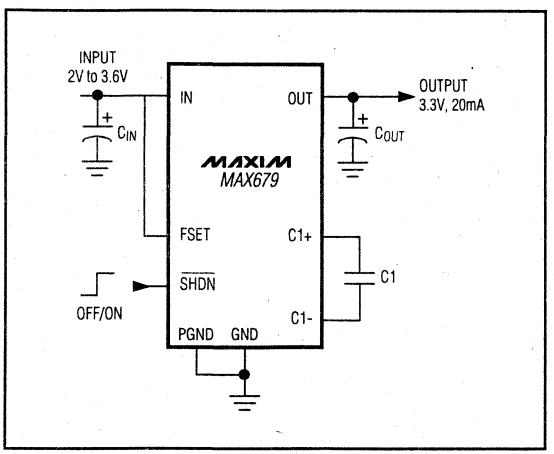
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX679C/D	0°C to +70°C	Dice*
MAX679EUA	-40°C to +85°C	8 µMAX

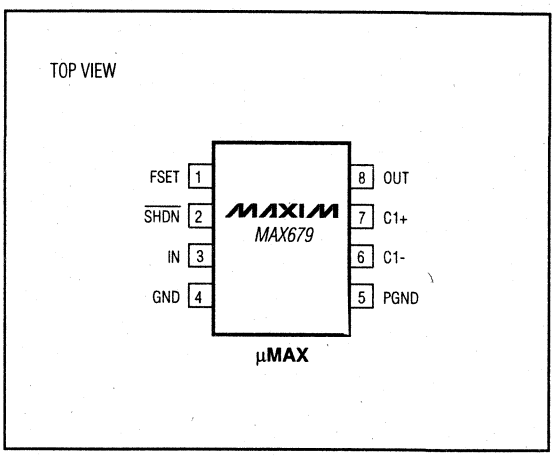
*Dice are tested at T_A = +25°C only.

4

Typical Operating Circuit



Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

Regulated 3.3V Charge Pump

ABSOLUTE MAXIMUM RATINGS

IN, OUT, $\overline{SHDN}$, FSET to GND .....-0.3V to 6V
PGND to GND .....±0.3V
C1- to GND .....-0.3V to (V_{IN} + 0.3V)
C1+ to GND .....-0.3V to (V_{OUT} + 0.3V)
OUT Short to GND 10sec

Continuous Power Dissipation (T_A = +70°C)
μMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = $V_{\overline{SHDN}}$ = V_{FSET} = 2V, C_{IN} = 4.7μF, C1 = 0.33μF, C_{OUT} = 10μF, **T_A = -40°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

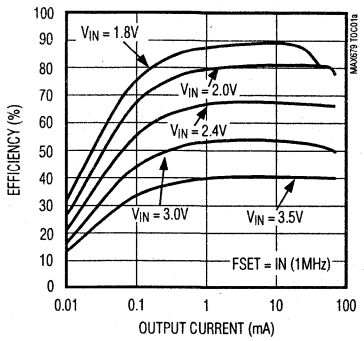
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage			1.8		3.6	V
Input Undervoltage Lockout Voltage			0.8		1.6	V
Output Voltage	2V < V_{IN} < 3.3V, 0mA < I_{OUT} < 20mA	T_A = 0°C to +85°C	3.17	3.3	3.43	V
		T_A = -40°C to +85°C	3.15		3.45	
Output Current	V_{IN} = 1.8V, V_{OUT} > 3.17V			20		mA
No-Load Supply Current	V_{IN} = 2.5V, FSET = IN or GND			50	80	μA
Leakage Current into OUT in Shutdown	V_{OUT} = 3.6V, $\overline{SHDN}$ = GND			15	25	μA
Supply Current in Shutdown	V_{IN} = 3.3V			1	5	μA
FSET, $\overline{SHDN}$ Input Voltage Low	V_{IN} = 1.8V			0.5 x V_{IN}	0.3 x V_{IN}	V
FSET, $\overline{SHDN}$ Input Voltage High	V_{IN} = 3.6V		0.7 x V_{IN}	0.5 x V_{IN}		V
FSET, $\overline{SHDN}$ Input Leakage Current	FSET, $\overline{SHDN}$ = GND or V_{IN}			0.1	1	μA
Switching Frequency	FSET = GND		260	330	450	kHz
	FSET = IN		700	1000	1300	
Output Short-Circuit Current	OUT = GND, V_{IN} = 3.3V			100	200	mA
Efficiency	V_{IN} = 2V, I_{OUT} = 10mA			80		%

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

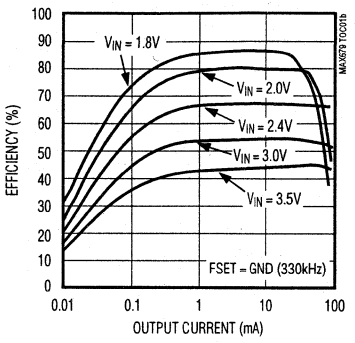
Typical Operating Characteristics

(Typical Operating Circuit with: V_{IN} = $V_{\overline{SHDN}}$ = 2V, C_{IN} = 4.7µF, C1 = 0.33µF, C_{OUT} = 10µF, tested in-circuit, T_A = +25°C, unless otherwise noted.)

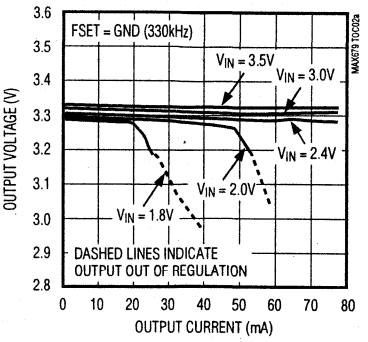
EFFICIENCY vs. OUTPUT CURRENT



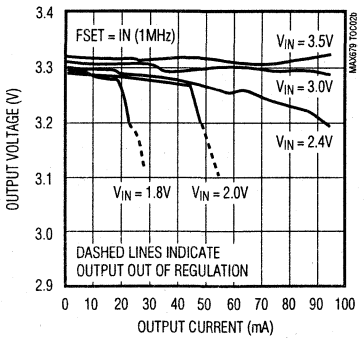
EFFICIENCY vs. OUTPUT CURRENT



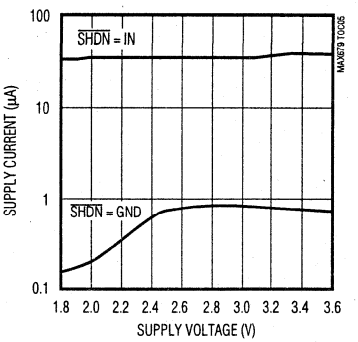
OUTPUT VOLTAGE vs. OUTPUT CURRENT



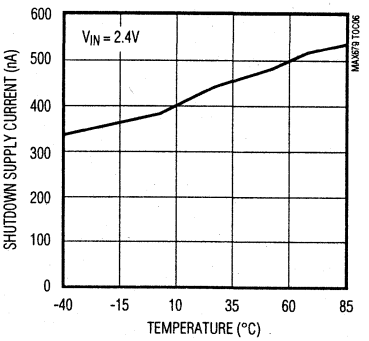
OUTPUT VOLTAGE vs. OUTPUT CURRENT



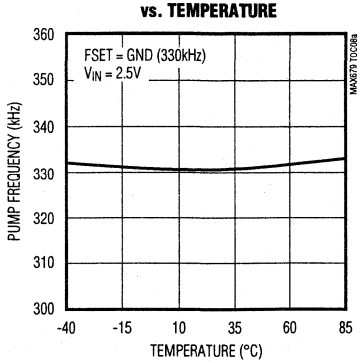
SUPPLY CURRENT vs. SUPPLY VOLTAGE



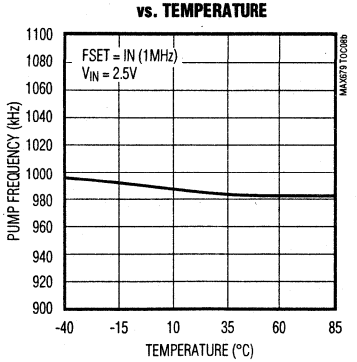
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



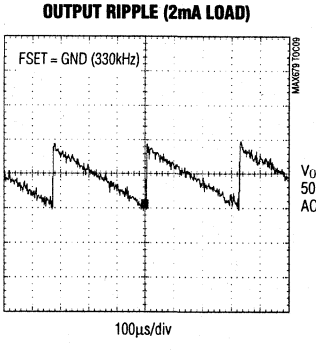
PUMP FREQUENCY vs. TEMPERATURE



PUMP FREQUENCY vs. TEMPERATURE



OUTPUT RIPPLE (2mA LOAD)

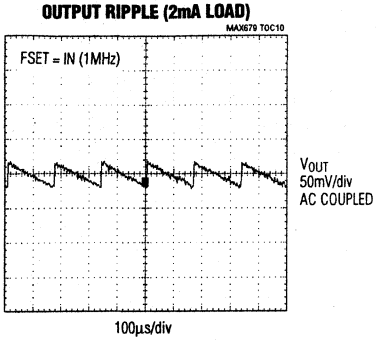


Regulated 3.3V Charge Pump

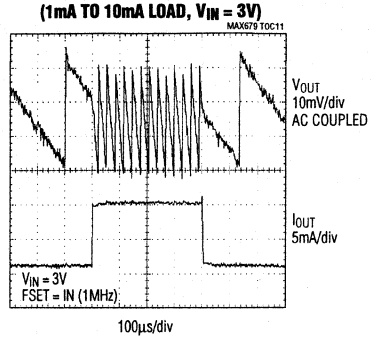
Typical Operating Characteristics (continued)

(Typical Operating Circuit with: V_{IN} = $V_{\overline{SHDN}}$ = 2V, C_{IN} = 4.7µF, C1 = 0.33µF, C_{OUT} = 10µF, tested in-circuit, T_A = +25°C, unless otherwise noted.)

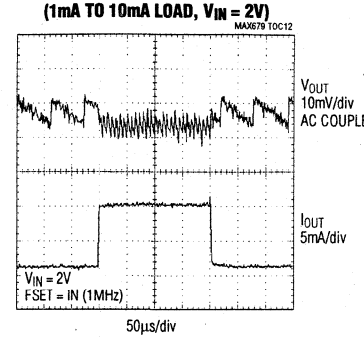
OUTPUT RIPPLE (2mA LOAD)



LOAD-TRANSIENT RESPONSE (1mA TO 10mA LOAD, V_{IN} = 3V)



LOAD-TRANSIENT RESPONSE (1mA TO 10mA LOAD, V_{IN} = 2V)



Pin Description

PIN	NAME	FUNCTION
1	FSET	Set Charge-Pump Frequency Input. FSET = GND selects 330kHz and FSET = IN selects 1MHz. Do not leave FSET unconnected.
2	$\overline{SHDN}$	Shutdown Input. The device shuts down, the output disconnects from the input, and the supply current decreases to 1µA when $\overline{SHDN}$ is a logic low. Connect $\overline{SHDN}$ to IN for normal operation.
3	IN	Supply Input. Connect to an input supply in the 1.8V to 3.6V range. Bypass IN to GND with a (C_{OUT} / 2)µF capacitor.
4	GND	Ground. Analog ground for internal reference and control circuitry.
5	PGND	Power Ground. Charge-pump current flows through this pin.
6	C1-	Negative Terminal of the Charge-Pump Capacitor
7	C1+	Positive Terminal of the Charge-Pump Capacitor
8	OUT	3.3V Power Output. Bypass OUT to GND with an output filter capacitor (see the *Design Procedure* section).

Detailed Description

The MAX679 regulated charge pump has a 50% duty-cycle clock. In phase one (charge phase), the charge-transfer capacitor (C1) charges to the input voltage, and output current is delivered by the output filter capacitor (C_{OUT}). In phase two (transfer phase), C1 is placed in series with the input and connects to the output, transferring its charge to C_{OUT}. If the clock were to run continuously, this process would eventually generate an output voltage equal to two times the input voltage (hence the name "doubler").

The charge pump regulates by gating the oscillator on and off as needed to maintain output regulation. This method has low quiescent current, but to achieve acceptable output ripple, C1 must be significantly lower in value than C_{OUT}.

Start-Up Sequence

The MAX679 soft-start circuitry prevents excessive current from being drawn from the battery at start-up or when the output is shorted. This is done by limiting the charge pump to 1/10 the normal current until either the output is in regulation or the first 4096 charge-pump

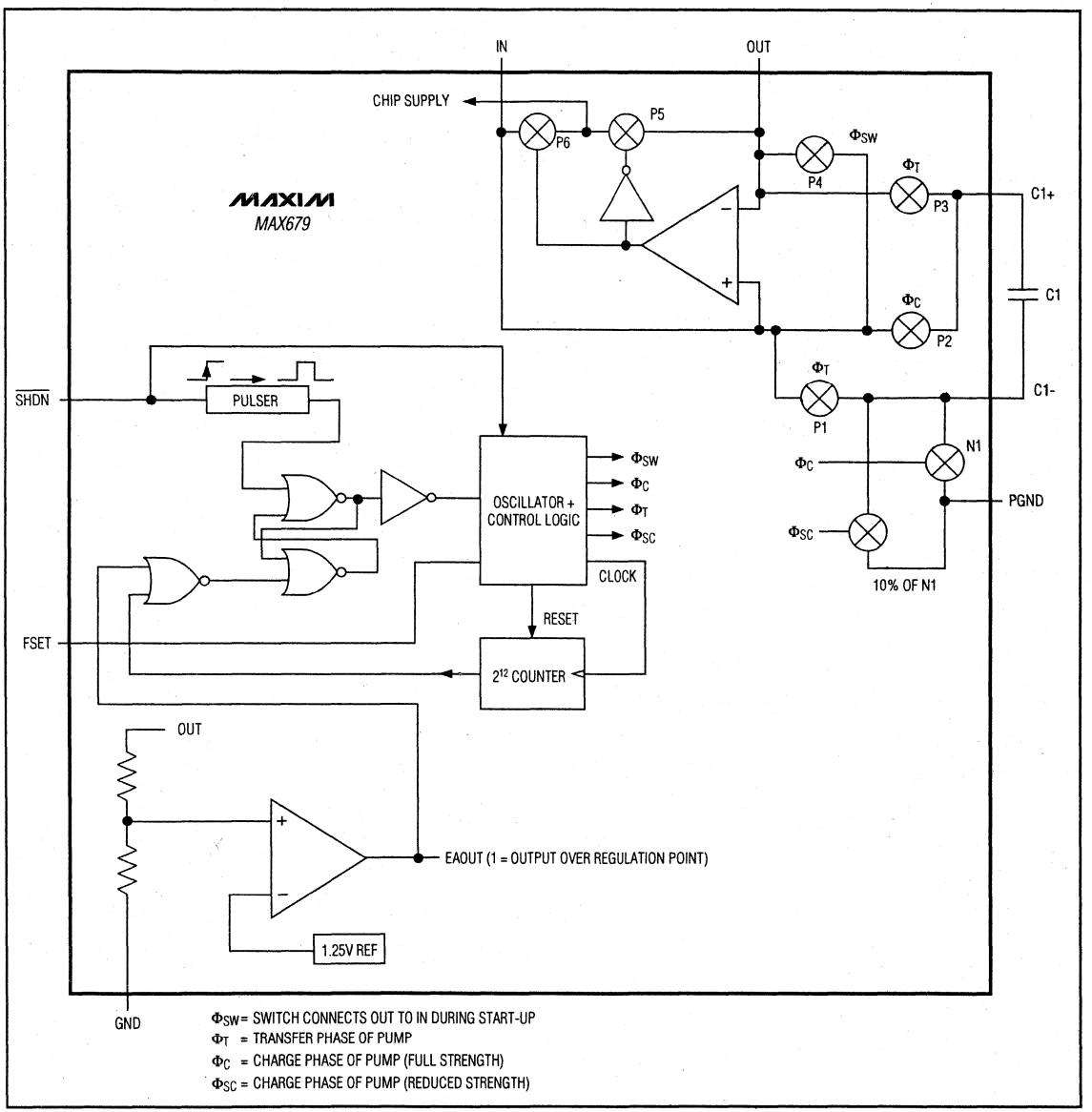


Figure 1. Block Diagram

Regulated 3.3V Charge Pump

cycles (about 4ms) have elapsed. The start-up sequence begins at power-up, when exiting shutdown, or when recovering from a short circuit. If V_{IN} is less than the 1.6V UVLO threshold, the device remains shut down and ignores a high $\overline{SHDN}$ input.

Design Procedure

Optimize the charge-pump circuit for size, quiescent current, and output ripple by properly selecting the operating frequency and capacitors C_{IN}, C1, and C_{OUT}.

For lowest output ripple, select 1MHz operation (FSET = IN). In addition, increasing C_{OUT} relative to C1 will further reduce ripple. For highest efficiency, select 330kHz operation (FSET = GND) and select the largest practical values for C_{OUT} and C1 while maintaining a 30-to-1 ratio. See Table 1 for some suggested values and the resulting output ripple.

Note that the capacitors must have low ESR (<20mΩ) to maintain low ripple. Currently, only ceramic capacitors can provide such low ESR; therefore, the output filter capacitors should be a combination of a 1µF ceramic capacitor and a 10µF tantalum capacitor.

Smallest Size

Set the frequency to 1MHz by connecting FSET to IN. Table 1 shows typical external component values.

Table 1. External Component Selection

V_{IN} (V)	C1 (µF)	C_{OUT} (µF)	FSET (Hz)	Vp-p (mV)
2	0.33	10	1M	7
2	0.33	10	330k	14
2	0.1	3.3	1M	16
2	0.1	3.3	330k	22
3	0.33	10	1M	27
3	0.33	10	330k	56
3	0.1	3.3	1M	72
3	0.1	3.3	330k	89

PC Board Layout

Place C1, C_{OUT}, and C_{IN} close to the IC. Connect PGND and GND with a short trace.

Efficiency

Charge-pump efficiency is best at low frequency (330kHz). The theoretical maximum efficiency is given in the following equation:

Theoretical maximum efficiency = V_{OUT} / (2 x V_{IN})

Gate-charge losses amount to approximately 1mA from the output at full switching frequency (about 5% to 7% loss).

Table 2. Manufacturers of Low-ESR Capacitors

PRODUCTION METHOD	MANUFACTURER	CAPACITORS	PHONE	FAX
Surface-Mount Tantalum Capacitors	AVX	TPS series	(803) 946-0690	(803) 626-3123
	Matsuo	267 series	(714) 969-2491	(714) 960-6492
	Sprague	593D, 595D series	(603) 224-1961	(603) 224-1430
Surface-Mount Ceramic Capacitors	AVX	X7R	(803) 946-0690	(803) 626-3123
	Matsuo	X7R	(714) 969-2491	(714) 960-6492

Chip Information

TRANSISTOR COUNT: 819

SUBSTRATE CONNECTED TO GND

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

3.3V to Regulated 5V Charge Pumps

General Description

The MAX682/MAX683/MAX684 generate a regulated 5V output voltage from 3V to 5.5V inputs. Only three capacitors are required to build a complete DC-DC converter. These devices use a regulating charge-pump doubler to generate a minimum of 50mA, 100mA, and 200mA, respectively. High switching frequency (up to 2MHz) and a unique regulation scheme permit the use of capacitors as small as 1µF per 100mA of load current.

The MAX682/MAX683/MAX684's voltage conversion requires no inductors, so the application circuits are small and low cost. The switching frequency is set using an external resistor. These DC-DC converters can be set by pin programming for either low-quiescent-current or low-noise operation. In logic-controlled shutdown, the input is disconnected from the load.

Features

- ♦ **Ultra-Small Size: 1µF Capacitor/100mA Load**
- ♦ **No Inductors Required**
- ♦ **1.1mm-High µMAX Package (MAX683/MAX684)**
- ♦ **50mA (MAX684), 100mA (MAX683), or 200mA (MAX682) Output Current**
- ♦ **Regulated 5V ±4% Output Voltage**
- ♦ **50kHz to 2MHz Switching Frequency**
- ♦ **3V to 5.5V Input Voltage**
- ♦ **5µA (max) Shutdown Current**
- ♦ **Low Quiescent Current (100µA) or Low-Noise Constant-Frequency Operation**
- ♦ **Load Disconnected from Input in Shutdown**

Applications

PCMCIA Cards

Flash Memory Supplies

Battery-Powered Applications

3.3V to 5V Local Conversion Applications

Miniature Equipment

Local 3.3V to 5V Supplies

3V to 5V GSM SIMM Cards

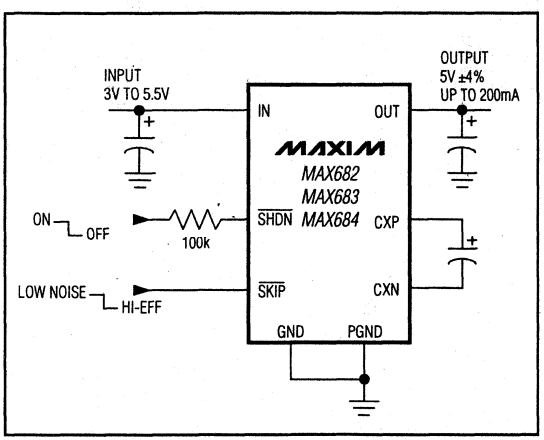
Backup-Battery Boost Converters

Ordering Information

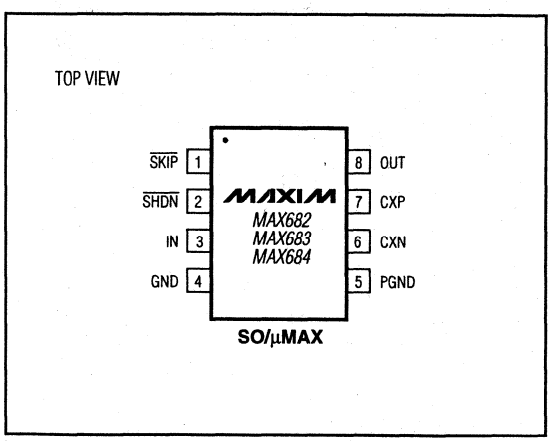
PART	TEMP. RANGE	PIN-PACKAGE
MAX682C/D	0°C to +70°C	Dice*
MAX682ESA	-40°C to +85°C	8 SO
MAX683C/D	0°C to +70°C	Dice*
MAX683EUA	-40°C to +85°C	8 µMAX
MAX684C/D	0°C to +70°C	Dice*
MAX684EUA	-40°C to +85°C	8 µMAX

**Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Noise, Dual-Output (Positive and Negative) DC-DC Converter for CCD and LCD

General Description

The MAX685 DC-DC converter provides low-noise dual outputs for powering CCD imaging devices and LCDs. This device uses a single inductor to provide independently regulated boosted and negative outputs. Integrated power switches are included in the small, 16-pin QSOP package (same size as an 8-pin SO) to save space and reduce cost.

Each output delivers up to 10mA from a 2.7V to 5.5V input. Output voltages are set independently up to 24V and down to -9V. With a few additional low-cost components, the output voltages can be set at up to 45V and down to -16V. Output ripple magnitude is 40mVp-p. The MAX685 uses a fixed-frequency, pulse-width-modulated (PWM) control scheme at 220kHz or 400kHz to permit output noise filtering and to reduce the size of external components. The frequency can also be synchronized to an external clock signal between 200kHz and 480kHz.

The MAX685 has a power-OK indicator output (POK) that signals when the outputs are within regulation. A logic-controlled shutdown turns off the outputs and reduces supply current to 0.1µA. The user can also set which output turns on first.

The preassembled MAX685 evaluation kit is available to reduce design time.

Features

- ♦ **Dual Output Using a Single Inductor**
- ♦ **Internal Switches in a Small Package**
- ♦ **Low-Noise Output, 40mVp-p Ripple**
- ♦ **Output Voltages up to 24V and down to -9V**
- ♦ **Output Voltages up to 45V and down to -16V (with added components)**
- ♦ **220kHz/400kHz Fixed-Frequency PWM Operation**
- ♦ **Frequency Synchronized to External Clock**
- ♦ **Power-OK Indicator**
- ♦ **Power-On Sequencing Select**
- ♦ **0.1µA Logic-Controlled Shutdown**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX685C/D	0°C to +70°C	Dice
MAX685EEE	-40°C to +85°C	16 QSOP

Applications

Camcorders

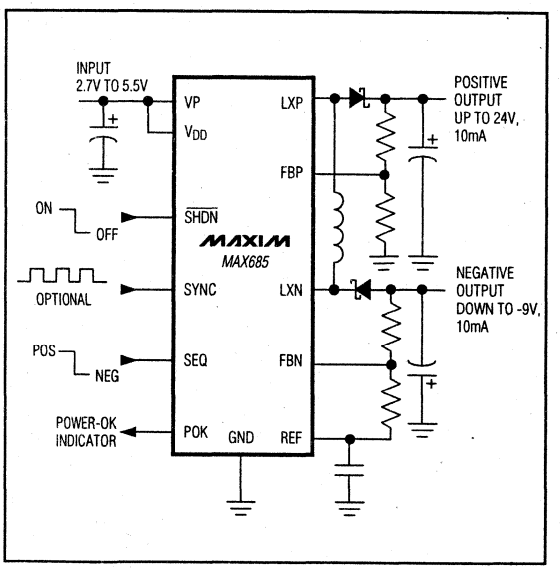
Digital Cameras

Notebooks

LCDs

CCD Imaging Devices

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

MAXIM

DAC-Controlled Boost or Inverter LCD Bias Supply with 28V Internal Switch

General Description

The MAX686 converts a positive input voltage to a positive or negative LCD bias voltage. The output can be boosted to any voltage up to +27.5V (or inverted down to -27.5V) that is higher than the input. The device features an internal N-channel MOSFET switch, programmable current limiting, and an internal 6-bit digital-to-analog converter (DAC) for digital adjustment of the output voltage. It comes in a small, 16-pin QSOP package (same size as an 8-pin SO).

The MAX686 uses a current-limited pulse-frequency-modulation (PFM) control scheme to provide high efficiency over a wide range of load conditions. Its high switching frequency (up to 300kHz) allows the use of small external components.

The $\overline{\text{LCDON}}$ pin option allows the LCD bias voltage to be automatically disabled when the display logic voltage is removed, protecting the display. The MAX686 has a 2.7V to 5.5V input voltage range for the IC, and a 0.8V to 27.5V input voltage range for the inductor. Shutdown current is 1.5µA.

The MAX686 offers integration in a small package to save space, and low power consumption and high efficiency to increase battery life, making it an excellent choice for battery-powered portable equipment. The MAX629 is similar to the MAX686, except that it does not contain a built-in DAC. Both devices have evaluation kits to facilitate designs.

Applications

Positive or Negative LCD Bias

Personal Digital Assistants

Notebook Computers

Portable Data-Collection Terminals

Palmtop Computers

Varactor-Tuning Diode Bias

Features

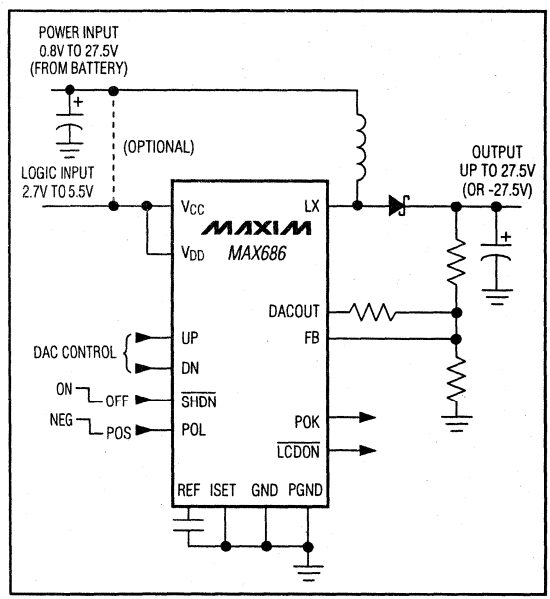
- **Internal 500mA, 28V N-Channel Switch (no external FET required)**
- **Small 16-Pin QSOP Package**
- **Adjustable Output Voltage to +27.5V or -27.5V**
- **6-Bit DAC-Controlled Output Voltage**
- **90% Efficiency**
- **Power-OK Indicator**
- **Low Quiescent Supply Current**
- **1.5µA Shutdown Current**
- **Up to 300kHz Switching Frequency**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX686C/D	0°C to +70°C	Dice*
MAX686EEE	-40°C to +85°C	16 QSOP

**Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

19-1254; Rev 0; 7/97

EVALUATION KIT AVAILABLE

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

General Description

The MAX710/MAX711 integrate a step-up DC-DC converter with a linear regulator to provide step-up/down voltage conversion. They are optimized for battery applications where the input varies above and below the regulated output voltage. They have an input range from +1.8V to +11V. Typical efficiency when boosting battery inputs is 85%.

The MAX710/MAX711 can be configured for minimum noise or optimum efficiency. Shutdown control turns off the part completely, disconnecting the input from the output (I_{SHDN} = 0.2µA). Standby control turns off only the step-up converter and leaves the low-power linear regulator active (I_Q = 7µA).

The MAX710 has a preset 3.3V or 5V output voltage. The MAX711 has an adjustable output that can be set from +2.7V to +5.5V with two resistors. Both devices come in 16-pin narrow SO packages.

Applications

Single-Cell, Lithium-Powered Portable Devices

Digital Cameras

2- to 4-Cell AA Alkaline Hand-Held Equipment

3.3V and Other Low-Voltage Systems

2-, 3-, and 4-Cell Battery-Powered Equipment

Battery-Powered Devices with AC Input Adapters

Features

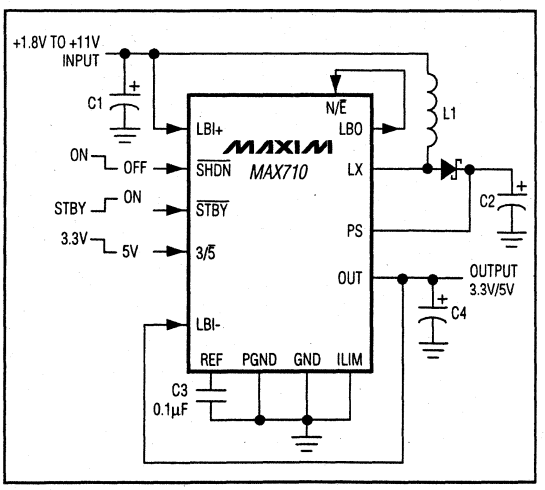
- **Step-Up/Down Voltage Conversion**
- **+1.8V to +11V Input Range**
- **Output:**
  5V/250mA at V_{IN} = 1.8V
  5V/500mA at V_{IN} = 3.6V
- **No External FETs Required**
- **Load Disconnected from Input in Shutdown**
- **Battery Drain:**
  200µA No-Load (V_{IN} = 4V)
  7µA in Standby
  0.2µA when Off
- **Low-Noise and High-Efficiency Modes**

Ordering Information

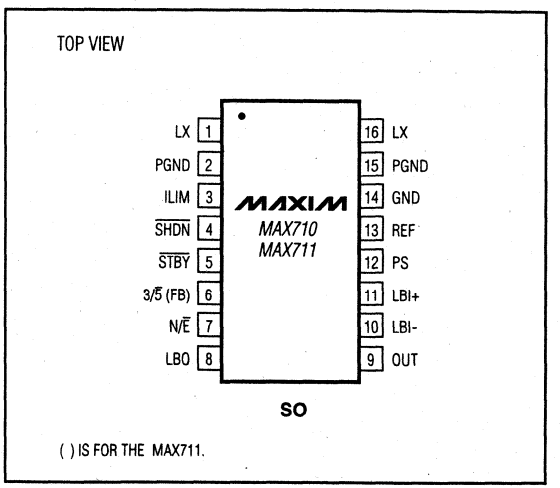
PART	TEMP. RANGE	PIN-PACKAGE
MAX710C/D	0°C to +70°C	Dice
MAX710ESE	-40°C to +85°C	16 Narrow SO
MAX711C/D	0°C to +70°C	Dice
MAX711ESE	-40°C to +85°C	16 Narrow SO

4

Typical Operating Circuit



Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

PS, LX, OUT to GND ..... -0.3V to +11.5V
ILIM, $\overline{SHDN}$, $\overline{STBY}$, FB, 3/$\overline{5}$, N/$\overline{E}$, LBO,
LBI-, LBI+, REF to GND ..... -0.3V to (V_{PS} + 0.3V)
PGND to GND ..... -0.3V to +0.3V
REF Short Circuit to GND ..... Continuous
I_{OUT} 700mA

Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{PS} = 5.6V, $\overline{STBY}$ = PS, C_{REF} = 0.1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	N/$\overline{E}$ = PS		1.8		11.0	V
	N/$\overline{E}$ = GND (Note 2)		1.8		7.0	
Full Load Start-Up Voltage				0.9		V
Output Voltage (MAX710)	3/$\overline{5}$ = low, I_{OUT} = 0 to 250mA	T_A = 0°C to +85°C	4.8	5.0	5.2	V
		T_A = -40°C to +85°C	4.6	5.0	5.3	
	3/$\overline{5}$ = high, I_{OUT} = 0 to 250mA, V_{PS} = 4.7V	T_A = 0°C to +85°C	3.17	3.3	3.43	
		T_A = -40°C to +85°C	3.05	3.3	3.55	
Output Voltage-Adjustment Range	MAX711		FB		5.5	V
Output Voltage Load Regulation	0 < I_{OUT} < 250mA, $\overline{STBY}$ = PS			0.5		%
Output Voltage Line Regulation	$\overline{STBY}$ = PS, 1.8V to 5V			0.3		%/V
Quiescent Current	$V_{\overline{STBY}}$ = $V_{\overline{SHDN}}$ = logic high, current measured into PS pin; I_{LOAD} = 0			100	140	µA
Standby Quiescent Current	$V_{\overline{STBY}}$ = 0V			7	16	µA
Shutdown Quiescent Current	$V_{\overline{SHDN}}$ = 0V			0.1	5	µA
Reference Voltage	T_A = 0°C to +85°C, I_{REF} = 0		1.24	1.28	1.31	V
	T_A = -40°C to +85°C, I_{REF} = 0		1.23	1.28	1.32	
Standby Output Current	$V_{\overline{STBY}}$ = 0V, linear regulator				10	mA
FB Voltage	MAX711, OUT = FB	T_A = 0°C to +85°C	1.20	1.25	1.29	mV
		T_A = -40°C to +85°C	1.18	1.25	1.31	
Load Regulation	MAX711, OUT = FB	0mA ≤ I_{LOAD} ≤ 250mA		0.1	1	%
FB Input Current	FB = 1.25V			1	50	nA
LX On-Resistance	V_{PS} = 5.6V			0.2	0.6	Ω
	MAX710, V_{PS} = 3.7V			0.3	0.9	
	MAX711, V_{PS} = 2.7V			0.6	1.2	
LX Leakage Current	V_{LX} = 5.6V			0.1	1	µA
LX Current Limit	ILIM = PS		0.5	0.8	1.3	A
	ILIM = GND		1.1	1.5	1.95	

ELECTRICAL CHARACTERISTICS (continued)

(V_{PS} = 5.6V, $\overline{STBY}$ = PS, C_{REF} = 0.1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output PFET Resistance	V_{OUT} = 5.0V		0.7	1.3	Ω
	MAX710, V_{OUT} = 3.0V		1.3	2.4	
	MAX711, V_{OUT} = 2.7V		1.6	3.0	
Output PFET Leakage	V_{PS} = 3V, V_{OUT} = 0V		0.4	3	µA
Thermal Shutdown	$\overline{STBY}$ = PS		150		°C
Thermal Shutdown Hysteresis	$\overline{STBY}$ = PS		20		°C
LOGIC					
Input Low Voltage	$\overline{STBY}$, $\overline{SHDN}$, N/$\overline{E}$, 3/$\overline{5}$, ILIM			0.4	V
Input High Voltage	$\overline{STBY}$, $\overline{SHDN}$, N/$\overline{E}$, 3/$\overline{5}$, ILIM	1.6			V
Input Bias Current	$\overline{STBY}$, $\overline{SHDN}$, N/$\overline{E}$, 3/$\overline{5}$, ILIM		1	50	nA
LBI/LBO COMPARATOR					
Input Range LBI-, LBI+	(Note 3)	1.2		10	V
Input Bias Current LBI-, LBI+	V_{LBI-}, V_{LBI+} = 1.25V		1	50	nA
Hysteresis		6	40	100	mV
LBI/LBO Offset Voltage	V_{LBI-} = 1.25V	-25		+25	mV
LBO Output Voltage	I_{LBO} = 2mA, V_{LBI-} = 1.25V, V_{LBI+} = 1V			0.4	V
	I_{LBO} = -300µA, V_{LBI-} = 1.25V, V_{LBI+} = 2V	V_{PS} - 0.2V			

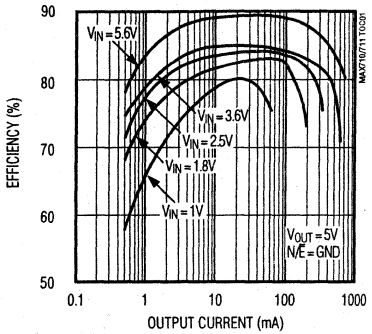
Note 1: Specifications at -40°C are guaranteed by design, not production tested.
Note 2: Guaranteed by design (see Table 1).
Note 3: The LBO comparator provides the correct result as long as one input is within the specified input range.

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

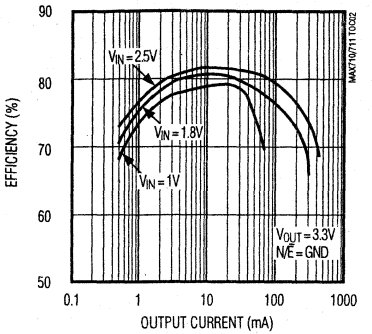
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

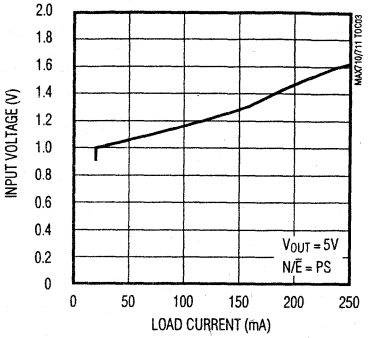
EFFICIENCY vs. OUTPUT CURRENT— HIGH-EFFICIENCY MODE (V_{OUT} = 5V)



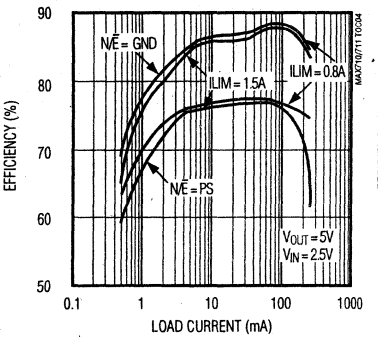
EFFICIENCY vs. OUTPUT CURRENT— HIGH-EFFICIENCY MODE (V_{OUT} = 3.3V)



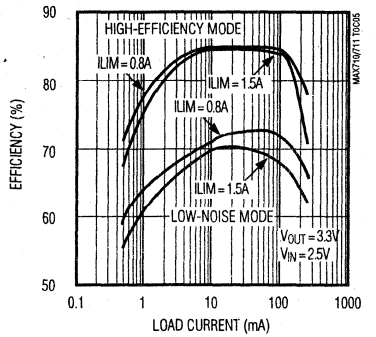
MINIMUM START-UP INPUT VOLTAGE vs. LOAD CURRENT



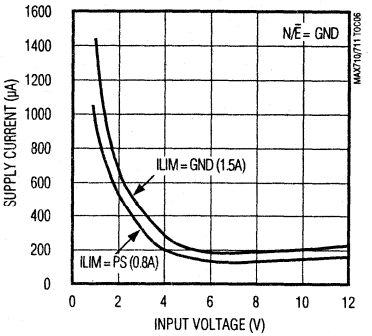
EFFICIENCY vs. LOAD CURRENT— HIGH-EFFICIENCY AND LOW-NOISE MODES (V_{OUT} = 5V)



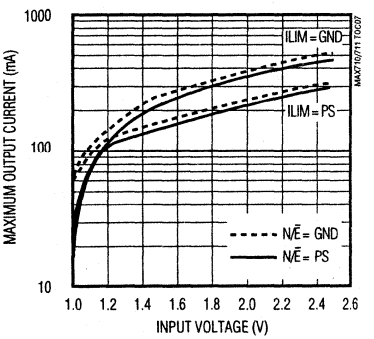
EFFICIENCY vs. LOAD CURRENT— HIGH-EFFICIENCY AND LOW-NOISE MODES (V_{OUT} = 3.3V)



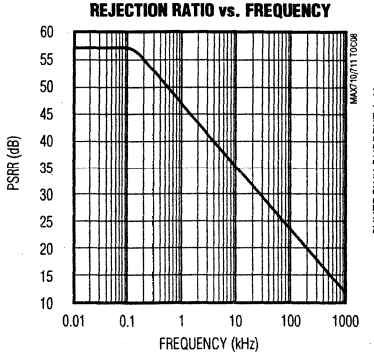
NO-LOAD BATTERY CURRENT vs. INPUT VOLTAGE



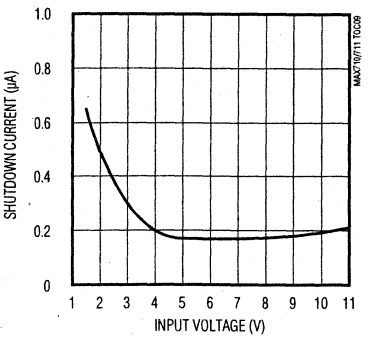
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



LINEAR-REGULATOR POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



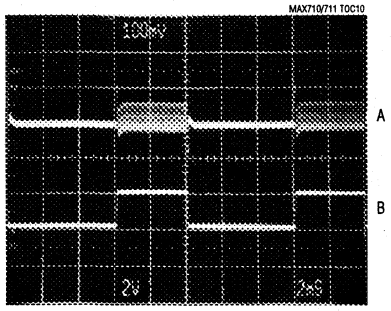
SHUTDOWN CURRENT vs. INPUT VOLTAGE



Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

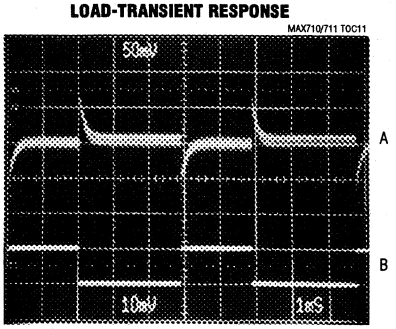
LINE-TRANSIENT RESPONSE



2ms/div

A: V_{OUT} = 3.3V (100mV/div, AC COUPLED), N/$\overline{E}$ = GND
B: V_{IN} = 2V TO 4V, I_{OUT} = 100mA

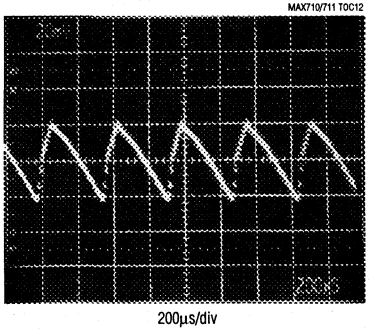
LOAD-TRANSIENT RESPONSE



1ms/div

A: V_{OUT} = 3.3V (50mV/div, AC COUPLED), N/$\overline{E}$ = PS
B: I_{OUT} = 10mA TO 100mA

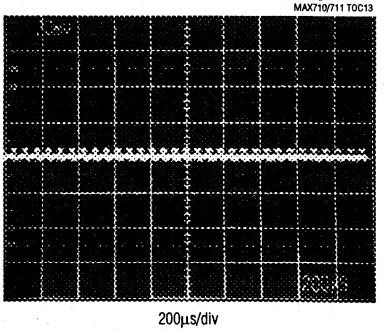
OUTPUT RIPPLE (HIGH-EFFICIENCY MODE)



200µs/div

V_{IN} = 2.5V, I_{OUT} = 20mA, N/$\overline{E}$ = GND
V_{OUT} = 5V (20mV/div, AC COUPLED), I_{OUT} = 20mA

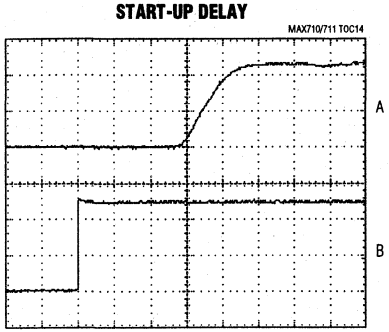
OUTPUT RIPPLE (LOW-NOISE MODE)



200µs/div

V_{IN} = 2.5V, I_{OUT} = 20mA, N/$\overline{E}$ = PS
V_{OUT} = 5V (20mV/div, AC COUPLED), I_{OUT} = 20mA

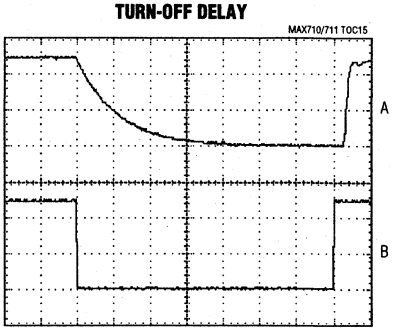
START-UP DELAY



20µs/div

A: V_{OUT} (2V/div), I_{OUT} = 100mA
B: $V_{\overline{SHDN}}$ (2V/div)

TURN-OFF DELAY



200µs/div

A: V_{OUT} (2V/div), I_{OUT} = 100mA
B: $V_{\overline{SHDN}}$ (2V/div)

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

Pin Description

PIN		NAME	FUNCTION
MAX710	MAX711		
1	1	LX	Drain Connection for internal N-channel power MOSFET
2	2	PGND	Power Ground
3	3	ILIM	Inductor Current-Limit-Select Input. Connect to GND for 1.5A limit and to PS for 0.8A limit.
4	4	$\overline{SHDN}$	Shutdown Input. When low, the entire circuit is off and OUT is actively pulled to GND.
5	5	$\overline{STBY}$	Standby Input. Connect to GND to disable boost circuit. Connect to PS for normal operation.
6	—	$3/\overline{5}$	Selects the output voltage. Connect to GND for 5V output and to OUT for 3.3V output.
—	6	FB	Feedback Input
7	7	N/$\overline{E}$	Selects low-noise or high-efficiency mode. Connect to GND for high efficiency and to PS for lowest noise. See *Operating Configurations* section.
8	8	LBO	Low-Battery Comparator Output
9	9	OUT	Linear-Regulator Output. Bypass with a 4.7µF capacitor to GND.
10	10	LBI-	Negative Input to Low-Battery Comparator
11	11	LBI+	Positive Input to Low-Battery Comparator
12	12	PS	Source of internal PFET regulator. The IC is powered from PS.
13	13	REF	1.28V Reference Voltage Output. Bypass with a 0.1µF capacitor to GND.
14	14	GND	Analog Ground. Must be low impedance. Solder directly to ground plane.
15	15	PGND	Power Ground
16	16	LX	Drain Connection for internal N-channel power MOSFET

Detailed Description

The MAX710/MAX711 integrate a step-up DC-DC converter with a linear regulator to provide step-up/down voltage conversion. The step-up switch-mode regulator contains an N-channel power MOSFET switch. It also shares a precision voltage reference with a linear regulator that contains a P-channel MOSFET pass element (Figure 1).

Step-Up Operation

A pulse-frequency-modulation (PFM) control scheme with a constant 1µs off-time and variable on-time controls the N-channel MOSFET switch. The N-channel switch turns off when the part reaches the peak current limit or the 4µs maximum on-time. The ripple frequency is a function of load current and input voltage.

Step-Down Operation

The low-dropout linear regulator consists of a reference, an error amplifier, and a P-channel MOSFET. The reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The difference is conditioned and applied to the P-channel pass transistor's gate.

Operating Configurations

The MAX710/MAX711 have several operating configurations to minimize noise and optimize efficiency for different input voltage ranges. These configurations are accomplished via the N/$\overline{E}$ input, which controls operation of the on-chip linear regulator.

With N/$\overline{E}$ low, the linear regulator behaves as a 0.7Ω (at 5V output) PFET switch when the IC is boosting, and as a conventional linear regulator when $V_{IN} > V_{OUT}$. This provides optimum boost efficiency, but the PFET does little to reject boost-converter output ripple. With N/$\overline{E}$ high, boost ripple rejection is optimized by maintaining headroom (V_{FV}, typically 0.5V at 5V output) across the linear regulator. Boost mode efficiency is then about 10% lower than with N/$\overline{E}$ high.

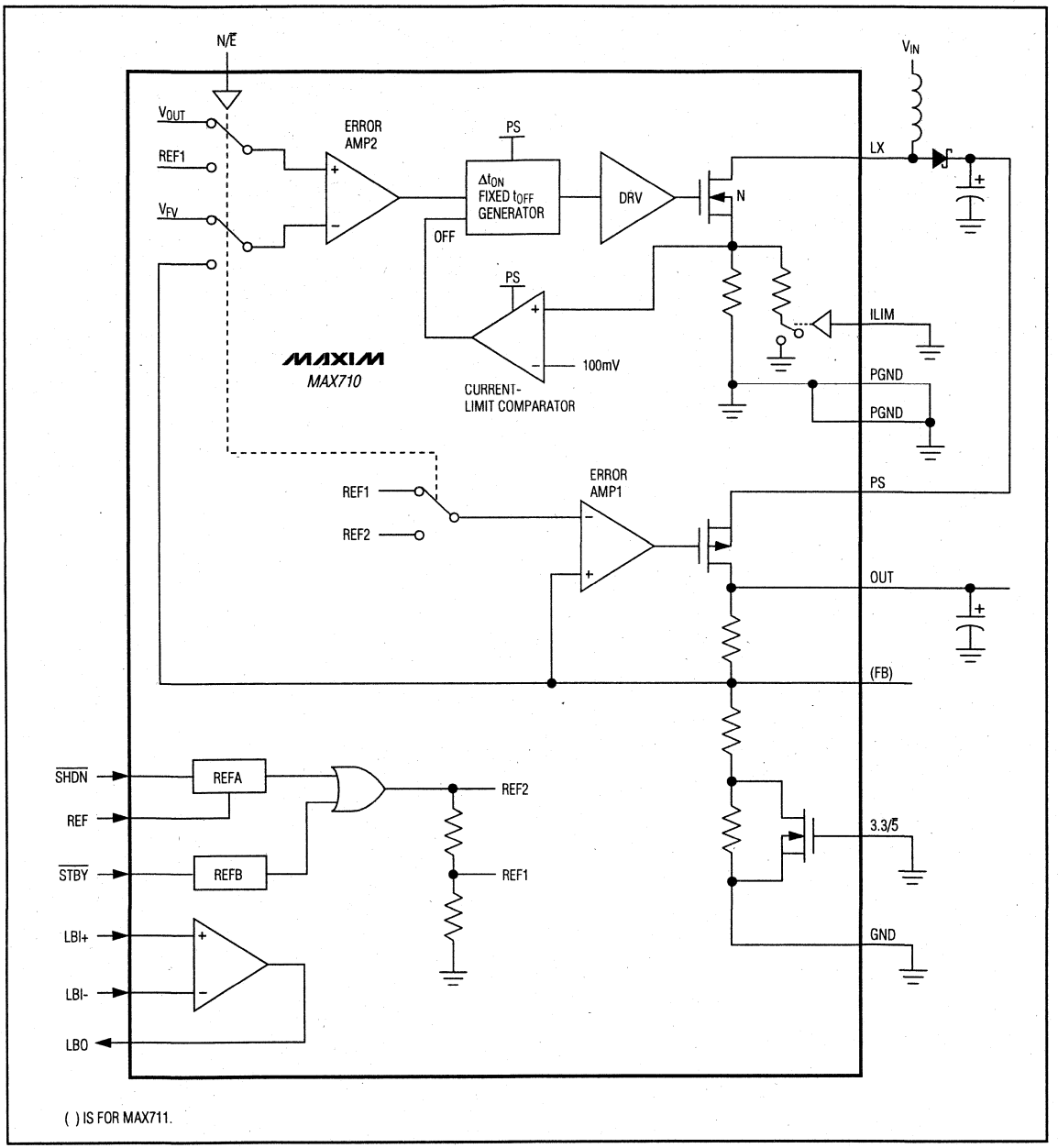


Figure 1. Functional Diagram

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

In high-efficiency mode (N/$\overline{E}$ = low), the maximum input voltage is limited to 7V. This voltage limitation is easily overcome, however, by configuring the LBO output to change modes based on input voltage, allowing an 11V maximum input with high-efficiency configurations. Four operating configurations are described in Table 1 and in the following subsections.

Table 1. Operating Configurations

NO.	DESCRIPTION	INPUT VOLTAGE	CONNECTIONS
1	High efficiency, 7V max V_{IN}	Up to 7V	N/$\overline{E}$ = GND
2	High efficiency, $V_{BATT} < V_{OUT}$ (Figure 2a)	Up to 11V	LBO = N/$\overline{E}$ LBI- = V_{OUT} LBI+ = V_{IN}
3	High efficiency, 11V, $V_{BATT} < 6.5V$ (Figure 2b)	Up to 11V	LBO = N/$\overline{E}$ LBI- = REF LBI+ = R5, R6
4	Low noise	Up to 11V	N/$\overline{E}$ = PS

Configuration 1: High Efficiency, 7V Max V_{IN}

With N/$\overline{E}$ connected to GND, when the IC boosts, the linear regulator operates only as a switch, with minimum forward drop, until $V_{IN} > V_{OUT}$ (where linear regulation begins). This configuration is limited to no more than 7V input, but provides best efficiency for battery-only operation or low-voltage AC adapter usage.

Configuration 2: High Efficiency, $V_{BATT} < V_{OUT}$

In this configuration, N/$\overline{E}$ is driven high by LBO when $V_{IN} > V_{OUT}$ (Figure 2a). When $V_{IN} < V_{OUT}$, the IC boosts, and the linear regulator operates as a switch, with minimum forward drop. When $V_{IN} > V_{OUT}$, the linear regulator operates with V_{FV} forward drop, while V_{PS} increases by V_{FV} so that OUT maintains regulation. V_{FV} is set inside the IC to approximately 0.5V (at 5V V_{OUT}). When V_{IN} is only slightly higher than V_{OUT}, conversion efficiency is poorer than in configuration 1, so configuration 2 is most suitable when the battery voltage is less than V_{OUT}, but the AC adapter output is greater than V_{OUT}.

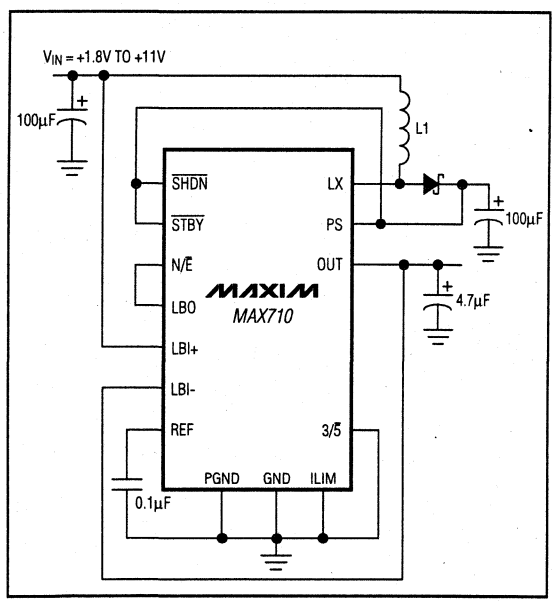


Figure 2a. High-Efficiency Operating Configuration for $V_{BATT} < V_{OUT}$

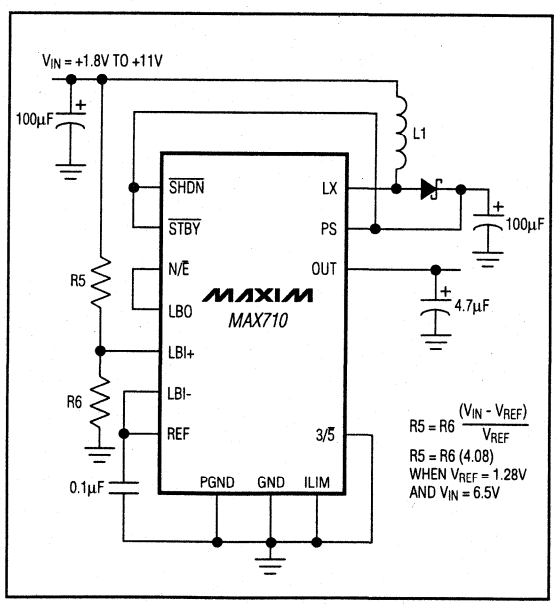


Figure 2b. High-Efficiency Operating Configuration for $V_{BATT} < 6.5V$

Configuration 3: High Efficiency, 11V, V_{BATT} < 6.5V

In this configuration, N/$\overline{E}$ is driven high by LBO when V_{IN} > 6.5V (Figure 2b). When V_{IN} < V_{OUT}, the IC boosts, and the linear regulator operates as a switch, with minimum forward drop. When V_{IN} > V_{OUT}, linear regulation begins. When V_{IN} > 6.5V (set by R5 and R6), the linear regulator forces a minimum forward drop of V_{FV} (typically 0.5V at 5V V_{OUT}) as LBO drives N/$\overline{E}$ high. This transition is not seen at the output, since the linear regulator already has an input-output voltage difference of 6.5V - 5V. Efficiency with V_{IN} slightly higher than V_{OUT} is equal to that of configuration 1, so configuration 3 is most suitable when the battery voltage may be near V_{OUT}. This hookup has no functional shortcomings compared with configuration 2, except that two additional resistors (R5 and R6) are needed.

Configuration 4: Low Noise

With N/$\overline{E}$ connected to PS, when the IC is boosting, the linear regulator operates with V_{FV} forward voltage (typically 0.5V at 5V V_{OUT}) for optimum noise rejection. Linear regulation occurs when V_{IN} > V_{OUT} + V_{FV}. The V_{FV} voltage differential results in boost efficiency typically 10% lower than with the high-efficiency configurations.

ILIM

The current-limit-select input, ILIM, selects between the two peak current limits: 1.5A (ILIM = GND) and 0.8A (ILIM = PS). If the application requires 200mA or less from the MAX710/MAX711, select 0.8A. The lower peak current limit permits the use of smaller, low-cost inductors. The ILIM input is internally diode clamped to GND and PS, and should not be connected to signals outside this range.

Shutdown and Standby Modes

Grounding $\overline{SHDN}$ turns off the MAX710/MAX711 completely, disconnecting the input from the output. Tie $\overline{SHDN}$ to PS for normal operation.

The MAX710/MAX711 have a standby mode that shuts down the step-up converter. The linear regulator remains on with a 7µA (typ) LDO quiescent current. Connect $\overline{STBY}$ to ground to enter standby mode; otherwise, connect $\overline{STBY}$ to PS.

Design Procedure

Output Voltage Selection

For the MAX710, you can obtain a 3.3V or 5V output voltage by tying 3/$\overline{5}$ to GND or PS. Efficiency is typically 85% over a 2mA to 250mA load range. The device is bootstrapped, with power derived from the step-up voltage output (at PS). Under all load conditions, the MAX710/MAX711 typically start up with a 1V input. If the battery voltage exceeds the programmed output voltage, the output will linear regulate down to the selected output voltage.

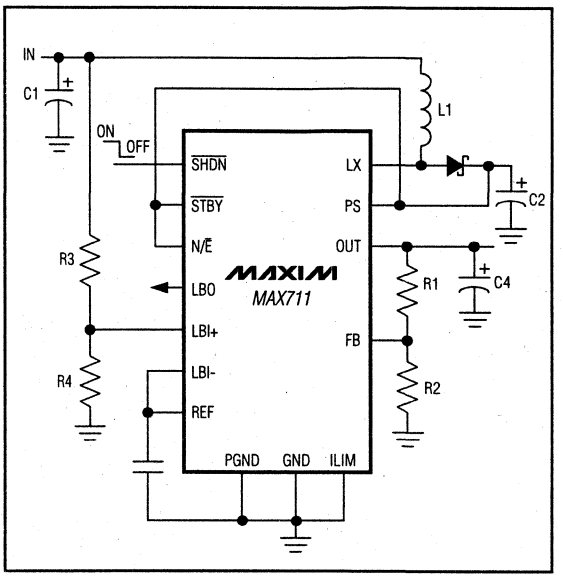


Figure 3. MAX711 Adjustable Output Voltage

The MAX711's adjustable output voltage is set by two resistors, R1 and R2 (Figure 3), which form a voltage divider between the output and FB. Use the following equation to determine the resistor values:

$$R1 = R2\ [(V_{OUT} / V_{REF}) - 1]$$

where V_{REF} = 1.25V.

Since the input bias current at FB has a maximum value of 50nA, R1 and R2 can be large with no significant accuracy loss. Choose R2 in the 100kΩ to 1MΩ range and calculate R1 using the formula above. For 1% error, the current through R1 should be at least 100 times FB's bias current.

Low-Battery Comparator

The MAX710/MAX711 contain a comparator for low-battery detection. If the voltage at LBI+ falls below that at LBI- (typically connected to REF), LBO goes low. Hysteresis is typically 50mV. Set the low-battery monitor's threshold with two resistors, R3 and R4 (Figure 2), using the following equation:

$$R3 = R4\ [(V_{LBT} / V_{LBI-}) - 1]$$

3.3V/5V or Adjustable, Step-Up/Down DC-DC Converters

Table 2. Component Selection

INDUCTORS (L1)	CAPACITORS	RECTIFIERS (D1)
Sumida CD75-220 (1.5A), CDRH-74-220 (1.23A), or CD54-220	100µF, 16V low-ESR tantalum capacitor AVX TPSE107M016R0100 or Sprague 593D107X0016E2W	Schottky diode Motorola MBRS130T3
Coilcraft DO33-08P-223	4.7µF, 16V tantalum capacitor Sprague 595D475X0016A2T	

where V_{LBT} is the desired threshold of the low-battery detector and V_{LBI-} is the voltage applied to the inverting input of the low-battery comparator. Since LBI current is less than 50nA, R3 and R4 can be large (typically 100kΩ to 1MΩ), minimizing input supply loading. If the low-battery comparator is not used, connect LBI+ to PS and LBI- to REF, leaving LBO unconnected.

Inductor Selection

A 22µH inductor value performs well in most MAX710/MAX711 applications. The inductance value is not critical, however, since the MAX710/MAX711 work with inductors in the 18µH to 100µH range. Smaller inductance values typically offer a smaller size for a given series resistance, allowing the smallest overall circuit dimensions. Circuits using larger inductance values exhibit higher output current capability and larger physical dimensions for a given series resistance. The inductor's incremental saturation current rating should be greater than the peak switch-current limit, which is 1.5A for ILIM = GND and 0.8A for ILIM = PS. However, it is generally acceptable to bias most inductors into saturation by as much as 20%, although this slightly reduces efficiency. The inductor's DC resistance significantly affects efficiency. See Tables 2 and 3 for a list of suggested inductors and suppliers.

Capacitor Selection

A 100µF, 16V, 0.1Ω equivalent series resistance (ESR), surface-mount tantalum (SMT) output filter capacitor, C2, typically exhibits 50mV output ripple when stepping up from 2V to 5V at 100mA. Smaller capacitors (down to 10µF with higher ESRs) are acceptable for light loads or in applications that can tolerate higher output ripple. The ESR of both bypass and filter capacitors affects efficiency and output ripple. Output voltage ripple is the product of the peak inductor current and the output capacitor's ESR. Use low-ESR capacitors for best performance, or connect two or more filter capacitors in parallel. Low-ESR, SMT capacitors are currently available from Sprague (595D series) and AVX (TPS series). Sanyo OS-CON organic-semiconductor through-hole capacitors also exhibit very low ESR and are especially useful for operation at cold temperatures. The output capacitor, C3, needs to be only 4.7µF to maintain linear regulator stability. See Tables 2 and 3 for a list of suggested capacitors and suppliers.

Rectifier Diode

For optimum performance, use a switching Schottky diode. Refer to Tables 2 and 3 for the suggested diode and supplier.

Applications Information

The MAX710/MAX711 high-frequency operation makes PC layout important for minimizing ground bounce and noise. Keep the IC's GND pin and the ground leads of C1 and C2 (Figure 1) less than 0.2in. (5mm) apart. Also keep all connections to the FB and LX pins as short as possible. To maximize output power and efficiency and minimize output ripple voltage, use a ground plane and solder the IC's GND pin directly to the ground plane.

Table 3. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	(803) 946-0690	(803) 626-3123
Coilcraft	(847) 639-6400	(847) 639-1469
Motorola	(602) 303-5454	(602) 994-6430
Sanyo	(619) 661-6835	(619) 661-1055
Sprague	(603) 224-1961	(603) 224-1430
Sumida	(847) 956-0666	(847) 956-0702

Chip Information

TRANSISTOR COUNT: 661

SUBSTRATE CONNECTED TO GND

19-1175; Rev 0; 12/96

MAXIM

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

General Description

The MAX798† high-performance, step-down DC-DC converter provides main CPU power in battery-powered systems. This buck controller achieves 96% efficiency by using synchronous rectification and Maxim's proprietary Idle Mode™ control scheme to extend battery life at full-load (up to 10A) and no-load outputs. The MAX798's high accuracy meets the demanding requirements of the latest-generation CPUs. Excellent dynamic response corrects output transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Unique bootstrap circuitry drives inexpensive N-channel MOSFETs, reducing system cost and eliminating the crowbar switching currents found in some PMOS/NMOS switch designs.

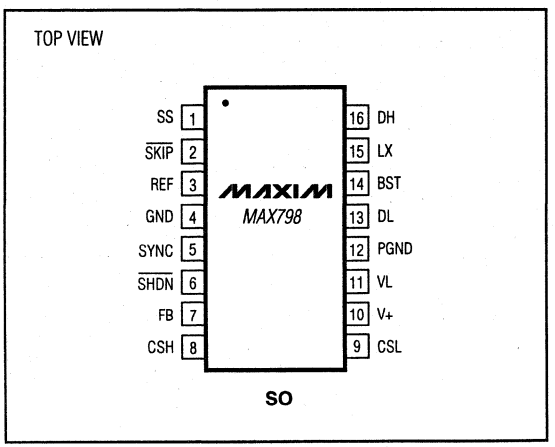
The MAX798 has a logic-controlled and synchronizable fixed-frequency pulse-width-modulating (PWM) operating mode, which reduces noise and RF interference in sensitive mobile-communications and pen-entry applications. The $\overline{SKIP}$ override input allows automatic switchover to idle-mode operation (for high-efficiency pulse skipping) at light loads, or forces fixed-frequency mode for lowest noise at all loads.

Applications

Notebook and Subnotebook Computers

PDAs and Mobile Communicators

Pin Configuration



Features

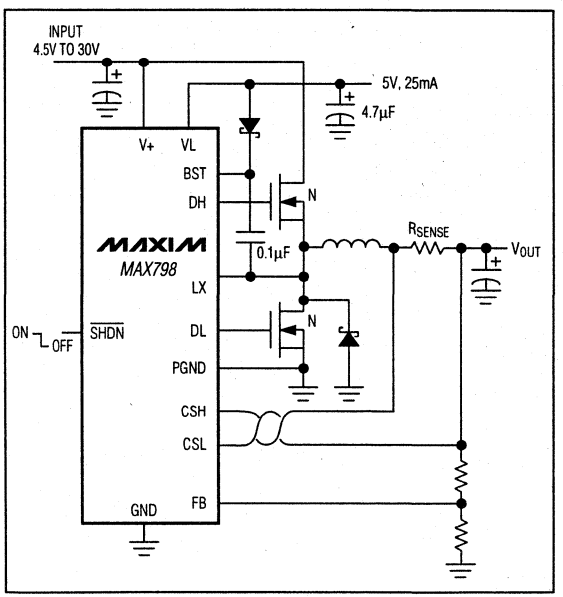
- ♦ **96% Efficiency**
- ♦ **4.5V to 30V Input Range**
- ♦ **1.6V to 6V Adjustable Precision Output**
- ♦ **±0.4% Max Total Load-Regulation Error**
- ♦ **0.06%/V Max Line-Regulation Error**
- ♦ **5V Linear-Regulator Output**
- ♦ **Precision 2.505V Reference Output**
- ♦ **Automatic Bootstrap Circuit**
- ♦ **150kHz/300kHz Fixed-Frequency PWM Operation**
- ♦ **Programmable Soft-Start**
- ♦ **1.2mA Typical Quiescent Current (V_{IN} = 12V, V_{OUT} = 2.5V)**
- ♦ **1µA Typical Shutdown Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX798ESE	-40°C to +85°C	16 Narrow SO

4

Typical Operating Circuit



Idle Mode is a trademark of Maxim Integrated Products.

†*U.S. and foreign patents pending.*

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V, +36V
GND to PGND .....±2V
VL to GND .....-0.3V, +7V
BST to GND .....-0.3V, +36V
DH to LX .....-0.3V, (BST + 0.3V)
LX to BST .....-7V, +0.3V
$\overline{SHDN}$ to GND .....-0.3V, +36V
SYNC, SS, REF, $\overline{SKIP}$, DL to GND .....-0.3V, (VL + 0.3V)
CSH, CSL to GND .....-0.3V, +7V
VL Short Circuit to GND .....Momentary
REF Short Circuit to GND .....Continuous
VL Output Current 50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range
MAX798ESE .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0A, T_A = 0°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-DOWN CONTROLLER					
Input Supply Range		4.5		30	V
Nominal Adjustable Output Voltage Range	External resistor divider	1.6		6	V
Feedback Voltage	CSH - CSL = 40mV, $\overline{SKIP}$ = VL	1.576	1.6	1.624	V
Load Regulation	0mV < (CSH - CSL) < 80mV, $\overline{SKIP}$ = VL			±0.4	%
Line Regulation	6V < V+ < 30V		0.04	0.05	%/V
Current-Limit Voltage	CSH - CSL, positive	80	100	120	mV
	CSH - CSL, negative	-40	-100	-160	
SS Source Current		2.0	4.0	6.5	µA
SS Fault Sink Current		2.0			mA
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	$\overline{SHDN}$ = 2V, 0mA < I_{VL} < 25mA, 5.5V < V+ < 30V	4.75		5.25	V
VL Fault Lockout Voltage	Rising edge, hysteresis = 15mV	3.8		4.0	V
VL/CSL Switchover Voltage	Rising edge, hysteresis = 25mV	4.2		4.7	V
Reference Output Voltage	No external load (Note 1)	2.463	2.505	2.537	V
Reference Fault Lockout Voltage	Falling edge	1.8		2.3	V
Reference Load Regulation	0µA < I_{REF} < 100µA			20	mV
CSL Shutdown Leakage Current	$\overline{SHDN}$ = 0V, CSL = 6V, V+ = 0V or 30V, VL = 0V		0.1	1	µA
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0V or 6V		1	5	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 6V, VL switched over to CSL		1	5	µA
Dropout Power Consumption	V+ = 4V, CSL = 0V (Note 2)		6.6	10.5	mW
Quiescent Power Consumption	CSH = CSL = 6V		6.4	8.5	mW

ELECTRICAL CHARACTERISTICS (continued)

(V+ = +15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0A, T_A = 0°C to +85°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator Frequency	SYNC = REF	270	300	330	kHz
	SYNC = 0V or 5V	125	150	175	
SYNC High Pulse Width		200			ns
SYNC Low Pulse Width		200			ns
SYNC Rise/Fall Time	Guaranteed by design			200	ns
Oscillator Sync Range		195		340	kHz
Maximum Duty Cycle	SYNC = REF	89	91		%
	SYNC = 0V or 5V	93	96		
Input High Voltage	SYNC	VL - 0.5			V
	$\overline{SHDN}$, $\overline{SKIP}$	2.0			
Input Low Voltage	SYNC			0.8	V
	$\overline{SHDN}$, $\overline{SKIP}$			0.5	
Input Current	$\overline{SHDN}$, 0V or 30V			2	µA
	SYNC, $\overline{SKIP}$			1	
	CSH, CSL, CSH = CSL = 4V, device not shut down			50	
	FB, FB = 1.6V			±100	nA
DL Sink/Source Current	DL forced to 2V		1		A
DH Sink/Source Current	DH forced to 2V, BST - LX = 4.5V		1		A
DL On-Resistance	High or low			7	Ω
DH On-Resistance	High or low, BST - LX = 4.5V			7	Ω

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

ELECTRICAL CHARACTERISTICS

(V+ = +15V, GND = PGND = 0V, I_{VL} = I_{REF} = 0A, T_A = -40°C to +85°C, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-DOWN CONTROLLER					
Input Supply Range		5.0		30	V
Nominal Adjustable Output Voltage Range	External resistor divider	1.6		6.0	V
Feedback Voltage	CSH - CSL = 40mV, $\overline{SKIP}$ = VL	1.560	1.6	1.640	V
Load Regulation	0mV < (CSH - CSL) < 80mV, $\overline{SKIP}$ = VL			±1	%
Line Regulation	6V < V+ < 30V		0.04	0.06	%/ V
Current-Limit Voltage	CSH - CSL, positive	70		130	mV
	CSH - CSL, negative	-40	-100	-160	
INTERNAL REGULATOR AND REFERENCE					
VL Output Voltage	$\overline{SHDN}$ = 2V, 0mA < I_{VL} < 25mA, 5.5V < V+ < 30V	4.7		5.3	V
VL Fault Lockout Voltage	Rising edge, hysteresis = 15mV	3.75		4.05	V
VL/CSL Switchover Voltage	Rising edge, hysteresis = 25mV	4.15		4.75	V
Reference Output Voltage	No external load (Note 1)	2.438	2.505	2.562	V
Reference Load Regulation	0µA < I_{REF} < 100µA			30	mV
V+ Shutdown Current	$\overline{SHDN}$ = 0V, V+ = 30V, CSL = 0V or 6V		1	10	µA
V+ Off-State Leakage Current	FB = CSH = CSL = 6V, VL switched over to CSL		1	10	µA
Quiescent Power Consumption	CSH = CSL = 6V		6.4	9.1	mW
OSCILLATOR AND INPUTS/OUTPUTS					
Oscillator Frequency	SYNC = REF	250	300	350	kHz
	SYNC = 0V or 5V	110	150	190	
SYNC High Pulse Width		250			ns
SYNC Low Pulse Width		250			ns
Oscillator Sync Range		210		320	kHz
Maximum Duty Cycle	SYNC = REF	88	91		%
	SYNC = 0V or 5V	92	96		
DL On-Resistance	High or low			7	Ω
DH On-Resistance	High or low, BST - LX = 4.5V			7	Ω

Note 1: Since the reference uses VL as its supply, V+ line-regulation error is insignificant.

Note 2: At very low input voltages, quiescent supply current can increase due to excess PNP base current in the VL linear regulator. This occurs only if V+ falls below the preset VL regulation point (5V nominal). The typical maximum quiescent current in dropout will not exceed 16mA.

Note 3: All -40°C to +85°C specifications above are guaranteed by design.

Pin Description

PIN	NAME	FUNCTION
1	SS	Soft-Start Timing Capacitor Connection. Ramp time to full current limit is approximately 1ms/nF.
2	$\overline{SKIP}$	Disables pulse-skipping mode when high. Connect to GND for normal use. **Don't leave $\overline{SKIP}$ unconnected.** With $\overline{SKIP}$ grounded, the device will *automatically* change from pulse-skipping operation to full PWM operation when the load current exceeds approximately 30% of maximum.
3	REF	Reference Voltage Output. Bypass to GND with 0.33µF minimum.
4	GND	Low-Noise Analog Ground and Feedback Reference Point
5	SYNC	Oscillator Synchronization and Frequency Select. Tie to GND or VL for 150kHz operation; tie to REF for 300kHz operation. A high-to-low transition begins a new cycle. Drive SYNC with 0V to 5V logic levels (see the *Electrical Characteristics* table for V_{IH} and V_{IL} specifications). SYNC capture range is 195kHz to 340kHz.
6	$\overline{SHDN}$	Shutdown Control Input, active low. Logic threshold is set at approximately 1V (V_{TH} of an internal N-channel MOSFET). Tie $\overline{SHDN}$ to V+ for automatic start-up.
7	FB	Feedback Input. Regulates at FB = 1.6V. Connect FB to a resistor divider to set the output voltage.
8	CSH	Current-Sense Input, high side. Current-limit level is 100mV referred to CSL.
9	CSL	Current-Sense Input, low side
10	V+	Battery Voltage Input (4.5V to 30V). Bypass V+ to PGND close to the IC with a 0.1µF capacitor. Connects to a linear regulator that powers VL.
11	VL	5V Internal Linear-Regulator Output. VL is also the supply voltage rail for the chip. VL is switched to the output voltage via CSL (V_{CSL} > 4.5V) for automatic bootstrapping. Bypass to GND with 4.7µF. VL can supply up to 5mA for external loads.
12	PGND	Power Ground
13	DL	Low-Side Gate-Drive Output. Normally drives the synchronous-rectifier MOSFET. Swings 0V to VL.
14	BST	Boost Capacitor Connection for high-side gate drive (0.1µF)
15	LX	Switching Node (inductor) Connection. Can swing 2V below ground without hazard.
16	DH	High-Side Gate-Drive Output. Normally drives the main buck switch. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage.

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

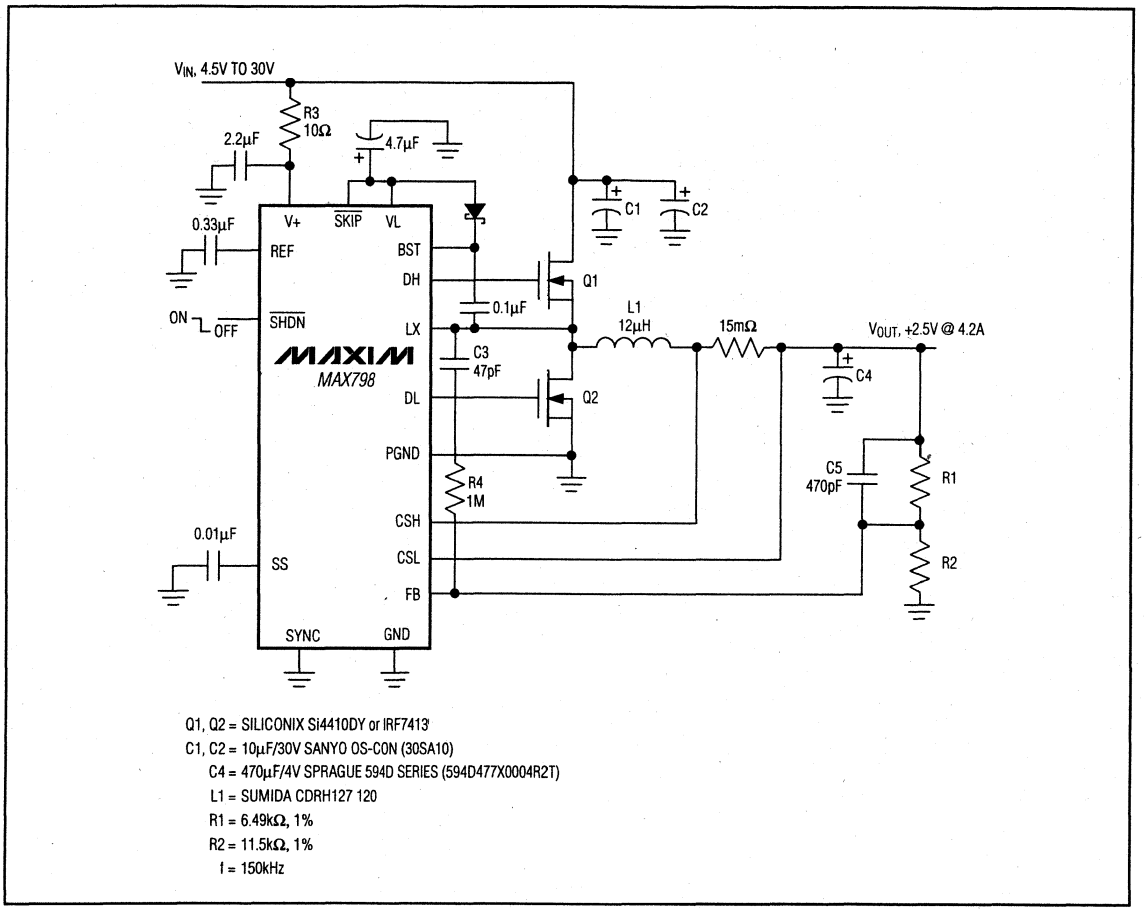


Figure 1. Standard Application Circuit

Detailed Description

The MAX798 is a BiCMOS, switch-mode power-supply controller designed primarily for buck-topology regulators in battery-powered applications where high accuracy, high efficiency, and low quiescent supply current are critical. The MAX798 also works well in other topologies such as boost, inverting, and CUK due to the flexibility of its floating high-speed gate driver. Light-load efficiency is enhanced by automatic idle-mode operation—a variable-frequency pulse-skipping mode that reduces losses due to MOSFET gate charge. The step-down power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET must exceed the battery voltage and is provided by a flying capacitor boost circuit that uses a 100nF capacitor connected between BST and LX.

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

The MAX798 contains the following seven major circuit blocks, which are shown in Figure 2.

PWM Controller Blocks:

- Multi-Input PWM Comparator
- Current-Sense Circuit
- PWM Logic Block
- Gate-Driver Outputs

Bias Generator Blocks:

- +5V Linear Regulator
- Automatic Bootstrap Switchover Circuit
- +2.505V Reference

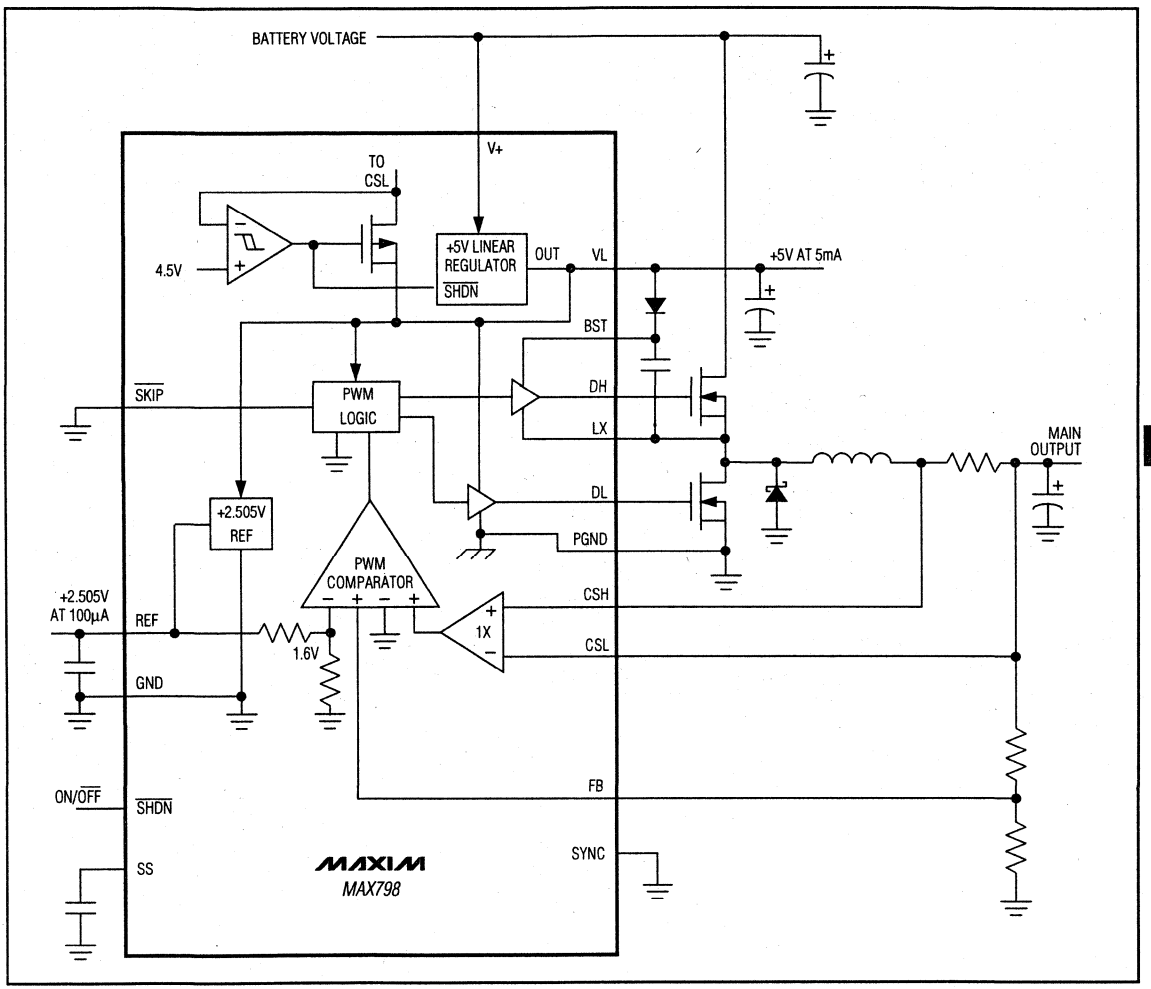


Figure 2. Functional Diagram

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

These internal IC blocks aren't powered directly from the battery. Instead, a +5V linear regulator steps down the battery voltage to supply both the IC internal rail (VL pin) as well as the gate drivers. The synchronous-switch gate driver is directly powered from +5V VL, while the high-side-switch gate driver is indirectly powered from VL via an external diode-capacitor boost circuit. An automatic bootstrap circuit turns off the +5V linear regulator and powers the IC from its output voltage if the output is above 4.5V.

PWM Controller Block

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: output voltage error signal with respect to the reference voltage, current-sense signal, and slope compensation ramp (Figure 3). The PWM controller is a direct summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches the ideal of cycle-by-cycle control over the output voltage.

For more comprehensive information on the MAX798 internal blocks, please refer to the MAX796/MAX797/MAX799 data sheet.

Applications Information

Powering VL from a +5V Supply

If the circuit's output voltage is greater than the VL/CSL switchover voltage, the IC automatically bootstraps and runs off its output. Running from the high-efficiency output rather than the VL linear regulator is particularly desirable if the input voltage is high. If the output is not greater than the VL/CSL switchover threshold, efficiency can be improved by powering VL from another efficient system supply (Figure 4).

VL can be connected directly to a +5V supply, provided its maximum excursions are within a 4.5V to 6V range and the main output voltage's maximum is less than 4.2V. If the circuit's output voltage is greater than 4.2V, the IC can activate its internal bootstrap switch and connect the circuit output to VL.

Adjusting the Output Voltage

The output voltage is set by an external resistor divider between the output voltage and GND, with the midpoint connected to FB (Figure 5). The output voltage can be adjusted from 1.6V to 6V, according to the formula in Figure 5. Recommended R2 values range from 5kΩ to 100kΩ. For best noise immunity, place R1 and R2 close to FB. For a 1.6V output, connect the output voltage directly to FB.

Remote sensing of the output voltage is easily achieved by connecting the top of R1 and, if desired, the bottom of R2, to the remote sense point.

Bypassing and Compensation Components

The MAX798 is designed to deliver a more accurate output voltage than the MAX797. A major source of the MAX797's output error is the decrease in output voltage with increasing load. This error is greatly reduced in the MAX798 by increasing the gain of the voltage-sense signal relative to the current-sense signal. As a result of this increased gain, the MAX798 is slightly more noise sensitive than the MAX797, and requires some small compensation components as well. On the other hand, output capacitor ESR requirements can be greatly relaxed compared to the MAX797, with the limiting factor being the maximum total output voltage ripple that the application can tolerate.

To control noise problems, place the bypass capacitors on REF, VL, and V+ as close as possible to the IC, and use a 10Ω series resistor (R3, Figure 1) on V+ to form a small lowpass filter. Feed-forward components (R4, C3, and C5) are chosen for stable switching at 150kHz with the components shown. For 300kHz switching and a 4.7µH inductor, use R4 = 470kΩ and C5 = 220pF. Keep the components that connect to FB (R4, C5, R1, R2) close to the IC's FB pin.

Design Procedure

With the exception of the items previously mentioned, follow the design procedure for the MAX797. The MAX796/MAX797/MAX799 data sheet contains all necessary information on component values, component selection, layout, and additional applications.

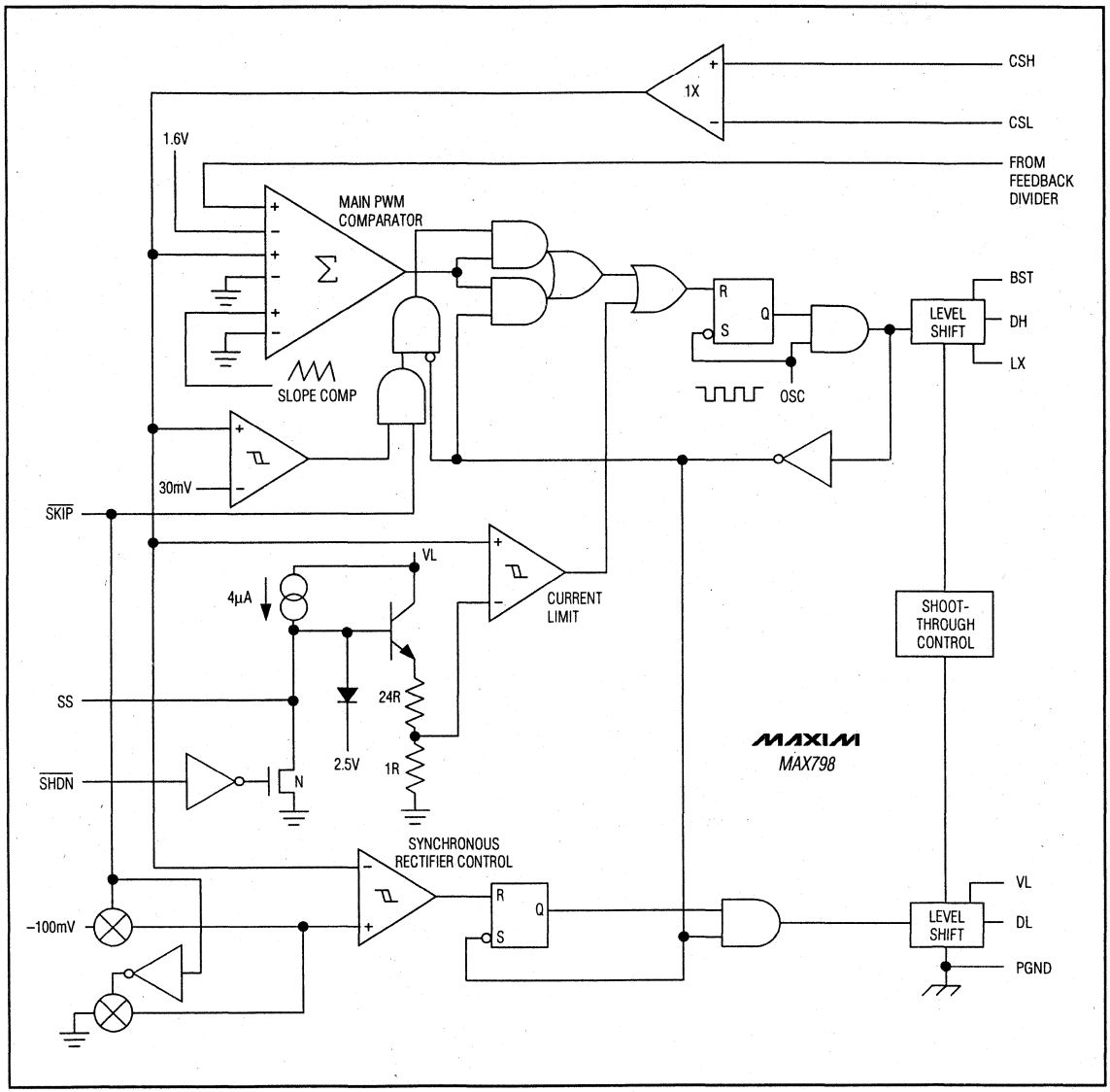


Figure 3. PWM Controller Detailed Block Diagram

High-Accuracy Step-Down Controller with Synchronous Rectifier for CPU Power

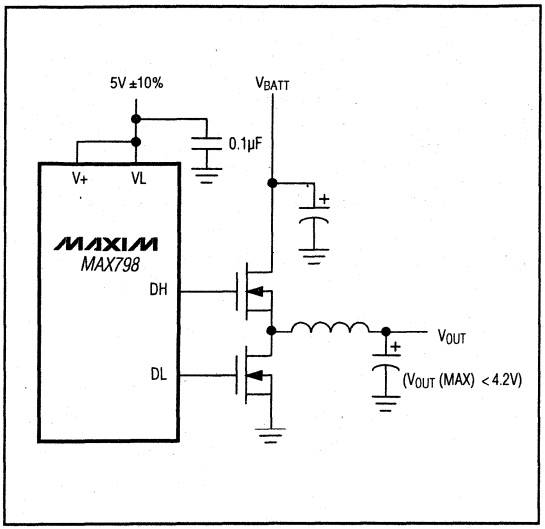


Figure 4. Powering VL from a Separate +5V Supply

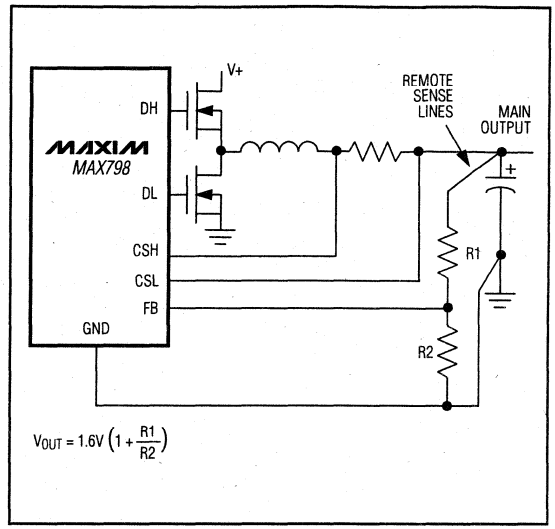


Figure 5. Adjusting the Output Voltage

Chip Information

TRANSISTOR COUNT: 1008

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

1-Cell, Step-Up, Two-Way Pager System IC

General Description

The MAX847 is a complete power-supply and monitoring system for two-way pagers or other low-power digital communications devices. It requires few external components. Included on-chip are:

- A 1-cell-input, 80mA, synchronous-rectified boost DC-DC regulator with a digitally controlled 1.8V to 4.9V output
- Three low-noise linear-regulator/switch outputs
- Three DAC-controlled comparators for software-driven 3-channel analog-to-digital conversion (CH0, NiCd, and BATT)
- SPI-compatible serial interface
- Reset and low-battery (LBO) warning outputs
- Charger for small NiCd, NiMH, lithium battery, or SuperCap for RF PA power or system backup
- Two 1.8Ω (typical) serial-controlled, open-drain MOSFET switches

An evaluation kit for the MAX847 (MAX847EVKIT) is available to aid in design and prototyping.

Features

- **80mA Output from One Cell at 90% Efficiency**
- **15µA Idle Mode™ (Coast) Current**
- **Selectable Low-Noise Pulse-Width-Modulation (PWM) or Low-Current Operation**
- **PWM Operating Frequency Synchronized to a Multiple of an External Clock Source**
- **Operates at 270kHz with No External Clock**
- **Automatic Backup-Battery Switchover**

Applications

Two-Way Pagers

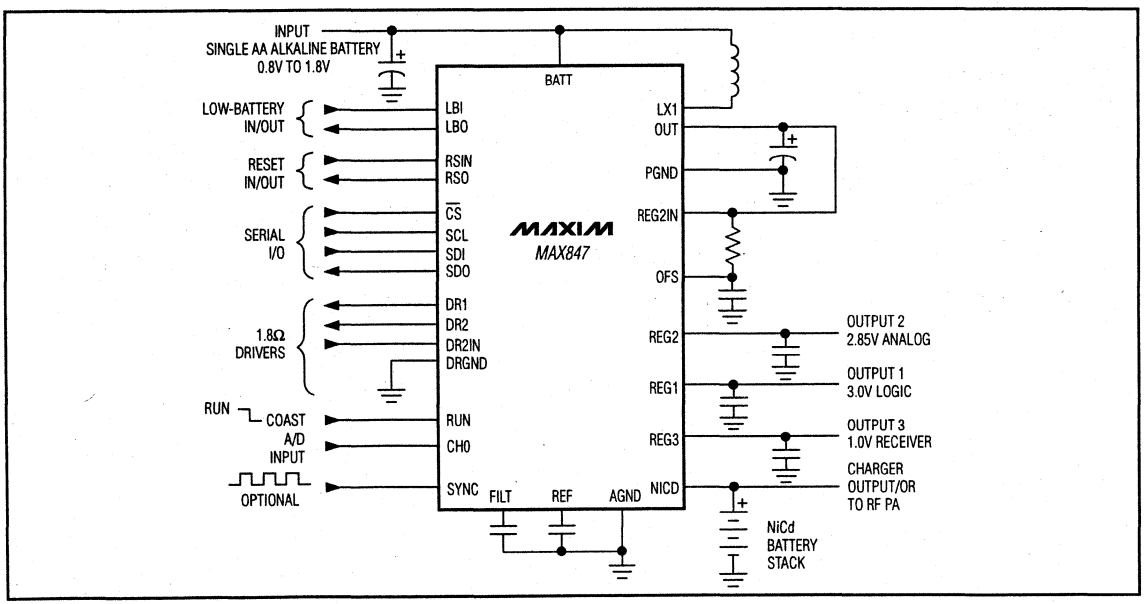
GPS Receivers

1-Cell-Powered, Hand-Held Equipment

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX847EEI	-40°C to +85°C	28 QSOP

Typical Operating Circuit



SuperCap is a trademark of Baknor Industries. Idle Mode is a trademark of Maxim Integrated Products.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

19-1218; Rev 1; 6/97

EVALUATION KIT AVAILABLE

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

General Description

The MAX863 dual-output DC-DC converter contains two independent step-up controllers in a single compact package. This monolithic Bi-CMOS design draws only 85µA when both controllers are on. The input range extends down to 1.5V, permitting use in organizers, translators, and other low-power hand-held products. The MAX863 provides 90% efficiency at output loads from 20mA to over 1A. This space-saving device is supplied in a 16-pin QSOP package that fits in the same area as an 8-pin SOIC.

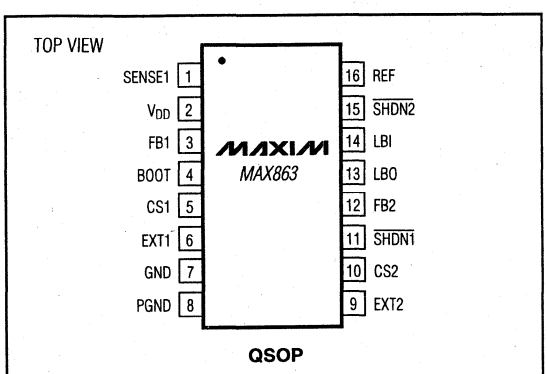
The device uses a current-limited, pulse-frequency-modulated (PFM) control architecture that reduces start-up surge currents and maintains low quiescent currents for excellent low-current efficiency. Each controller drives a low-cost, external, N-channel MOSFET switch, whose size can be optimized for any output current or voltage.

In larger systems, two MAX863s can be used to generate 5V, 3.3V, 12V, and 28V from just two or three battery cells. An evaluation kit (MAX863EVKIT) is available to speed designs. For a single-output controller, refer to the MAX608 and MAX1771 data sheets.

Applications

2- and 3-Cell Portable Equipment
Organizers
Translators
Hand-Held Instruments
Palmtop Computers
Personal Digital Assistants (PDAs)
Dual Supply (Logic and LCD)

Pin Configuration



Features

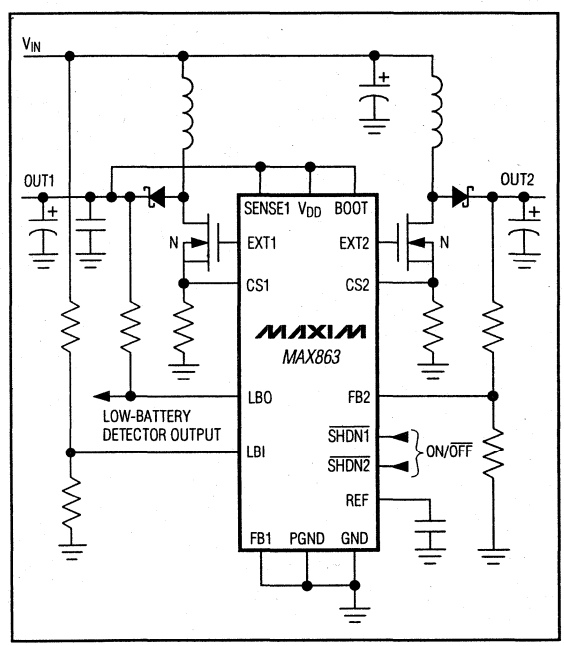
- ♦ **Smallest Dual Step-Up Converter: 16-Pin QSOP**
- ♦ **90% Efficiency**
- ♦ **1.5V Start-Up Voltage**
- ♦ **85µA Max Total Quiescent Supply Current**
- ♦ **1µA Shutdown Mode**
- ♦ **Independent Shutdown Inputs**
- ♦ **Drives Surface-Mount, Dual N-Channel MOSFETs**
- ♦ **Low-Battery Input/Output Comparator**
- ♦ **Step-Up/Down Configurable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX863C/D	0°C to +70°C	Dice*
MAX863EEE	-40°C to +85°C	16 QSOP

*Dice are tested at T_A = +25°C.

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +12V
PGND to GND .....-0.3V to +0.3V
$\overline{SHDN1}$, $\overline{SHDN2}$, SENSE1, LBO to GND .....-0.3V to +12V
EXT1, EXT2 to PGND.....-0.3V to (V_{DD} + 0.3V)
FB1, FB2, CS1, CS2, SEL,
LBI, BOOT to GND.....-0.3V to (V_{DD} + 0.3V)
LBO Continuous Output Current.....15mA
EXT1, EXT2 Continuous Output Current 50mA

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.30mW/°C above +70°C) 667mW
Operating Temperature Range
MAX863EEE .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, I_{LOAD} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Input Voltage	V_{DD}	V_{DD} = OUT1 = BOOT (Note 1)	1.5		11	V
		(Note 2)	2.7		11	
OUT1 Output Voltage (Note 3)	V_{OUT1}	FB1 = V_{DD}	3.2	3.3	3.4	V
		FB1 = GND	4.85	5	5.15	
Quiescent Current	I_{DD}	$\overline{SHDN1}$ = $\overline{SHDN2}$ = V_{DD}, measured from V_{DD}		50	85	µA
		$\overline{SHDN1}$ = V_{DD}, $\overline{SHDN2}$ = GND, measured from V_{DD}		35	60	
Shutdown Current	$I_{DD, \overline{SHDN}}$	$\overline{SHDN1}$ = $\overline{SHDN2}$ = GND			1	µA
Load Regulation		V_{IN} = 3.3V, V_{OUT1} = 5V, I_{LOAD} = 0mA to 500mA, Figure 2		40		mV/A
Line Regulation		V_{IN} = 2.7V to 5V, V_{OUT1} = 5V, I_{LOAD} = 300mA, Figure 2		8		mV/V
FB1, FB2, LBI Threshold Voltage (Note 4)	V_{FB}, V_{LBI}		1.225	1.25	1.275	V
FB1, FB2, LBI Input Current	I_{FB}, I_{LBI}			2	10	nA
$\overline{SHDN1}$, $\overline{SHDN2}$, SEL, BOOT Input High Voltage	V_{IH}	2.7V < V_{DD} < 11V	1.6			V
		V_{DD} = 1.5V	0.7 x V_{DD}			
$\overline{SHDN1}$, $\overline{SHDN2}$, SEL, BOOT Input Low Voltage	V_{IL}	2.7V < V_{DD} < 11V			0.4	V
		V_{DD} = 1.5V			0.2 x V_{DD}	
$\overline{SHDN1}$, $\overline{SHDN2}$, SEL, BOOT Input Current	I_I	Logic input = V_{DD} or GND			1	µA
CS1, CS2 Threshold Voltage	V_{CS}		85	100	115	mV
CS1, CS2 Input Current				1	25	µA
Maximum Switch On-Time	t_{ON}		14	17.5	22	µs
Minimum Switch Off-Time	t_{OFF}		1.6	2	2.4	µs
EXT Rise/Fall Time (Note 5)		C_{LOAD} = 1nF, 10% to 90%		50		ns
EXT On-Resistance				5		Ω
LBO Leakage Current	I_{LBO}	V_{LBO} = 11V, V_{LBI} > 1.275V			1	µA
LBO Low Level	$V_{LBO,L}$	$I_{LBO,SINK}$ = 1mA, V_{LBI} < 1.225V		0.1	0.4	V

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, I_{LOAD} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted.) (Note 6)

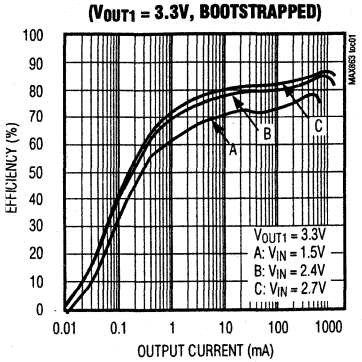
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Input Voltage	V_{DD}	V_{DD} = OUT1 (Note 1)	1.6		11	V
		(Note 2)	2.8		11	
OUT1 Output Voltage (Note 3)	V_{OUT1}	FB1 = V_{DD}	3.15		3.45	V
		FB1 = GND	4.8		5.2	
Quiescent Current	I_{DD}	$\overline{SHDN1}$ = $\overline{SHDN2}$ = V_{DD}, measured from V_{DD}			85	µA
		$\overline{SHDN1}$ = V_{DD}, $\overline{SHDN2}$ = GND, measured from V_{DD}			60	
Shutdown Current	I_{DD}, $\overline{SHDN}$	$\overline{SHDN1}$ = $\overline{SHDN2}$ = GND			1	µA
FB1, FB2 Threshold Voltage	V_{FB}		1.21		1.285	V
CS1, CS2 Threshold Voltage	V_{CS}		85		115	mV

Note 1: When bootstrapped, an internal low-voltage oscillator drives the EXT1 pin rail-to-rail for low supply voltages.
Note 2: For non-bootstrapped operation, V_{DD} > 2.7V is required to allow valid operation of all internal circuitry.
Note 3: For adjustable output voltages, see the *Set the Output Voltage* section.
Note 4: Measured with LBI falling. Typical hysteresis is 15mV.
Note 5: EXT1 and EXT2 swing from V_{DD} to GND.
Note 6: Specifications to -40°C are guaranteed by design and not production tested.

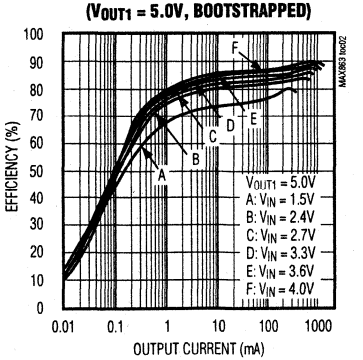
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

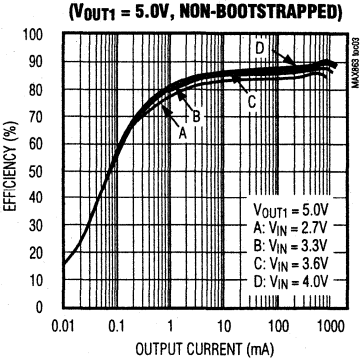
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT1} = 3.3V, BOOTSTRAPPED)



EFFICIENCY vs. OUTPUT CURRENT (V_{OUT1} = 5.0V, BOOTSTRAPPED)



EFFICIENCY vs. OUTPUT CURRENT (V_{OUT1} = 5.0V, NON-BOOTSTRAPPED)

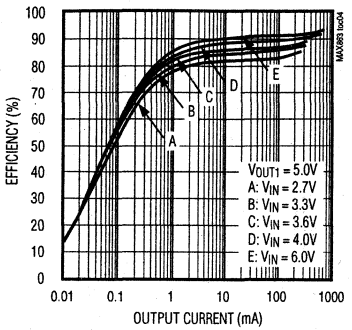


Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

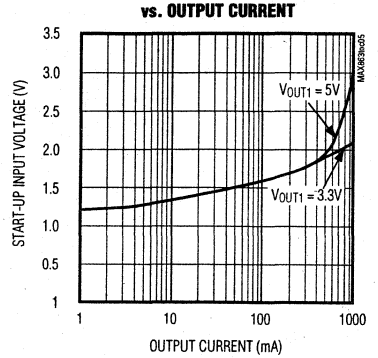
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

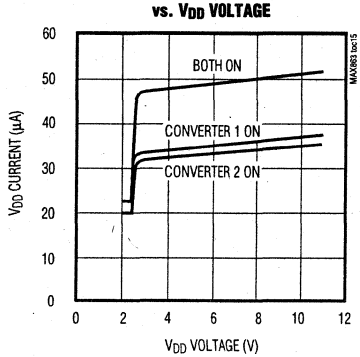
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT1} = 12V, NON-BOOTSTRAPPED)



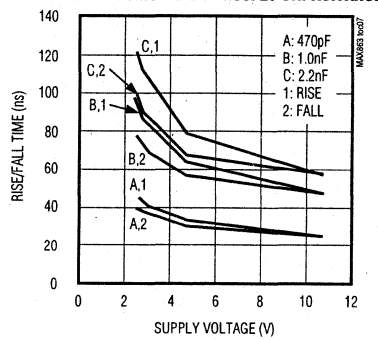
BOOTSTRAPPED-MODE MINIMUM START-UP INPUT VOLTAGE vs. OUTPUT CURRENT



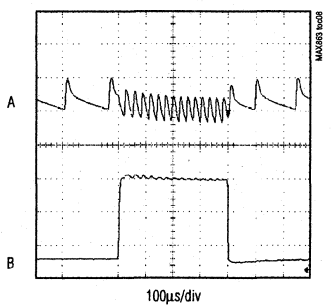
V_{DD} CURRENT vs. V_{DD} VOLTAGE



EXT RISE AND FALL TIMES vs. SUPPLY VOLTAGE AND MOSFET CAPACITANCE

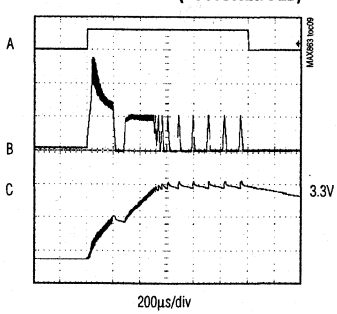


LOAD-TRANSIENT RESPONSE



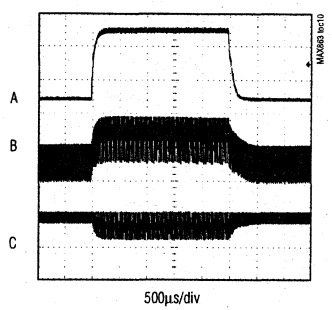
V_{OUT1} = 3.3V, I_{OUT1} = 100mA TO 600mA
A: V_{OUT1}, 100mV/div, 3.3V DC OFFSET
B: I_{OUT1}, 200mA/div

RESPONSE ENTERING/ EXITING SHUTDOWN (BOOTSTRAPPED)



V_{OUT1} = 3.3V, I_{OUT1} = 100mA, V_{IN} = 2.4V
A: SHDN1, 5V/div
B: INDUCTOR CURRENT, 2A/div
C: V_{OUT1}, 3.3V OFFSET, 500mV/div

LINE-TRANSIENT RESPONSE



V_{OUT1} = 5V, I_{OUT1} = 800mA
A: V_{IN} = 2.7V TO 3.7V, 500mV/div
B: V_{OUT1}, AC COUPLED, 50mV/div
C: INDUCTOR CURRENT, 2A/div

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

Pin Description

PIN	NAME	FUNCTION
1	SENSE1	Feedback Input for DC-DC Controller 1 in Fixed-Output Mode
2	V_{DD}	IC Power-Supply Input
3	FB1	Adjustable Feedback and Preset Output Voltage Selection Input for DC-DC Controller 1. Connect to V_{DD} for 3.3V preset output or to GND for 5V output. Connect a resistor voltage divider to adjust the output voltage. See the section *Set the Output Voltage.*
4	BOOT	Bootstrap Low-Voltage-Oscillator Enable Input. BOOT is an active-high, logic-level input. It enables the low-voltage oscillator to allow start-up from input voltages down to 1.5V while in a bootstrapped circuit configuration. Connect BOOT to GND when in a non-bootstrapped configuration. **If BOOT is high, V_{DD} must be connected to OUT1.**
5	CS1	Input to the Current-Sense Comparator of DC-DC Controller 1
6	EXT1	Gate-Drive Output of DC-DC Controller 1. Drives an external N-channel power MOSFET.
7	GND	Analog Ground for Internal Reference, Feedback, and Control Circuits
8	PGND	High-Current Ground Return for Internal MOSFET Drivers
9	EXT2	Gate-Drive Output of DC-DC Controller 2. Drives an external N-channel power MOSFET.
10	CS2	Input to the Current-Sense Amplifier of DC-DC Controller 2
11	$\overline{SHDN1}$	Active-Low Shutdown Input for DC-DC Controller 1. Connect to V_{DD} for normal operation.
12	FB2	Adjustable Feedback Input for DC-DC Controller 2. Connect a resistor voltage divider to adjust the output voltage. See the section *Set the Output Voltage.*
13	LBO	Low-Battery Output. An open-drain N-channel MOSFET output. Sinks current when the voltage on LBI drops below 1.25V. If unused, connect to GND.
14	LBI	Low-Battery Comparator Input. When the voltage on LBI drops below 1.25V, LBO sinks current. If unused, connect to GND.
15	$\overline{SHDN2}$	Active-Low Shutdown Input for DC-DC Controller 2. Connect to V_{DD} for normal operation.
16	REF	Reference Bypass Input. Connect a 0.1µF ceramic capacitor from REF to GND.

Detailed Description

The MAX863 dual, bi-CMOS, step-up, switch-mode power-supply controller provides preset 3.3V, 5V, or adjustable outputs. Its pulse-frequency-modulated (PFM) control scheme combines the advantages of low supply current at light loads and high efficiency with heavy loads. These attributes make the MAX863 ideal for use in portable battery-powered systems where small size and low cost are extremely important, and where low quiescent current and high efficiency are needed to maximize operational battery life. Use of external current-sense resistors and MOSFETs allows the designer to tailor the output current and voltage capability for a diverse range of applications.

PFM Control Scheme

Each DC-DC controller in the MAX863 uses a one-shot-sequenced, current-limited PFM design, as shown in Figure 1. Referring to the Typical Operating Circuit (Figure 2) and the switching waveforms (Figures 3a–3f), the circuit works as follows. Output voltage is sensed by the error comparator using either an internal voltage divider connected to SENSE1 or an external voltage divider connected to FB1. When the output voltage drops, the error comparator sets an internal flip-flop. The flip-flop turns on an external MOSFET, which allows inductor current to ramp-up, storing energy in a magnetic field.

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

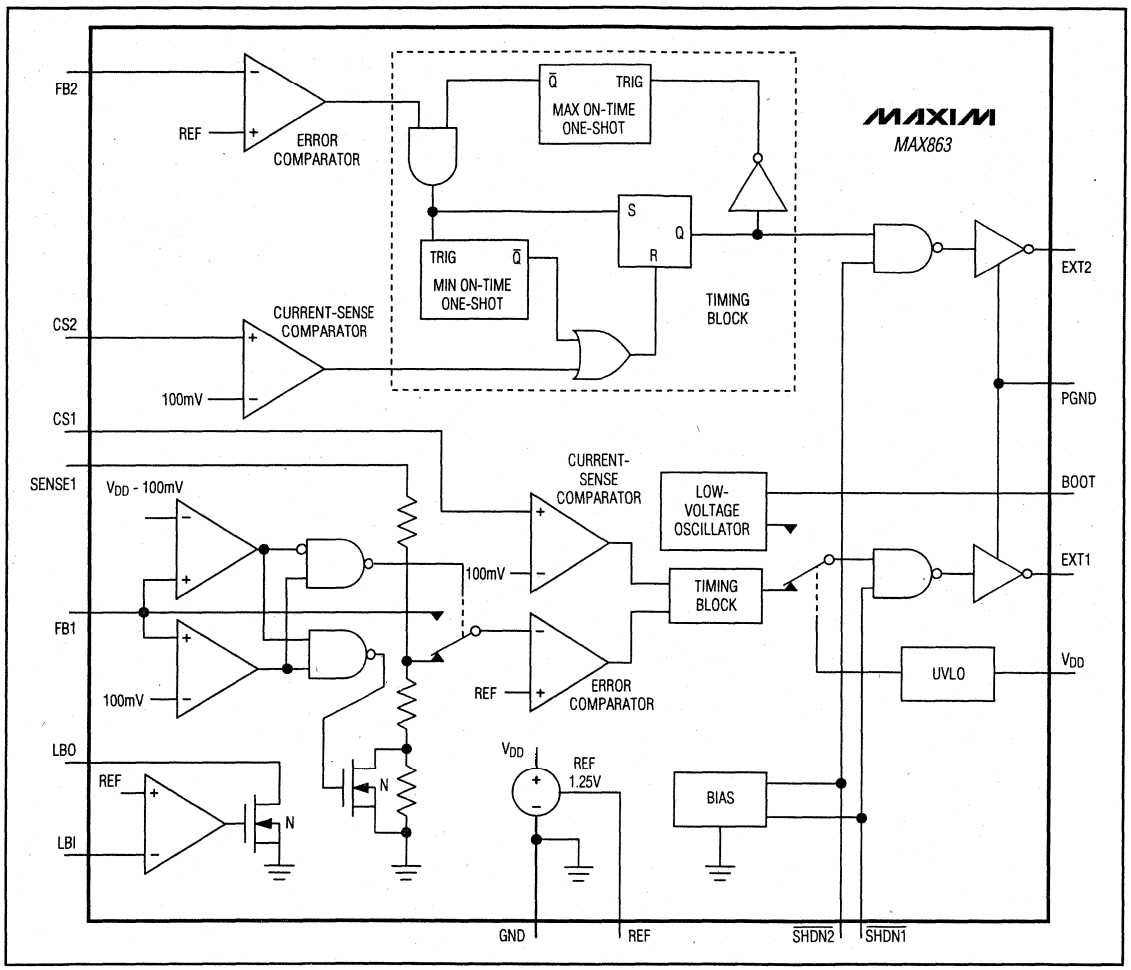


Figure 1. Functional Diagram

The flip-flop resets and turns off the MOSFET when either a) the voltage across the current-sense resistor exceeds 100mV, or b) the 17.5µs maximum on-time one-shot trips. When the MOSFET turns off, the magnetic field begins to collapse, and forces current into the output capacitor and load. As the stored energy is transferred to the output, the inductor current ramps down. The output capacitor smoothes out the energy transfer by storing charge when the diode current is high, then supplying current to the load during the first half of each cycle, maintaining a steady output voltage. Resetting the flip-flop sets the off-time one-shot, disabling the error-comparator output and forcing the MOSFET off for at least 2µs to enforce a minimum time for energy transfer to the output. The MAX863 waits until the output voltage drops again before beginning another cycle. The MAX863's switching frequency depends on the load current and input voltage.

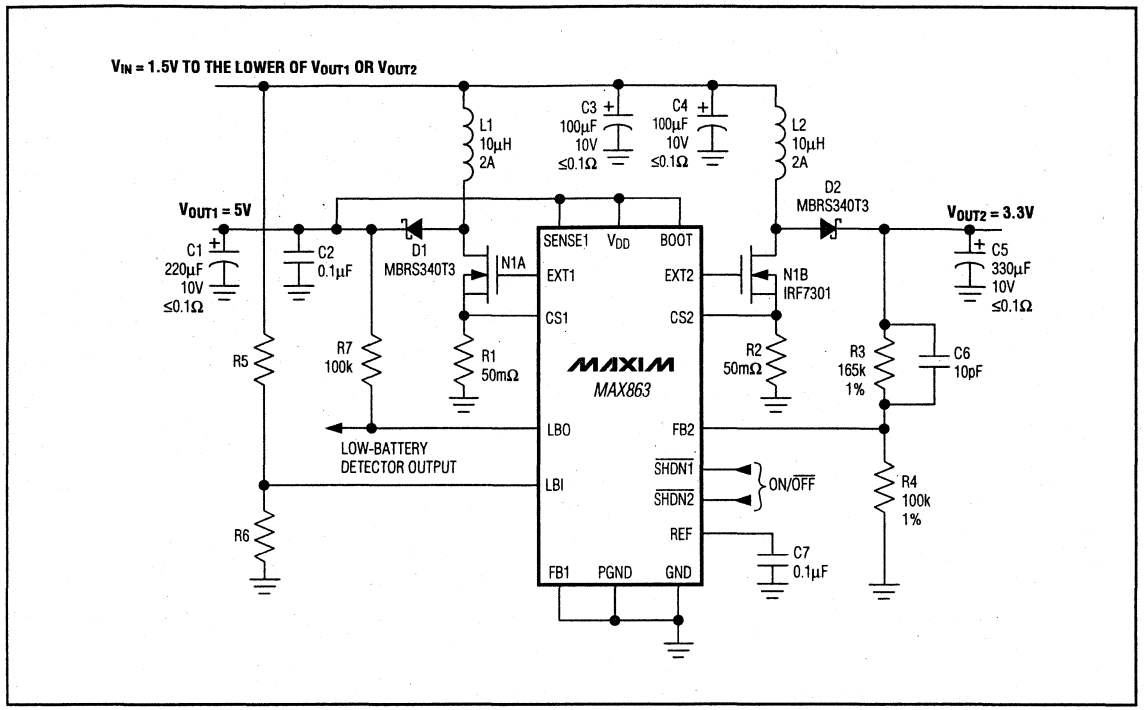


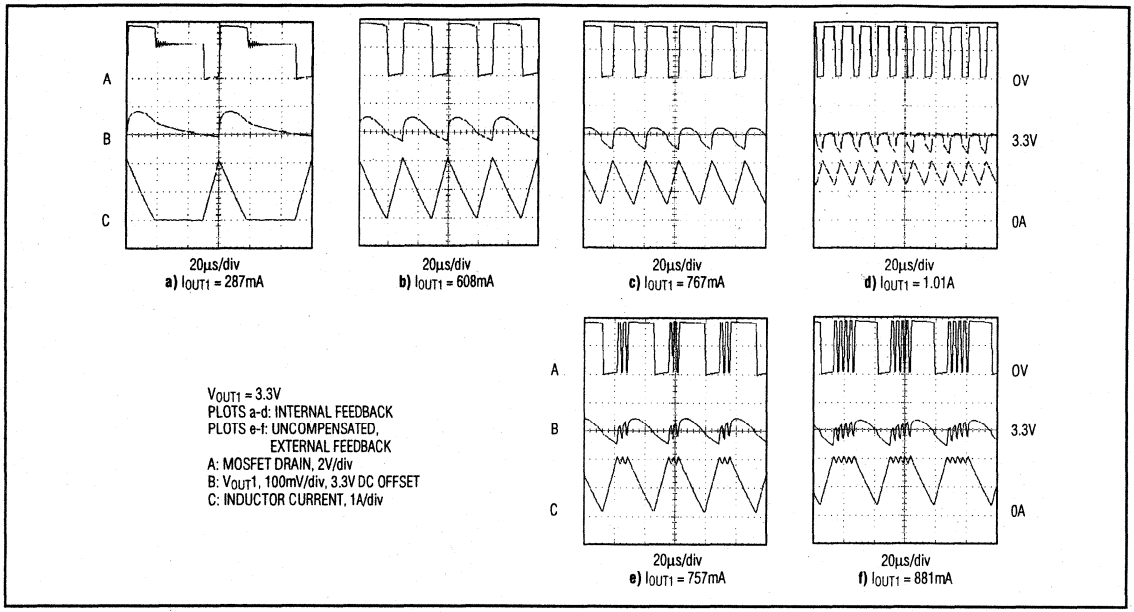
Figure 2. Bootstrapped Typical Operating Circuit

Continuous/Discontinuous-Conduction Modes

Each converter in the MAX863 determines from moment to moment whether to switch or not, waiting until the output voltage drops before initiating another cycle. Under light loads, the inductor current ramps to zero before the next cycle; this is discontinuous-conduction mode. Continuous-conduction mode occurs when the next switching cycle begins while current is still flowing through the inductor. The transition point between discontinuous- and continuous-conduction mode is determined by input and output voltages, and by the size of the inductor relative to the peak switching current. In general, reducing inductance toward the minimum recommended value pushes the transition point closer to the maximum load current. If the inductor value is low enough or the output/input voltage ratio high enough, the DC-DC converter may remain in discontinuous-conduction mode throughout its entire load range.

The MAX863 transitions into continuous-conduction mode in two ways, depending on whether preset or adjustable mode is used and how the external feedback network is compensated. Under light loads, the IC switches in single pulses (Figure 3a). The threshold of transition into continuous-conduction mode is reached when the inductor current waveforms are adjacent to one another, as shown in Figure 3b. As the load increases, the transition into continuous-conduction mode progresses by raising the minimum inductor current (Figures 3c, 3d). Depending on feedback compensation, transition into continuous-conduction mode may also progress with grouped pulses (Figures 3e, 3f). Pulse groups should be separated by less than two or three switching cycles. Output ripple should not be significantly more than the single-cycle no-load case.

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller



Figures 3a–3f. MAX863 Switching Waveforms During Transition into Continuous Conduction

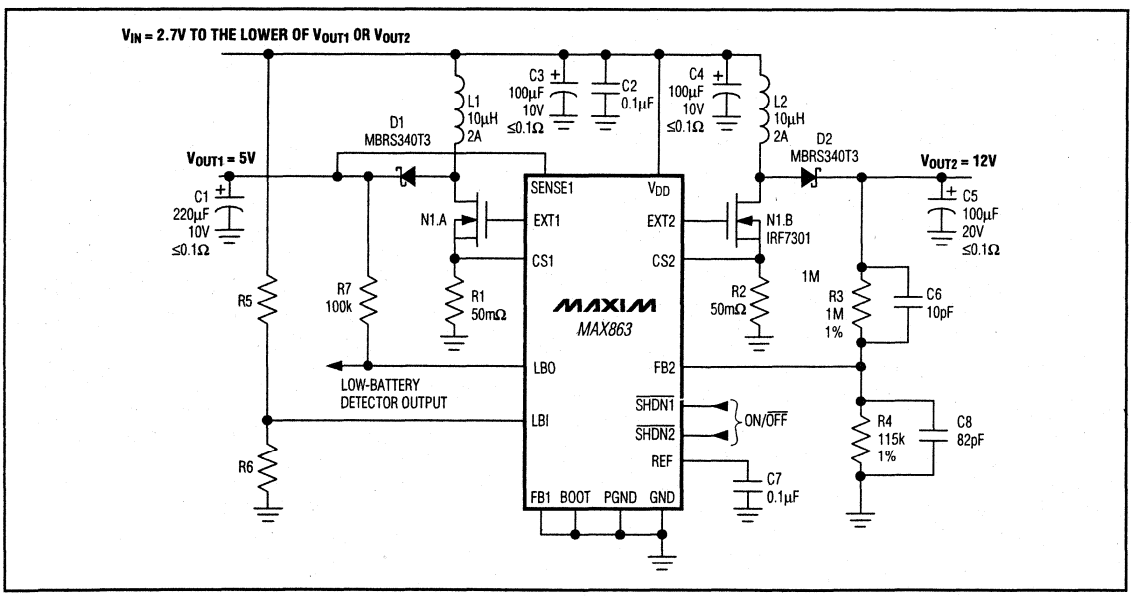


Figure 4a. Non-Bootstrapped Typical Operating Circuit

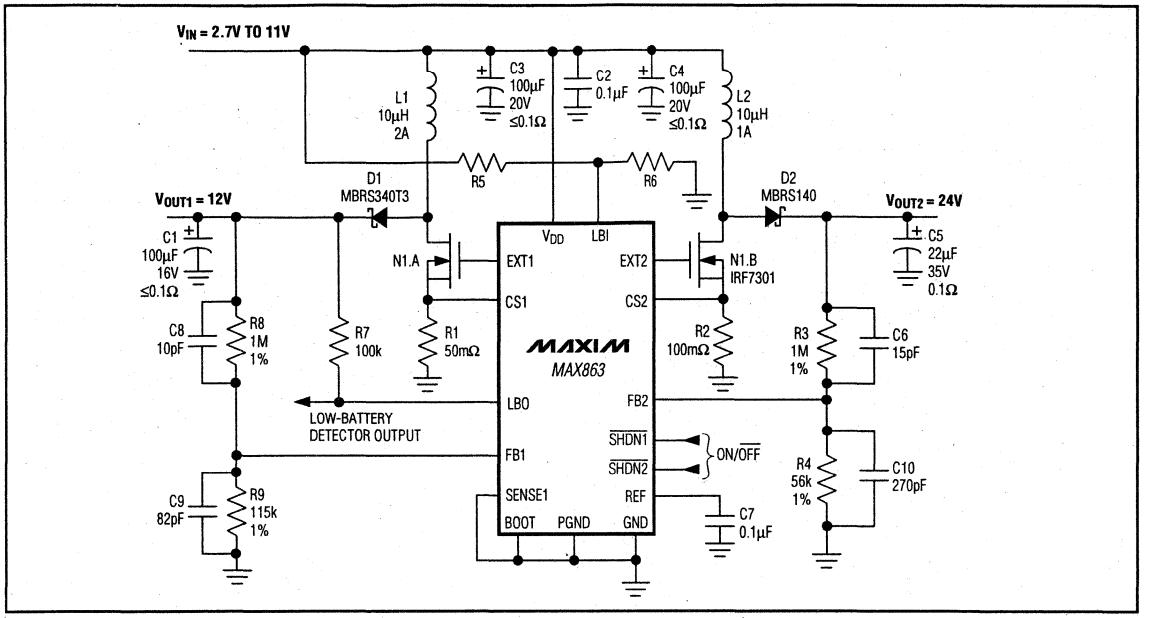


Figure 4b. Adjustable Non-Bootstrapped Typical Operating Circuit

Low-Voltage Start-Up Oscillator (BOOT Pin)

The MAX863 features a low-voltage start-up oscillator that guarantees start-up in bootstrapped configuration down to 1.5V. At these low supply voltages, the error comparator and internal biasing of the IC are locked out. The low-voltage oscillator switches the external MOSFET with around 30% duty cycle until the voltage at V_{DD} rises above 2.7V. At this point, the error comparator and one-shot timing circuitry turn on. The low-voltage oscillator is enabled by connecting the BOOT pin to V_{DD}. When BOOT is high, V_{DD} must be connected to V_{OUT1}.

Use the start-up oscillator in the bootstrapped configuration only, since the MAX863 operates in an open-loop state while the start-up oscillator is active. **When using a non-bootstrapped circuit configuration, connect BOOT to GND** to disable the start-up oscillator. This prevents the output from rising too high when V_{DD} is between 1.5V and 2.7V, such as during power-up and low-battery conditions.

Bootstrapped/Non-Bootstrapped Modes

Figures 2 and 4 show standard applications in bootstrapped and non-bootstrapped modes. In bootstrapped mode, the IC is powered from the output (V_{DD} is connected to OUT1, BOOT is connected to V_{DD}). Bootstrapped-mode operation is useful for increasing the gate drive to the MOSFETs in low-input-voltage applications, since EXT1 and EXT2 swing from V_{DD} to GND. Increasing the gate-drive voltage reduces MOSFET on-resistance, which improves efficiency and increases the load range. For supply voltages below 5V, bootstrapped mode is recommended. In bootstrapped mode, the output connected to V_{DD} must not exceed 11V. **If BOOT is high, V_{DD} must be connected to OUT1**.

In non-bootstrapped mode, the IC is powered by a direct connection from the input voltage to V_{DD}. Since the voltage swing applied to the gate of the external MOSFET is derived from V_{DD}, the external MOSFET on-resistance increases at low input voltages. The minimum input voltage is 2.7V. For operation down to 4V, use logic-level MOSFETs. For lower input voltages, use low-threshold logic-level MOSFETs. When both output voltages are set above 11V, non-bootstrapped mode is mandatory.

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

Shutdown Mode

The MAX863 has two shutdown inputs useful for conserving power and extending battery life. Driving SHDN1 or SHDN2 low turns off the corresponding DC-DC controller and reduces quiescent current. Driving both shutdown pins low turns off the reference, control, and biasing circuitry, putting the MAX863 in a 1µA shutdown mode. Connect SHDN1 and SHDN2 to V_{DD} for normal operation.

Design Procedure

Boost DC-DC converters using the MAX863 can be designed in a few simple steps to yield a working first-iteration design. All designs should be prototyped and tested prior to production. Table 1 provides a list of component suppliers.

Two design methods are included. The first uses graphs for selecting the peak current required for 3.3V, 5V, 12V, and 24V outputs. The second uses equations for selecting the peak current and inductor value in circuits with other outputs. When designing high-voltage, flyback, SEPIC, and autotransformer boost circuits, contact Maxim's Applications Department for the appropriate design equations.

Specify Design Objectives

For each of the two outputs, specify the output voltage and maximum load current, as well as maximum and

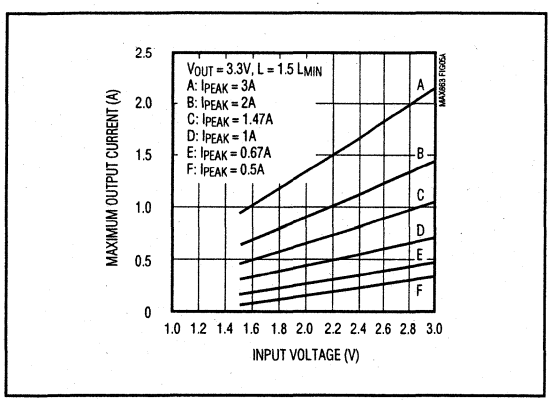


Figure 5a. Maximum Output Current vs. Input Voltage and IPEAK (VOUT = 3.3V)

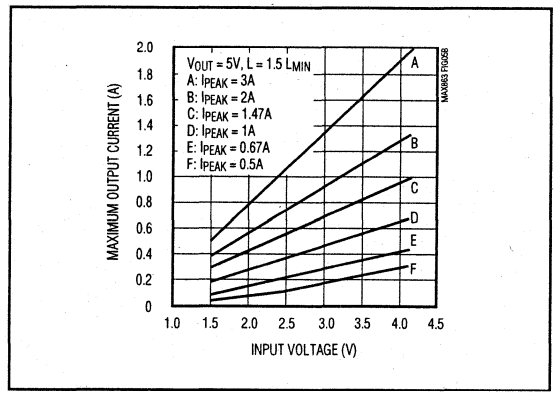


Figure 5b. Maximum Output Current vs. Input Voltage and IPEAK (VOUT = 5V)

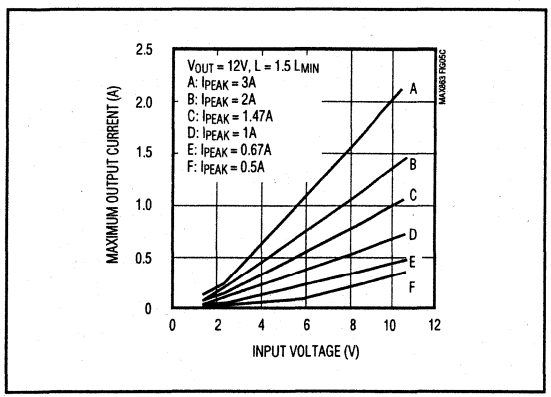


Figure 5c. Maximum Output Current vs. Input Voltage and IPEAK (VOUT = 12V)

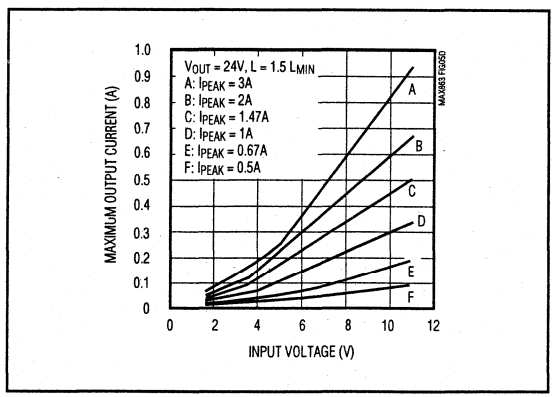


Figure 5d. Maximum Output Current vs. Input Voltage and IPEAK (VOUT = 24V)

minimum input voltages. Estimate the maximum input currents for each output based on the minimum input voltage and desired output power:

$$I_{IN,DC(MAX)} \cong \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN(MIN)}}$$

where 0.8 is chosen as a working value for the nominal efficiency. The power source must be capable of delivering the sum of the maximum input currents of both DC-DC converters.

Determine the Peak Switching Current (Graphical Method)

The peak switching current set by RSENSE determines the amount of energy transferred from the input on each cycle. For 3.3V, 5V, 12V, and 24V output circuits, the peak current can be selected using the output current curves shown in Figures 5a–5d.

Determine the Peak Switching Current and Inductance (Analytical Method)

The following boost-circuit equations are useful when the desired output voltage differs from those listed in Figure 5. They allow trading off peak current and inductor value in consideration of component availability, size, and cost.

Begin by calculating the minimum allowable ratio of inductor AC ripple current to peak current, ξ_{MIN} (Figure 6):

$$\xi_{MIN} = \frac{t_{OFF(MIN)}}{t_{ON(MAX)}} \times \frac{V_{OUT} - V_{IN(MIN)}}{V_{IN(MIN)}}$$

where $t_{OFF(MIN)}$ = 2µs and $t_{ON(MAX)}$ = 17.5µs.

Select a value for ξ greater than ξ_{MIN}. If ξ_{MIN} is less than 1, an acceptable choice is (ξ_{MIN} + 1) / 2. If ξ_{MIN} is greater than 1, values between ξ_{MIN} and 2 x ξ_{MIN} are acceptable (1.5 x ξ_{MIN}, for example). Values greater than 1 represent designs with full-load operation in discontinuous-conduction mode.

Now calculate the peak switching current and inductance. If $\xi_{MIN} \le \xi \le 1$, use:

$$I_{PEAK} = I_{IN,DC(MAX)} \times \frac{2}{2 - \xi}$$

For $\xi \ge 1\%$, use:

$$I_{PEAK} = 2 \times I_{IN,DC(MAX)} \times \frac{V_{OUT} + V_{IN} \times (\xi - 1)}{V_{OUT}}$$

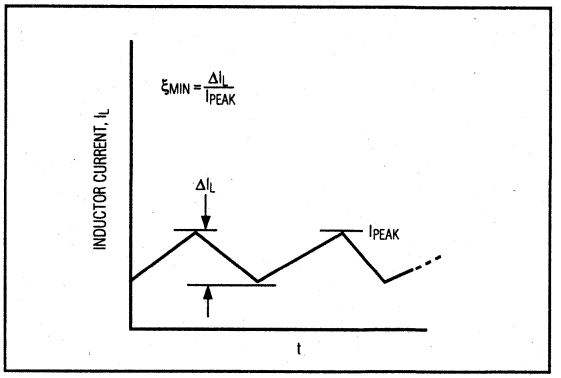


Figure 6. Ratio of Inductor AC Ripple Current to Peak Current

The suggested inductor value is:

$$L \cong \frac{\left(V_{OUT} - V_{IN(MIN)}\right) \times t_{OFF(MIN)}}{I_{PEAK} \times \xi}$$

Round L up to the next standard inductor value.

Choose RSENSE

The peak switching current is set by RSENSE (R1 and R2 in Figure 2):

$$R_{SENSE} \le \frac{V_{CS(MIN)}}{I_{PEAK}} = \frac{85mV}{I_{PEAK}}$$

Verify that you've selected the correct RSENSE by testing the prototype using the minimum input voltage while supplying the maximum output current. If the output voltage droops, then decrease the value of the current-sense resistor and adjust the other components as necessary.

The current-sense resistor must be a small, low-inductance type such as a surface-mount metal-strip resistor. Do not use wire-wound resistors, since their high inductance will corrupt the current feedback signal. In order to allow use of standard resistor values, round RSENSE to the next lowest value.

The current-sense resistor's power rating should be higher than:

$$R_{POWER\ RATING} = \frac{V^2_{CS(MAX)}}{R_{SENSE}}$$

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

Select the Inductor Component

Two essential parameters are required for selecting the inductor: inductance and current rating.

Inductance should be low enough to allow the MAX863 to reach the peak current limit during each cycle before the 17.5µs maximum on-time. Conversely, if the inductance is too low, the current will ramp up to a high level before the current-sense comparator can turn the switch off. A practical minimum on-time ($t_{ON(MIN)}$) is 1.5µs.

$$L_{MIN} \geq \frac{V_{IN(MAX)} \times t_{ON(MIN)}}{I_{PEAK}}$$

and:

$$L_{MAX} \geq \frac{V_{IN(MIN)} \times t_{ON(MAX)}}{I_{PEAK}}$$

When selecting I_{PEAK} using the graphs in Figure 5, choose inductance values between 1.3 and 1.7 times the minimum inductance value to provide a good trade-off between switching frequency and efficiency.

The lower of the inductor saturation current rating or heating current rating should be greater than I_{PEAK}:

$$I_{SATURATION} \text{ and } I_{HEATING} > I_{PEAK}$$

The saturation current limit is the current level where the magnetic field in the inductor has reached the maximum the core can sustain, and inductance starts to fall. The heating current rating is the maximum DC current the inductor can sustain without overheating. Disregarding the inductor's saturation current rating is a common mistake that results in poor efficiency, bad regulation, component overheating, or other problems. The resistance of the inductor windings should be comparable to or less than that of the current-sense resistor. To minimize radiated noise in sensitive applications, use a toroid, pot core, or shielded bobbin core inductor.

Choose the MOSFET Power Transistor

Use N-channel MOSFETs with the MAX863. When selecting an N-channel MOSFET, five important parameters are gate-drive voltage, drain-to-source breakdown voltage, current rating, on-resistance ($R_{DS(ON)}$), and total gate charge (Q_g).

The MAX863's EXT1 and EXT2 outputs swing from GND to V_{DD}. To ensure the external N-channel MOSFET is turned on sufficiently, use logic-level MOSFETs when V_{DD} is less than 8V and low-threshold logic-level MOSFETs when starting from input voltages below 4V. This also applies in bootstrapped mode to ensure start-up.

The MOSFET in a simple boost converter must withstand the output voltage plus the diode forward voltage. Voltage ratings in SEPIC, flyback, and autotransformer-boost circuits are more stringent. Choose a MOSFET with a maximum continuous drain-current rating higher than the current limit set by CS.

The two most significant losses contributing to the MOSFET's power dissipation are I^2R losses and switching losses. Reduce I^2R losses by choosing a MOSFET with low $R_{DS(ON)}$, preferably near the current-sense resistor value or lower.

A MOSFET with a gate charge (Q_g) of 50nC or smaller is recommended for rise and fall times less than 100ns on the EXT pins. Exceeding this limit results in slower MOSFET switching speeds and higher switching losses, due to a longer transition time through the linear region as the MOSFET turns on and off.

Select the Output Diode

Schottky diodes, such as the 1N5817–1N5822 family or surface-mount equivalents, are recommended. Ultra-fast silicon rectifiers with reverse recovery times around 60ns or faster, such as the MUR series, are acceptable but have greater forward voltage drop. Make sure that the diode's peak current rating exceeds the current limit set by R_{SENSE}, and that its breakdown voltage exceeds V_{OUT}. Schottky diodes are preferred for heavy loads, especially in low-voltage applications, due to their low forward voltage. For high-temperature applications, some Schottky diodes may be inadequate due to high leakage currents. In such cases, ultra-fast silicon rectifiers are recommended, although acceptable performance can often be achieved by using a Schottky diode with a higher reverse voltage rating.

Determine Input and Output Filter Capacitors

Low-ESR capacitors are recommended for both input bypassing and output filtering. Capacitor equivalent series resistance (ESR) is a major contributor to output ripple—typically 60% to 90%. Low-ESR tantalum capacitors offer a good tradeoff between price and performance. Ceramic and Sanyo OS-CON capacitors have the lowest ESR. Ceramic capacitors are often a good choice in high-output-voltage applications where large capacitor values may not be needed. Low-ESR aluminum-electrolytic capacitors are tolerable and can be used when cost is the primary consideration; however, standard aluminum-electrolytic capacitors should be avoided.

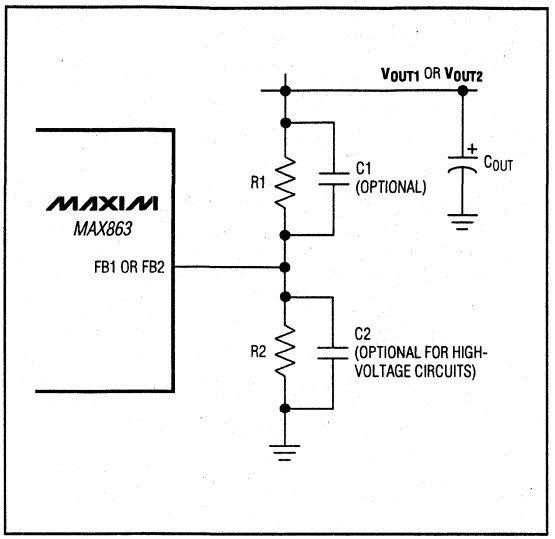


Figure 7. Adjustable Output Circuit

Voltage ripple is the sum of contributions associated with ESR and the capacitor value, as shown below:

$$V_{RIPPLE} \cong V_{RIPPLE,ESR} + V_{RIPPLE,C}$$

To simplify selection, assume that 75% of the ripple results from ESR and that 25% results from the capacitor value. Voltage ripple as a consequence of ESR is approximated by:

$$V_{RIPPLE,ESR} \cong R_{ESR} \times I_{PEAK}$$

so:

$$R_{ESR} \leq \frac{V_{RIPPLE,ESR}}{I_{PEAK}}$$

Estimate input and output capacitor values for a given voltage ripple as follows:

$$C \geq \frac{0.5L \times I^2_{PEAK}}{V_{RIPPLE,C} \times V}$$

where V is the input or output voltage, depending on which capacitor is being calculated.

Choose input capacitors with working voltage ratings over the maximum input voltage, and output capacitors with working voltage ratings higher than their respective outputs.

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
Inductors		
Coilcraft	(847) 639-6400	(847) 639-1469
Coiltronics	(561) 241-7876	(561) 241-9339
Dale Inductors	(605) 668-4131	(605) 665-1627
Sumida USA	(847) 956-0666	(847) 956-0702
MOSFETs and Diodes		
Central Semiconductor	(516) 435-1110	(516) 435-1824
International Rectifier	(310) 322-3331	(310) 322-3232
Motorola	(602) 303-5454	(602) 994-6430
Current-Sense Resistors		
Dale/Vishay	(402) 564-3131	(402) 563-6418
IRC	(512) 992-7900	(512) 992-3377
Electrolytic Capacitors		
AVX	(803) 946-0690	(803) 626-3123
Sanyo USA	(619) 661-6835	(619) 661-1055
Sprague	(603) 224-1961	(603) 224-1430
Large-Value Ceramic Capacitors		
Marcon/United Chemi-Con	(847) 696-2000	(847) 696-9278
TDK	(847) 390-4373	(847) 390-4428
Vishay/Vitramon	(203) 268-6261	(203) 452-5670

Add V_{DD} and REF Bypass Capacitors

Bypass the MAX863 with 0.1µF or higher value ceramic capacitors placed as close to the V_{DD}, REF, and GND pins as possible.

Set the Output Voltage

DC-DC converter 1 operates with a 3.3V, 5V, or adjustable output. For a preset output, connect SENSE1 to OUT1 (Figures 2 and 4a), then set FB1 to V_{DD} for 3.3V operation or to GND for 5V operation. For an adjustable output, connect a resistor voltage divider to the FB1 pin (Figure 7). In adjustable output circuits, connect SENSE1 to GND.

DC-DC converter 2 can be adjusted from very high voltages down to V_{IN} using external resistors connected to the FB2 pin, as shown in Figure 7. Select feedback resistor R2 in the 10kΩ to 500kΩ range. R1 is given by:

$$R1 = R2\left(\frac{V_{OUT}}{1.25V} - 1\right)$$

where 1.25V is the voltage of the internal reference.

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

Set Feedback Compensation

External voltage feedback to the MAX863 should be compensated for stray capacitance and EMI in the feedback network. Proper compensation is achieved when the MAX863 switches evenly, rather than in widely spaced bursts of pulses with large output ripple. Typically, lead compensation consisting of a 10pF to 220pF ceramic capacitor (C1 in Figure 7) across the upper feedback resistor is adequate. Circuits with V_{OUT} or V_{DD} greater than 7.5V may require a second capacitor across the lower feedback resistor. Initially, choose this capacitor so that R2C2 = R1C1. Set the final values of the compensation capacitors based on empirical analysis of a prototype.

PC Board Layout and Routing

High switching speeds and large peak currents make PC board layout an important part of design. Poor layout can cause excessive EMI and ground-bounce, both of which can cause instability or regulation errors by corrupting the voltage and current-feedback signals. Place power components as close together as possible, and keep their traces short, direct, and wide. Keep the extra copper on the board and integrate it into ground as an additional plane. On multi-layer boards, avoid interconnecting the ground pins of the power components using vias through an internal ground plane. Instead, place the ground pins of the power components close together and route them in a "star" ground configuration using component-side copper, then connect the star ground to the internal ground plane using multiple vias.

The current-sense resistor and voltage-feedback networks should be very close to the MAX863. Noisy traces, such as from the EXT pins, should be kept away from the voltage-feedback networks and isolated from them using grounded copper. Consult the MAX863 evaluation kit manual for a full PC board example.

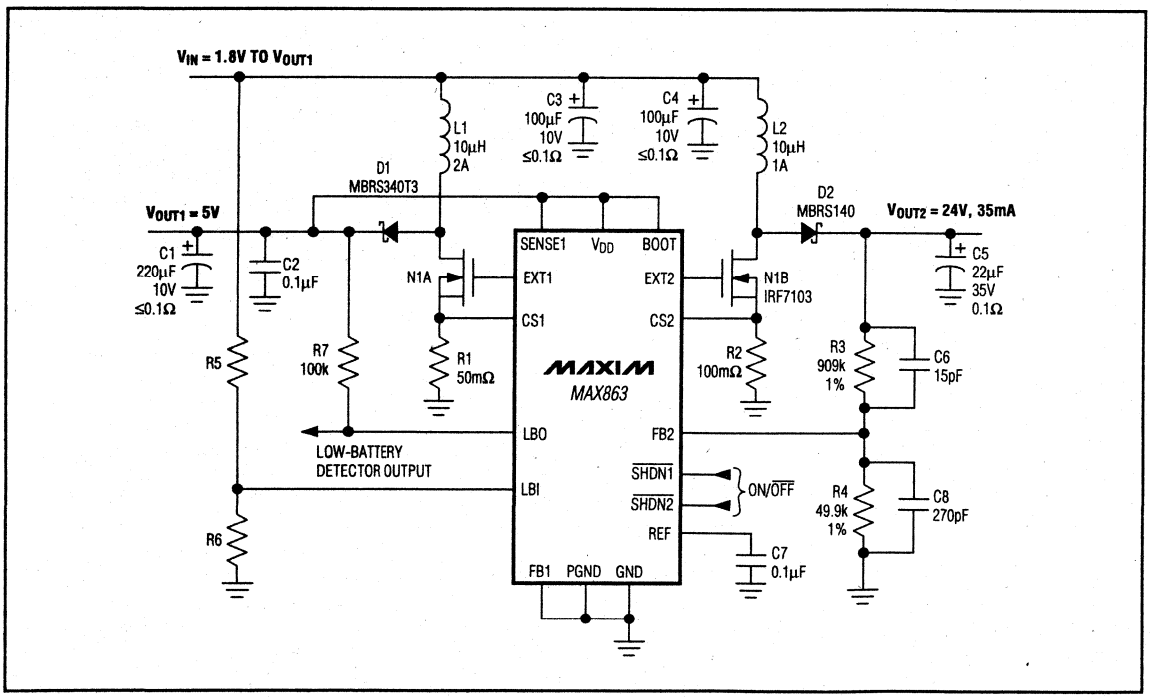


Figure 8. Bootstrapped 3.3V Logic and 24V LCD Bias Supply

Applications Information

Low-Input-Voltage Operation

When the voltage at V_{DD} falls and EXT1 or EXT2 approaches the MOSFET gate-to-source threshold voltage, the MOSFET may operate in its linear region and dissipate excessive power. Prolonged operation in this mode may damage the MOSFET if power dissipation ratings are inadequate. This effect is more significant in non-bootstrapped mode, but can occur in bootstrapped mode if the input voltage drops so low that it cannot support the load and causes the output voltage to collapse. To avoid this condition, use logic-level or low-threshold MOSFETs.

Starting Up Under Load

The *Typical Operating Characteristics* show the Bootstrapped-Mode Minimum Start-Up Input Voltage vs. Output Current graph. The MAX863 is not intended to start up under full load in bootstrapped mode with low input voltages.

Application Circuits

Bootstrapped 5V Logic and 24V LCD Bias Supply

The circuit in Figure 8 operates from two AA or AAA cells, and generates 5V (up to 750mA) for logic and 24V (up to 35mA) for an LCD bias supply. OUT1 is used to bootstrap the MAX863 for better MOSFET gate drive. V_{OUT1} can be set to 3.3V if low threshold MOSFETs are used.

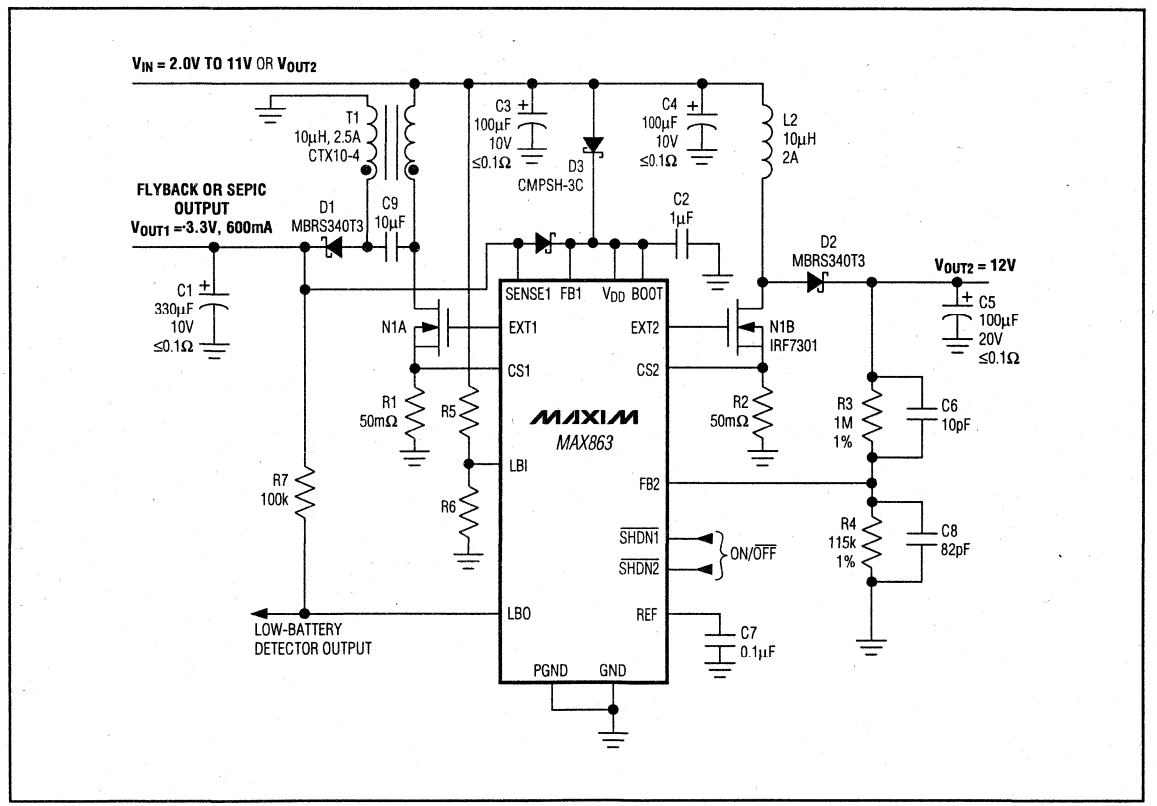


Figure 9. 3-Cell to 3.3V Step-Up/Step-Down Logic Supply with 12V for Flash Memory or Analog Functions

Dual, High-Efficiency, PFM, Step-Up DC-DC Controller

Step-Up/Down SEPIC Converter and 12V Supply

The circuit in Figure 9 provides a buck/boost function for applications where the input voltage range can be greater than or less than V_{OUT1}. It provides 3.3V (up to 600mA) or 5V, as well as 12V (up to 200mA at V_{IN} = 2.4V) for powering flash memory or analog functions.

The main output employs a SEPIC topology using a coupled inductor and a capacitor to transfer energy to the output. C2 must be a low-ESR type capable of withstanding high ripple current. Ceramic and Sanyo OS-CONs work well, but low-ESR aluminum electrolytics (which are less costly) are tolerable. Do not use a tantalum capacitor for C2. C2's voltage rating must be higher than the maximum input voltage. The MOSFET must withstand a voltage equal to the sum of the input and output voltages; i.e., when converting 11V to 3.3V, the MOSFET must withstand 14.3V. The dual Schottky diode D3 bootstraps power to the MAX863, allowing use of the low-voltage start-up oscillator, as well as improved gate-drive voltages during normal operation.

Chip Information

TRANSISTOR COUNT: 858

SUBSTRATE CONNECTED TO GND

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Regulated, 30mA-Output Charge-Pump DC-DC Inverter

General Description

The MAX868 charge-pump inverter provides a low-cost and compact means of generating a regulated negative output from a positive input at up to 30mA. The MAX868 requires only four ceramic capacitors and regulates its output by varying its switching frequency. This unique on-demand switching gives the MAX868 two advantages: very small capacitors and very low quiescent supply current. For example, at heavy loads, the MAX868 transfers energy from the input to the output by switching small 0.1µF capacitors at up to 500kHz. At light loads, it switches more slowly, thereby using only 35µA quiescent supply current.

The MAX868 comes in a 10-pin µMAX package (half the size of a standard 8-pin SO and only 1.11mm high). A logic-controlled shutdown turns off the output and reduces supply current to 0.1µA. Input range is 1.8V to 5.5V. The regulated output can be set from 0.0V to (-2 x V_{IN}) using two resistors.

Applications

- Small LCD panels
- Cell Phones
- Cordless Phones
- Modems
- Camcorders
- PCS Phones
- Handy-Terminals, PDAs
- Medical Instruments
- Battery-Operated Equipment

Features

- ♦ **Regulated Negative Output Voltage (up to -2 x V_{IN})**
- ♦ **Ultra-Small 10-pin µMAX Package**
- ♦ **On-Demand Switching at up to 500kHz**
- ♦ **35µA Quiescent Supply Current**
- ♦ **Requires Only Four Small External Capacitors**
- ♦ **1.8V to 5.5V Input Voltage Range**
- ♦ **0.1µA Logic-Controlled Shutdown**
- ♦ **Up to 30mA Output Current**

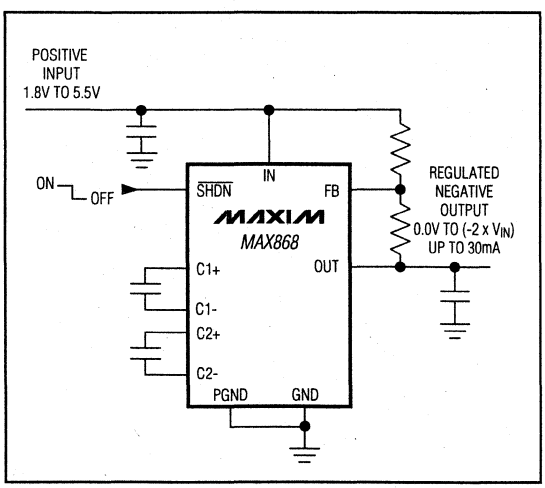
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX868C/D	0°C to +70°C	Dice*
MAX868EUB	-40°C to +85°C	10 µMAX

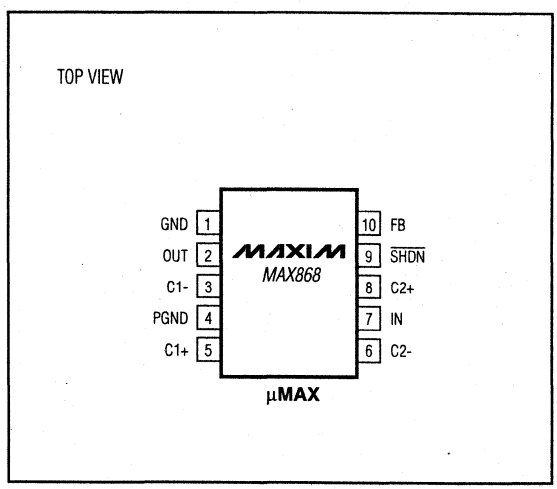
**Dice are tested at T_A = +25°C, DC parameters only.*

4

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

MAXIM

2A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

General Description

The MAX869L P-channel load switch features an accurate user-set current limit and low on-resistance. This switch is designed to protect your power source from shorts and surges by limiting current and preventing the system supply from being pulled low. The input voltage range is 2.7V to 5.5V.

The MAX869L features a 2A, 45mΩ switch controlled by a logic signal. Current-limit accuracy is ±21%, and can be set from 400mA to 2.4A using a single resistor.

The device has a low 12µA quiescent supply current, which reduces to 2µA max in shutdown. It features thermal-shutdown protection and a logic-signal output pin ($\overline{FAULT}$) that signals when there is an overcurrent or overtemperature condition.

For other devices in this family, consult the *Selector Guide*.

Features

- **Very Small Footprint (16-pin QSOP is the same size as an 8-pin SO)**
- **Low Resistance: 45mΩ at 3V**
- **±21%-Accurate, User-Set Current Limit**
- **12µA (typ) Quiescent Current**
- **0.01µA (typ) Shutdown Current**
- **0.04µA (typ) Leakage to Output when Switch is Off**
- **2.7V to 5.5V Input Range**
- **Thermal Shutdown**
- **$\overline{FAULT}$ Output**

Selector Guide

PART	R_{ON} AT 3V (mΩ)	NOMINAL CURRENT (A)	COUNT	PACKAGE
MAX869L	45	2	Single	16 QSOP
MAX890L	90	1	Single	8 SO
MAX891L	150	0.5	Single	8 µMAX
MAX892L	300	0.25	Single	8 µMAX
MAX894L	150	0.5	Dual	8 SO
MAX895L	300	0.25	Dual	8 SO

Ordering Information

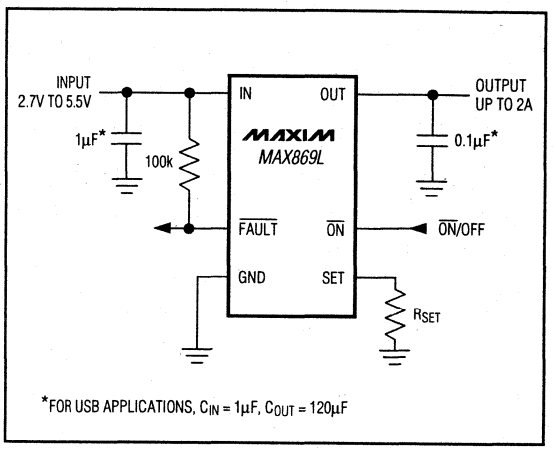
PART	TEMP. RANGE	PIN-PACKAGE
MAX869LC/D	0°C to +70°C	Dice*
MAX869LEEE	-40°C to +85°C	16 QSOP

**Dice are specified at T_A = +25°C.*

Applications

Universal Serial Bus (USB)
Notebook Computers
Personal Communicators
Palmtop Computers
Hand-Held Instruments
Portable Medical Instruments

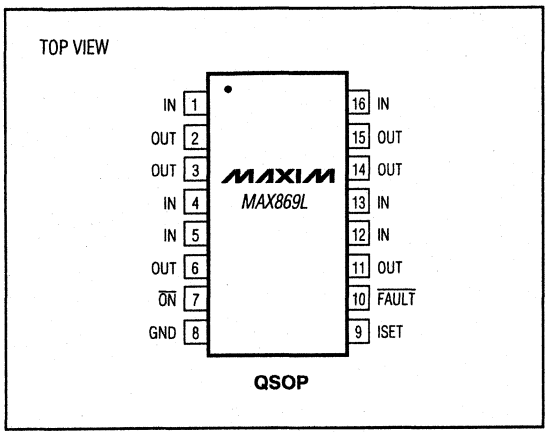
Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

2A, Current-Limited, High-Side P-Channel Switch with Thermal Shutdown

Pin Configuration



19-1240; Rev 0; 6/97

MAXIM

Switched-Capacitor Voltage Inverters

General Description

The ultra-small MAX870/MAX871 monolithic, CMOS charge-pump inverters accept input voltages ranging from +1.4V to +5.5V. The MAX870 operates at 125kHz, and the MAX871 operates at 500kHz. Their high efficiency (90%) and low operating current (0.7mA for the MAX870) make these devices ideal for both battery-powered and board-level voltage-conversion applications.

Oscillator control circuitry and four power MOSFET switches are included on-chip. A typical MAX870/MAX871 application is generating a -5V supply from a +5V logic supply to power analog circuitry. Both parts come in a 5-pin SOT23-5 package and can deliver 25mA with a voltage drop of 500mV.

For applications requiring more power, the MAX860 delivers up to 50mA with a voltage drop of 600mV, in a space-saving µMAX package.

Applications

Local -5V Supply from 5V Logic Supply

Small LCD Panels

Cell Phones

Medical Instruments

Handy-Terminals, PDAs

Battery-Operated Equipment

Features

- **5-Pin SOT23-5 Package**
- **99% Voltage Conversion Efficiency**
- **Invert Input Supply Voltage**
- **0.7mA Quiescent Current (MAX870)**
- **+1.4V to +5.5V Input Voltage Range**
- **Require Only Two Capacitors**
- **25mA Output Current**
- **Shutdown Control**

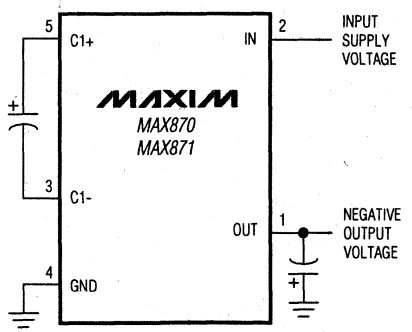
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX870C/D	0°C to +70°C	Dice*	—
MAX870EUK	-40°C to +85°C	5 SOT23-5	ABZN
MAX871C/D	0°C to +70°C	Dice*	—
MAX871EUK	-40°C to +85°C	5 SOT23-5	ABZO

** Dice are tested at T_A = +25°C.*

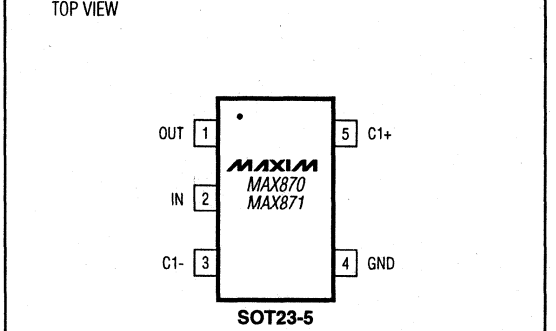
4

Typical Operating Circuit



NEGATIVE VOLTAGE CONVERTER

Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

Switched-Capacitor Voltage Inverters

ABSOLUTE MAXIMUM RATINGS

IN to GND .....+6.0V to -0.3V
OUT to GND .....-6.0V to +0.3V
C1+ .....(V_{IN} + 0.3V) to -0.3V
C1- .....(V_{OUT} - 0.3V) to +0.3V
OUT Output Current 50mA
OUT Short Circuit to GND .....Indefinite

Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range
MAX870EUK/MAX871EUK .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V, C1 = C2 = 1µF (MAX870), C1 = C2 = 0.33µF (MAX871), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS				MIN	TYP	MAX	UNITS
Supply Current	T_A = +25°C		MAX870			0.7	1.0	mA
			MAX871			2.7	3.8	
Minimum Supply Voltage	R_{LOAD} = 10kΩ		T_A = +25°C		1.4	1.0		V
			T_A = 0°C to + 85°C		1.5			
Maximum Supply Voltage	R_{LOAD} = 10kΩ						5.5	V
Oscillator Frequency	T_A = +25°C		MAX870		81	125	169	kHz
			MAX871		325	500	675	
Power Efficiency	R_{LOAD} = 500kΩ, T_A =+25°C		MAX870			90		%
			MAX871			75		
Voltage Conversion Efficiency	R_{LOAD} = ∞, T_A =+25°C		MAX870		98	99.3		%
			MAX871		96	99		
Output Resistance (Note 1)	I_{OUT} = 5mA	T_A = +25°C	MAX870	C1 = C2 = 1µF		20	50	Ω
				C1 = C2 = 0.47µF		25		
			MAX871	C1 = C2 = 0.33µF		20	50	
				C1 = C2 = 0.22µF		25		
				C1 = C2 = 0.1µF		35		
		T_A = 0°C to + 85°C					65	

Note 1: Capacitor contribution is approximately 20% of the output impedance [ESR + 1 / (pump frequency x capacitance)].

ELECTRICAL CHARACTERISTICS

(V_{IN} = +5V, C1 = C2 = 1µF (MAX870), C1 = C2 = 0.33µF (MAX871), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

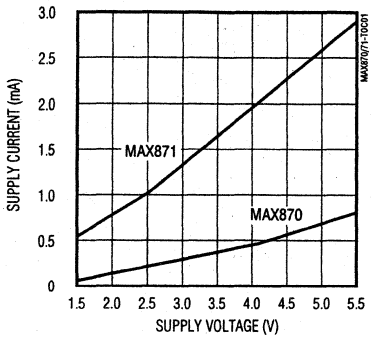
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	MAX870				1.3	mA
	MAX871				4.4	
Minimum Supply-Voltage Range	R_{LOAD} = 10kΩ		1.6			V
Maximum Supply-Voltage Range	R_{LOAD} = 10kΩ				5.5	V
Oscillator Frequency	MAX870		56		194	kHz
	MAX871		225		775	
Output Resistance	I_{OUT} = 5mA				65	Ω
Voltage Conversion Efficiency	R_{LOAD} = ∞	MAX870	97			%
		MAX871	95			

Note 2: All -40°C to +85°C specifications are guaranteed by design.

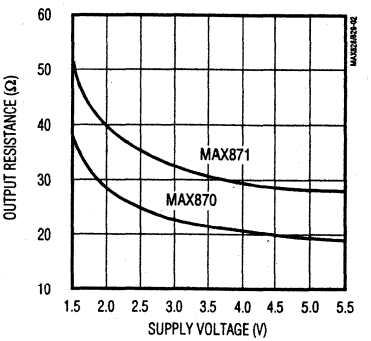
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = +5V, C1 = C2 = C3, T_A = +25°C, unless otherwise noted.)

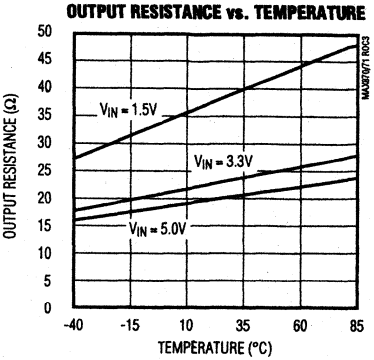
SUPPLY CURRENT vs. SUPPLY VOLTAGE



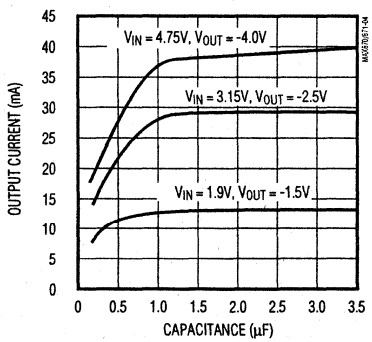
OUTPUT RESISTANCE vs. SUPPLY VOLTAGE



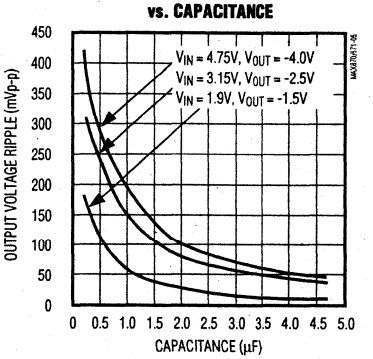
MAX870 OUTPUT RESISTANCE vs. TEMPERATURE



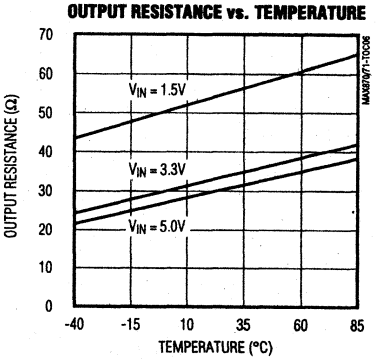
MAX870 OUTPUT CURRENT vs. CAPACITANCE



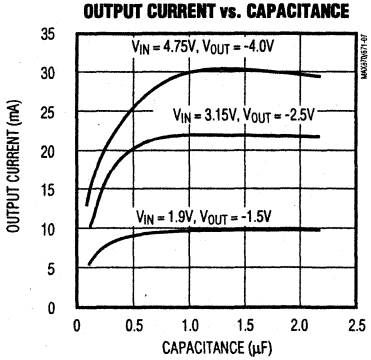
MAX870 OUTPUT VOLTAGE RIPPLE vs. CAPACITANCE



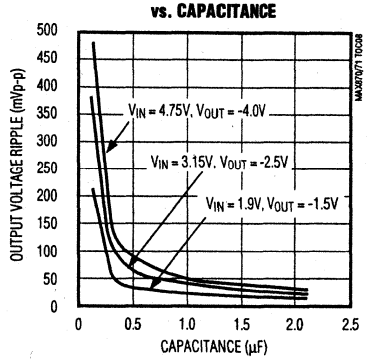
MAX871 OUTPUT RESISTANCE vs. TEMPERATURE



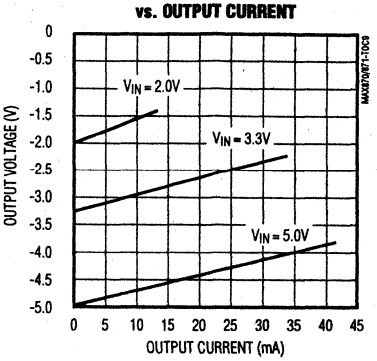
MAX871 OUTPUT CURRENT vs. CAPACITANCE



MAX871 OUTPUT VOLTAGE RIPPLE vs. CAPACITANCE



MAX870 OUTPUT VOLTAGE vs. OUTPUT CURRENT

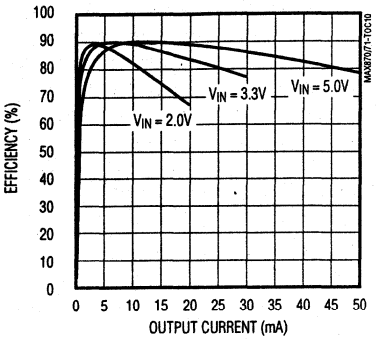


Switched-Capacitor Voltage Inverters

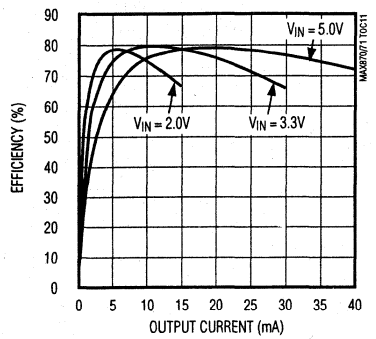
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +5V, C1 = C2 = C3, T_A = +25°C, unless otherwise noted.)

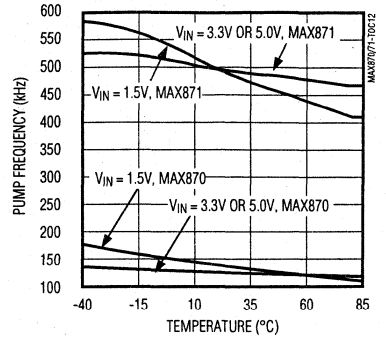
MAX870
EFFICIENCY vs. OUTPUT CURRENT



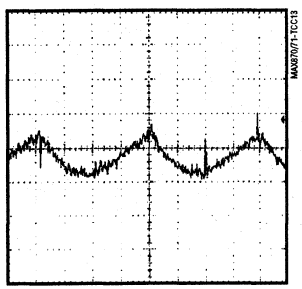
MAX871
EFFICIENCY vs. OUTPUT CURRENT



PUMP FREQUENCY vs. TEMPERATURE

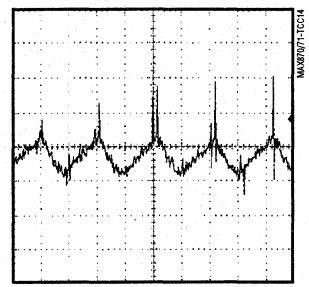


MAX870
OUTPUT NOISE AND RIPPLE



V_{IN} = 3.3V, V_{OUT} = -3.18V, I_{OUT} = 5mA,
20mV/div, AC COUPLED

MAX871
OUTPUT NOISE AND RIPPLE



V_{IN} = 3.3V, V_{OUT} = -3.14V, I_{OUT} = 5mA,
20mV/div, AC COUPLED

Pin Description

PIN	NAME	FUNCTION
1	OUT	Inverting Charge-Pump Output
2	IN	Positive Power-Supply Input
3	C1-	Flying Capacitor's Negative Terminal
4	GND	Ground
5	C1+	Flying Capacitor's Positive Terminal

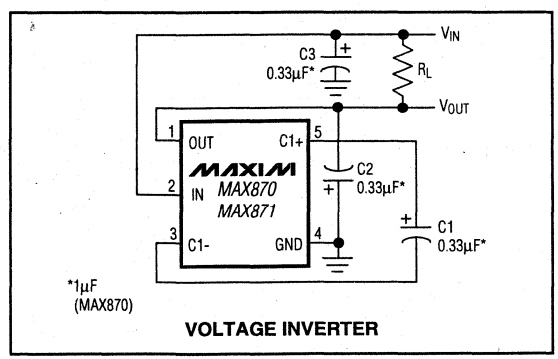


Figure 1. Test Circuit

Detailed Description

The MAX870/MAX871 capacitive charge pumps invert the voltage applied to their input. For highest performance, use low equivalent series resistance (ESR) capacitors (e.g., ceramic).

During the first half-cycle, switches S2 and S4 open, switches S1 and S3 close, and capacitor C1 charges to the voltage at IN (Figure 2). During the second half-cycle, S1 and S3 open, S2 and S4 close, and C1 is level shifted downward by V_{IN} volts. This connects C1 in parallel with the reservoir capacitor C2. If the voltage across C2 is smaller than the voltage across C1, then charge flows from C1 to C2 until the voltage across C2 reaches $-V_{IN}$. The actual voltage at the output is more positive than $-V_{IN}$, since switches S1–S4 have resistance and the load drains charge from C2.

Charge-Pump Output

The MAX870/MAX871 are not voltage regulators: the charge pump's output source resistance is approximately 20Ω at room temperature (with V_{IN} = +5V), and V_{OUT} approaches -5V when lightly loaded. V_{OUT} will droop toward GND as load current increases. The droop of the negative supply (V_{DROOP-}) equals the current draw from OUT (I_{OUT}) times the negative converter's source resistance (RS-):

$$V_{DROOP-} = I_{OUT} \times RS-$$

The negative output voltage will be:

$$V_{OUT} = -(V_{IN} - V_{DROOP-})$$

Efficiency Considerations

The power efficiency of a switched-capacitor voltage converter is affected by three factors: the internal losses in the converter IC, the resistive losses of the pump capacitors, and the conversion losses during charge transfer between the capacitors. The total power loss is:

$$\Sigma P_{LOSS} = P_{INTERNAL\ LOSSES} + P_{SWITCH\ LOSSES} + P_{PUMP\ CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES}$$

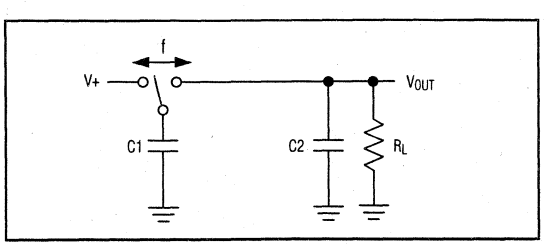


Figure 3a. Switched-Capacitor Model

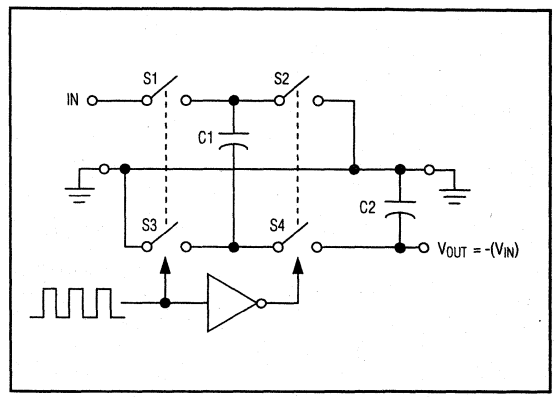


Figure 2. Ideal Voltage Inverter

The internal losses are associated with the IC's internal functions, such as driving the switches, oscillator, etc. These losses are affected by operating conditions such as input voltage, temperature, and frequency.

The next two losses are associated with the voltage converter circuit's output resistance. Switch losses occur because of the on-resistance of the MOSFET switches in the IC. Charge-pump capacitor losses occur because of their ESR. The relationship between these losses and the output resistance is as follows:

$$P_{PUMP\ CAPACITOR\ LOSSES} + P_{CONVERSION\ LOSSES} = I_{OUT}^2 \times R_{OUT}$$

$$R_{OUT} \cong \frac{1}{(f_{OSC}) \times C1} + 2R_{SWITCHES} + 4ESR_{C1} + ESR_{C2}$$

where f_{OSC} is the oscillator frequency. The first term is the effective resistance from an ideal switched-capacitor circuit. See Figures 3a and 3b.

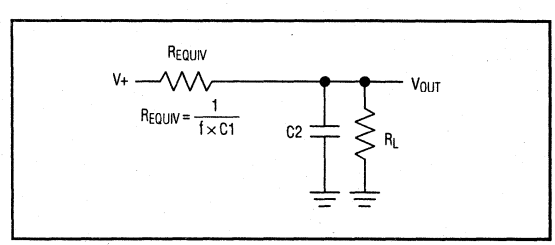


Figure 3b. Equivalent Circuit

Switched-Capacitor Voltage Inverters

Conversion losses occur during the charge transfer between C1 and C2 when there is a voltage difference between them. The power loss is:

$$P_{CONV.LOSS} = [1/2\ C1\left(V_{IN}^2 - V_{OUT}^2\right) + 1/2\ C2\left(V_{RIPPLE}^2 - 2V_{OUT}V_{RIPPLE}\right)] \times f_{OSC}$$

Applications Information

Capacitor Selection

To maintain the lowest output resistance, use capacitors with low ESR (Table 1). The charge-pump output resistance is a function of C1's and C2's ESR. Therefore, minimizing the charge-pump capacitor's ESR minimizes the total output resistance.

Flying Capacitor (C1)

Increasing the flying capacitor's size reduces the output resistance. Small C1 values increase the output resistance. Above a certain point, increasing C1's capacitance has a negligible effect, because the output resistance becomes dominated by the internal switch resistance and capacitor ESR.

Output Capacitor (C2)

Increasing the output capacitor's size reduces the output ripple voltage. Decreasing its ESR reduces both output resistance and ripple. Smaller capacitance values can be used with light loads if higher output ripple can be tolerated. Use the following equation to calculate the peak-to-peak ripple:

$$V_{RIPPLE} = \frac{I_{OUT}}{f_{OSC} \times C2} + 2 \times I_{OUT} \times ESR_{C2}$$

Input Bypass Capacitor

Bypass the incoming supply to reduce its AC impedance and the impact of the MAX870/MAX871's switching noise. The recommended bypassing depends on the circuit configuration and on where the load is connected.

When the inverter is loaded from OUT to GND, current from the supply switches between 2 x I_{OUT} and zero. Therefore, use a large bypass capacitor (e.g., equal to the value of C1) if the supply has a high AC impedance.

When the inverter is loaded from IN to OUT, the circuit draws 2 x I_{OUT} constantly, except for short switching spikes. A 0.1µF bypass capacitor is sufficient.

Voltage Inverter

The most common application for these devices is a charge-pump voltage inverter (Figure 1). This application requires only two external components—capacitors C1 and C2—plus a bypass capacitor, if necessary. Refer to the *Capacitor Selection* section for suggested capacitor types.

Cascading Devices

Two devices can be cascaded to produce an even larger negative voltage (Figure 4). The unloaded output voltage is normally -2 x V_{IN}, but this is reduced slightly by the output resistance of the first device multiplied by the quiescent current of the second. When cascading more than two devices, the output resistance rises dramatically. For applications requiring larger negative voltages, see the MAX864 and MAX865 data sheets.

Paralleling Devices

Paralleling multiple MAX870s or MAX871s reduces the output resistance. Each device requires its own pump capacitor (C1), but the reservoir capacitor (C2) serves all devices (Figure 5). Increase C2's value by a factor of n, where n is the number of parallel devices. Figure 5 shows the equation for calculating output resistance.

Combined Doubler/Inverter

In the circuit of Figure 6, capacitors C1 and C2 form the inverter, while C3 and C4 form the doubler. C1 and C3 are the pump capacitors; C2 and C4 are the reservoir

Table 1. Low-ESR Capacitor Manufacturers

PRODUCTION METHOD	MANUFACTURER	SERIES	PHONE	FAX
Surface-Mount Tantalum	AVX	TPS series	(803) 946-0690	(803) 626-3123
	Matsuo	267 series	(714) 969-2491	(714) 960-6492
	Sprague	593D, 595D series	(603) 224-1961	(603) 224-1430
Surface-Mount Ceramic	AVX	X7R	(803) 946-0690	(803) 626-3123
	Matsuo	X7R	(714) 969-2491	(714) 960-6492

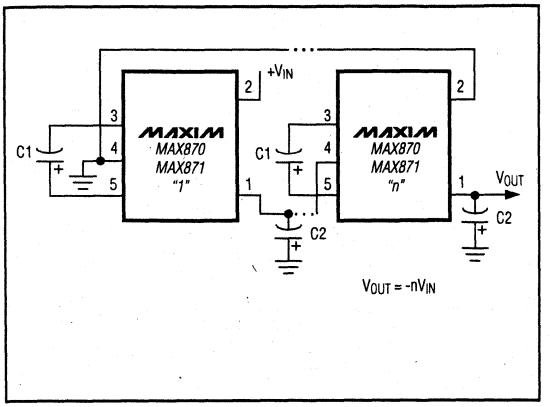


Figure 4. Cascading MAX870s or MAX871s to Increase Output Voltage

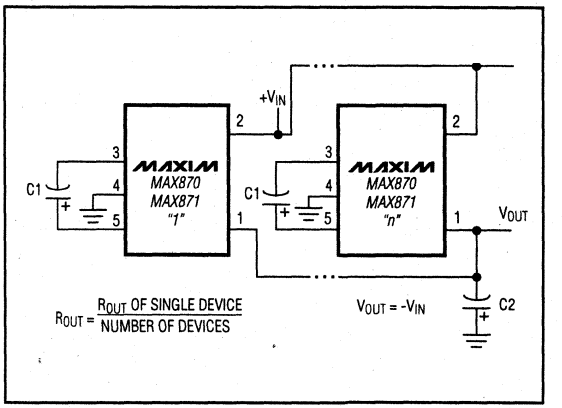


Figure 5. Paralleling MAX870s or MAX871s to Reduce Output Resistance

capacitors. Because both the inverter and doubler use part of the charge-pump circuit, loading either output causes both outputs to decline toward GND. Make sure the sum of the currents drawn from the two outputs does not exceed 40mA.

Heavy Output Current Loads

Under heavy loads, where higher supply is sourcing current into OUT, the OUT supply must not be pulled above ground. Applications that sink heavy current into OUT require a Schottky diode (1N5817) between GND and OUT, with the anode connected to OUT (Figure 7).

Layout and Grounding

Good layout is important, primarily for good noise performance. To ensure good layout, mount all components as close together as possible, keep traces short to minimize parasitic inductance and capacitance, and use a ground plane.

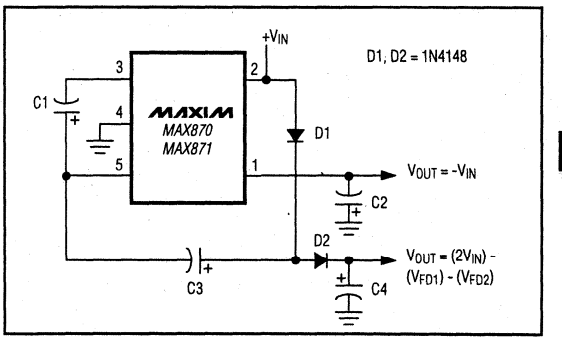


Figure 6. Combined Doubler and Inverter

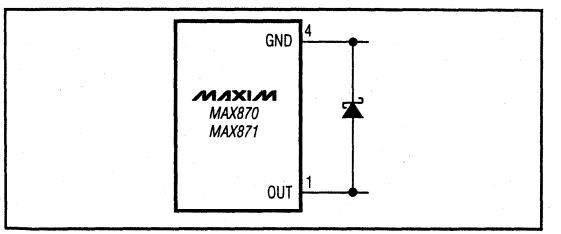


Figure 7. High V- Load Current

Switched-Capacitor Voltage Inverters

Shutdown Control

If shutdown control is necessary, use the circuit in Figure 8. The output resistance of the MAX870/MAX871 will typically be 20Ω plus two times the output resistance of the buffer driving IN. The 0.1µF capacitor at the IN pin absorbs the transient input currents of the MAX870/MAX871.

The output resistance of the buffer driving the IN pin can be reduced by connecting multiple buffers in parallel. The polarity of the shutdown signal can also be changed by using a noninverting buffer to drive IN.

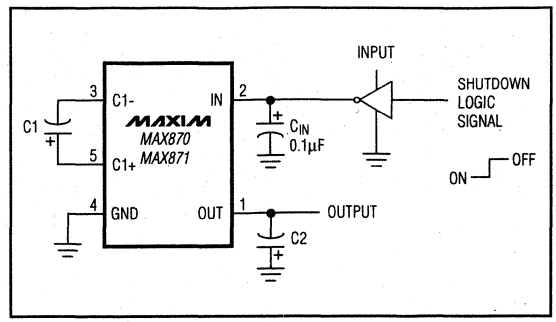


Figure 8. Shutdown Control

Chip Information

TRANSISTOR COUNT: 58

SUBSTRATE CONNECTED TO IN

MAXIM

Low-Noise Bias Supply for GaAsFET PA with Power-OK in µMAX

General Description

The MAX881R low-noise, inverting power supply is designed for biasing GaAsFET power amplifiers in portable wireless applications. This device is a charge-pump inverter followed by a negative linear regulator. The input voltage range is 2.5V to 5.5V. The output can be set, using two resistors, to any voltage from -0.5V to -V_{IN}. It can deliver up to 4mA. The internal linear regulator also filters the output to 1mVp-p ripple and noise.

Other features include a power-OK ($\overline{POK}$) output that signals when the negative voltage is within 10% of its set point. It protects the GaAsFET by not allowing power to be applied to the GaAsFET's drain until it is properly biased. The signal can be routed either to a microcontroller or directly to a switch at the GaAsFET drain.

Applications

Cell Phones
PCS Phones
PHS Phones
Wireless Handsets
Wireless Modems
Two-Way Pagers
Mobile Radios
Wireless Computers

Features

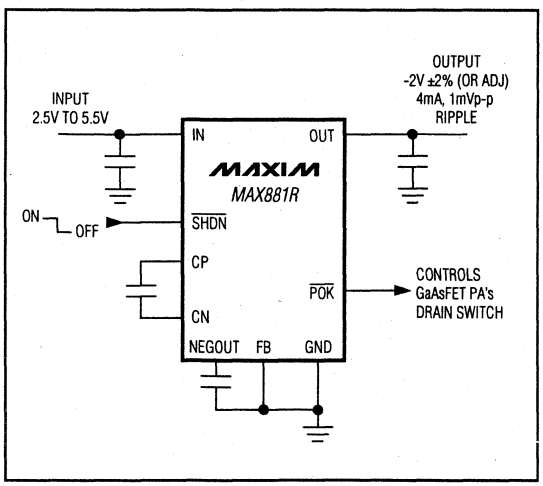
- **1mVp-p Low-Noise Output Voltage Ripple**
- **Power-OK Signal to Control Drain Switch on GaAsFET**
- **Small µMAX Package**
- **1µA Logic-Controlled Shutdown**
- **1ms Guaranteed Start-Up**
- **2.5V to 5.5V Input**
- **-0.5V to -V_{IN} Output at up to 4mA**
- **Operates with 0.22µF Capacitors (no inductors needed)**

Ordering Information

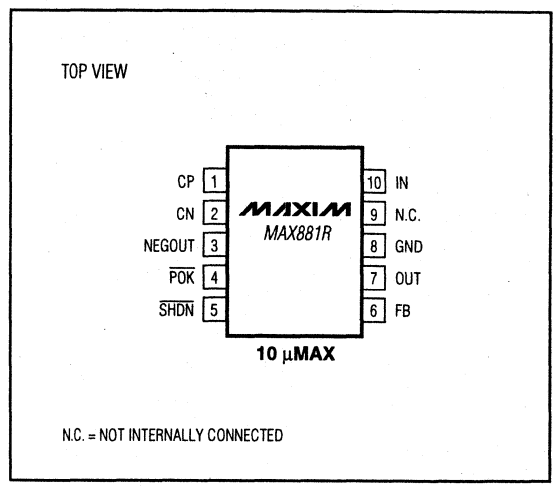
PART	TEMP. RANGE	PIN-PACKAGE
MAX881RC/D	0°C to +70°C	Dice*
MAX881REUB	-40°C to +85°C	10 µMAX

**Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

19-1223; Rev 0; 4/97

MAXIM

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

General Description

The MAX891L/MAX892L smart, low-voltage, P-channel, MOSFET power switches are intended for high-side load-switching applications. These switches operate with inputs from 2.7V to 5.5V, making them ideal for both 3V and 5V systems. Internal current-limiting circuitry protects the input supply against overload. Thermal-overload protection limits power dissipation and junction temperatures.

The MAX891L/MAX892L's maximum current limits are 500mA and 250mA, respectively. The current limit through the switch is programmed with a resistor from SET to ground. When the switch is on, the quiescent supply current is a low 13µA. When the switch is off, the quiescent current decreases to 0.1µA.

The MAX891L/MAX892L are available in 8-pin µMAX packages.

Applications

PCMCIA Slots

Access Bus Slots

Portable Equipment

Features

- ♦ **Ultra-Small µMAX Package—Only 1.11mm High**
- ♦ **2.7V to 5.5V Input Range**
- ♦ **Programmable Current Limit**
- ♦ **Low 13µA Quiescent Current at V_{IN} = 3.3V, 0.1µA Switch Off**
- ♦ **Thermal Shutdown**
- ♦ **$\overline{FAULT}$ Indicator Output**
- ♦ **On-Resistances:**
  0.12Ω (MAX891L)
  0.25Ω (MAX892L)

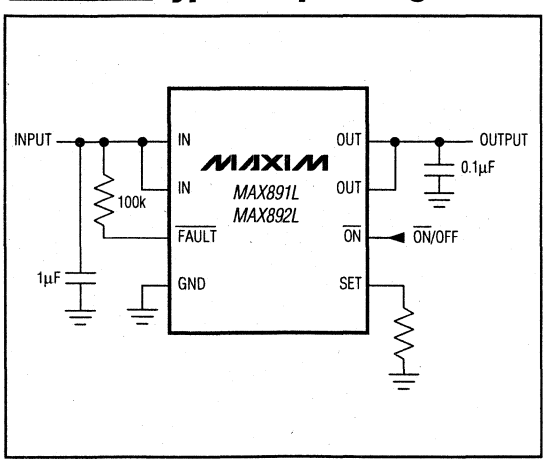
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	CURRENT LIMIT
MAX891LC/D	0°C to +70°C	Dice**	500mA
MAX891LEUA*	-40°C to +85°C	8 µMAX	500mA
MAX892LC/D	0°C to +70°C	Dice**	250mA
MAX892LEUA*	-40°C to +85°C	8 µMAX	250mA

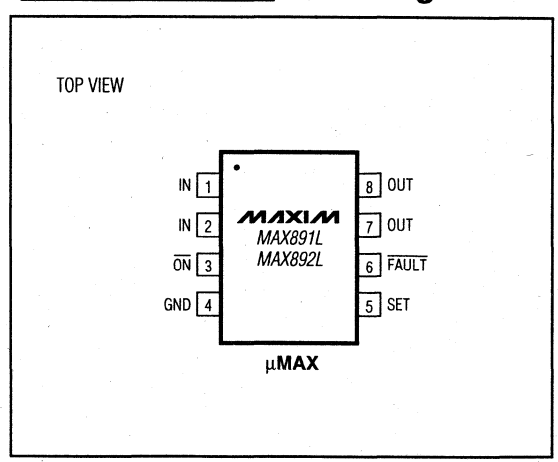
* *To order these units in tape and reel, add (-T) to the end of the part number.*

** *Dice are tested at T_A = +25°C.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to 6V
$\overline{ON}$, $\overline{FAULT}$ to GND..... -0.3V to 6V
SET, OUT to GND .....-0.3V to (V_{IN} + 0.3V)
Maximum Continuous Switch Current
MAX891L 0.75A
MAX892L 0.375A

Continuous Power Dissipation (T_A = +70°C)
µMAX (derate 4.1mW/°C above +70°C) 330mW
Operating Temperature Range
MAX891LEUA/MAX892LEUA .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Operating Voltage				2.7		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ON}$ = GND, I_{OUT} = 0mA				13	20	µA
Off-Supply Current	$\overline{ON}$ = IN, V_{IN} = V_{OUT} = 5.5V				0.02	1	µA
Off-Switch Current	$\overline{ON}$ = IN, V_{IN} = 5.5V, V_{OUT} = 0V				0.02	3	µA
Undervoltage Lockout	Rising edge, 1% hysteresis			2.0	2.3	2.6	V
On-Resistance	V_{IN} = 4.5V	MAX891L			120	225	mΩ
		MAX892L			250	420	
	V_{IN} = 3.0V	MAX891L			150	300	mΩ
		MAX892L			300	500	
Current-Limit-Amplifier Accuracy	V_{SET} required to turn the switch off (Note 1)			1.178	1.240	1.302	V
Maximum Output Current	MAX891L				500		mA
	MAX892L				250		
I_{OUT} to I_{SET} Current Ratio	V_{OUT} = 1.6V to 2.8V	MAX891L, I_{OUT} = 250mA		840	965	1130	A/A
		MAX892L, I_{OUT} = 125mA		840	965	1130	
$\overline{ON}$ Input Low Voltage	V_{IN} = 2.7V to 5.5V					0.8	V
$\overline{ON}$ Input High Voltage	V_{IN} = 2.7V to 3.6V			2.0			V
	V_{IN} = 4.5V to 5.5V			2.4			
$\overline{ON}$ Input Leakage	V $\overline{ON}$ = 5.5V			-1	0.01	1	µA
I_{SET} Bias Current	V_{SET} = 1.24V, I_{OUT} = 0mA				0.5	3	µA
$\overline{FAULT}$ Logic Output Low Voltage	I_{SINK} = 1mA, V_{SET} = 1.4V					0.4	V
$\overline{FAULT}$ Logic Output High Leakage	V $\overline{FAULT}$ = 5.5V, V_{SET} = 1V				0.05	1	µA
Slow-Current-Loop Response Time	20% current overdrive, V_{IN} = 5V				5		µs
Fast-Current-Loop Response Time					2		µs
Turn-On Time	I_{OUT} = 250mA (MAX891L), or 125mA (MAX892L)		V_{IN} = 5V		100	200	µs
			V_{IN} = 3V		150		
Turn-Off Time	V_{IN} = 5V			0.8	2	20	µs

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage			3.0		5.5	V
Quiescent Current	V_{IN} = 5V, $\overline{ON}$ = GND, I_{OUT} = 0mA				50	µA
Off-Supply Current	$\overline{ON}$ = IN, V_{IN} = V_{OUT} = 5.5V				2.2	µA
Off-Switch Current	$\overline{ON}$ = IN, V_{IN} = 5.5V, V_{OUT} = 0V				8	µA
Undervoltage Lockout	Rising edge, 1% hysteresis		2.0		2.9	V
On-Resistance	V_{IN} = 4.5V	MAX891L			225	mΩ
		MAX892L			420	
	V_{IN} = 3.0V	MAX891L			300	mΩ
		MAX892L			500	
Current-Limit-Amplifier Accuracy	V_{SET} required to turn the switch off (Note 1)		1.14		1.34	V
I_{OUT} to I_{SET} Current Ratio	V_{OUT} = 1.6V to 2.8V	MAX891L, I_{OUT} = 250mA	805		1210	A/A
		MAX892L, I_{OUT} = 125mA	805		1210	
$\overline{FAULT}$ Logic Output Low Voltage	I_{SINK} = 1mA, V_{SET} = 1.4V				0.4	V
Turn-On Time	V_{IN} = 5V				200	µs
Turn-Off Time	V_{IN} = 5V		0.25		20	µs

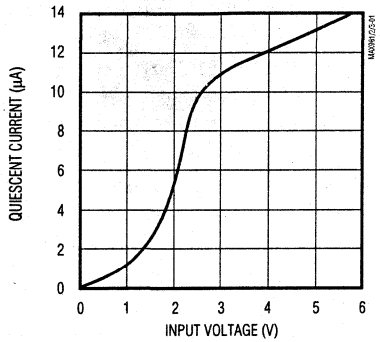
Note 1: Tested with I_{OUT} = 50mA for the MAX891L, 25mA for the MAX892L, and V_{SET} raised until V_{IN} - V_{OUT} ≥ 0.8V.
Note 2: Parameters to -40°C are guaranteed by design, not production tested.

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

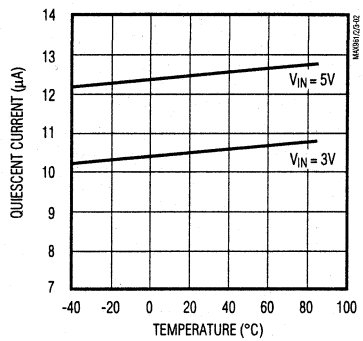
Typical Operating Characteristics

(Typical Operating Circuit, T_A = +25°C, unless otherwise noted.)

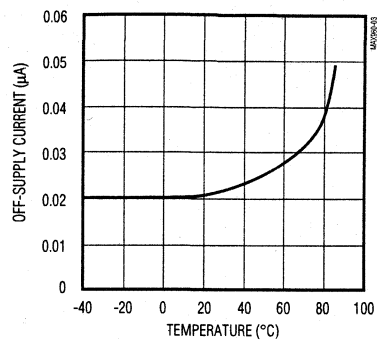
QUIESCENT CURRENT vs. INPUT VOLTAGE



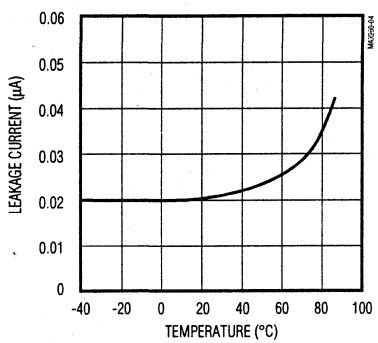
QUIESCENT CURRENT vs. TEMPERATURE



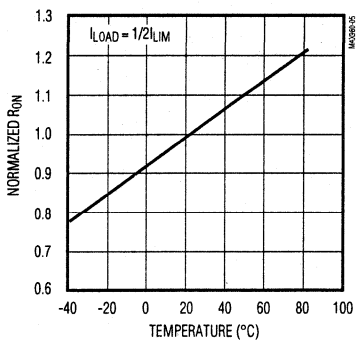
OFF-SUPPLY CURRENT vs. TEMPERATURE



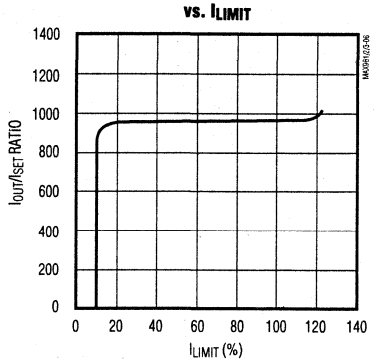
OFF-SWITCH LEAKAGE CURRENT vs. TEMPERATURE



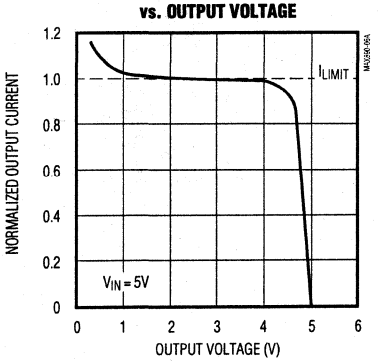
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



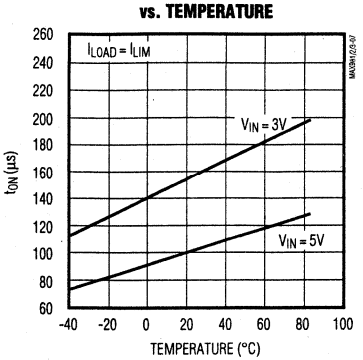
IOUT/ISET RATIO vs. ILIMIT



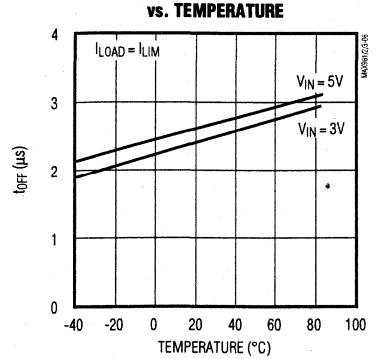
NORMALIZED OUTPUT CURRENT vs. OUTPUT VOLTAGE



TURN-ON TIME vs. TEMPERATURE



TURN-OFF TIME vs. TEMPERATURE

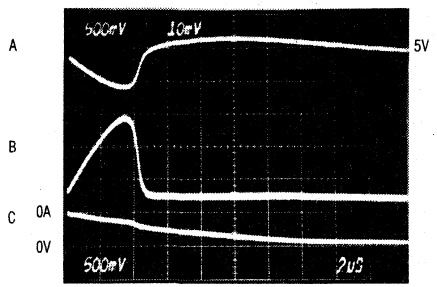


Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Typical Operating Characteristics (continued)

(Typical Operating Circuit, T_A = +25°C, unless otherwise noted.)

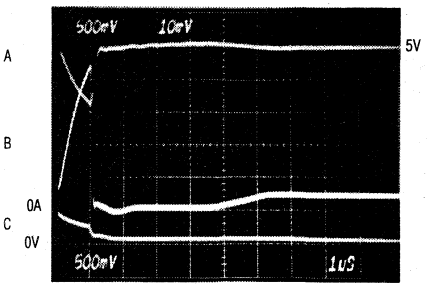
CURRENT-LIMIT RESPONSE
(MAX891L, R_L = 0.8Ω)



2µs/div

C_{IN} = 47µF, C_{OUT} = 0.1µF
A: V_{IN}, 500mV/div, AC COUPLED
B: I_{OUT}, 2A/div
C: V_{OUT}, 5V/div

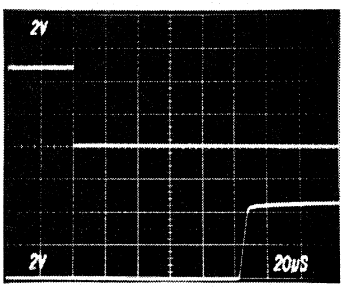
CURRENT-LIMIT RESPONSE
(MAX891L, R_L = 0.5Ω)



1µs/div

C_{IN} = 47µF, C_{OUT} = 0.1µF
A: V_{IN}, 500mV/div, AC COUPLED
B: I_{OUT}, 2A/div
C: V_{OUT}, 5V/div

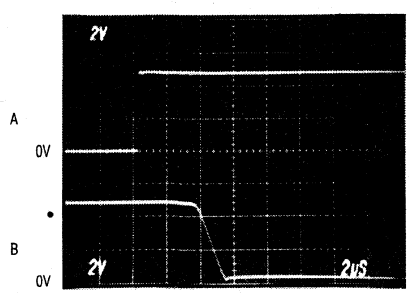
SWITCH TURN-ON TIME



20µs/div

V_{IN} = 5V, I_{OUT} = I_{LIM}
A: $V_{\overline{ON}}$, 2V/div
B: V_{OUT}, 2V/div

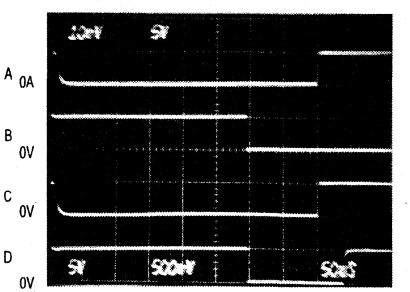
SWITCH TURN-OFF TIME



2µs/div

V_{IN} = 5V, I_{OUT} = I_{LIM}
A: $V_{\overline{ON}}$, 2V/div
B: V_{OUT}, 2V/div

SWITCH TIMING CHARACTERISTICS



50µs/div

V_{IN} = 5V
A: I_{LOAD}, 0.1A/div
B: $V_{\overline{ON}}$, 5V/div
C: V_{OUT}, 5V/div
D: V_{FAULT}, 5V/div

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Pin Description

PIN	NAME	FUNCTION
1, 2	IN	Input. P-channel MOSFET source. Bypass IN with a 1µF capacitor to ground.
3	$\overline{ON}$	Active-Low Switch On Input. A logic low turns the switch on.
4	GND	Ground
5	SET	Set Current-Limit Input. A resistor from SET to ground sets the current limit for the switch. See *Setting the Current Limit* section.
6	$\overline{FAULT}$	Fault-Indicator Output. This open-drain output goes low when in current limit or when the die temperature exceeds +135°C.
7, 8	OUT	Switch Output. P-channel MOSFET drain. Bypass OUT with a 0.1µF capacitor to ground.

Detailed Description

The MAX891L/MAX892L P-channel MOSFET power switches limit output current to a user-programmed level. When the output current is increased beyond the set current level, the current is also increased through the replica switch ($I_{OUT}/965$) and through R_{SET} (Figure 1). The current-limit error amplifier compares the voltage across R_{SET} to the internal 1.24V reference and regulates the current back to the lesser of the programmed current limit (I_{LIMIT}) or the maximum current limit (I_{MAX}).

These switches are not bidirectional; therefore, the input voltage must be higher than the output voltage.

Setting the Current Limit

The MAX891L/MAX892L feature internal current-limiting circuitry with maximum programmable values (I_{MAX}) of 500mA and 250mA, respectively. For best performance, set the current limit (I_{LIMIT}) between $0.2I_{MAX} \le I_{LIMIT} \le I_{MAX}$. This current limit remains in effect throughout the input supply-voltage range.

Program the current limit with a resistor (R_{SET}) from SET to ground (Figure 2) as follows:

$$I_{SET} = I_{LIMIT} / I_{RATIO}$$

$$R_{SET} = 1.240 / I_{SET}$$

where I_{LIMIT} is the desired current limit, and I_{RATIO} is the I_{OUT} to I_{SET} current ratio (965).

Short-Circuit Protection

The MAX891L/MAX892L are short-circuit-protected switches. In the event of an output short circuit or current-overload condition, the current through the switch is limited by the internal current-limiting error amplifier to 1.5 x I_{LIMIT}. When the fault condition is removed, the replica error amplifier sets the current limit back to I_{LIMIT}.

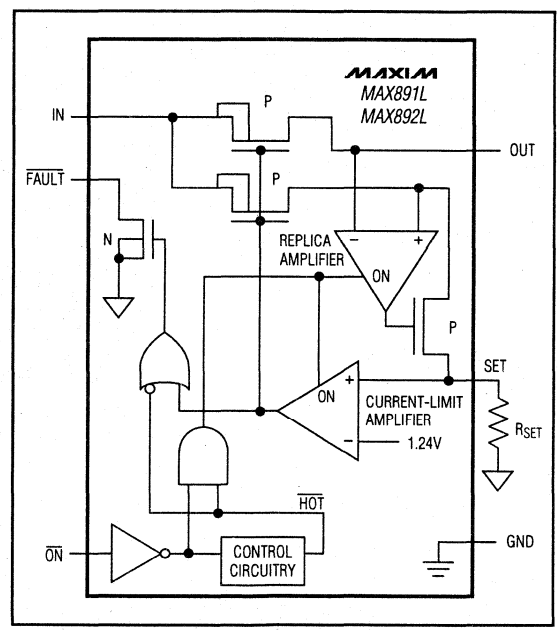


Figure 1. Functional Diagram

For a high $\Delta V_{DS}/\Delta t$ during an output short-circuit condition, the switch turns off and disconnects the input supply from the output. The current-limiting amplifier then slowly turns the switch on with the output current limited to 1.5 x I_{LIMIT}. When the fault condition is removed, the current limit is set back to I_{LIMIT}. Refer to the Current-Limit Response graphs in the *Typical Operating Characteristics*.

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

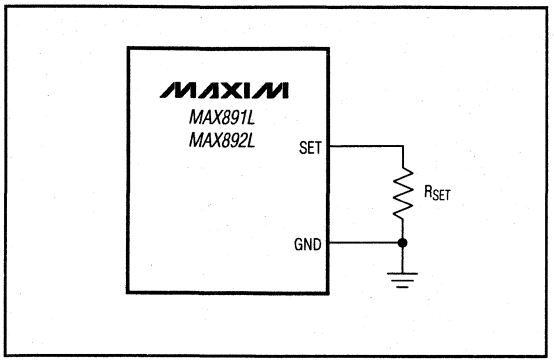


Figure 2. Setting the Current Limit

Thermal Shutdown

The MAX891L/MAX892L feature thermal shutdown. The switch turns off when the junction temperature exceeds +135°C. Once the device cools by 10°C, the switch turns back on. If the fault short-circuit condition is not removed, the switch will cycle on and off, resulting in a pulsed output.

Fault Indicator

The MAX891L/MAX892L provide a fault output ($\overline{FAULT}$). This open-drain output goes low when in current limit or when the die temperature exceeds +135°C. During start-up, $\overline{FAULT}$ is low until the switch is fully on and no over-current condition exists. A 100kΩ pull-up resistor from $\overline{FAULT}$ to IN provides a logic-control signal.

Applications Information

Input Capacitor

To limit input voltage drop during momentary output short-circuit conditions, connect a capacitor from IN to GND. A 1µF ceramic capacitor is adequate for most applications; however, higher capacitor values further reduce voltage drop at the input.

Output Capacitor

Connect a 0.1µF capacitor from OUT to GND. One function of this capacitor is to prevent inductive parasitics from pulling OUT negative during turn-off.

Layout and Thermal-Dissipation Consideration

To take full advantage of the switch-response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm).

Under normal operating conditions, the package dissipates and channels heat away. Calculate maximum power as follows:

$$P = I^2_{LIM} \times R_{ON}$$

where R_{ON} is the on-resistance of the switch.

When the output is short circuited, voltage drop across the switch equals the input supply. Hence, the power dissipated across the switch increases, as does the die temperature. If the fault condition is not removed, the thermal-overload-protection circuitry turns the switch off until the die temperature falls by 10°C. A ground plane in contact with the device helps dissipate additional heat.

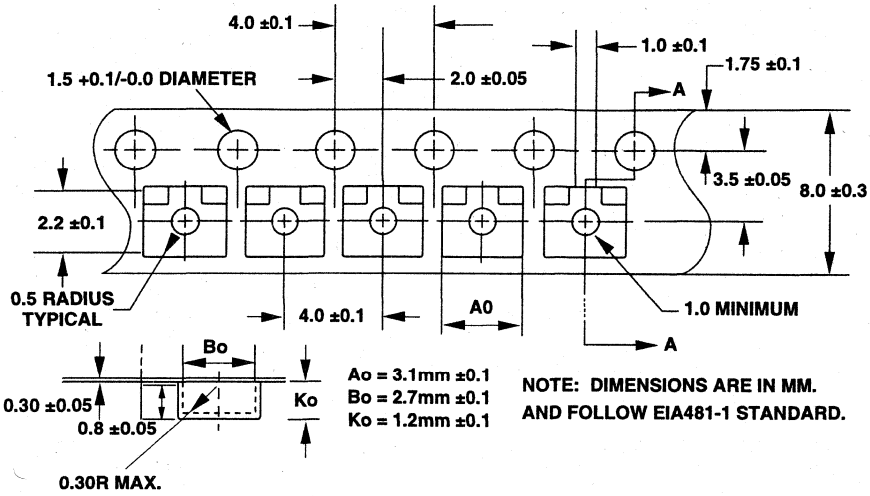
Chip Information

TRANSISTOR COUNT: 396

SUBSTRATE CONNECTED TO GND

Current-Limited, High-Side P-Channel Switches with Thermal Shutdown

Tape-and-Reel Information



19-1225; Rev 1; 10/97

MAXIM

High-Voltage, Low-Power Linear Regulator for Notebook Computers

General Description

The MAX1615 is a micropower, SOT23-5 linear regulator that supplies always-on, keep-alive power to CMOS RAM and microcontrollers (µCs) in systems with high-voltage batteries. Key features include wide input voltage range, low dropout voltage, and low quiescent supply current.

Despite its miserly 8µA (max) no-load supply current, the MAX1615 has excellent line-transient response and AC PSRR. It provides a clean, fixed 5V or 3.3V output, even when subjected to fast supply-voltage changes that occur during the switchover from battery to AC adapter input power. The space-saving SOT23-5 package has excellent thermal characteristics and tolerates up to 571mW of power dissipation. Fault protection is provided by internal foldback current limiting and thermal-shutdown circuitry.

Features

- **Low Cost**
- **4V to 28V Input Range**
- **8µA (max) Quiescent Supply Current**
- **<1µA Shutdown Supply Current**
- **3.3V or 5V, Pin-Selectable Output**
- **30mA Output Current**
- **±2% Initial Output Accuracy**
- **Thermal-Overload Protection**
- **5-Pin SOT23 Package**

Applications

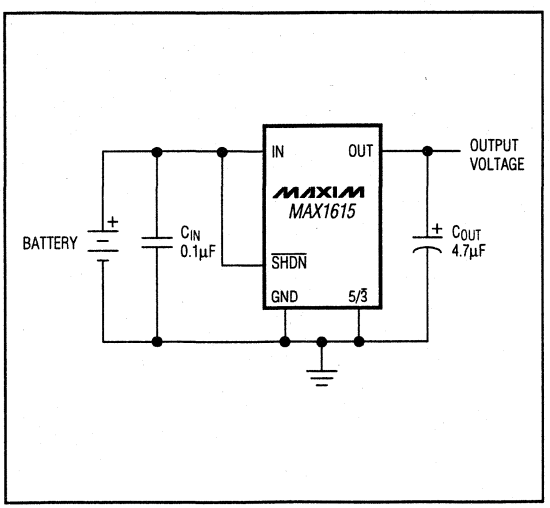
CMOS/RTC Backup Power
Microcontroller Power
Notebook Computers
Smart-Battery Packs
PDAs and Handy-Terminals
Battery-Powered Systems

Ordering Information

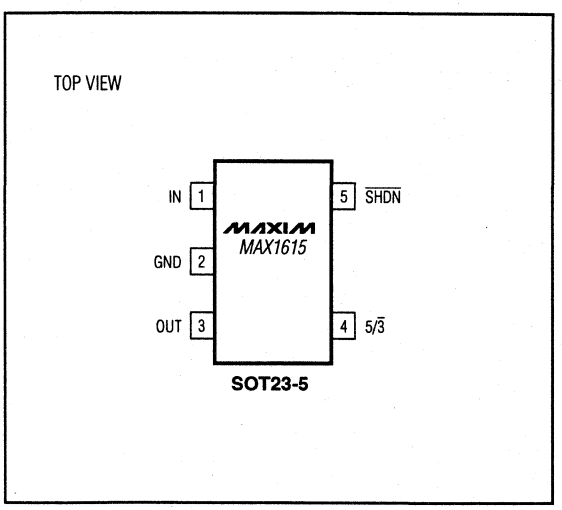
PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX1615EUK-T	-40°C to +85°C	5 SOT23-5	ABZD

4

Typical Operating Circuit



Pin Configuration



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High-Voltage, Low-Power Linear Regulator for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to 30V
Terminal Voltages to GND
  $\overline{SHDN}$ to GND .....-0.3V to (V_{IN} + 0.3V)
  5/$\overline{3}$ to GND .....-0.3V to (V_{OUT} + 0.3V)
  OUT to GND.....-0.3V to 30V
  OUT Short-Circuit to GND 30sec
Continuous OUT Current.....40mA

Continuous Power Dissipation (T_A = +70°C, Note 1)
  SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range
  MAX1615EUK-T .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: See *Operating Region and Power Dissipation* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 15V, $\overline{SHDN}$ = V_{IN}, I_{LOAD} = 5µA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			4		28	V
Supply Current	I_{IN}	$\overline{SHDN}$ = IN, T_A = +25°C			6.2	8	µA
		$\overline{SHDN}$ = IN, V_{IN} = 6V to 28V, T_A = T_{MIN} to T_{MAX}				15	
Minimum Load Current						5	µA
Shutdown Supply Current	I_{IN}	$\overline{SHDN}$ = GND (shutdown mode)	T_A = +25°C			1.5	µA
			T_{MIN} = T_{MIN} to T_{MAX}			3	
Dropout Supply Current		3/$\overline{5}$ = OUT, V_{IN} = 4V	T_A = +25°C		55		µA
Output Voltage (Note 3)		V_{IN} = 6V to 28V, 5/$\overline{3}$ = GND, I_{LOAD} = 1mA, T_A = +25°C		3.26	3.33	3.40	V
		V_{IN} = 6V to 28V, 5/$\overline{3}$ = GND, I_{LOAD} = 5µA to 30mA, T_A = T_{MIN} to T_{MAX}		3.15		3.48	
		V_{IN} = 6V to 28V, 5/$\overline{3}$ = OUT, I_{LOAD} = 1mA, T_A = +25°C		4.95	5.05	5.15	
		V_{IN} = 6V to 28V, 5/$\overline{3}$ = OUT, I_{LOAD} = 5µA to 30mA, T_A = T_{MIN} to T_{MAX}		4.75		5.25	
Dropout Voltage	ΔV_{DO}	I_{LOAD} = 30mA (Note 4)				350	mV
Output Current Limit		V_{IN} = 6V			100		mA
OUT Reverse Leakage Current		IN = unconnected; V_{OUT} forced to 5V			55		µA
Capacitive Load Requirements		(Notes 5, 6)		0.16			µF/mA
Start-Up Time Response		Rising edge of IN or $\overline{SHDN}$ to OUT within specification limits, R_L = 500Ω, C_{OUT} = 4.7µF, 5/$\overline{3}$ = IN				1	ms
Start-Up Overshoot	V_{OSH}	R_L = 500Ω, C_{OUT} = 10µF within 90% of nominal output voltage			0.5		%V_{OUT}
$\overline{SHDN}$ Input Threshold Voltage	V_{IL}					0.25	V
	V_{IH}			1.4			
$\overline{SHDN}$ Input Current		$V_{\overline{SHDN}}$ = 0V or 15V		-1	0.1	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 15V, $\overline{SHDN}$ = V_{IN}, I_{LOAD} = 5µA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

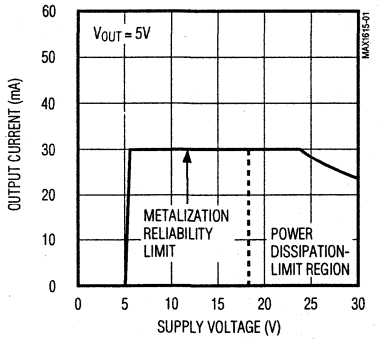
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal-Shutdown Temperature	T_{SHDN}	$V_{\overline{SHDN}}$ = 0V or 15V		150		°C
Thermal-Shutdown Hysteresis	$\Delta T_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = 0V or 15V		20		°C

Note 2: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using standard quality-control (SQC) methods.
Note 3: Pulse tested at V_{IN} = 28V, I_{LOAD} = 30mA to avoid exceeding package power-dissipation limits.
Note 4: Guaranteed by design. Tested with 5/$\overline{3}$ = OUT. Dropout voltage is tested by reducing the input voltage until V_{OUT} drops to 100mV below its nominal value, measured with V_{IN} starting 2V above V_{OUT}.
Note 5: Use at least 1µF minimum for light loads. Add 0.125µF/mA for loads greater than 100µA.
Note 6: Guaranteed by design.

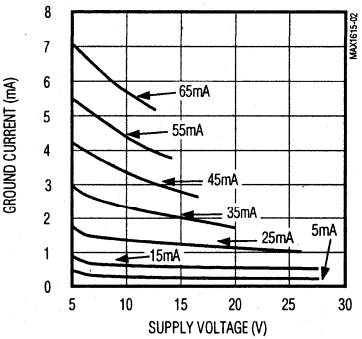
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

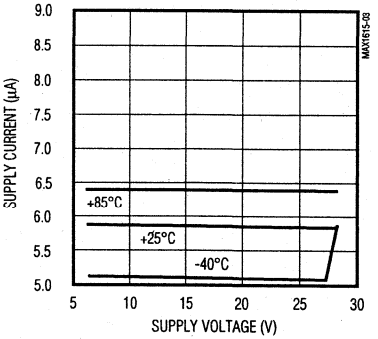
SAFE LOAD-CURRENT OPERATING AREA vs. SUPPLY VOLTAGE



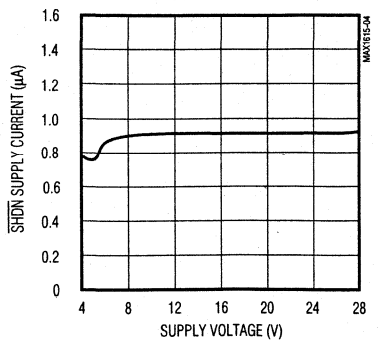
GROUND CURRENT vs. SUPPLY VOLTAGE AT VARIOUS LOADS



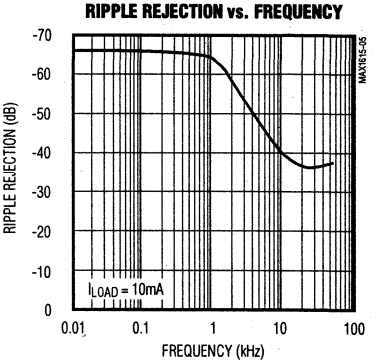
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



RIPPLE REJECTION vs. FREQUENCY

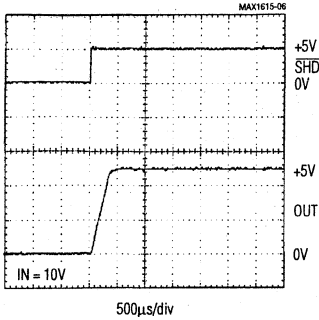


High-Voltage, Low-Power Linear Regulator for Notebook Computers

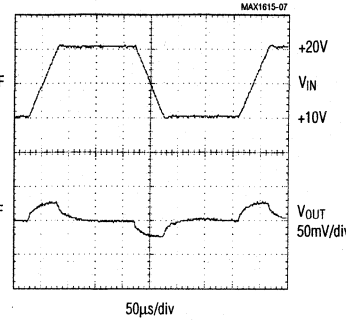
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

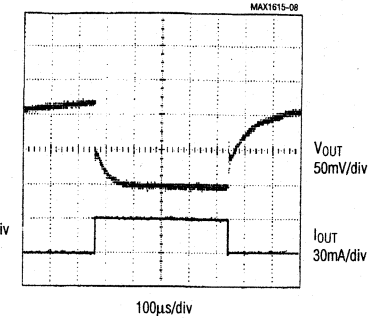
TIME TO EXIT SHUTDOWN



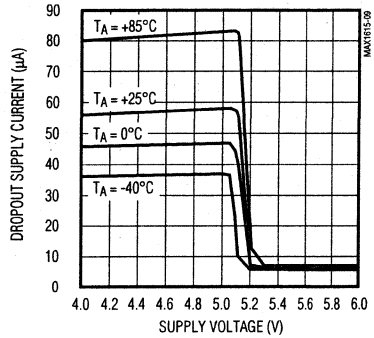
LINE-TRANSIENT RESPONSE



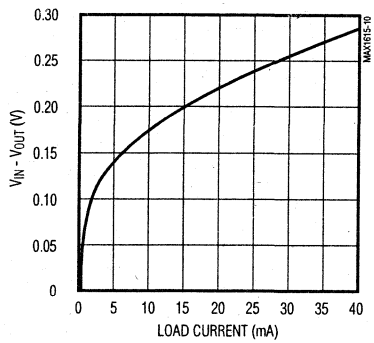
LOAD-TRANSIENT RESPONSE



DROPOUT SUPPLY CURRENT vs. SUPPLY VOLTAGE



DROPOUT VOLTAGE vs. LOAD CURRENT



Pin Description

PIN	NAME	FUNCTION
1	IN	Positive Input Voltage. Connect to a +4V to +28V supply.
2	GND	Ground
3	OUT	Regulator Output
4	5/$\overline{3}$	Preset Output Voltage Select. Connect to GND for 3.3V output, or to OUT for 5.0V output.
5	$\overline{SHDN}$	Shutdown, active low input. Connect to IN if unused.

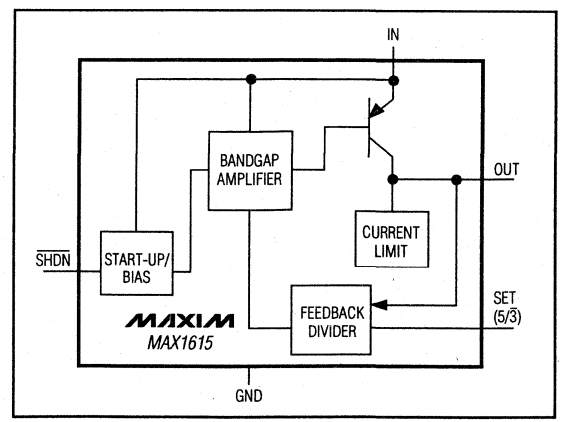


Figure 1. Block Diagram

High-Voltage, Low-Power Linear Regulator for Notebook Computers

Detailed Description

The MAX1615 low-quiescent-current linear regulator is designed primarily for high input voltage applications. It supplies a preselected 3.3V or 5.0V output for loads up to 30mA. The maximum output current is a function of the package's maximum power dissipation for a given temperature. A 5µA load is required to maintain output regulation.

Output voltage is fed back through an internal resistor voltage divider connected to OUT. Set the output voltage to either 3.3V or 5.0V with the 5/$\overline{3}$ pin.

Select 5V output by connecting 5/$\overline{3}$ to OUT, or 3.3V output by connecting 5/$\overline{3}$ to GND.

Shutdown

The device enters shutdown mode when $\overline{SHDN}$ is low. In shutdown mode, the pass transistor, control circuit, reference, and all biases turn off, reducing the supply current to below 1µA. Connect $\overline{SHDN}$ to IN for normal operation.

Current Limit

The MAX1615 includes a current limiter that monitors and controls the pass transistor's gate voltage, estimating the output current and typically limiting it to 100mA. The current limit exceeds the 30mA (max) safe operating limit. A repetitive short-circuit condition results in reduced reliability due to electron-metal migration. The output can be shorted to ground for 30 seconds without damaging the part.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1615. When the junction temperature exceeds T_J = +150°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by +20°C (typ), resulting in a pulsating output during continuous thermal-overload conditions.

Thermal-overload protection is designed to protect the MAX1615 in the event of fault conditions. Stressing the device with high-load currents and high input-output differential voltages (which result in die temperatures above +125°C) can cause a momentary overshoot (2% to 8% for 200ms) when the load is completely removed. Minimize this overshoot by raising the minimum load current from 5µA to 100µA. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_j = +150°C.

Operating Region and Power Dissipation

The MAX1615 maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The device's power dissipation is $P = I_{OUT} (V_{IN} - V_{OUT})$. The power dissipation at +70°C ambient is 571mW (see *Absolute Maximum Ratings*). The thermal resistance junction-to-case of the SOT23-5 package is 81°C/W, and the maximum safe junction temperature is +150°C.

The GND pin performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

Applications Information

Capacitor Selection

Use 0.1µF minimum on the input. Higher values will improve line-transient response.

Use 1.0µF minimum on the output, or 4.7µF for the full 30mA load current. Otherwise, use 1µF plus 0.125µF/mA. The output capacitor effective series resistance (ESR) must be less than 1Ω for stable operation.

Noise

The MAX1615 typically exhibits 5mVp-p of noise during normal operation. This is negligible in most applications. In applications that include analog-to-digital converters (ADCs) of more than 12 bits, consider the ADC's power-supply-rejection specifications.

Transient Conditions

The *Typical Operating Characteristics* show the MAX1615's load-transient response. Two of the output response's components can be observed on the load-transient graph: a DC shift from the output impedance due to the different load currents, and the transient response. Typical step changes in the load current from 10mA to 20mA produce 50mV transients. Increasing the output capacitor's value attenuates transient spikes.

High-Voltage, Low-Power Linear Regulator for Notebook Computers

Table 1. Surface-Mount Capacitor Manufacturers

TYPE	MANUFACTURER	CAPACITOR
Electrolytic	AVX	TPS series
	Matsuo	267 series
	Sprague	593D, 595 series
Ceramic	AVX	X7R
	Matsuo	X7R

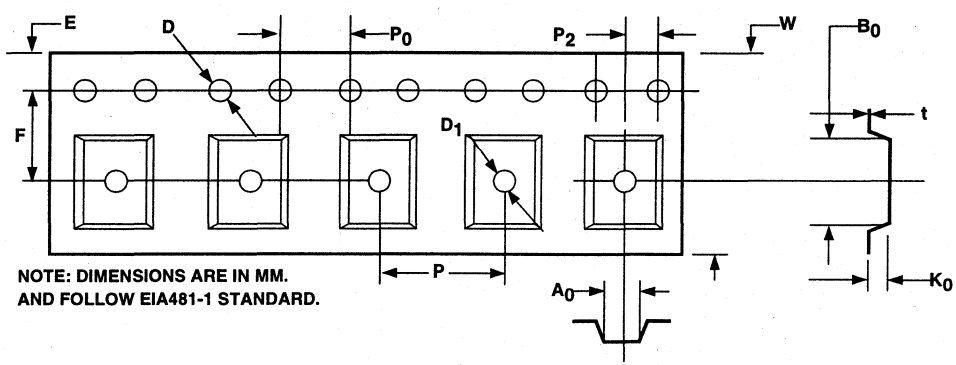
Table 2. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	(803) 946-0690	(803) 626-3123
Matsuo	(714) 969-2491	(714) 960-6492
Sprague	(603) 224-1961	(603) 224-1430

Chip Information

TRANSISTOR COUNT: 386

Tape-and-Reel Information



A_0	3.200	±0.102
B_0	3.099	±0.102
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000

E	1.753	±0.102
F	3.505	±0.051
K_0	1.397	±0.102
P	3.988	±0.102

P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
t	0.254	±0.127
W	8.001	+0.305 -0.102

5 SOT23-5

19-1214; Rev 0; 7/97

EVALUATION KIT AVAILABLE

MAXIM

Digitally Adjustable LCD Bias Supplies

General Description

The MAX1620/MAX1621 convert a 1.8V to 20V battery voltage to a positive or negative LCD backplane bias voltage. Backplane bias voltage can be automatically disabled when the display logic voltage is removed, protecting the display. These devices use very little PC board area, come in ultra-small QSOP packages, and require only small, low-profile external components.

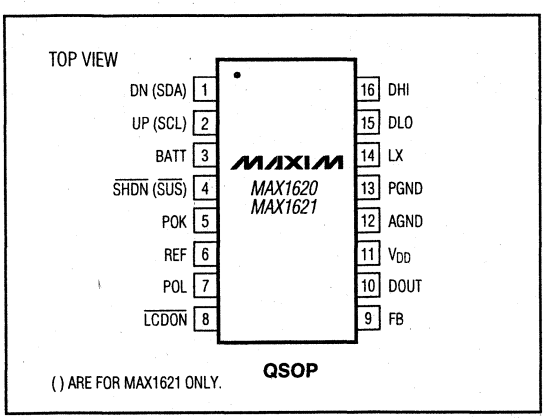
Output voltage can be set to a desired positive or negative voltage range with external resistors, and adjusted over that range with the on-board digital-to-analog converter (DAC) or with a potentiometer. The MAX1620/MAX1621 include a 5-bit DAC, allowing digital software control of the bias voltage. The MAX1620 uses up/down digital signaling to adjust the DAC, and the MAX1621 uses the System Management Bus (SMBus™) 2-wire serial interface.

These devices use a low-cost, external, N-channel MOSFET power switch or NPN transistor, and can be configured for positive or negative output voltages. Operating current is a low 150µA, typically provided from a display's logic supply of 3.0V to 5.5V. The MAX1620/MAX1621 are available in a 16-pin QSOP package.

Applications

Notebook Computers
Palmtop Computers
Personal Digital Assistants
Portable Data-Collection Terminals

Pin Configuration



Features

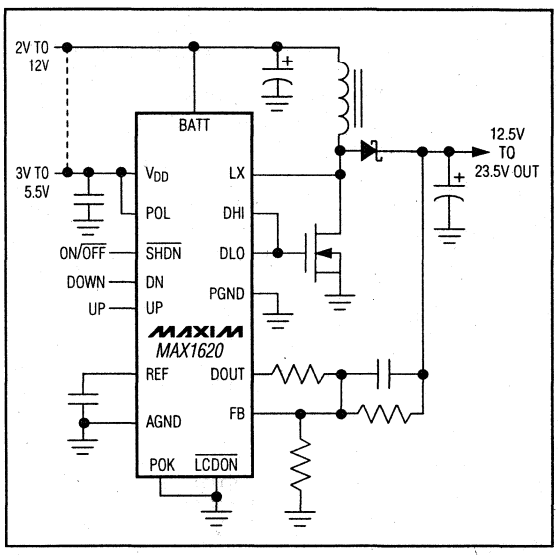
- ♦ **1.8V to 20V Battery Input Voltage**
- ♦ **Automatic Disable when Display Logic is Shut Down**
- ♦ **Extremely Small QSOP Package**
- ♦ **32-Level Internal DAC**
- ♦ **SMBus Serial Interface (MAX1621)**
- ♦ **Positive or Negative Output Voltage**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1620EEE	-40°C to +85°C	16 QSOP
MAX1621EEE	-40°C to +85°C	16 QSOP

4

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

Digitally Adjustable LCD Bias Supplies

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to 6V
PGND to AGND .....±0.3V
BATT, LX, $\overline{LCDON}$ to AGND .....-0.3V to 30V
DHI, DLO to PGND .....-0.3V to (V_{DD} + 0.3V)
DOUT, FB, POL, POK, REF to AGND .....-0.3V to (V_{DD} + 0.3V)
UP, DN, $\overline{SHDN}$ to AGND .....-0.3V to 6V
SCL, SDA, $\overline{SUS}$ to AGND .....-0.3V to 6V
I_{DHI} 60mA
I_{DLO} .....-30mA
$I_{\overline{LCDON}}$ .....-10mA
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range
MAX1620EEE/MAX1621EEE .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
V_{DD} Operating Range		3.0		5.5	V
V_{DD} Supply Current	Operating mode, output in regulation, V_{DD} = 5.5V		150	250	µA
	Shutdown mode, $V_{\overline{SHDN}}$ = V_{DD}, V_{DD} = 5.5V		9	20	
Positive Output Voltage				27	V
Negative Output Voltage				-27	V
Undervoltage Lockout Threshold (Note 1)		1.5		2.8	V
BATT Input Current	BATT = 12V, operating mode		13	20	µA
	BATT = 12V, shutdown mode			1	
LX Input Current	LX = 12V, operating mode		13	20	µA
	LX = 12V, shutdown mode			1	
BATT Operating Range (Note 2)		1.8		20	V
Microsecond-Volt Time Constant (k-factor)	1.8V ≤ BATT ≤ 20V, T_A = +25°C		20		µs-V
	4V ≤ BATT ≤ 12V, T_A = 0°C to +85°C	16.5		23.5	
On-Resistance (DLO, DHI)	V_{DD} = 4.5V		7		Ω
	V_{DD} = 3.0V		14		
DHI Output Current (Note 3)	V_{DD} = 5V		50		mA
DLO Output Current (Note 3)	V_{DD} = 5V		-25		mA
FB Regulation Voltage	POL = V_{DD}, 3.0V ≤ V_{DD} ≤ 5.5V	1.46	1.5	1.53	V
	POL = AGND, 3.0V ≤ V_{DD} ≤ 5.5V	-8	0	8	mV
FB Input Current (Note 3)	FB = REF + 100mV	-20		10	nA
	FB = -50mV	-10		85	
$\overline{LCDON}$ Low, Sinking Current	$V_{\overline{LCDON}}$ = 0.4V, POK = 1.017V	-2	-6		mA
$\overline{LCDON}$ High, Leakage Current	$V_{\overline{LCDON}}$ = 28V, POK = 0.967V			1	µA
POK Threshold Voltage	Voltage on POK rising	0.967	0.992	1.017	V
POK Hysteresis			12		mV
REFERENCE AND DAC OUTPUT					
REF Voltage	No load	1.47	1.5	1.53	V
REF Load Regulation	0µA ≤ I_{REF} ≤ 25mA		3	10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DOUT Maximum Output Voltage (Note 3)	0µA ≤ I_{DOUT} ≤ 40µA	REF - 0.02		REF + 0.02	V
DOUT Minimum Output Voltage (Note 3)	-20µA ≤ I_{DOUT} ≤ 0µA	0		0.007	V
DOUT Resolution	48.39mV step size	5			Bits
DOUT Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS AND OUTPUTS					
UP, DN, $\overline{SHDN}$, POL Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
UP, DN, $\overline{SHDN}$, POL Input Low Voltage				0.6	V
UP, DN, $\overline{SHDN}$, POL Input Leakage Current	V_{IN} = 0V or V_{IN} = V_{DD}			±1	µA
SCL, SDA, $\overline{SUS}$ Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
SCL, SDA, $\overline{SUS}$ Input Low Voltage				0.6	V
SCL, SDA, $\overline{SUS}$ Input Leakage Current	V_{IN} = 0V or V_{IN} = V_{DD}			±1	µA
SDA Output Low Voltage	I_{SDA} = -6mA			0.4	V

TIMING CHARACTERISTICS

(**T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX1620 (Figure 1)						
Pulse Width High (UP, DN)	t_1		1			µs
Pulse Width Low (UP, DN)	t_2		1			µs
Pulse Separation (UP, DN)	t_3		1			µs
Counter Reset Time	t_4		1			µs
MAX1621 (Figures 2 and 3)						
SDA to SCL Data-Setup Time	$t_{SU:DAT}$		500			ns
SCL to SDA Data-Hold Time	$t_{HD:DAT}$	(Note 4)	0			ns
SCL/SDA Rise Time	t_R	(Note 4)			1	µs
SCL/SDA Fall Time	t_F	(Note 4)			300	ns
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
Start Condition SCL to SDA Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition SDA to SCL Hold Time	$t_{HD:STA}$		4			µs
Stop Condition SCL_ to SDA_ Setup Time	$t_{SU:STO}$		4			µs
SCL Falling Edge to SDA Valid Master Clocking in Data	t_{DV}				1	µs

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING REGULATOR					
V_{DD} Operating Range		3.0		5.5	V
V_{DD} Supply Current	Operating mode, output in regulation		150	250	µA
	Shutdown mode, $V_{\overline{SHDN}} = V_{DD}$			20	
Positive Output Voltage				27	V
Negative Output Voltage				-27	V
Undervoltage Lockout Threshold (Note 1)		1.5		2.8	V
BATT Operating Range (Note 2)		1.8		20	V
Microsecond-Volt Time Constant (k-factor)	4V ≤ BATT ≤ 12V	16		24	µs-V
FB Regulation Voltage	POL = V_{DD}, 3.0V ≤ V_{DD} ≤ 5.5V	1.44	1.5	1.56	V
	POL = AGND, 3.0V ≤ V_{DD} ≤ 5.5V	-10	0	10	mV
FB Input Current (Note 3)	FB = REF + 100mV	-30		10	nA
	FB = 0V - 50mV	-10		120	
POK Threshold Voltage	Voltage on POK rising	0.957	0.992	1.027	V
REFERENCE AND OUTPUT					
REF Voltage	No load	1.44	1.5	1.56	V
REF Load Regulation	0µA ≤ I_{REF} ≤ 25µA		5	10	mV
DOUT Maximum Output Voltage (Note 3)	0µA ≤ I_{DOUT} ≤ 40µA	REF - 0.02		REF + 0.02	V
DOUT Minimum Output Voltage (Note 3)	-20µA ≤ I_{DOUT} ≤ 0µA	0		0.01	V
DOUT Differential Nonlinearity	Guaranteed monotonic			±1	LSB
DIGITAL INPUTS AND OUTPUTS					
UP, DN, $\overline{SHDN}$, POL Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
UP, DN, $\overline{SHDN}$, POL Input Low Voltage				0.6	V
SCL, SDA, $\overline{SUS}$ Input High Voltage	3.0V ≤ V_{DD} ≤ 3.6V	1.4			V
	V_{DD} = 5.5V	2.3			
SCL, SDA, $\overline{SUS}$ Input Low Voltage				0.6	V
SDA Output Low Voltage	I_{SDA} = -6mA			0.4	V

TIMING CHARACTERISTICS

(V_{DD} = 3.3V, V_{BATT} = 10V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

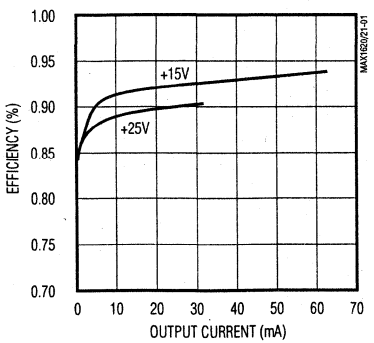
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAX1620 (Figure 1)						
Pulse Width High (UP, DN)	t_1		1			µs
Pulse Width Low (UP, DN)	t_2		1			µs
Pulse Separation (UP, DN)	t_3		1			µs
Counter Reset Time	t_4		1			µs
MAX1621 (Figures 2 and 3)						
SDA_ to SCL_ Data-Setup Time	$t_{SU:DAT}$		500			ns
SCL_ to SDA_ Data-Hold Time	$t_{HD:DAT}$		0			ns
SCL/SDA Rise Time	t_R				1	µs
SCL/SDA Fall Time	t_F				300	ns
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
Start Condition SCL_ to SDA_ Setup Time	$t_{SU:STA}$		4.7			µs
Start Condition SDA_ to SCL_ Hold Time	$t_{HD:STA}$		4			µs
Stop Condition SCL_ to SDA_ Setup Time	$t_{SU:STO}$		4			µs
SCL Falling Time to SDA Valid Master Clocking in Data	t_{DV}				1	µs

Note 1: The setting in the DAC is guaranteed to remain valid as long as V_{DD} is greater than the UVLO threshold.
Note 2: BATT Operating Range is guaranteed by the Microsecond-Volt Time Constant specification.
Note 3: Current sourced from a pin is denoted as positive current. Current sunk into a pin is denoted as negative current.
Note 4: Guaranteed by design.

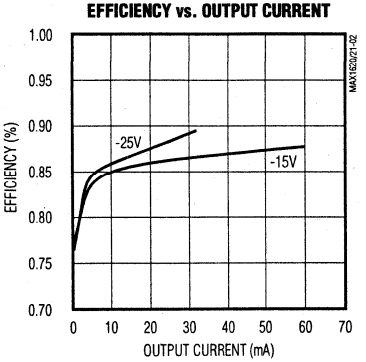
Typical Operating Characteristics

(V_{DD} = 5V, V_{BATT} = 10V, L1 = 100µH, T_A = +25°C, unless otherwise noted.)

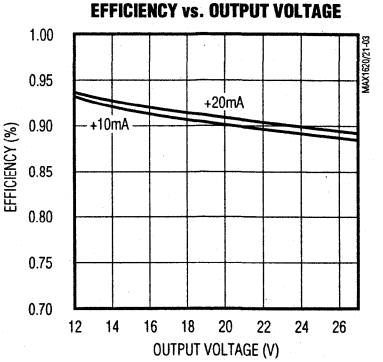
EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT CURRENT



EFFICIENCY vs. OUTPUT VOLTAGE

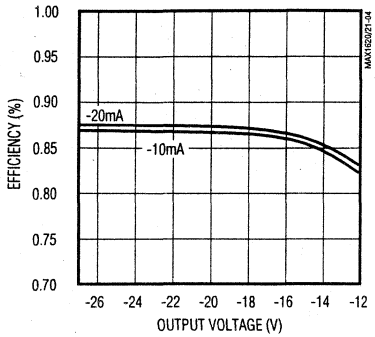


Digitally Adjustable LCD Bias Supplies

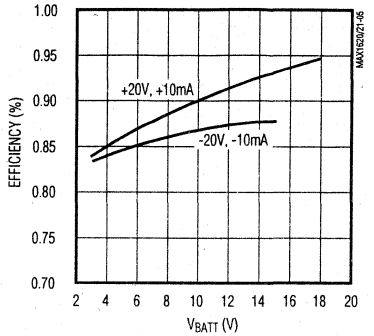
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{BATT} = 10V, L1 = 100µH, T_A = +25°C, unless otherwise noted.)

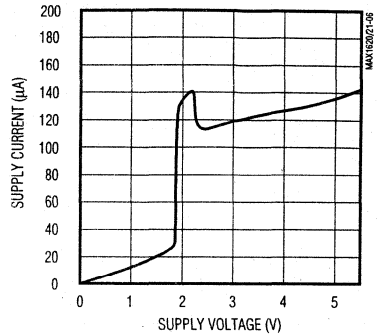
EFFICIENCY vs. OUTPUT VOLTAGE



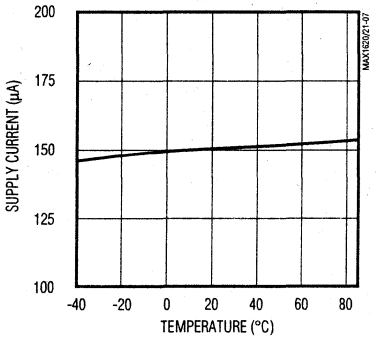
EFFICIENCY vs. V_{BATT}



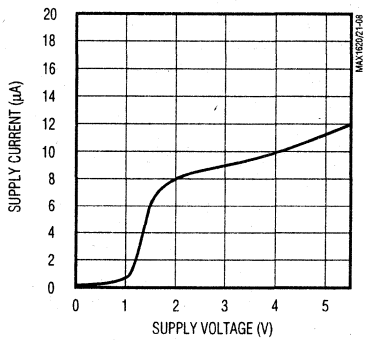
SUPPLY CURRENT vs. SUPPLY VOLTAGE



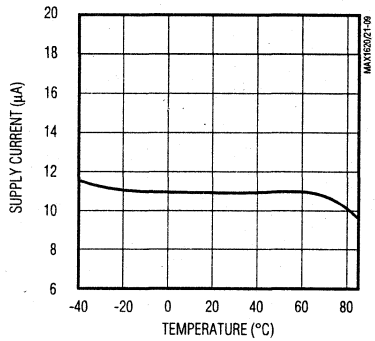
SUPPLY CURRENT vs. TEMPERATURE



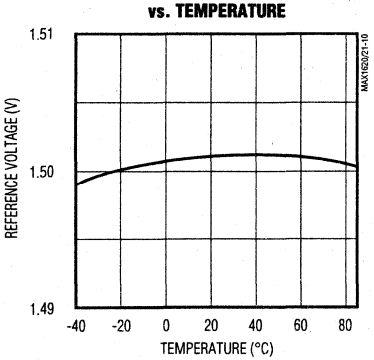
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



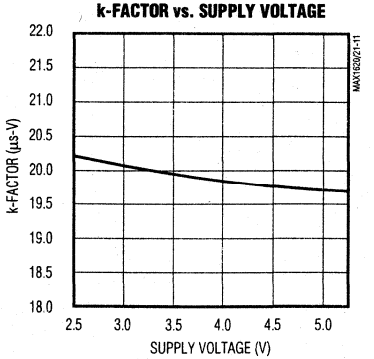
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



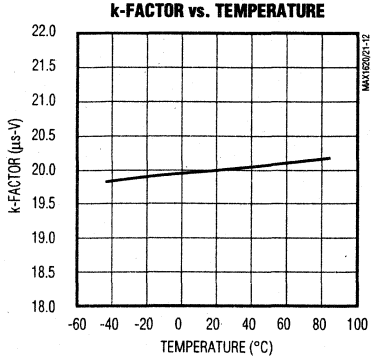
REFERENCE VOLTAGE vs. TEMPERATURE



k-FACTOR vs. SUPPLY VOLTAGE



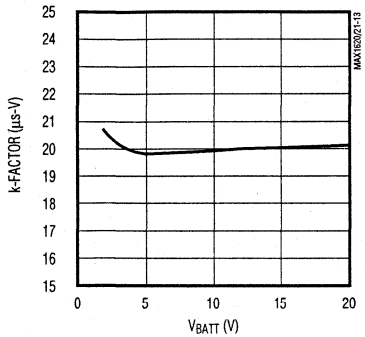
k-FACTOR vs. TEMPERATURE



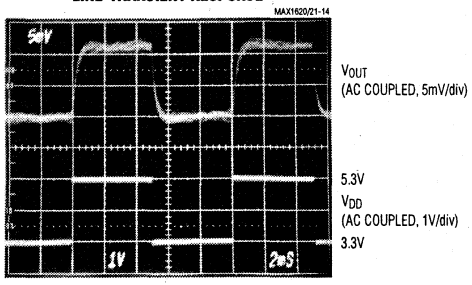
Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{BATT} = 10V L1 = 100µH, V_{OUT} = 22.3V, T_A = +25°C, unless otherwise noted.)

k-FACTOR vs. V_{BATT}



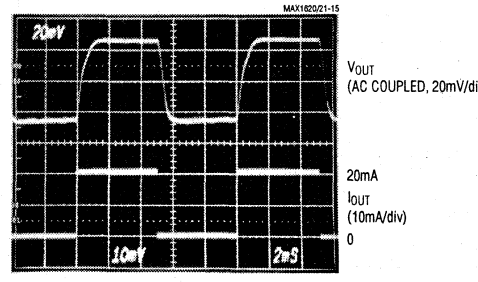
LINE-TRANSIENT RESPONSE



2ms/div

I_{LOAD} = 20mA

LOAD-TRANSIENT RESPONSE



2ms/div

I_{LOAD} = 0mA TO 20mA

Digitally Adjustable LCD Bias Supplies

Pin Description

PIN		NAME	FUNCTION
MAX1620	MAX1621		
1	—	DN	Logic-Level Input. A rising edge on DN decreases $\lvert V_{OUT} \rvert$. UP = DN = high resets the counter to mid-scale.
—	1	SDA	System Management Bus Serial-Data Input and Open-Drain Output
2	—	UP	Logic-Level Input. A rising edge on UP increases $\lvert V_{OUT} \rvert$. UP = DN = high resets the counter to mid-scale.
—	2	SCL	System Management Bus Serial-Clock Input
3	3	BATT	Battery Voltage-Sense Input
4	—	$\overline{SHDN}$	Logic-Level Shutdown Input (active-low)
—	4	$\overline{SUS}$	System Management Bus Suspend-Mode Input (active-low)
5	5	POK	Power OK Voltage-Sense Input, 1V threshold
6	6	REF	Reference Voltage Output. Bypass REF with 0.1µF to AGND.
7	7	POL	Logic-Level Input. POL selects output voltage polarity: high = positive boost, low = negative boost.
8	8	$\overline{LCDON}$	Open-Drain Output. $\overline{LCDON}$ controls LCD with external PNP.
9	9	FB	Feedback Voltage Input
10	10	DOUT	DAC Output Voltage
11	11	V_{DD}	IC Input Supply, 3.0V to 5.5V
12	12	AGND	Analog Ground
13	13	PGND	Power Ground
14	14	LX	Switching-Voltage Sense Input
15	15	DLO	External Transistor Drive, Low
16	16	DHI	External Transistor Drive, High

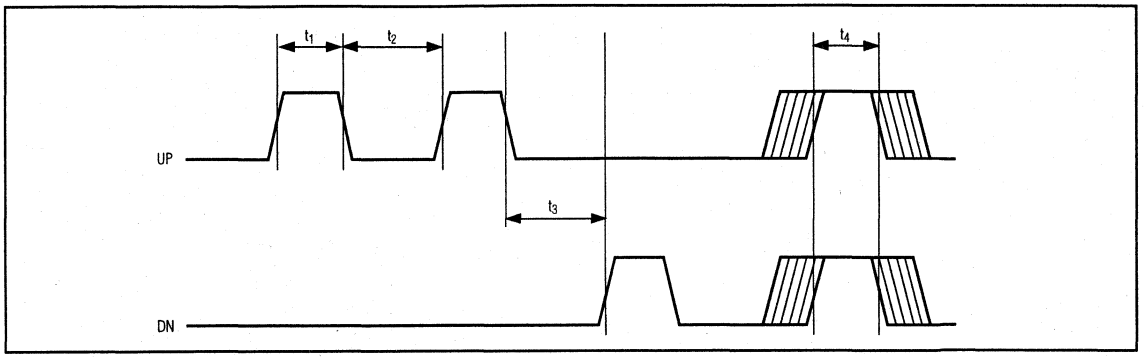


Figure 1. MAX1620 UP and DN Signal Timing

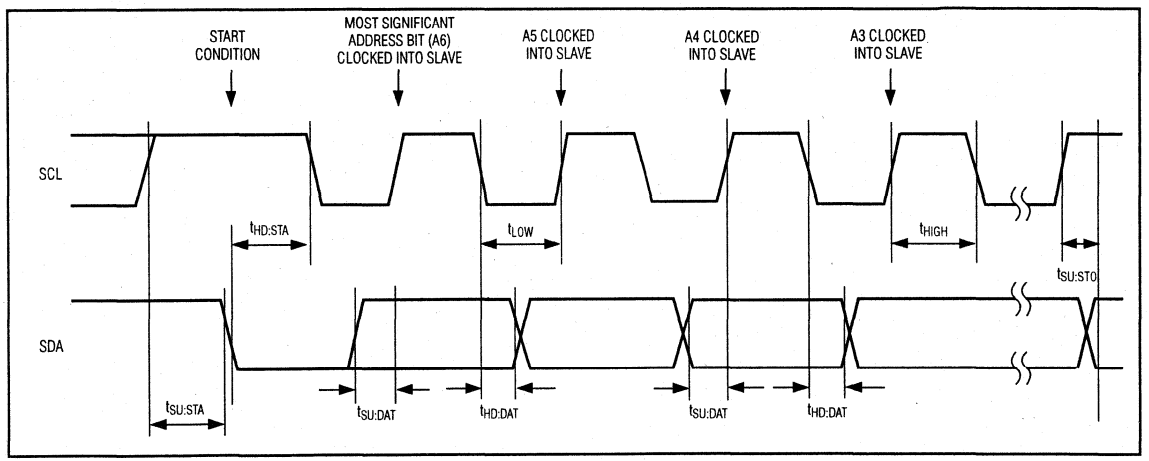


Figure 2. MAX1621 SMB Serial-Interface Timing—Address

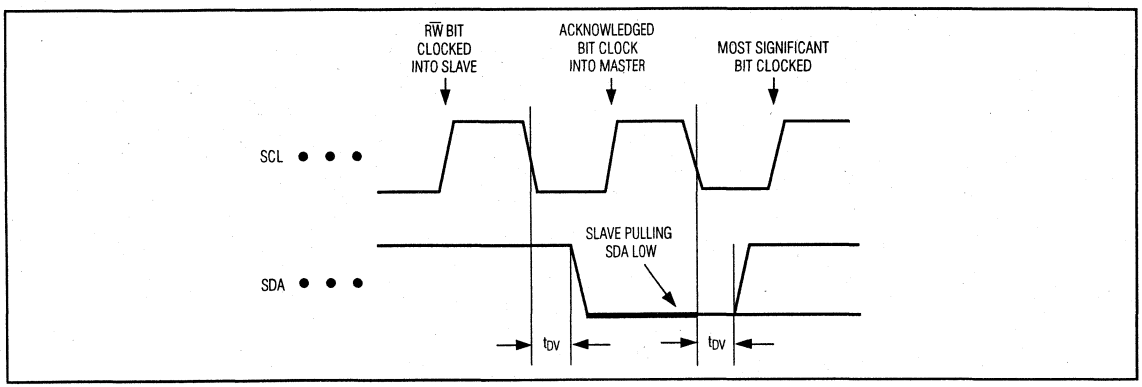


Figure 3. MAX1621 SMB Serial-Interface Timing—Acknowledge

Digitally Adjustable LCD Bias Supplies

Detailed Description

The MAX1620/MAX1621 are step-up power controllers that drive an external N-channel FET or NPN transistor to convert power from a 1.8V to 20V battery to a higher positive or negative voltage. They are configured as negative-output, inverting power controllers with one additional diode and one additional capacitor. Either configuration's output voltage can be adjusted with external resistors, or digitally adjusted with an internal digital-to-analog converter (DAC). The MAX1620 uses pin-defined controls for the DAC, while the MAX1621 communicates with the DAC via the SMBus™ interface.

Operating Principle

The MAX1620/MAX1621 operate in discontinuous-conduction mode (where the inductor current ramps to zero by the end of each switching cycle) and with a constant peak current, without requiring a current-sense resistor. Switch on-time is inversely proportional to the input voltage V_{BATT} by a microsecond-volt constant, or k-factor, of 20µs-V (e.g., for V_{BATT} = 10V, on-time = 2µs).

For an ideal boost converter operating in discontinuous-conduction mode (no power losses), output current is proportional to input voltage and peak inductor current:

$$I_{OUT} = \frac{1}{2} \times I_{PK} \times V_{BATT} / V_{OUT}$$

I_{PK} is proportional to on-time (t_{ON}), which, for these parts, is determined by the k-factor:

$$I_{PK} = \text{k-factor} / L$$

Discontinuous conduction is detected by monitoring the LX node voltage. When the inductor's energy is completely delivered, the LX node voltage snaps back to the BATT voltage. When this crossing is sensed, another pulse is issued if the output is still out of regulation.

Positive Output Voltage

To select a positive output voltage, tie the polarity pin (POL) to V_{DD} and use the typical boost topology shown in Figure 4. FB regulation voltage is 1.5V. For optimum stability, V_{OUT} should be greater than 1.1 (V_{BATT}).

Negative Output Voltage

To select a negative output voltage, tie POL to GND (Figure 5). In this configuration, the internal error amplifier's output is inverted to provide the correct feedback polarity. FB regulation voltage is 0V. D1, D2, C4, and C5 form an inverting charge pump to generate the negative voltage. This allows application of the positive boost switching topology to negative output voltages.

The negative output circuit has two possible connections. In the standard connection, D1's cathode is connected to BATT. This connection features the best output ripple performance, but $|V_{OUT}|$ must be limited to no more than 27V - 1.1(V_{BATT}). If a larger negative voltage is needed, an alternative connection allows a maximum negative output of -27V, but with the additional constraint that $|V_{OUT}| > 1.1V_{BATT}$. To use the alternative circuit, connect D1's cathode to ground rather than BATT (Figure 6). Increase C4 to 2.2µF to improve output ripple performance.

The negative charge pump limits the output current to the charge transferred each cycle multiplied by the

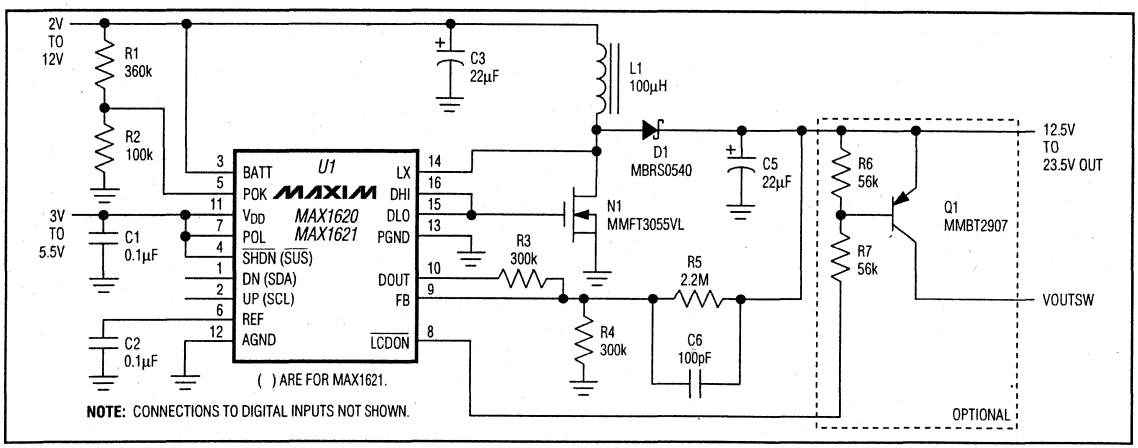


Figure 4. Typical Operating Circuit—Positive Output

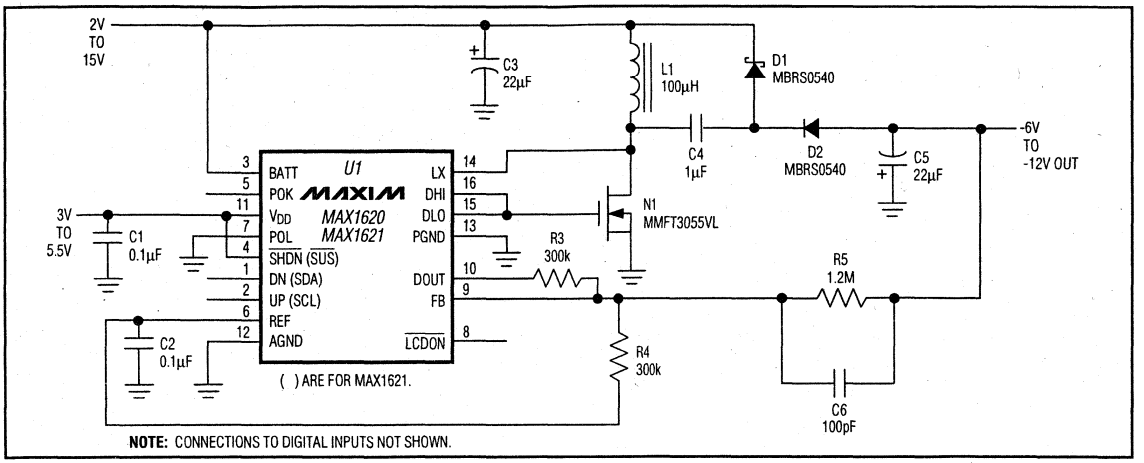


Figure 5. Typical Operating Circuit—Negative Output

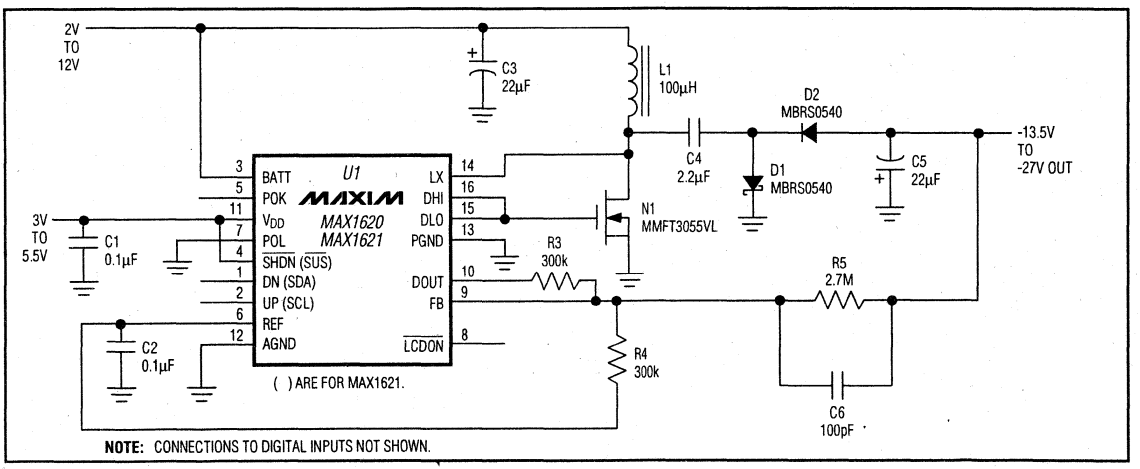


Figure 6. Alternative Negative Output—Maximum Voltage

maximum switching frequency. The following equation represents the output current for the ideal case (no power losses) of Figure 5:

$$I_{OUT} = \frac{1}{2} \times (k\text{-factor} / L) \times V_{BATT} / (V_{BATT} + V_{OUT})$$

This means that a higher peak current is required to achieve the same output current in the negative output circuit as in the positive output circuit.

The output current for Figure 6 uses the same current equation as the positive boost.

Output Voltage Control

The output voltage is set with a voltage divider to the feedback pin (FB). For a positive output, the divider is referred to GND; for a negative output, the divider is referred to REF.

Output voltage can be adjusted with an internal DAC summing current into FB through an external resistor. The 5-bit DAC is controlled with a user-programmable up/down counter. On power-up or after a reset, the counter sets the DAC output to 10000 binary, or half-scale.

Digitally Adjustable LCD Bias Supplies

The MAX1620 controls the DAC counter with the UP and DN pins. A rising edge on UP increases $|V_{OUT}|$ by decrementing the counter and decreasing the DAC output voltage one step; a rising edge on DN decreases $|V_{OUT}|$ by incrementing the counter and increasing the DAC output voltage one step. Holding both UP and DN high resets the counter to half-scale. The counter will **not** roll over at either the FS or ZERO code. The control direction of UP and DN reverses for a negative output, to maintain the same control direction of the output voltage in absolute magnitude.

The MAX1621 controls the counter to the DAC through the SMBus interface. The counter is treated as a 5-bit register and resets on power-up. The setting in the DAC is guaranteed to remain valid as long as V_{DD} is greater than the UVLO threshold (see Note 1 in the *Electrical Characteristics*).

The MAX1620/MAX1621's open-drain DMOSFET ($\overline{LCDON}$) can be used to disconnect the LCD panel from the positive bias voltage with an external transistor. The FET turns off ($\overline{LCDON}$ = float) if power-OK voltage (POK) falls below 1V. In the MAX1621, $\overline{LCDON}$ can also be controlled by the SMB command. $\overline{LCDON}$ cannot switch negative output voltages.

To prevent uncontrolled boosting when the output is disconnected, the feedback resistors must sense the boosted voltage rather than the output of the $\overline{LCDON}$ switch (Figure 4).

Shutdown Mode

The MAX1620 shuts down when the $\overline{SHDN}$ pin is low. The internal reference and biasing circuitry turn off, and the supply current drops to 9µA. In shutdown, DOUT = 0V and $\overline{LCDON}$ floats. UP/DN are ignored to preserve the DAC state for the MAX1620. Tie unused logic inputs to AGND for lowest operating current.

The MAX1621 can be shut down using the SMBus interface (Table 2).

Reset Modes

If the MAX1620 is not in shutdown mode, the DAC can be reset to mid-scale by holding UP and DN high. Mid-scale is 16 steps from the minimum DAC output and 15 steps from the maximum.

The MAX1620/MAX1621 reset the DAC counter to mid-scale at power-up or when V_{DD} is below the undervoltage lockout threshold of 2.2V (typ).

MAX1621 Digital Interface

A single byte of data written over the Intel SMBus controls the MAX1621. Figures 7 and 8 show example single-byte writes. The MAX1621 contains two 2-bit registers for storing configuration data, and one register for the 5-bit DAC data. Tables 1 and 2 describe the data format for the configuration registers. The MAX1621 responds only to its own address (0101100 binary).

The REGSEL bit addresses the configuration registers. REGSEL = 0 for the $\overline{SUS}$ register; REGSEL = 1 for the OPR register. Each configuration register consists of a $\overline{SHDN}$ bit and an LCDON bit. One of the two configuration registers is always active. The state of the $\overline{SUS}$ pin determines the active register. The OPR register is active with $\overline{SUS}$ = high. The $\overline{SUS}$ register is active with $\overline{SUS}$ = low.

Each byte written to the MAX1621 updates the DAC register. DAC data is preserved in shutdown and when toggling between configuration registers. Since there is only one DAC register, $\overline{SUS}$ cannot be used to toggle between two DAC codes.

Status information can be read from the MAX1621 using the SMBus read-byte protocol. Figure 9 shows an example status read and Table 3 describes the status-information format.

During shutdown ($\overline{SUS}$ = 1 and OPR-$\overline{SHDN}$ = 0, or $\overline{SUS}$ = 0 and $\overline{SUS}$-$\overline{SHDN}$ = 0), the MAX1621 serial interface remains fully functional and can be used to set either the OPR-$\overline{SHDN}$ or $\overline{SUS}$-$\overline{SHDN}$ bits to return the MAX1621 to its normal operational state.

Table 1. MAX1621 Configuration Byte with REGSEL = 0 (write to $\overline{SUS}$ register)

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A zero in this bit writes the next two bits into the $\overline{SUS}$ register and the remaining five bits into the DAC register (Figure 7).
6	$\overline{SUS}$-$\overline{SHDN}$	0	With $\overline{SUS}$ = low, 1 = operating, and 0 = shutdown.
5	$\overline{SUS}$-LCDON	0	With $\overline{SUS}$ = low, 1 = LCD on, and 0 = LCD off.
4	D4 (MSB)	1	DAC Input Data
3	D3	0	
2	D2	0	
1	D1	0	
0	D0	0	

**Initial register state after power-up.*

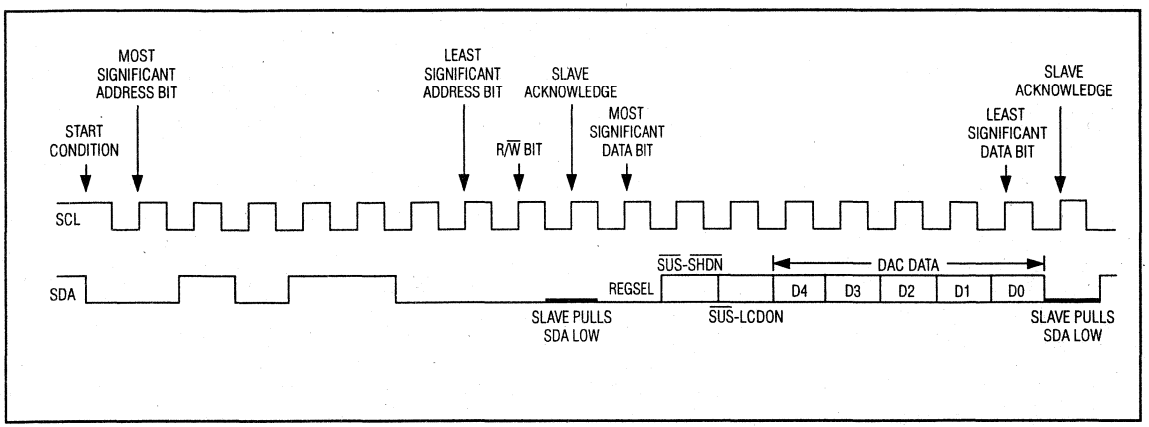


Figure 7. MAX1621 Serial-Interface Single-Byte Write Example (REGSEL = 0)

Table 2. MAX1621 Configuration Byte with REGSEL = 1 (write to OPR register)

BIT	NAME	POR STATE*	DESCRIPTION
7	REGSEL	—	Register Select. A one in this bit writes the next two bits into the OPR register and the remaining five bits into the DAC register (Figure 7).
6	OPR-$\overline{SHDN}$	1	With $\overline{SUS}$ = high, 1 = operating, and 0 = shutdown.
5	OPR-LCDON	1	With $\overline{SUS}$ = high, 1 = LCD on, and 0 = LCD off.
4 3 2 1 0	D4 (MSB) D3 D2 D1 D0	1 0 0 0 0	DAC Input Data

**Initial register state after power-up.*

Table 3. MAX1621 Status Bits

BIT	NAME	DESCRIPTION
7	POK	If the voltage applied to POK is greater than 0.992V and the MAX1621 is not shut down, this bit returns 1; otherwise, it returns 0.
6	—	Reserved for future use.
5	—	Reserved for future use.
4 3 2 1 0	D4 (MSB) D3 D2 D1 D0	DAC Register Data

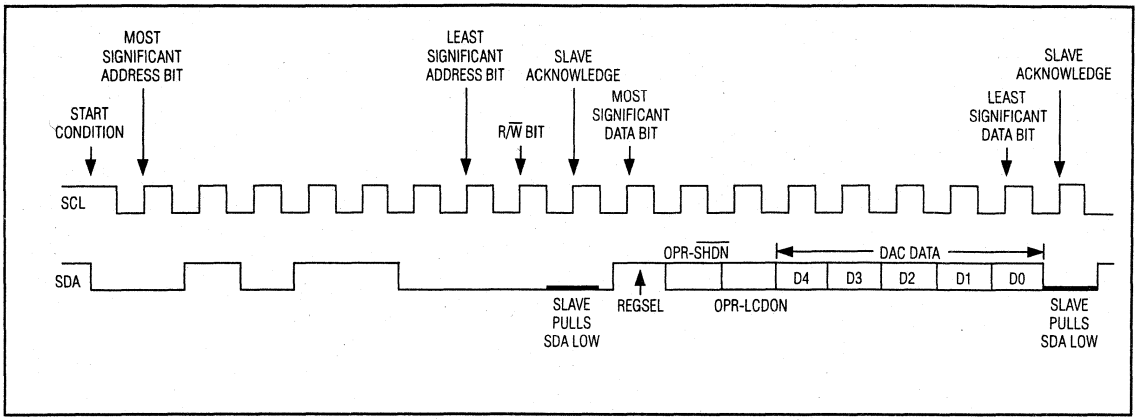


Figure 8. MAX1621 Serial-Interface Single-Byte Write Example (REGSEL = 1)

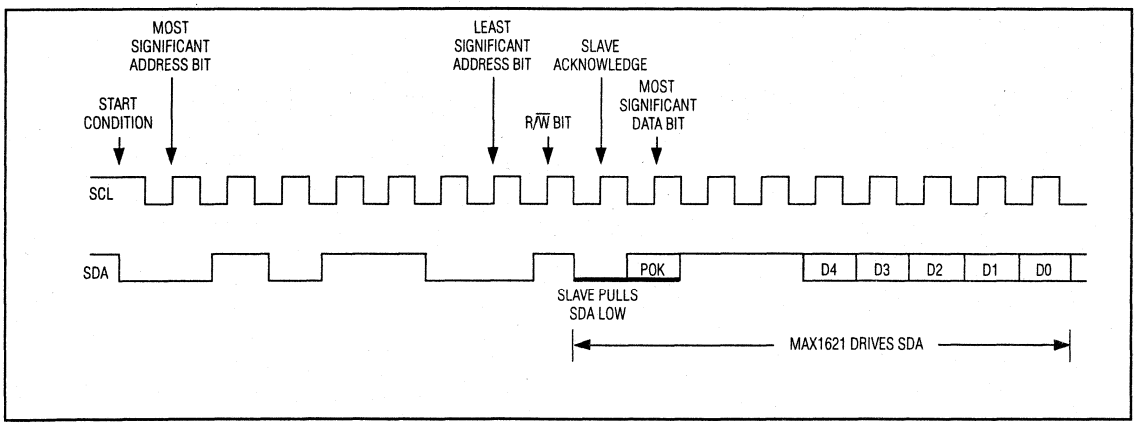


Figure 9. MAX1621 Serial-Interface Read Example

Design Procedure and Component Selection

The MAX1620/MAX1621 output voltage can be adjusted manually or via a digital interface. In addition, positive bias voltage can be switched with $\overline{LCDON}$ using an external PFET or PNP transistor.

Output Adjustment

Setting the Minimum Output Voltage

The minimum output voltage is set with a resistor-divider (R4-R5, Figure 4) from V_{OUT} to AGND. The FB threshold voltage is 1.5V. Choose R4 to be 300kΩ so that the current in the divider is about 5µA. Determine R5 as follows:

$$R5 = R4 \times (V_{OUT,MIN} - V_{FB}) / V_{FB}$$

For example, if $V_{OUT,MIN}$ = 12.5V:

$$R5 = 300k\Omega \times (12.5 - 1.5) / (1.5) = 2.2M\Omega$$

Mount R4 and R5 close to the FB pin to minimize parasitic capacitance.

For a negative output voltage, the FB threshold voltage is 0V, and R4 is placed between FB and REF (Figures 5 and 6). Again, choose R4 to be 300kΩ so that the current in the divider is about 5µA. Then determine R5 as follows:

$$R5 = R4 \times |V_{OUT,MIN} / V_{REF}|$$

For example, if $V_{OUT,MIN}$ = -12.5V:

$$R5 = 300k\Omega \times |(12.5) / (1.5)| = 2.5M\Omega$$

Setting the Maximum Output Voltage (DAC Adjustment)

The DAC is adjustable from 0V to 1.5V in 32 steps, and 1LSB = 1.5V / 31. DAC adjustment of V_{OUT} is provided by adding R3 to the divider circuit (Figure 4). Be sure that $V_{OUT,MAX}$ does not exceed the LCD panel rating.

For $V_{OUT,MAX}$ = 25V and $V_{OUT,MIN}$ = 12.5V, R3 is determined as follows:

$$R3 = R5 \times (V_{FB}) / (V_{OUT,MAX} - V_{OUT,MIN})$$
$$= 2.2M\Omega \times (1.5) / (25 - 12.5) = 264k\Omega$$

The general form for V_{OUT} as a function of the DAC output (V_{DOUT}) is:

$$V_{OUT} = V_{OUT,MIN} + (V_{FB} - V_{DOUT}) \times R5 / R3$$

At power-up the DAC resets to mid-scale (10000), which corresponds to V_{DOUT} = 0.774V; therefore, the output voltage after reset is as follows:

$$V_{OUT,RESET} = V_{OUT,MIN} + (1.5 - 0.774) \times R5 / R3$$

Note that for a positive output voltage, V_{OUT} increases as V_{DOUT} decreases. $V_{OUT,MAX}$ corresponds to V_{DOUT} = 0V, and $V_{OUT,MIN}$ corresponds to V_{DOUT} = 1.5V.

For a negative output voltage, $V_{OUT} = V_{OUT,MIN} + (V_{FB} - V_{DOUT}) \times R5 / R3$. Assume $V_{OUT,MAX}$ = -25V and $V_{OUT,MIN}$ = -12.5V; then determine R3 and $V_{OUT,RESET}$ as follows:

$$R3 = R5 \times (V_{FB} - V_{DOUT,MAX}) / (V_{OUT,MAX} - V_{OUT,MIN})$$
$$= 2.5M\Omega \times (0 - 1.5) / (-25 - -12.5) = 300k\Omega$$

$$V_{OUT,RESET} = -12.5 + (0 - 0.774) \times (2.5M) / (300k) = -18.95V$$

Note that for a negative output voltage, $|V_{OUT}|$ increases as V_{DOUT} increases. $|V_{OUT,MAX}|$ corresponds to V_{DOUT} = 1.5V, and $|V_{OUT,MIN}|$ corresponds to V_{DOUT} = 0V.

Potentiometer Adjustment

The output can be adjusted with a potentiometer instead of the DAC. Choose R_{POT} = 100kΩ, and connect it between REF and GND. Connect R3 to the potentiometer's wiper, instead of to DOUT. The same design equations as above apply.

Controlling the LCD Using POK and $\overline{LCDON}$

When voltage at POK is greater than 1V, the open-drain $\overline{LCDON}$ output pulls low. $\overline{LCDON}$ withstands 27V; therefore, it can drive a PFET or PNP transistor to switch on the MAX1620/MAX1621's positive output. The following represent three cases for using this feature:

1) As an off switch, to ensure that a positive boosted output goes to 0V during shutdown. In this case, connect POK to $\overline{SHDN}$. Without this switch, the positive output falls to one diode-drop below the input voltage (V_{BATT}) in shutdown. $\overline{LCDON}$ is not needed for negative outputs, which will fall to 0V in shutdown anyway.
2) As an output sensing cutoff for positive outputs. Connect POK to the feedback voltage divider to sense the output voltage. The output is switched on only when it reaches a set percentage of the set voltage.
3) As an input sensing output cutoff for positive outputs. Connect POK to a voltage divider to sense the input voltage. The output is switched on only when the input reaches the set level (Figure 4).

To control the open-drain output $\overline{LCDON}$ by sensing the input voltage, connect a resistor-divider (R1-R2, Figure 4) from V_{BATT} to POK. Choose R2 = 100k. For example, if the minimum battery voltage is 5.3V, determine R1 as follows:

$$R1 = R2 \times [(V_{BATT} / V_{POK}) - 1]$$
$$= 100k \times [(5.3 / 0.992) - 1] = 434k\Omega$$

$\overline{LCDON}$ can also be controlled via software (MAX1621, Table 4).

Table 4. MAX1621 $\overline{LCDON}$ Output Truth Table

POK Pin	LCDON Bit	$\overline{LCDON}$ Output
<1V	0	Floating
<1V	1	Floating
>1V	0	Floating
>1V	1	ON, pulls low

Digitally Adjustable LCD Bias Supplies

$\overline{LCDON}$ typically drives an external PNP transistor, switching a positive V_{OUT} to the LCD. R7 limits the base current in the PNP; R6 turns off the PNP when $\overline{LCDON}$ is floating. R6 and R7 can be the same value. Choose R7 such that the minimum base current is greater than 1/50 of the collector current. For example, assume $V_{OUT,MIN}$ = 12.5V and I_{LCD} = 10mA, then determine R7 as follows:

$$R7 \leq 50 \times (12.5 - 0.7) / 10mA = 59k\Omega$$

Remember that LCD voltage is the regulated output voltage minus the drop across the PNP switch. The drop across the external transistor (typically 300mV) must be accounted for.

If a PFET is preferred for the $\overline{LCDON}$ switch, R6 and R7 in Figure 4 may both be raised to 1MΩ or more to reduce operating current. Be sure to choose a P_{FET} with adequate breakdown voltage. Since load current is typically on the order of 10mA, an on-resistance of 10Ω or less is usually adequate.

Choosing an Inductor

Practical inductor values range from 33µH to 1mH; however, 100µH is a good choice for a wide range of applications. Inductors with a ferrite core or equivalent are recommended. The inductor's current rating should exceed the peak current as set by the k-factor and the coil inductance; however, for most inductor types, the coil's specified current can be exceeded by 20% with no impact on efficiency.

The peak current is set by the coil inductance as follows:

$$I_{PK} = \text{k-factor} / L$$

and

$$I_{OUT,MIN} = \frac{1}{2} \times I_{PK} \times V_{BATT,MIN} / V_{OUT,MAX}$$

If we assume that $V_{BATT,MIN}$ = 5.3V, $V_{OUT,MAX}$ = 25V, $I_{OUT,MIN}$ = 15mA, and a minimum k-factor of 16µs-V, then the required I_{PK} is:

$$I_{PK} = 2 \times 15mA \times 25 / 5.3 = 142mA$$

and

$$L \leq = 16\mu s\text{-}V / 142mA = 113\mu H$$

The next-lowest practical inductor value is 100µH. Its current rating must be:

$$24\mu s\text{-}V \text{ (maximum k-factor)} / 100\mu H = 240mA$$

Table 5 summarizes the minimum inductance value needed to provide various output currents at several minimum input voltages. Table 6 lists some suitable coil types and manufacturers, but is not intended to be a complete list.

Table 5. Maximum Inductance vs. I_{OUT} and $V_{BATT,MIN}$ (20V output)

		$V_{BATT,MIN}$					
		1.8V	**2.7V**	**3.6V**	**5.4V**	**7.2V**	**12V**
IOUT	**5mA**	100µH	150µH	220µH	330µH	390µH	680µH
	10mA	56µH	82µH	100µH	150µH	220µH	330µH
	20mA	27µH	39µH	56µH	82µH	100µH	180µH
	30mA	18µH	27µH	33µH	56µH	68µH	120µH

Table 6. Inductor List

COMPANY	PART	µH RANGE	SIZE IN mm (H x W x L)	COMMENTS
Sumida USA (847) 956-0666 Japan 81-3-3607-5111	CD43	Up to 68µH	3.2 x 4 diameter	
	CD54	Up to 220µH	4.5 x 5.2 diameter	
	CDRH62B	Up to 330µH	3 x 6.2 x 6.2	Shielded
Coilcraft (847) 639-6400	DO1608	Up to 1mH	3.18 x 4.45 x 6.6	
	DT1608	Up to 400µH	3.18 x 4.45 x 6.6	Shielded
TDK (847) 390-4373	NLC565050	Up to 1mH	5 x 5 x 5.6	
	TPF0410	Up to 1mH	4 diameter x 10 L	Leaded coil

Diode Selection

The high maximum switching frequency of 300kHz requires a high-speed rectifier. Schottky diodes, such as the MBRS0540, are recommended. To maintain high efficiency, the average current rating of the Schottky diode must be greater than the peak switching current. Choose a reverse breakdown voltage greater than the positive output voltage or greater than the negative output voltage plus V_{BATT}.

External Switching Transistor

Again, the high maximum switching frequency requires a high-speed switching transistor to maintain efficiency. Logic-level N-channel MOSFETs, such as the MMFT3055VL, are recommended (N1). Choose a V_{DS} rating greater than the positive output voltage or greater than the negative output voltage plus V_{BATT}.

To save cost in certain applications, a bipolar transistor may be substituted for the MOSFET with a decrease in efficiency. The conditions favoring substitution are limited input voltage range (V_{DD}), low maximum battery voltage (V_{BATT}), and low output current. For example, V_{DD} = 3.0V to 3.6V, $V_{BATT,MAX}$ = 12V, and I_{OUT} = 5mA favors a bipolar transistor substitution to reduce cost.

To modify the Typical Operating Circuit (Figures 4 and 5) for a bipolar switching transistor, connect the collector to the inductor, the base to DLO, and the emitter to PGND (Figure 10). Connect the base to DHI through a series resistor to limit the base current. Choose the resistor such that the minimum base current is greater than 1/20 of the peak inductor current. For example, assume $V_{DD,MIN}$ = 3V and I_{PK} = 100mA; then $R_S \leq 20 \times (3 - 0.7) / 100mA = 460\Omega$.

Output Filter Capacitor

A 22µF, 35V, low-ESR, surface-mount tantalum output capacitor is sufficient for most applications. Output ripple voltage is dominated by the peak switch current multiplied by the output capacitor's effective series resistance (ESR). 100mVp-p output ripple is a good target for the trade-off between cost and performance. Capacitors smaller than 22µF may be used for light loads and lower peak current. Surface-mount capacitors are generally preferred because they lack the inductance and resistance of their through-hole equivalents. The AVX TPS series and the Sprague 593D and 595D series are good choices for low-ESR surface-mount tantalum capacitors.

Moderate-performance aluminum-electrolytic or tantalum capacitors can be successfully substituted in cost-sensitive applications with low output current. Matsuo and Nichicon provide suitable choices.

Input Bypass Capacitor

Two inputs, V_{DD} and V_{BATT}, require bypass capacitors. Bypass V_{DD} with a 0.1µF ceramic capacitor as close to the IC as possible. The battery supplies high currents to the inductor and requires local bulk bypassing close to the inductor. A 22µF low-ESR surface-mount capacitor is sufficient for most applications. Smaller capacitors are acceptable if peak inductor current is low or the battery's internal impedance is low and the battery is close to the inductor.

Charge-Pump Capacitor (Negative Output)

Possible negative output topologies are shown in Figures 5 and 6. Overall efficiency for the negative output configuration is less than for the positive output circuit because of the extra components in the power-transfer path. For efficient charge transfer, C4 must have low ESR and should be smaller than the output capacitor (C5). C4 sees the same voltage as C5, and should have the same voltage rating. A 1µF ceramic capacitor is a practical choice for cost and performance considerations. 2.2µF is suggested for Figure 6's circuit.

Feedback-Compensation Capacitor

The high value of the feedback resistors (R3, R4, R5, Figure 4) makes the feedback loop susceptible to phase lag because of the parasitic capacitance at the FB pin. To compensate for this, connect a capacitor (C6, Figure 4) in parallel with R5. The value of C6 depends on the parallel combination of R3, R4, R5, and the individual circuit layout. Typical values range from 33pF to 220pF.

Reference-Compensation Capacitor

The internal reference uses an external capacitor for frequency compensation. Connect a ceramic capacitor with a 0.1µF minimum value between REF and ground.

PC Board Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. In particular, keep all traces short, especially those connected to the FB pin and those connecting N1, L1, D1, D2, C4, and C5. Place R3, R4, and R5 as close to the feedback pin as possible.

Use a star ground configuration: connect the grounds of the input bypass capacitor, the output capacitor, and the switching transistor together, close to the IC's PGND pin. Tie AGND and PGND together at the chip.

Digitally Adjustable LCD Bias Supplies

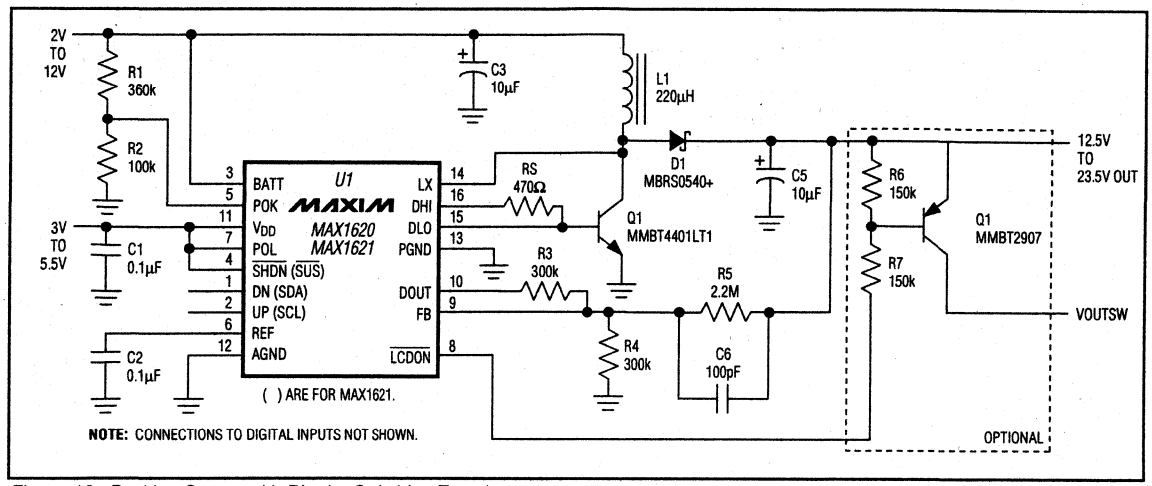
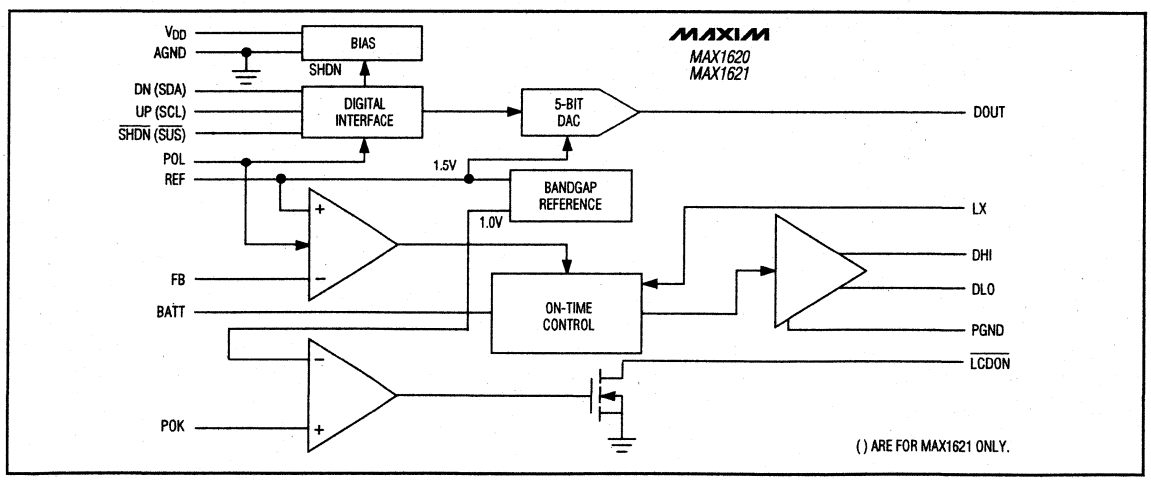


Figure 10. Positive Output with Bipolar Switching Transistor

Simplified Block Diagram



Chip Information

TRANSISTOR COUNT: 341

SUBSTRATE CONNECTED TO AGND

19-1227; Rev 1; 6/97

EVALUATION KIT AVAILABLE

MAXIM

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

General Description

The MAX1624/MAX1625 are ultra-high-performance, step-down DC-DC controllers for CPU power in high-end computer systems. Designed for demanding applications in which output voltage precision and good transient response are critical for proper operation, they deliver over 35A from 1.1V to 3.5V with ±1% total accuracy from a +5V ±10% supply. Excellent dynamic response corrects output transients caused by the latest dynamically clocked CPUs. These controllers achieve over 90% efficiency by using synchronous rectification. Flying-capacitor bootstrap circuitry drives inexpensive, external N-channel MOSFETs.

The switching frequency is resistor programmable from 100kHz to 1MHz. High switching frequencies allow the use of a small surface-mount inductor and decrease output filter capacitor requirements, reducing board area and system cost.

The MAX1624 is available in a 24-pin SSOP and offers additional features such as a digitally programmable output in 100mV increments; adjustable transient response; selectable 0.5%, 1%, or 2% AC load regulation; and gate drive for a current-boost MOSFET. The MAX1625 is resistor adjustable and comes in a 16-pin narrow SO package. Other features in both controllers include internal digital soft-start, a power-good output, and a 3.5V ±1% reference output. For a similar controller compatible with the latest Intel V_{RM}/V_{ID} specification, see the MAX1638* data sheet.

Applications

Pentium Pro™, Pentium II™, PowerPC™, Alpha™, and K6™ Systems

Desktop Computers

LAN Servers

Industrial Computers

GTL Bus Termination

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1624EAG	-40°C to +85°C	24 SSOP
MAX1625ESE	-40°C to +85°C	16 Narrow SO

Pin Configurations appear at end of data sheet.

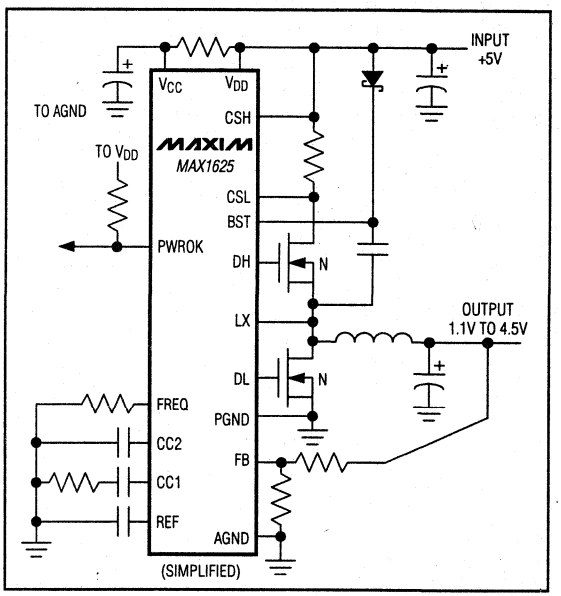
**Future product.*

Pentium Pro and Pentium II are trademarks of Intel Corp.
PowerPC is a trademark of IBM Corp.
Alpha is a trademark of Digital Equipment Corp.
K6 is a trademark of Advanced Micro Devices.
GlitchCatcher is a trademark of Maxim Integrated Products.

Features

- ♦ **Better than ±1% Output Accuracy Over Line and Load**
- ♦ **90% Efficiency**
- ♦ **Excellent Transient Response**
- ♦ **Resistor-Programmable Fixed Switching Frequency from 100kHz to 1MHz**
- ♦ **Over 35A Output Current**
- ♦ **Digitally Programmable Output from 1.1V to 3.5V in 100mV Increments (MAX1624)**
- ♦ **Resistor-Adjustable Output down to 1.1V (MAX1625)**
- ♦ **Remote Sensing**
- ♦ **Adjustable AC Loop Gain (MAX1624)**
- ♦ **GlitchCatcher™ Circuit for Fast Load-Transient Response (MAX1624)**
- ♦ **Power-Good (PWROK) Output**
- ♦ **Current-Mode Feedback**
- ♦ **Digital Soft-Start**
- ♦ **Strong 2A Gate Drivers**
- ♦ **Current-Limited Output**

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{CC}, PWROK to AGND .....-0.3V to 6V
PGND to AGND .....±0.3V
CSH, CSL to AGND .....-0.3V to (V_{CC} + 0.3V)
NDRV, PDRV, DL to PGND.....-0.3V to (V_{DD} + 0.3V)
REF, CC1, CC2, LG, D0–D4, FREQ,
FB to AGND.....-0.3V to (V_{CC} + 0.3V)
BST to PGND .....-0.3V to 12V
BST to LX.....-0.3V to 6V
DH to LX.....(LX - 0.3V) to (BST + 0.3V)

Continuous Power Dissipation (T_A = ±70°C)
24 Pin SSOP (derate 8.00mW/°C above +70°C) 640mW
16 Pin Narrow SO (derate 8.70mW/°C above 70°C).....696mW
Operating Temperature Range
MAX162_E_ _.....-40°C to +85°C
Storage Temperature Range .....-65°C to +125°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, R_{FREQ} = 33.3kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC} = V_{DD}			4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis			4.0		4.2	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV	Operating mode				2.5	mA
		Standby mode				0.3	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV, operating or standby mode					0.1	mA
Reference Voltage	No load			3.465	3.5	3.535	V
Reference Load Regulation	0µA < I_{LOAD} < 100µA					10	mV
Reference Undervoltage Lockout	Rising edge, 1% hysteresis			2.7		3.0	V
Reference Short-Circuit Current	V_{REF} = 0V			0.5		4.0	mA
FB Accuracy	MAX1624, over line and load (Note 1)	T_A = +25°C to +85°C				±1	%
		T_A = 0°C to +85°C				±1.5	
FB Set Voltage	MAX1625, over line and load (Note 2)	T_A = +25°C to +85°C				±1	%
		T_A = 0°C to +85°C				±1.5	
AC Load Regulation (Note 3)	CSH - CSL = 0mV to 80mV	MAX1624	LG = GND		0.5		%
			LG = REF		1		
			LG = V_{CC}		2		
		MAX1625			1		
DC Load Regulation (Note 3)	CSH - CSL = 0mV to 80mV	MAX1624	LG = GND		0.05		%
			LG = REF		0.1		
			LG = V_{CC}		0.2		
		MAX1625			0.1		
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}			-7.5	-6	-4.5	%
	Falling FB, 1% hysteresis with respect to V_{REF}			6.5	8	9.5	
PWROK Output Voltage Low	I_{SINK} = 2mA, V_{CC} = 4.5V					0.4	V
PWROK Output Current High	PWROK = 5.5V					1	µA
Switching Frequency	R_{FREQ} = 20kΩ			850	1000	1150	kHz
	R_{FREQ} = 33.3kΩ			540	600	660	
	R_{FREQ} = 200kΩ			85	100	115	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, R_{FREQ} = 33.3kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle	R_{FREQ} = 20kΩ		85	90		%
LG Input Voltage	LG = GND (low)				0.2	V
	LG = REF (mid)		3.3		3.7	
	LG = V_{CC} (high)		V_{CC} - 0.2			
Logic Input Voltage Low	D0–D4; V_{CC} = 5.5V				0.8	V
Logic Input Voltage High	D0–D4; V_{CC} = 4.5V		2.0			V
D0–D4 Input Current	D0–D4 = 0V, 5V				±1	µA
LG Input Current					4	µA
CSH, CSL Input Current	MAX1624, CSH = CSL = 1.3V, D0–D3 = 5V, D4 = 0V				50	µA
	MAX1625, CSH = CSL = 1.1V				50	
FB Input Current	FB = 1.1V				±0.1	µA
CC1 Output Resistance				10		kΩ
CC2 Transconductance				1		mmho
CC2 Clamp Voltage	Minimum		2.4		3.0	V
	Maximum		4		V_{CC}	
CC2 Source/Sink Current	100mV overdrive			100		µA
DH On-Resistance	BST - LX = 4.5V			0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V			0.7	2	Ω
DH, DL Source/Sink Current	DH = DL = 2.5V			2		A
DH, DL Dead Time			0	30		ns
PDRV Trip Level	With respect to V_{REF}, FB going low	T_A = +25°C	-2.75	-2	-1.25	%
		T_A = 0°C to +85°C	-3		-1	
NDRV Trip Level	With respect to V_{REF}, FB going high	T_A = +25°C	1.25	2	2.75	%
		T_A = 0°C to +85°C	1		3	
PDRV, NDRV Response Time	FB overdrive = 5%			75		ns
PDRV, NDRV On-Resistance	V_{DD} = 4.5V			2	5	Ω
PDRV, NDRV Source/Sink Current	PDRV = NDRV = 2.5V			0.5		A
PDRV, NDRV Minimum On-Time				100		ns
Current-Limit Trip Voltage			85	100	115	mV
Soft-Start Time	To full current limit			1536		1 / fosc
BST Leakage Current	BST = 12V, LX = 7V, REF = GND				50	µA

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3= 0V, R_{FREQ} = 33.3kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC} = V_{DD}		4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis		3.9		4.3	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV	Operating mode			3	mA
		Standby mode			0.4	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV, operating or standby mode				0.2	mA
Reference Voltage	No load		3.447	3.5	3.553	V
FB Accuracy	MAX1624, over line and load				±2.5	%
FB Set Voltage	MAX1625				±2.5	%
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}		-8	-6	-4	%
	Falling FB, 1% hysteresis with respect to V_{REF}		6	8	10	
Switching Frequency	R_{FREQ} = 20kΩ		800	1000	1200	kHz
	R_{FREQ} = 33.3kΩ		510	600	690	
	R_{FREQ} = 200kΩ		80	100	120	
Maximum Duty Cycle	R_{FREQ} = 20kΩ		84	90		%
DH On-Resistance	BST - LX = 4.5V			0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V			0.7	2	Ω
Current-Limit Trip Voltage			70	100	130	mV

Note 1: FB accuracy is 100% tested at FB = 3.5V (code 10000) with V_{CC} = V_{DD} = 4.5V to 5.5V and CSH - CSL = 0mV to 80mV. The other DAC codes are tested at the major transition points with V_{CC} = V_{DD} = 5V and CSH - CSL = 0. FB accuracy at other DAC codes over line and load is guaranteed by design.

Note 2: FB set voltage is 100% tested with V_{CC} = V_{DD} = 4.5V to 5.5V and CSH - CSL = 0mV to 80mV.

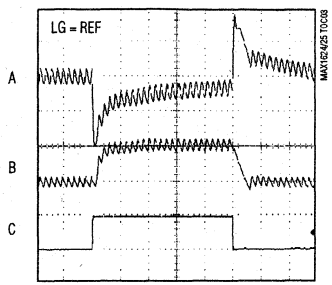
Note 3: AC load regulation sets the AC loop gain, to make tradeoffs between output filter capacitor size and transient response, and has only a slight effect on DC accuracy or DC load-regulation error.

Note 4: Specifications from 0°C to -40°C are not production tested.

Typical Operating Characteristics

(T_A = +25°C, using the MAX1624 evaluation kit, unless otherwise noted.)

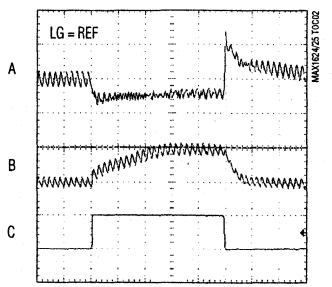
MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(1.1V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

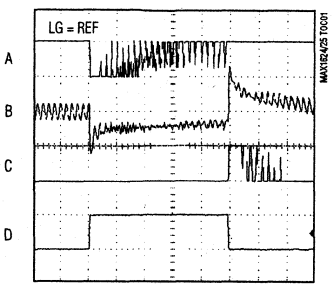
MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(1.1V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

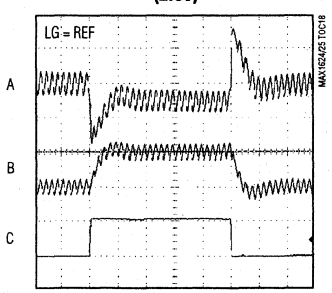
MAX1624
LOAD-TRANSIENT RESPONSE DETAIL
(WITH GLITCHCATCHER)
(1.1V)



10µs/div

A: PDRV, 5V/div
B: V_{OUT}, 50mV/div, AC COUPLED
C: NDRV, 5V/div
D: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

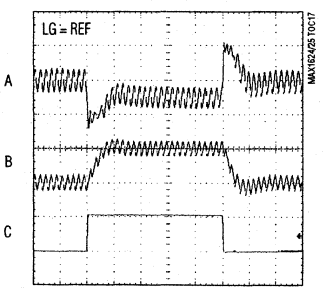
MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(2.5V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

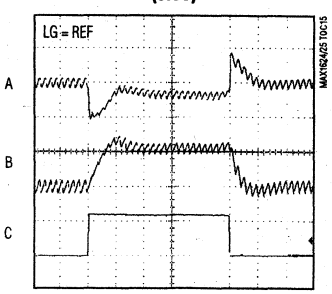
MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(2.5V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(3.5V)



10µs/div

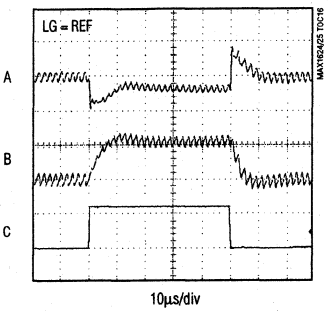
A: V_{OUT}, 100mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 11A, t_{RISE} = t_{FALL} = 100ns

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Typical Operating Characteristics (continued)

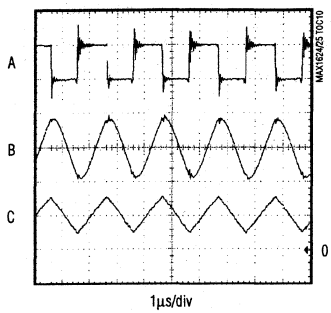
(T_A = +25°C, using the MAX1624 evaluation kit, unless otherwise noted.)

MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(3.5V)



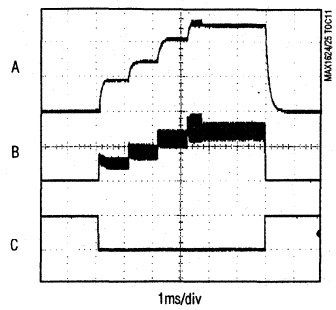
A: V_{OUT}, 100mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 11A, t_{RISE} = t_{FALL} = 100ns

MAX1624
SWITCHING WAVEFORMS



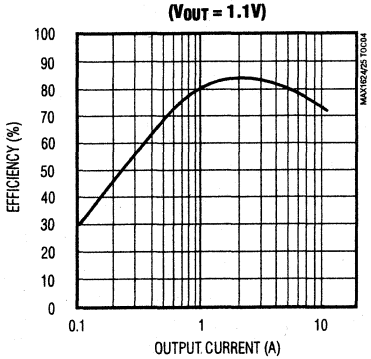
V_{IN} = 5V, V_{OUT} = 2.5V, LOAD = 5A
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 5A/div

MAX1624
STARTUP AND STANDBY RESPONSE

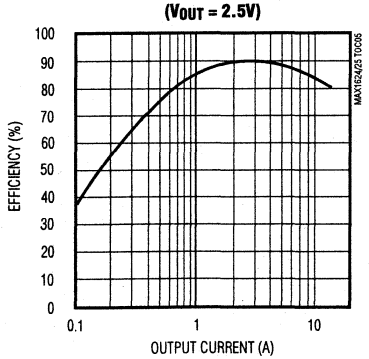


V_{IN} = 5V, V_{OUT} = 2.5V, LOAD = 13.8A
A: V_{OUT}, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: STANDBY, D0–D4

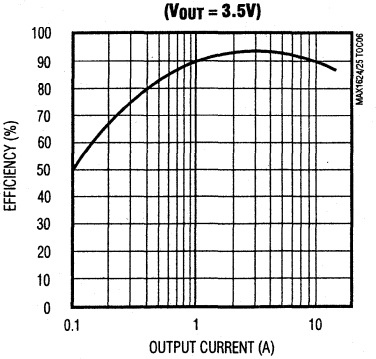
MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 1.1V)



MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 2.5V)



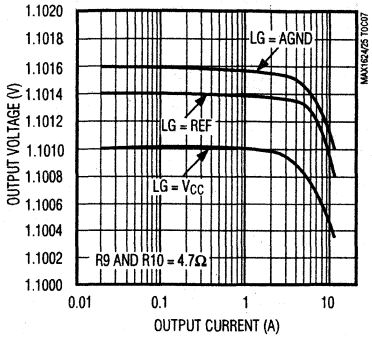
MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 3.5V)



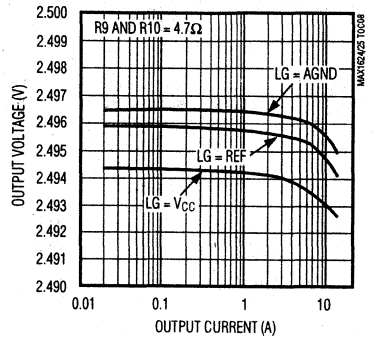
Typical Operating Characteristics (continued)

(T_A = +25°C, using the MAX1624 evaluation kit, unless otherwise noted.)

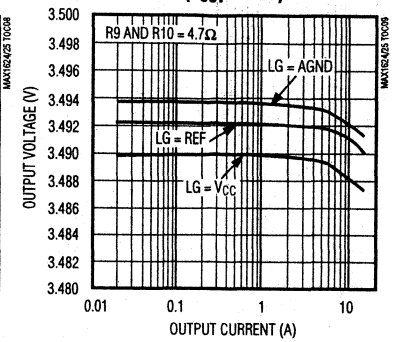
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 1.1V)



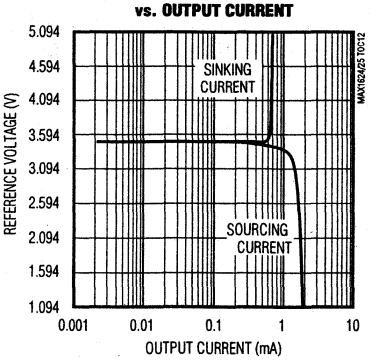
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 2.5V)



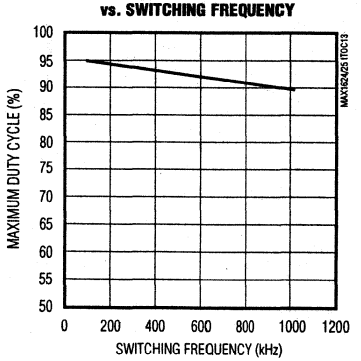
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 3.5V)



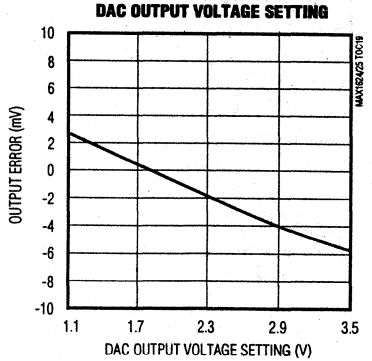
REFERENCE VOLTAGE
vs. OUTPUT CURRENT



MAXIMUM DUTY CYCLE
vs. SWITCHING FREQUENCY



MAX1624
OUTPUT ERROR vs.
DAC OUTPUT VOLTAGE SETTING



High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Pin Description

PIN		NAME	FUNCTION
MAX1624	MAX1625		
1	1	BST	Boost-Capacitor Bypass for High-Side MOSFET Gate Drive. Connect a 0.1µF capacitor and low-leakage Schottky diode as a bootstrapped charge-pump circuit to derive a 5V gate drive from V_{DD} for DH.
2	2	PWROK	Open-Drain Logic Output. PWROK is high when the voltage on FB is within +8% and -6% of its setpoint.
3	3	CSL	Current-Sense Amplifier's Inverting Input. Place the current-sense resistor very close to the controller IC, and use a Kelvin connection. Use an RC filter network at CSL (Figure 1).
4	4	CSH	Current-Sense Amplifier's Noninverting Input. Use an RC filter network at CSH (Figure 1).
5, 6, 7	—	D2, D1, D0	Digital Inputs for Programming the Output Voltage. D0–D4 are logic inputs that set the output to a voltage between 1.1V and 3.5V in 100mV increments.
8	—	LG	Loop Gain-Control Input. LG is a three-level input that is used to trade off loop gain vs. AC load-regulation and load-transient response. Connect LG to V_{CC}, REF, or AGND for 2%, 1%, or 0.5% AC load-regulation errors, respectively.
9	5	V_{CC}	Analog Supply Input, 5V. Use an RC filter network, as shown in Figure 1.
10	6	REF	Reference Output, 3.5V. Bypass REF to AGND with 0.1µF (min). Sources up to 100µA for external loads. Force REF below 2V to turn off the controller.
11	7	AGND	Analog Ground
12	8	FB	Voltage-Feedback Input. **MAX1624:** Connect FB to the CPU's remote voltage-sense point. The voltage at this input is regulated to a value determined by D0–D4. **MAX1625:** Connect a feedback resistor voltage divider close to FB from the output to AGND. FB is regulated to 1.1V.
13	9	CC1	Fast-Loop Compensation Capacitor Input. Connect a ceramic capacitor and resistor in series from CC1 to AGND. See the section *Compensating the Feedback Loop.*
14	10	CC2	Slow-Loop Compensation Capacitor Input. Connect a ceramic capacitor from CC2 to AGND. See the section *Compensating the Feedback Loop.*
15	11	FREQ	Frequency-Programming Input. Attach a resistor within 0.2 in. (5mm) of FREQ to AGND to set the switching frequency between 100kHz and 1MHz. The FREQ pin is normally 2V DC.
16, 17	—	D4, D3	Digital Inputs for Programming the Output Voltage
18	—	NDRV	GlitchCatcher N-Channel MOSFET Driver Output. NDRV swings between V_{DD} and PGND.
19	—	PDRV	GlitchCatcher P-Channel MOSFET Driver Output. PDRV swings between V_{DD} and PGND.
20	12	V_{DD}	5V Power Input for MOSFET Drivers. Bypass V_{DD} to PGND within 0.2 in. (5mm) of the V_{DD} pin using a 0.1µF capacitor and 4.7µF capacitor connected in parallel.
21	13	DL	Low-Side Synchronous Rectifier Gate-Drive Output. DL swings between PGND and V_{DD}. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers.*
22	14	PGND	Power Ground
23	15	LX	Switching Node. Connect LX to the high-side MOSFET source and inductor.
24	16	DH	High-Side Main MOSFET Switch Gate-Drive Output. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers.*

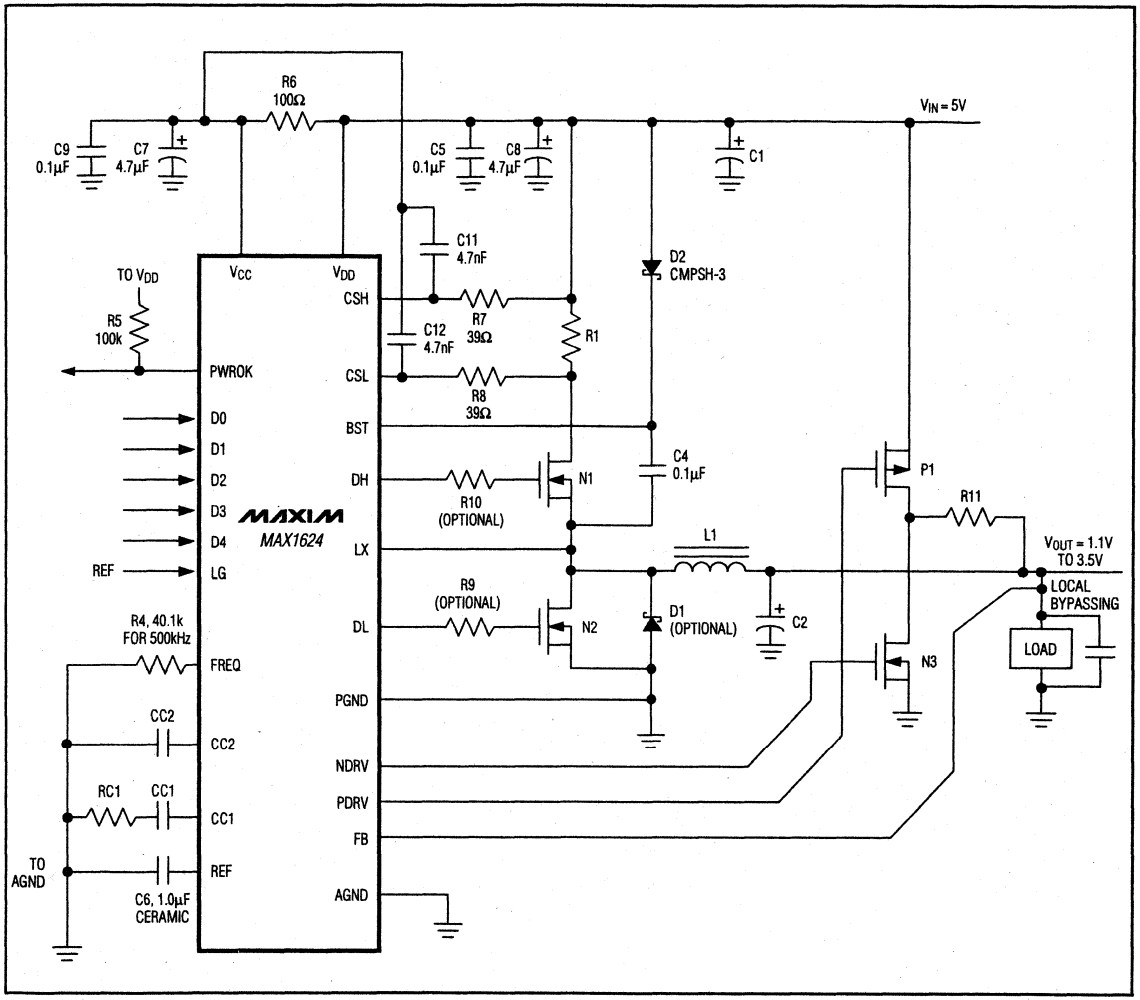


Figure 1. MAX1624 Standard Application Circuit

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

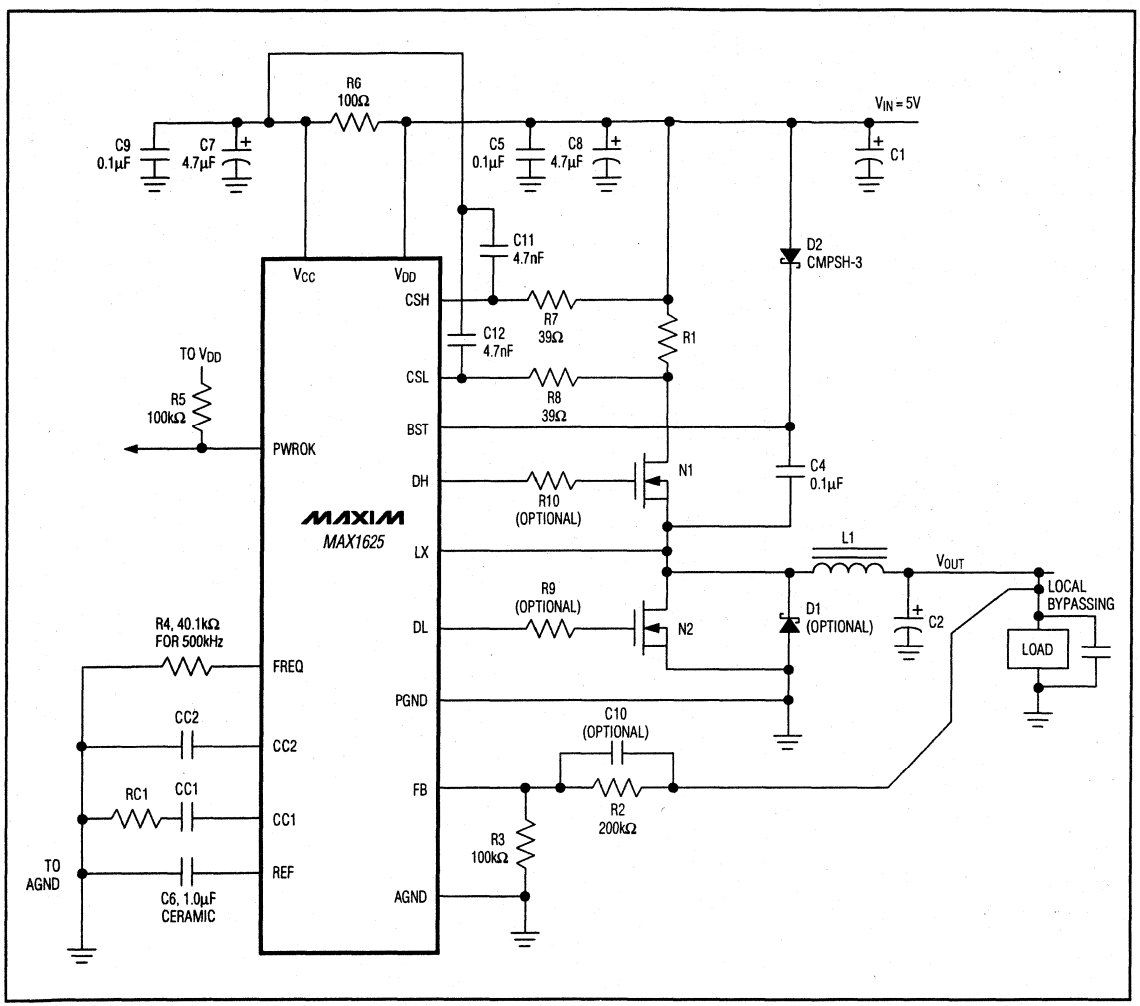


Figure 2. MAX1625 Standard Application Circuit

Table 1. Component List for Standard 3.3V Applications by Load Current* (Output Voltage = 3.3V, Frequency = 500kHz)

COMPONENT	DESCRIPTION BY LOAD CURRENT		
	6A	12A	11A (LOW-COST V_{RM})
Application Equipment	Power PC/Pentium/GTL bus termination	Pentium Pro	Pentium Pro
C1 Input Capacitor	100µF, 10V Sanyo OS-CON 10SL100M	3 x 100µF, 10V Sanyo OS-CON 10SL100M	3 x 2700µF, 6.3V aluminum electrolytic, Sanyo 6MV2700GX
C2 Output Capacitor	2 x 220µF, 4V Sanyo OS-CON 4SP220M	3 x 220µF, 4V Sanyo OS-CON 4SP220M	4 x 2700µF, 6.3V aluminum electrolytic, Sanyo 6MV2700GX
C10 Capacitor	Optional (see text)		
CC1 Capacitor	680pF ceramic	1000pF ceramic	1000pF ceramic
CC2 Capacitor	0.056µF ceramic	0.056µF ceramic	0.056µF ceramic
D1 Rectifier	Optional Schottky, Nihon NSQ03A02	Optional Schottky, Nihon NSQ03A02	Optional Schottky, Nihon NSQ03A02
D2 Rectifier	Central Semiconductor CMPSH-3	Central Semiconductor CMPSH-3	Central Semiconductor CMPSH-3
L1 Inductor	1.5µH, 8A Coiltronics UP2-1R5	0.5µH, 17A Coilcraft DO5022P-501HC	0.5µH Coiltronics UP4-R47, Coilcraft DO5022P-501HC
N1 High-Side MOSFET	International Rectifier IRF7413	International Rectifier IRL3103S, D^2PAK	International Rectifier IRF7413 x 2
N2 Low-Side MOSFET	International Rectifier IRF7413	International Rectifier IRL3103S, D^2PAK	International Rectifier IRF7413 x 2
N3/P1 (MAX1624)		International Rectifier IRF7107	
R1 Resistor	12mΩ Dale WSL-2512-R012-F	2 x 12mΩ in parallel, Dale WSL-2512-R012-F	2 x 12mΩ in parallel Dale WSL-2512-R012-F
R2 Resistor	200kΩ, 1% resistor	N/A	N/A
R3 Resistor	100kΩ, 1% resistor	N/A	N/A
R11 Resistor (MAX1624)		500mΩ Dale WSL-2512-R500	N/A
RC1 Resistor	1kΩ, 5% resistor	1kΩ, 5% resistor	1kΩ, 5% resistor

**MAX1624: LG = REF, D4–D0 = 10010.*

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Table 2. Component Suppliers

SUPPLIER	USA PHONE	FACTORY FAX
AVX	(803) 946-0690	(803) 626-3123
Central Semiconductor	(516) 435-1110	(516) 435-1824
Coilcraft	(847) 639-6400	(847) 639-1469
Coiltronics	(561) 241-7876	(561) 241-9339
Dale Inductors	(605) 668-4131	(605) 665-1627
International Rectifier	(310) 322-3331	(310) 322-3332
IRC	(512) 992-7900	(512) 992-3377
Matsuo	(714) 969-2491	(714) 960-6492
Motorola	(602) 303-5454	(602) 994-6430
Murata-Erie	(814) 237-1431	(814) 238-0490
Nichicon	(847) 843-7500	(847) 843-2798
NIEC	(805) 867-2555*	[81] 3-3494-7414
Sanyo	(619) 661-6835	[81] 7-2070-1174
Siliconix	(408) 988-8000	(408) 970-3950
Sprague	(603) 224-1961	(603) 224-1430
Sumida	(847) 956-0666	[81] 3-3607-5144

**Distributor*

Table 3. MAX1624 Output Voltage Adjustment Settings (Abbreviated†)

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	COMPATIBILITY
1	0	0	0	0	3.5	Intel-compatible codes
1	0	0	0	1	3.4	
1	—	—	—	—	Decreases in 100mV increments	
1	1	1	1	0	2.1	
1	1	1	1	1	No CPU (OFF)	
0	0	0	0	0	1.9	Non-Intel compatible codes
0	0	0	0	1	1.8	
0	0	—	—	—	Decreases in 100mV increments	
0	0	1	1	1	1.2	
0	1	0	0	0	1.1	
0	1	—	—	—	1.1	
0	1	1	1	0	1.1	
0	1	1	1	1	No CPU (OFF)	

†*See Table 4 for a complete listing.*

Standard Application Circuits

The predesigned MAX1624/MAX1625 circuits shown in Figures 1 and 2 meet a wide range of applications with output currents up to 12A and higher. Use Table 1 to select components appropriate for the desired output current range, and adapt the evaluation kit PC board layout as necessary. Table 2 lists suggested vendors. These circuits represent a good set of trade-offs between cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current.

These MAX1624/MAX1625 circuits were designed for the specified frequencies. Do not change the switching frequency without first recalculating component values—particularly the inductance, output filter capacitance, and RC1 resistance values. Recalculate the voltage-feedback resistor and compensation-capacitor values (CC1 and CC2) as necessary to reconfigure them for different output voltages. Table 3 lists voltage adjustment DAC codes for the MAX1624.

Detailed Description

The MAX1624/MAX1625 are BiCMOS switch-mode, power-supply controllers designed for buck-topology regulators. They are optimized for powering the latest high-performance CPUs—demanding applications where output voltage precision, good transient response, and high efficiency are critical for proper operation. With appropriate external components, the MAX1624/MAX1625 deliver over 15A between 1.1V and 3.5V with ±1% accuracy. The MAX1625 offers 1% typical transient-load regulation from a +5V supply, while the MAX1624 offers a selectable transient-load regulation of 0.5%, 1%, or 2%. Remote output sensing ensures voltage precision by eliminating errors caused by PC board trace impedance. These controllers achieve 90% efficiency by using synchronous rectification.

A typical application circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter (Figure 1). At each of the internal oscillator's rising edges, the high-side MOSFET switch (N1) is turned on and allows current to ramp up through the inductor to the output filter capacitor and load, storing energy in a magnetic field. The current is monitored by reading the voltage

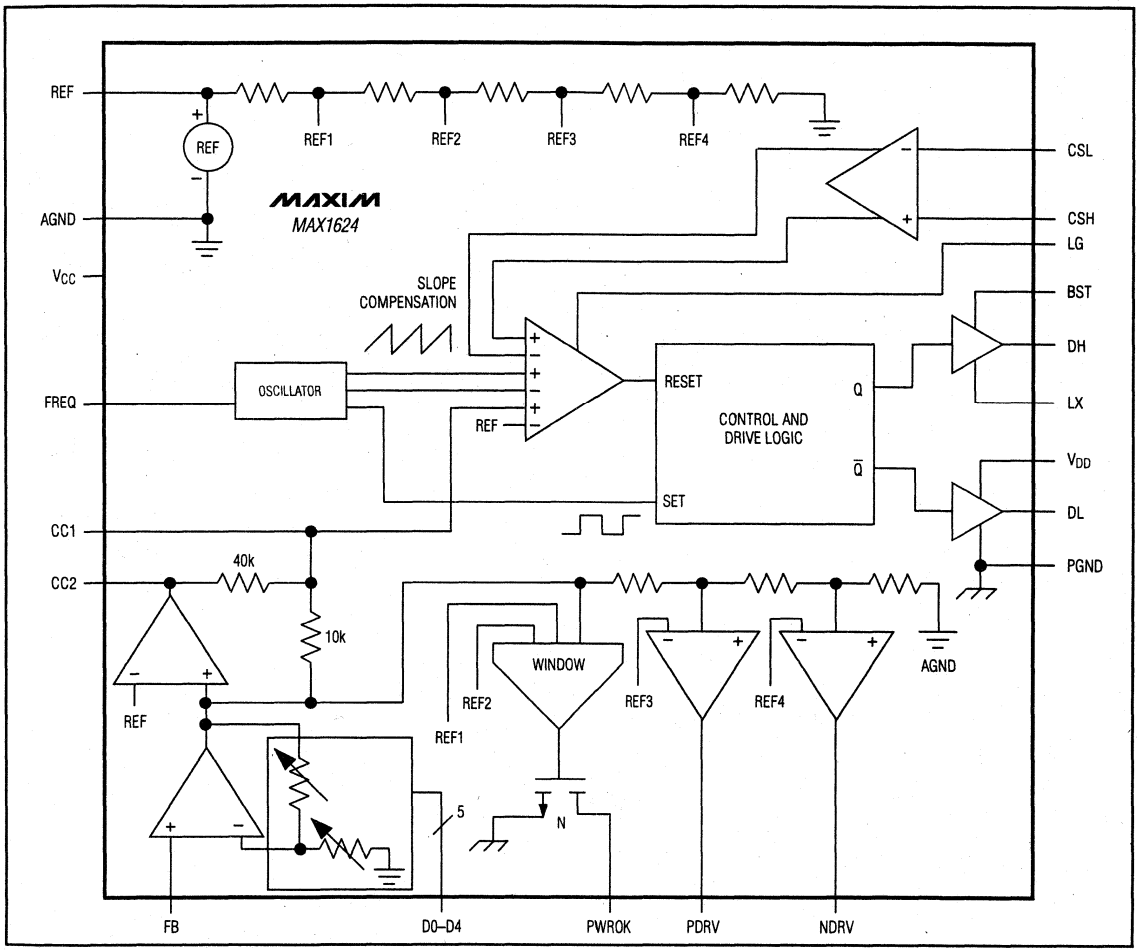


Figure 3. MAX1624 Simplified Block Diagram

across the current-sense resistor (R1). When the inductor current ramps up to the current-sense threshold, the MOSFET turns off and interrupts the flow of current from the supply. This causes the magnetic field in the inductor to collapse, resulting in a voltage surge that forces the rectifier diode (D1) or MOSFET body diode (N2) on and keeps the inductor current flowing in the same amplitude and direction. At this point, the synchronous rectifier MOSFET turns on until the end of the cycle to reduce conduction losses across the rectifier diode. The current through the inductor ramps back down, transferring the stored energy to the output filter capacitor and load. The output filter capacitor stores energy when inductor current is high and releases it when inductor current is low, smoothing the voltage delivered to the load.

The MAX1624/MAX1625 use a current-mode pulse-width-modulation (PWM) control scheme (Figures 3 and 4). The output voltage is regulated by switching at a constant frequency and then modulating the peak inductor current to change the energy transferred per pulse and to adjust to changes in the load. The output

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

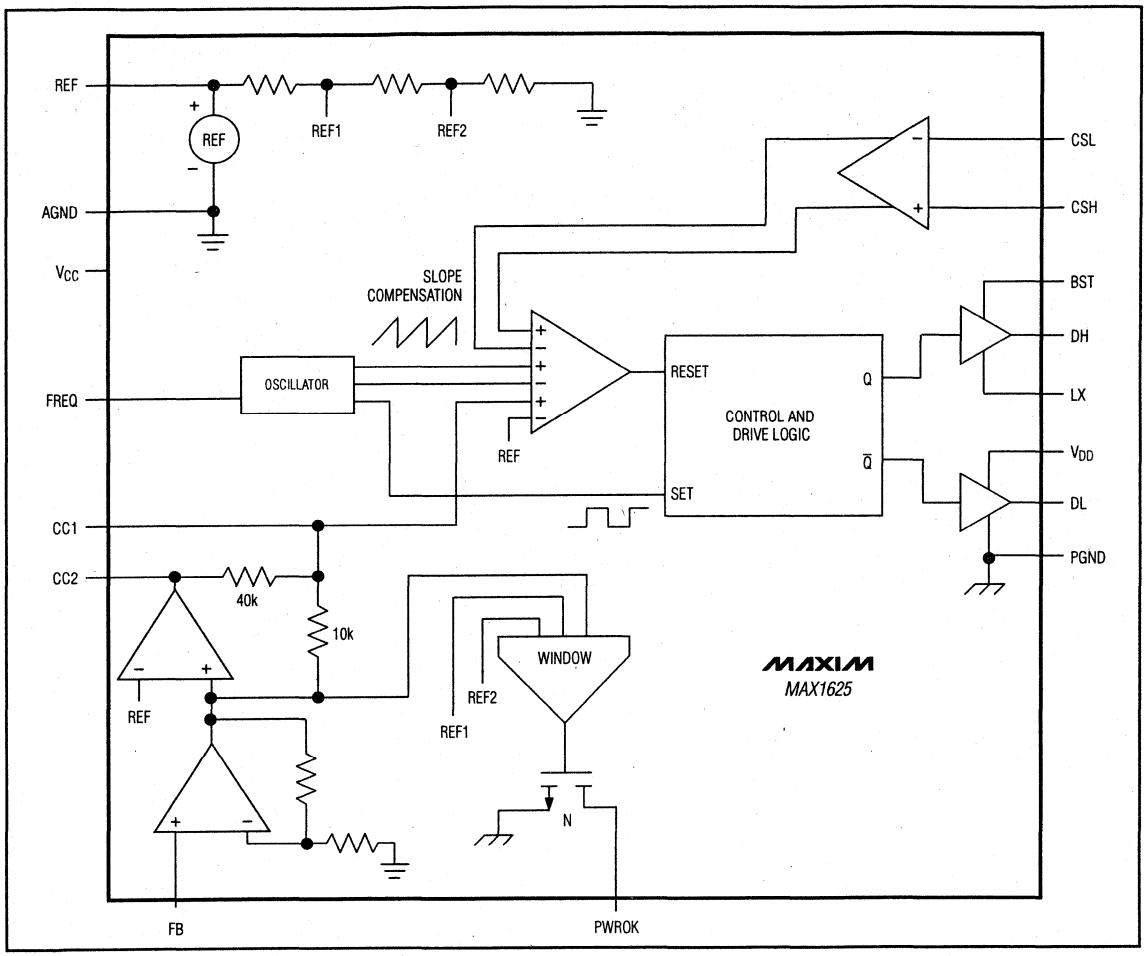


Figure 4. MAX1625 Simplified Block Diagram

voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. Slope compensation is necessary to stabilize current-mode feedback controllers with a duty cycle greater than 50%. Maximum duty cycle is greater than 85% (see *Typical Operating Characteristics*).

PWM Controller Block and Integrator

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: the buffered feedback signal, the current-sense signal, and the slope-compensation ramp. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage. The output voltage error signal is generated by an error amplifier that compares the amplified feedback voltage to an internal reference.

Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). The current-mode feedback system regulates the peak inductor current as a function of the output voltage

error signal. Since average inductor current is nearly the same as peak current (assuming the inductor value is set relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current staircasing, a slope-compensation ramp is summed into the main PWM comparator. As the high-side switch turns off, the synchronous rectifier latch is set. The low-side switch turns on 30ns later and stays on until the beginning of the next clock cycle. Under fault conditions where the inductor current exceeds the maximum current-limit threshold, the high-side latch resets, and the high-side switch turns off.

Internal Reference

The internal 3.5V reference (REF) is accurate to ±1% from 0°C to +85°C, making REF useful as a system reference. Bypass REF to AGND with a 0.1µF (min) ceramic capacitor. A larger value (such as 1µF) is recommended for high-current applications. Load regulation is 10mV for loads up to 100µA. Loading REF reduces the main output voltage slightly, according to the reference-voltage load-regulation error (see *Typical Operating Characteristics*). Reference undervoltage lockout is between 2.7V and 3V. Short-circuit current is less than 4mA.

Synchronous-Rectifier Driver

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode or MOSFET body diode with a low-on-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up by precharging the boost-charge pump used for the high-side switch gate-drive circuit. Thus, if you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

The DL drive waveform is simply the complement of the DH high-side drive waveform (with typical controlled dead time of 30ns to prevent cross-conduction or shoot-through). The DL output's on-resistance is 0.7Ω (typ) and 2Ω (max).

BST High-Side Gate-Driver Supply and MOSFET Drivers

Gate-drive voltage for the high-side N-channel switch is generated using a flying-capacitor boost circuit (Figure 5). The capacitor is alternately charged from the +5V supply and placed in parallel with the high-side MOSFET's gate and source terminals.

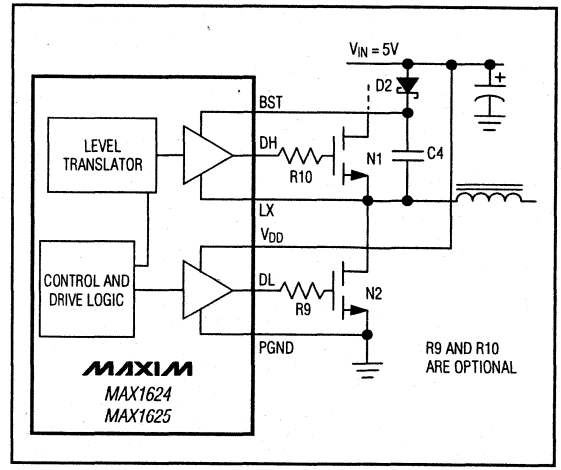


Figure 5. Boost Supply for Gate Drivers

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and precharges the BST capacitor (C4) to 5V through a diode (D2). This provides the necessary enhancement voltage to turn on the high-side switch. On the next half-cycle, the PWM control logic turns on the high-side MOSFET by closing an internal switch between BST and DH. As the MOSFET turns on, the LX node rises to the input voltage, an action that boosts the 5V gate-drive signal above the +5V supply. DH on-resistance is 0.7Ω (typical) and 2Ω (max). Do not bias D2 with voltages greater than 5.5V, as this will destroy the DH gate driver.

A 0.1µF minimum ceramic capacitor is recommended for the boost supply. Use a low-power, SOT23 Schottky diode to minimize reduction of the gate drive from the diode's forward voltage. Use a low-leakage Schottky diode, such as a CMPSH-3 from Central Semiconductor or a 1N4148, to prevent reverse leakage from discharging the BST capacitor when the ambient temperature is high. Place the BST capacitor and diode within 0.4 in. (10mm) of the BST pin.

Gate-drive resistors (R9 and R10) can often be useful to reduce jitter in the switching waveforms by slowing down the fast-slewing LX node and reducing ground bounce at the controller IC. Low-valued resistors from around 1Ω to 5Ω are sufficient for many applications.

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

GlitchCatcher Current-Boost Driver (MAX1624)

Drivers for an optional current-boost circuit are included in the MAX1624 to improve transient response. Some dynamically clocked CPUs switch computational blocks on and off as needed to reduce power consumption, and can generate load steps of several amperes in a few tens of nanoseconds. The current-boost circuit is intended to improve transient response to such load steps by bypassing the inductor's lowpass filter operation. When the output drops out of regulation by more than ±1.5% to ±2.5%, the P-channel or N-channel switches turn on and force the output back into regulation. The MOSFET drivers' response time is typically 75ns, and their minimum on-time is typically 100ns.

Current Sense and Overload Current Limiting

The current-sense circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL from current through the sense resistor (R1) exceeds the peak current limit (100mV typical).

Current-mode control offers a practical level of overload protection in response to many fault conditions. During normal operation, maximum output current is enforced by the peak current limit. If the output is shorted directly to GND through a low-resistance path, the current-sense comparator may be unable to enforce a current limit. Under such conditions, circuit parasitics such as MOSFET $R_{DS(ON)}$ typically limit the short-circuit current to a value around the peak-current-limit setting.

Attach a lowpass-filter network between the current-sense pins and resistor to reduce high-frequency common-mode noise (Figure 6). The filter should be designed with a time constant of around 200ns. Resistors in the 20Ω to 100Ω range are recommended for R7 and R8. Connect the filter capacitors C11 and C12 from V_{CC} to CSH and CSL, respectively.

Values of 39Ω and 4.7nF are suitable for many designs. Place the current-sense filter network close to the IC, within 0.1 in. (2.5mm) of the CSH and CSL pins.

Internal Soft-Start

Soft-start allows a gradual increase of the internal current limit at start-up to reduce input surge currents. In the MAX1624/MAX1625, an internal DAC raises the current-limit threshold from 0V to 100mV in four steps (25mV, 50mV, 75mV, and 100mV) over the span of 1536 oscillator cycles.

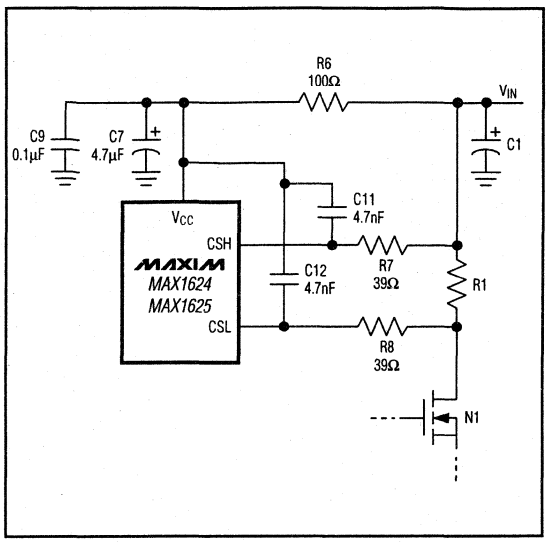


Figure 6. Current-Sense Filter

Design Procedure

Setting the Output Voltage

MAX1624

Select the output voltage using the D0–D4 pins. The MAX1624 uses an internal 5-bit DAC as a feedback-resistor voltage divider. The output voltage can be digitally set in 100mV increments from 1.1V to 3.5V using the D0–D4 inputs (Table 4).

D0–D4 are logic inputs and accept both TTL and CMOS voltage levels. The MAX1624 has both FB and AGND inputs, allowing a Kelvin connection for remote voltage and ground sensing to eliminate the effects of trace resistance on the feedback voltage. (See *PC Board Layout Considerations* for further details.) FB input current is 0.1µA (max).

The MAX1624 DAC codes were designed for compatibility with Intel specifications for output voltages between 3.5V and 2.1V. Codes 10000 through 11110 are compatible with Intel specifications, while codes 00000 through 01111 are not. Codes 11111 and 01111 turn off the buck controller, placing the IC in a low-current mode (0.2mA typical). For compatibility with Intel codes for output voltages below 2.1V, see the MAX1638/MAX1639 data sheet.

Table 4. Output Voltage-Adjustment Settings

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	COMPATIBILITY
1	0	0	0	0	3.5	Intel-compatible DAC codes
1	0	0	0	1	3.4	
1	0	0	1	0	3.3	
1	0	0	1	1	3.2	
1	0	1	0	0	3.1	
1	0	1	0	1	3.0	
1	0	1	1	0	2.9	
1	0	1	1	1	2.8	
1	1	0	0	0	2.7	
1	1	0	0	1	2.6	
1	1	0	1	0	2.5	
1	1	0	1	1	2.4	
1	1	1	0	0	2.3	
1	1	1	0	1	2.2	
1	1	1	1	0	2.1	
1	1	1	1	1	No CPU (off)	
0	0	0	0	0	1.9	Non-Intel-compatible DAC codes
0	0	0	0	1	1.8	
0	0	0	1	0	1.7	
0	0	0	1	1	1.6	
0	0	1	0	0	1.5	
0	0	1	0	1	1.4	
0	0	1	1	0	1.3	
0	0	1	1	1	1.2	
0	1	0	0	0	1.1	
0	1	0	0	1	1.1	
0	1	—	—	—	1.1	
0	1	1	1	0	1.1	
0	1	1	1	1	No CPU (off)	

MAX1625

Set the output voltage by connecting R2 and R3 (Figure 7) to the FB pin from the output to AGND. R2 is given by the following equation:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 1.1V. Since the input bias current at FB has a maximum value of ±0.1µA, values up to 100kΩ can be used for R3 with no significant accuracy loss. Values under 1kΩ are recommended to improve noise immunity and minimize parasitic capacitance at the FB node. Place R2 and R3 very close to the MAX1625, within 0.2 in. (5mm) of the FB pin.

Selecting the Oscillator Frequency

Set the switching frequency between 100kHz and 1MHz by connecting a resistor from FREQ to AGND. Select the resistor according to the following equation:

$$R4 = \frac{2 \times 10^{10}}{f_{OSC}}$$

Low-frequency operation reduces controller IC quiescent current and improves efficiency. High-frequency operation reduces cost and PC board area by allowing the use of smaller inductors and fewer and smaller output capacitors. Inductor energy-storage requirements and output capacitor requirements at 1MHz are one-third those at 300kHz.

Choosing the Error-Amplifier Gain (MAX1624)

Set the error-amplifier gain to match the voltage-precision requirements of the CPU used. The MAX1624's loop-gain control input (LG) allows trade-offs in DC/AC voltage accuracy versus output filter capacitor requirements. AC load regulation can be set to 0.5%, 1%, or 2% by connecting LG as shown in Table 5. The MAX1625's default AC regulation is 1%.

DC load regulation is typically 10 times better than AC load regulation, and is determined by the gain set by the LG pin.

Table 5. LG Pin Adjustment Settings

LG CONNECTED TO	AC LOAD-REGULATION ERROR (%)	DC LOAD-REGULATION ERROR (%)	TYPICAL A_E (V_{GAIN}/ I_{GAIN})
V_{CC}	2	0.2	2
REF	1	0.1	4
GND	0.5	0.05	8

Specifying the Inductor

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows for smaller inductors and better transient response, but results in higher losses and output ripple.

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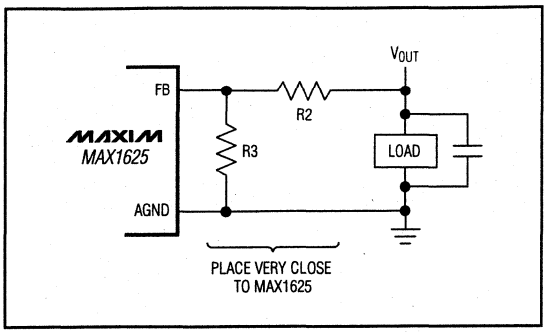

Figure 7. MAX1625 Adjustable Output Operation

A good compromise between size and loss is a 45% ripple current to load current ratio (LIR = 0.45), which corresponds to a peak inductor current 1.23 times higher than the DC load current.

$$L = \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times f_{OSC} \times I_{OUT} \times LIR}$$

where f is the switching frequency, between 100kHz and 1MHz; I_{OUT} is the maximum DC load current; and LIR is the ratio of AC to DC inductor current (typically 0.45). The exact inductor value is not critical and can be adjusted to make trade-offs among size, transient response, cost, and efficiency. Although lower inductor values minimize size and cost, they also reduce efficiency due to higher peak currents. In general, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Load-transient response can be adversely affected by high inductor values, especially at low (V_{IN} - V_{OUT}) differentials.

The peak inductor current at full load is 1.23 x I_{OUT} if the previous equation is used; otherwise, the peak current can be calculated using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{2f_{OSC} \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficient performance, and should be less than the current-sense resistor value.

Calculating the Current-Sense Resistor Value

Calculate the current-sense resistor value according to the worst-case minimum current-limit threshold voltage (from the *Electrical Characteristics*) and the peak inductor current required to service the maximum load. Use I_{PEAK} from the equation in the section *Specifying the Inductor.*

$$R_{SENSE} = \frac{85mV}{I_{PEAK}}$$

The high inductance of standard wire-wound resistors can degrade performance. Low-inductance resistors, such as surface-mount power metal-strip resistors, are preferred. The current-sense resistor's power rating should be higher than the following:

$$R_{POWER\ RATING} = \frac{(115mV)^2}{R_{SENSE}}$$

In high-current applications, connect several resistors in parallel as necessary, to obtain the desired resistance and power rating.

Selecting the Output Filter Capacitor

Output filter capacitor values are generally determined by effective series resistance (ESR) and voltage-rating requirements, rather than by the actual capacitance value required for loop stability. Due to the high switching currents and demanding regulation requirements in a typical MAX1624/MAX1625 application, use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. Do not use standard aluminum-electrolytic capacitors, which can cause high output ripple and instability due to high ESR. The output voltage ripple is usually dominated by the filter capacitor's ESR, and can be approximated as $I_{RIPPLE} \times R_{ESR}$. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}\left(1 + \frac{V_{OUT}}{V_{IN(MIN)}}\right)}{V_{OUT} \times R_{SENSE} \times f_{OSC}}$$

$$R_{ESR} < R_{SENSE}$$

Compensating the Feedback Loop

The feedback loop needs proper compensation to prevent excessive output ripple and poor efficiency caused by instability. Compensation cancels unwanted poles and zeros in the DC-DC converter's transfer function that are due to the power-switching and filter elements with corresponding zeros and poles in the feedback network. These compensation zeros and poles are set by the compensation components CC1, CC2, and RC1. The objective of compensation is to ensure stability by ensuring that the DC-DC converter's phase shift is less than 180° by a safe margin, at the frequency where the loop gain falls below unity.

One simple method for ensuring adequate phase margin is to place pole-zero pairs to approximate a single-pole response with a -20dB/decade slope all the way to unity-gain crossover (Figure 8). (Other compensation schemes are possible.) The order of undesired poles and zeros may differ from that shown in Figure 8, depending on the characteristics of the load, output filter capacitor, switching frequency, and inductor. These procedures are guidelines only, and empirical experimentation is needed to select the compensation components' final values.

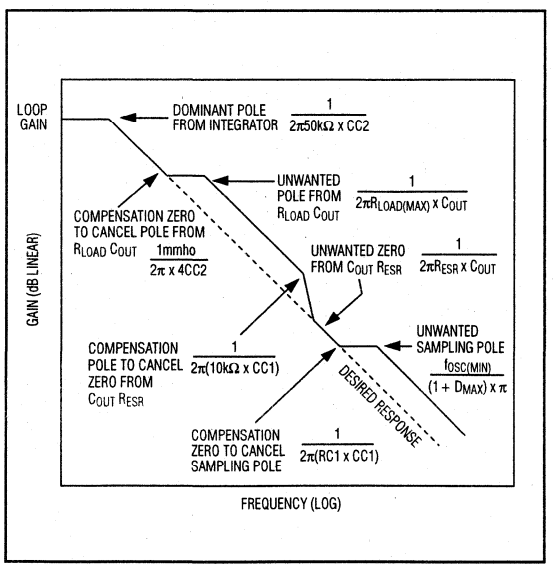

Figure 8. MAX1624/MAX1625 Bode Plot with Compensation Poles and Zeros

Canceling the Sampling Pole and Output Filter ESR Zero

Compensate the fast-voltage feedback loop by connecting a resistor and a capacitor in series from the CC1 pin to AGND. The pole from CC1 can be set to cancel the zero from the filter-capacitor ESR. Thus the capacitor at CC1 should be as follows:

$$CC1 = \frac{C_{OUT} \times R_{ESR}}{10k\Omega}$$

Resistor RC1 sets a zero that can be used to compensate for the sampling pole generated by the switching frequency. Set RC1 to the following:

$$RC1 = \frac{\left(1 + \frac{V_{OUT}}{V_{IN}}\right)}{2f_{OSC} \times CC1}$$

The CC1 pin's output resistance is 10kΩ. In the sampling pole equation (Figure 8), D_{MAX} is the maximum duty cycle, or $V_{OUT} / V_{IN(MIN)}$.

Setting the Dominant Pole and Canceling the Load and Output Filter Pole

Compensate the slow-voltage feedback loop by adding a ceramic capacitor from the CC2 pin to AGND. This is an integrator loop used to cancel out the DC load-regulation error. Selection of capacitor CC2 sets the dominant pole and a compensation zero. The zero is typically used to cancel the unwanted pole generated by the load and output filter capacitor at the maximum load current. Select CC2 to place the zero close to or slightly lower than the frequency of the unwanted pole, as follows:

$$CC2 = \frac{1mmho \times C_{OUT}}{4} \times \frac{V_{OUT}}{I_{OUT(MAX)}}$$

The transconductance of the integrator amplifier at CC2 is 1mmho. The voltage swing at CC2 is internally clamped around 2.4V to 3V minimum and 4V to V_{CC} maximum to improve transient response times. CC2 can source and sink up to 100µA.

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Calculating the Loop Gain (Optional)

The loop gain is an important parameter in alternative compensation schemes:

$$\text{Loop Gain (dB)} = 20\text{Log}\left(A_E \frac{V_{REF}}{V_{OUT}} \times \frac{R_{LOAD}}{R_{CS}} \times A_I\right)$$

$$= 20\text{Log}\left(A_E \frac{V_{REF}}{85mV} \times 10\right)$$

where A_E is the error-comparator relative gain, and A_I = 10 is the integrator gain. A_E is 4 for the MAX1625, but it is 2, 4, or 8 for LG pin settings of V_{CC}, REF, or AGND, respectively, for the MAX1624.

Feed-Forward Compensation (MAX1625)

An optional compensation capacitor, typically 220pF, may be needed across the upper feedback resistor to counter the effects of stray capacitance on the FB pin, and to help ensure stable operation when high-value feedback resistors are used (Figure 9). Empirically adjust the feed-forward capacitor as needed.

Choosing the MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate-threshold specs are better (i.e., 2V max rather than 3V max). Gate charge should be less than 100nC to minimize switching losses and reduce power dissipation.

I^2R losses are the greatest heat contributor to MOSFET power dissipation and are distributed between the high- and low-side MOSFETs according to duty factor, as follows:

$$P_D \text{ (high side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}}$$

$$P_D \text{ (low side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$P_D \text{ (low side, shorted)} = I_{LIMIT}^2 \times R_{DS(ON)}$$

where $I_{LIMIT} = 115mV / R_{SENSE}$.

Switching losses affect the upper MOSFET only, and are insignificant at 5V input voltages. Gate-charge losses are dissipated in the IC, and do not heat the MOSFETs. Ensure that both MOSFETs are at a safe junction temperature by calculating the temperature rise according to package thermal-resistance specifications. The high-side MOSFET's worst-case dissipation occurs at the maximum output voltage and minimum input voltage. For the low-side MOSFET, the worst case is at the maximum input voltage when the output is short-circuited (consider the duty factor to be 100%).

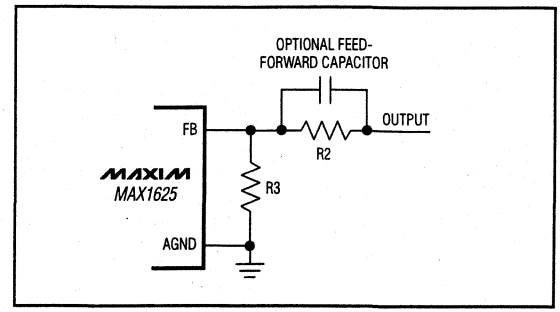

Figure 9. MAX1625 Optional Feed-Forward Compensation Capacitors

Selecting the Rectifier Diode

The rectifier diode D1 is a clamp that catches the negative inductor swing during the 30ns typical dead time between turning off the high-side MOSFET and turning on the low-side MOSFET synchronous rectifier. D1 must be a Schottky diode, to prevent the MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop 1% or 2% as a result. Use a 1N5819 diode for loads up to 3A, or a 1N5822 for loads up to 10A.

Adding the BST Supply Diode and Capacitor

A signal diode, such as a 1N4148, works well for D2 in most applications, although a low-leakage Schottky diode provides slightly improved efficiency. Do not use large power diodes, such as the 1N4001 or 1N5817. Exercise caution in the selection of Schottky diodes, since some types exhibit high reverse leakage at high operating temperatures. Bypass BST to LX using a 0.1µF capacitor.

Selecting the Input Capacitors

Place a 0.1µF ceramic capacitor and 4.7µF capacitor between V_{CC} and AGND, as well as between V_{DD} and PGND, within 0.2 in. (5mm) of the V_{CC} and V_{DD} pins.

Select low-ESR input filter capacitors with a ripple-current rating exceeding the RMS input ripple current, connecting several capacitors in parallel if necessary. RMS input ripple current is determined by the input voltage and load current, with the worst-possible case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = I_{OUT}/2 \text{ when } V_{IN} = 2V_{OUT}$$

Bypassing the Internal Reference

Bypass the internal 3.5V reference at the REF pin by connecting a 0.1µF capacitor to AGND. Use a larger value, such as 1µF, for high-current applications.

Choosing the GlitchCatcher MOSFETs

P-channel and N-channel switches and a series resistor are required for the current-boost circuit (Figure 10). Current through the MOSFETs and current-limiting resistors must be sufficient to supply the load current, with enough extra for prompt output regulation without excessive overshoot. Design for boost-current values 1.5 times the maximum load current, and choose MOSFETs and current-limiting resistors such that:

$$R_{DSON,P(MAX)} + R_{LIMIT} \approx \frac{V_{IN} - V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

and

$$R_{DSON,N(MAX)} + R_{LIMIT} \approx \frac{V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

Applications Information

Efficiency Considerations

Refer to the MAX796–MAX799 data sheet for information on calculating losses and improving efficiency.

PC Board Layout Considerations

Good PC board layout and routing are *required* in high-current, high-frequency switching power supplies to achieve good regulation, high efficiency, and stability. The PC board layout artist must be provided with explicit instructions concerning the placement of power-switching components and high-current routing. It is strongly recommended that the evaluation kit PC board layouts be followed as closely as possible. Contact Maxim's Applications Department concerning the availability of PC board examples for higher-current circuits.

In most applications, the circuit is on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current power and ground connections. Leave the extra copper on the board as a pseudo-ground plane. Use the bottom layer for quiet connections (REF, FB, AGND), and the inner layers for an uninterrupted ground plane. A ground plane and pseudo-ground plane are essential for reducing ground bounce and switching noise.

Follow these steps:

1) **Place the high-power components (C1, R1, N1, D1, N2, L1, and C2 in Figure 1) as close together as possible, following these priorities:**

   - **Minimize ground-trace lengths** in high-current paths. The surface-mount power components should be butted up to one another with their ground terminals almost touching. Connect their ground terminals using a wide, filled zone of top-layer copper (the pseudo-ground plane), rather than through the internal ground plane. At the output terminal, use vias to connect the top-layer pseudo-ground plane to the normal inner-layer ground plane at the output filter capacitor ground terminals. This minimizes interference from IR drops and ground noise, and ensures that the IC's AGND is sensing at the supply's output terminals.

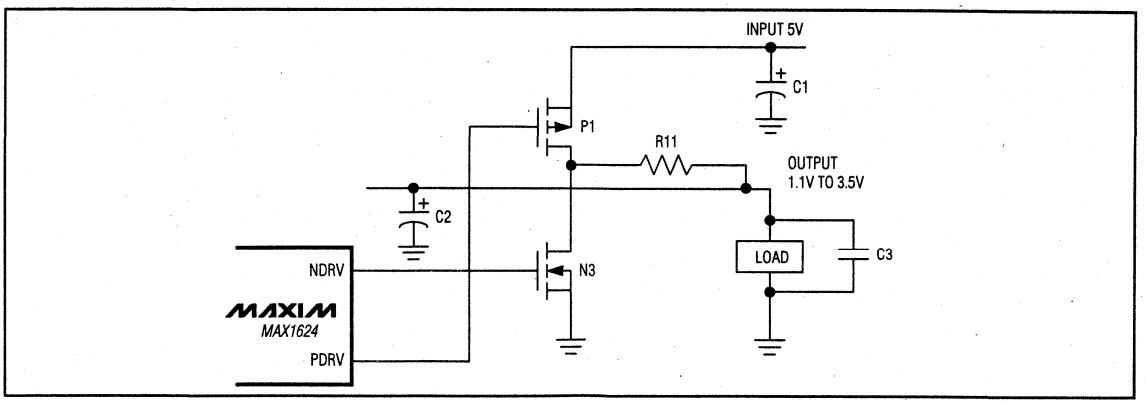

Figure 10. GlitchCatcher Circuit

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- **Minimize high-current path trace lengths.** Use very short and wide traces. From C1 to N1: 0.4 in. (10mm) max length; D1 cathode to N2: 0.2 in. (5mm) max length; LX node (N1 source, N2 drain, D1 cathode, inductor L1): 0.6 in. (15mm) max length.

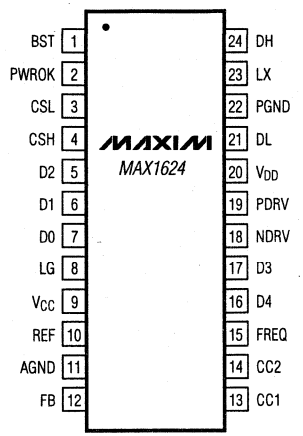
2) **Place the MAX1624/MAX1625 and supporting components following these rules:**

- **Minimize trace lengths to the current-sense resistor.** The IC must be no farther than 0.4 in. (10mm) from the current-sense resistor. Use a Kelvin connection.
- **Minimize ground trace lengths between the MAX1624/MAX1625 and supporting components.** Connect components for the REF, CC1, CC2, and FREQ pin directly to AGND. Connect AGND and PGND at the IC.
- **Keep noisy nodes and components away from sensitive analog nodes,** such as the current-sense, voltage-feedback, REF, CC1, CC2, and FREQ pins. Placing the IC and analog components on the opposite side of the board from the power-switching node is desirable. Noisy nodes include the main switching node (LX), inductor, and gate-drive outputs.
- **Place components for the FREQ, REF, CC1, and CC2 pins as close to the IC as possible,** within 0.2 in. (5mm).
- Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm, and route them away from CSH, CSL, REF, FB, etc.
- Filter the V_{CC} supply input to the IC. Bypass the IC directly from V_{DD} to PGND using a 0.1µF ceramic capacitor and 4.7µF electrolytic capacitor placed within 0.2 in. (5mm) of the IC.
- Place the voltage-feedback components close to the FB pin of the MAX1625, within 0.2 in. (5mm). Connect the voltage-feedback trace directly to the CPU's power input and route it to avoid noisy traces.

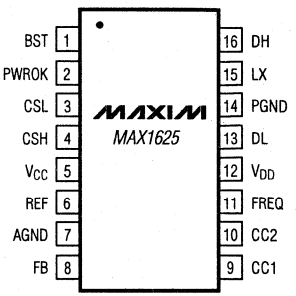
High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Pin Configurations

TOP VIEW



SSOP



SO

Chip Information

TRANSISTOR COUNT: 2472

SUBSTRATE CONNECTED TO AGND

19-1268; Rev 0; 8/97

EVALUATION KIT AVAILABLE

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

General Description

The MAX1636 is a synchronous, buck, switch-mode, power-supply controller that generates the CPU supply voltage in battery-powered systems. It achieves ±1% output voltage accuracy and offers the excellent load-transient response needed by upcoming generations of dynamic-clock CPUs.

Up to 95% efficiency is achieved through synchronous rectification and Maxim's proprietary Idle Mode™ control scheme. Efficiency is greater than 80% over a 1000:1 load-current range, extending battery life in system-suspend or standby modes. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Strong, 1A, on-board gate drivers ensure fast, external N-channel MOSFET switching.

The MAX1636 features a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode that reduces noise and RF interference in sensitive mobile communications and pen-entry applications. Holding $\overline{SKIP}$ high forces fixed-frequency mode for lowest noise under all load conditions.

For a low-cost version that omits the +5V VL linear-regulator block and comes in a smaller 16-pin QSOP package, refer to the MAX1637 data sheet.

Applications

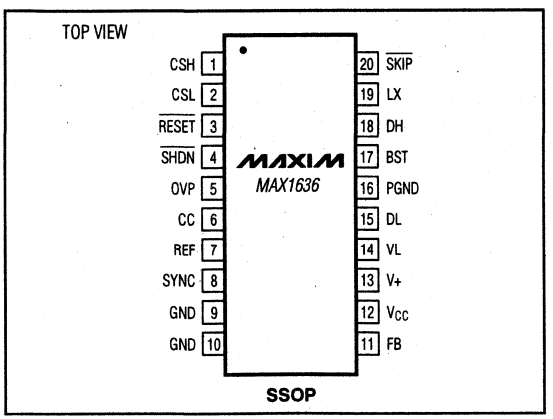
Notebook Computers

Subnotebook Computers

Desktop Computers

Bus-Termination Supplies

Pin Configuration



Idle Mode is a trademark of Maxim Integrated Products.

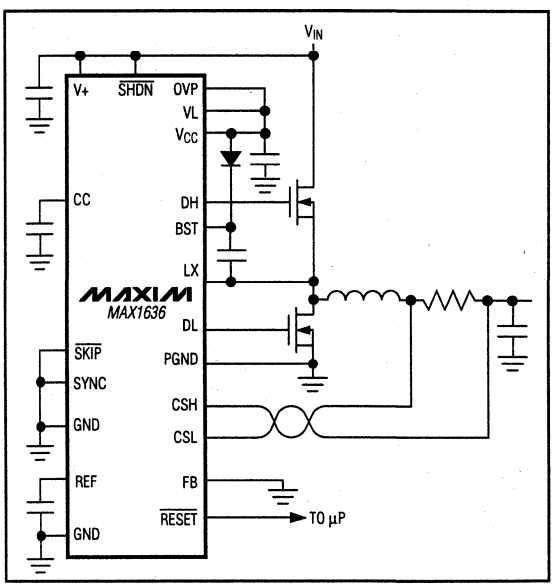
Features

- ♦ ±1% DC Accuracy (Adjustable Mode)
- ♦ Output Overvoltage Crowbar Protection
- ♦ Output Undervoltage Shutdown
- ♦ Adjustable Switching Frequency to 340kHz
- ♦ Low-Dropout Operation
- ♦ Idle Mode Pulse-Skipping Operation
- ♦ 1.10V to 5.5V Adjustable Output Voltage
- ♦ 2.5V/3.3V Dual-Mode Fixed-Output Settings
- ♦ Internal Digital Soft-Start
- ♦ 1.1V ±1% Reference Output
- ♦ 3µA (typ) Shutdown Current
- ♦ Open-Drain Power-Good Output ($\overline{RESET}$)
- ♦ 20-Pin SSOP Package

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1636EAP	-40°C to +85°C	20 SSOP

Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

ABSOLUTE MAXIMUM RATINGS

V+ to GND .....-0.3V to 36V
GND to PGND.....±2V
$\overline{SHDN}$ to GND..... -0.3V to 36V
LX, BST to GND..... -0.3V to 36V
DH, BST to LX.....-0.3V to 6V
VL, V_{CC}, CSL, CSH, FB, $\overline{SKIP}$ to GND ..... -0.3V to 6V
DL to GND.. .....-0.3V to (VL + 0.3V)
REF, $\overline{RESET}$, SYNC, CC, OVP to GND..... -0.3V to (V_{CC} + 0.3V)
VL Output Current.....50mA
VL Short Circuit to GND.....Momentary

REF Output Current 20mA
REF Short Circuit to GND ....Indefinite
Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Range
MAX1636EAP. .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
Input Voltage Range, V+	Input source for VL regulator	4.5		30	V
Input Voltage Range, VL	Gate-driver supply rail	4.2		5.5	V
Input Voltage Range, V_{CC}	Internal chip supply rail	3.15		5.5	V
Output Voltage, Adj Mode	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	1.090	1.100	1.110	V
Output Voltage, Fixed 2.5V Mode	FB tied to V_{CC}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	2.486	2.55	2.614	V
Output Voltage, Fixed 3.3V Mode	FB tied to GND, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	3.282	3.366	3.450	V
Output Adjustment Range	V_{CC} = VL = 5V	V_{REF}		5.5	V
	V_{CC} = 3.3V, VL = 5V	V_{REF}		3.6	
Current-Limit Threshold	Positive direction	80	100	120	mV
	Negative direction	-145	-100	-55	
Power Consumption	V_{CC} = 5V, output not switching			2.0	mW
	V_{CC} = 3.3V, output not switching			1.5	
Shutdown Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = GND		3	10	µA
FB Input Current	FB forced to REF	-50		50	nA
Soft-Start Ramp Time	$\overline{SHDN}$ to full current limit, five levels		512		clks
Idle Mode Switchover Threshold	CSH - CSL	20	30	40	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL VL REGULATOR AND REFERENCE					
Regulator Supply Current (V+)	V_{CC} = 5V, I(VL) = 0			60	µA
	V_{CC} = 5V, I(VL) = 0, V+ = 4.5V (includes PNP base current)			500	
Standby Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = V_{CC}			60	µA
VL Output Voltage	I(VL) = 0 to 25mA, 5V < V+ < 30V	4.5	5.0	5.3	V
	I(VL) = 0 to 25mA, 6V < V+ < 30V	4.7	5.0	5.3	
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 25mV	3.45	3.60	3.75	V
VL/ V_{CC} Switchover Threshold	Rising edge, hysteresis = 25mV		3.15		V
REF Output Voltage	No REF load	1.090	1.100	1.110	V
REF Load Regulation	REF load = 0 to 50µA			10	mV
REF Line Regulation	V_{CC} = 3.3V to 5.5V			3	mV
OSCILLATOR					
Oscillator Frequency	SYNC = V_{CC}	270	300	330	kHz
	SYNC = GND	170	200	230	
Maximum Duty Factor	SYNC = V_{CC}	91	94		%
	SYNC = GND	93	96		
Maximum Duty Factor, Dropout Mode	SYNC = GND	98	99		%
SYNC Input Pulse Width High		200			ns
SYNC Input Pulse Width Low		200			ns
SYNC Input Rise/Fall Time	Guaranteed by design			200	ns
SYNC Input Frequency Range		240		340	kHz
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	4	7	10	%
Overvoltage Fault Propagation Delay	FB to DL delay, 22mV overdrive, C_{GATE} = 2000pF		1.25		µs
Thermal Shutdown Threshold	Hysteresis = 10°C		150		°C
Catastrophic Output Undervoltage Lockout Threshold	% of nominal output	60	70	80	%
Catastrophic Output Undervoltage Lockout Delay	From shutdown or power-on-reset state		6144		clks
$\overline{RESET}$ Trip Threshold	Falling edge (hysteresis = 1%)	-6		-3	%
$\overline{RESET}$ Delay Time			32768		clks
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC	2.4			V
Logic Input Voltage Low	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC			0.8	V
Logic Input Bias Current	Pin at GND or V_{CC}; $\overline{SKIP}$, OVP, SYNC	-1		1	µA
$\overline{SHDN}$ Input Bias Current	$\overline{SHDN}$ = GND or V+	-3		3	µA
$\overline{RESET}$ Output Voltage Low	I_{SINK} = 4mA			0.4	V
$\overline{RESET}$ Output Leakage Current	+5.5V stress voltage applied			1	µA

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Current-Sense Input Leakage Current	CSH = CSL = 5V, V+ = VL = V_{CC} = GND, either CSH or CSL input			10	µA
Gate-Driver Sink/Source Current	DH or DL forced to 2V		1		A
Gate-Driver On-Resistance	High or low, DH or DL			7	Ω

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A =-40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS CONTROLLER					
Input Voltage Range, V+	Input source for VL regulator	4.5		30	V
Input Voltage Range, VL	Gate-driver supply rail	4.2		5.5	V
Input Voltage Range, V_{CC}	Internal chip supply rail	3.15		5.5	V
Output Voltage, Adj Mode	FB tied to V_{OUT}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	1.086		1.114	V
Output Voltage, Fixed 2.5V Mode	FB tied to V_{CC}, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	2.432		2.635	V
Output Voltage, Fixed 3.3V Mode	FB tied to GND, 0mV < (CSH - CSL) < 80mV, 4.5V < V+ < 30V (includes line and load regulation)	3.195		3.497	V
Output Adjustment Range	V_{CC} = VL = 5V	V_{REF}		5.5	V
	V_{CC} = 3.3V, VL = 5V	V_{REF}		3.6	
Current-Limit Threshold	Positive direction	70		130	mV
Power Consumption	V_{CC} = 5V, output not switching			2.0	mW
	V_{CC} = 3.3V, output not switching			1.5	
INTERNAL VL REGULATOR AND REFERENCE					
Regulator Supply Current (V+)	V_{CC} = 5V, I(VL) = 0			60	µA
	V_{CC} = 5V, I(VL) = 0, V+ = 4.5V (includes PNP base current)			500	
Standby Supply Current (V+)	$\overline{SHDN}$ = GND, OVP = V_{CC}			60	µA
VL Output Voltage	I(VL) = 0 to 25mA, 5V < V+ < 30V	4.5		5.3	V
	I(VL) = 0 to 25mA, 6V < V+ < 30V	4.7		5.3	
VL Undervoltage Lockout Threshold	Rising edge, hysteresis = 25mV	3.45		3.91	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V+ = 15V, SYNC = VL = V_{CC}, I_{VL} = 0mA, I_{REF} = 0mA, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR					
Oscillator Frequency	SYNC = V_{CC}	270		330	kHz
	SYNC = GND	170		230	
SYNC Input Pulse Width High		200			ns
SYNC Input Pulse Width Low		200			ns
SYNC Input Rise/Fall Time	Guaranteed by design			200	ns
SYNC Input Frequency Range		240		340	kHz
OVERVOLTAGE PROTECTION					
Overvoltage Trip Threshold	FB, with respect to regulation point	3.5		10	%
Catastrophic Output Undervoltage Lockout Threshold	% of nominal output	60		80	%
$\overline{RESET}$ Trip Threshold	Falling edge (hysteresis = 1%)	-7		-1.5	%
INPUTS AND OUTPUTS					
Logic Input Voltage High	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC	2.4			V
Logic Input Voltage Low	$\overline{SHDN}$, $\overline{SKIP}$, OVP, SYNC			0.8	V
$\overline{RESET}$ Output Voltage Low	I_{SINK} = 4mA			0.4	V
Gate-Driver On-Resistance	High or low, DH or DL			7	Ω

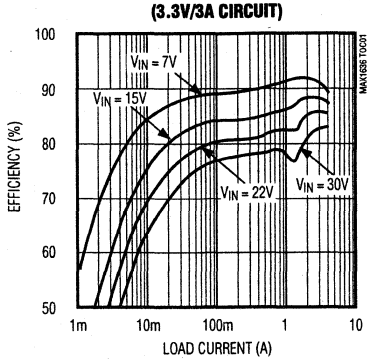
Note 1: Specifications to -40°C are guaranteed by design and not production tested.

4

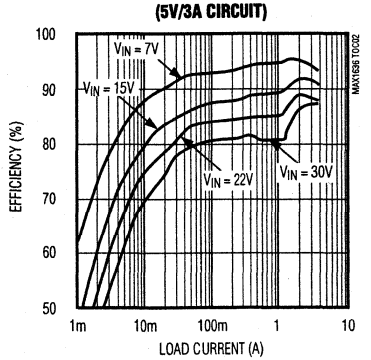
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

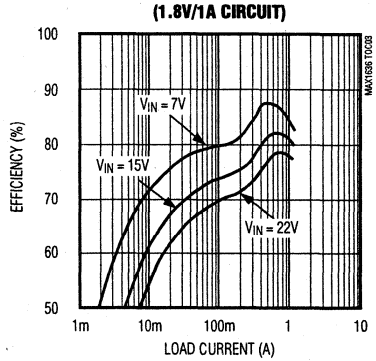
EFFICIENCY vs. LOAD CURRENT (3.3V/3A CIRCUIT)



EFFICIENCY vs. LOAD CURRENT (5V/3A CIRCUIT)



EFFICIENCY vs. LOAD CURRENT (1.8V/1A CIRCUIT)

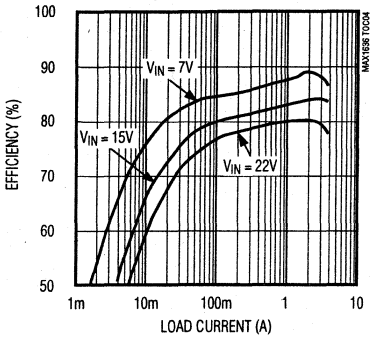


Low-Voltage, Precision Step-Down Controller for Portable CPU Power

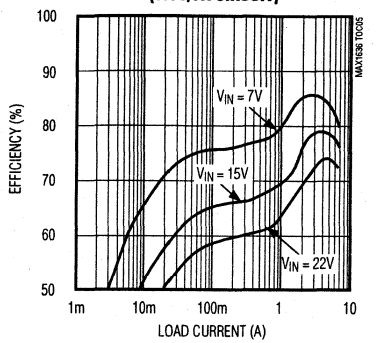
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

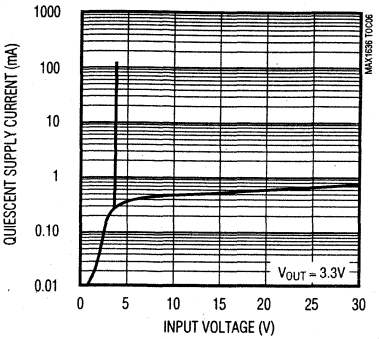
EFFICIENCY vs. LOAD CURRENT (1.8V/4A CIRCUIT)



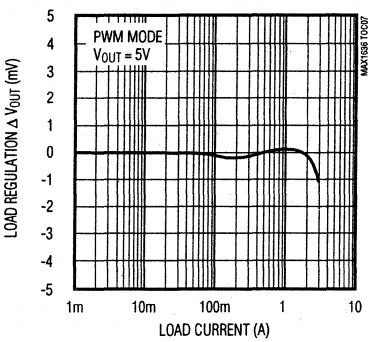
EFFICIENCY vs. LOAD CURRENT (1.8V/7A CIRCUIT)



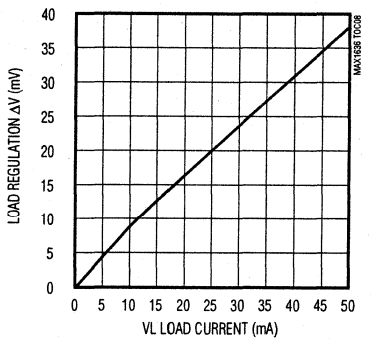
QUIESCENT SUPPLY CURRENT vs. INPUT VOLTAGE



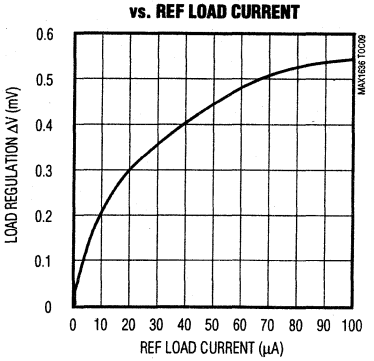
LOAD REGULATION vs. LOAD CURRENT



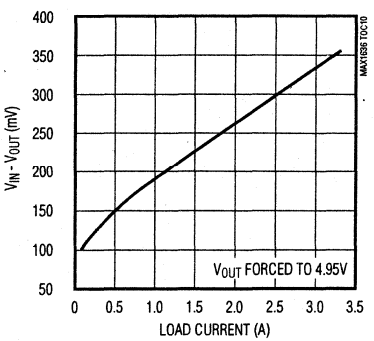
VL LOAD-REGULATION ERROR vs. VL LOAD CURRENT



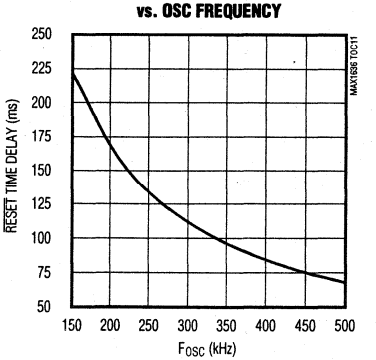
REF LOAD-REGULATION ERROR vs. REF LOAD CURRENT



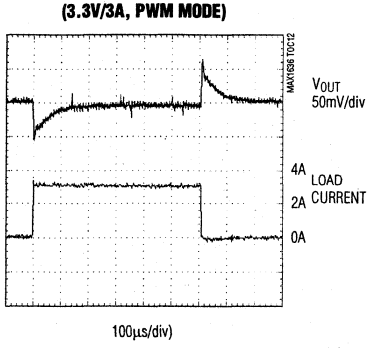
DROPOUT VOLTAGE vs. LOAD CURRENT



RESET TIME DELAY vs. OSC FREQUENCY



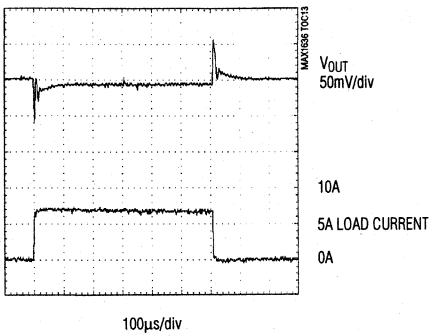
LOAD-TRANSIENT RESPONSE (3.3V/3A, PWM MODE)



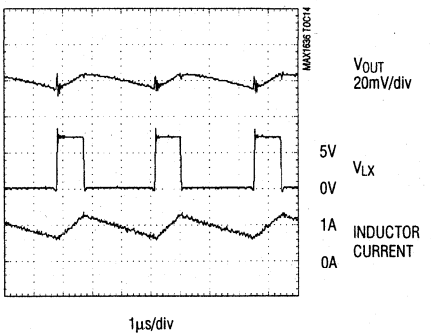
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 7V, T_A = +25°C, unless otherwise noted.)

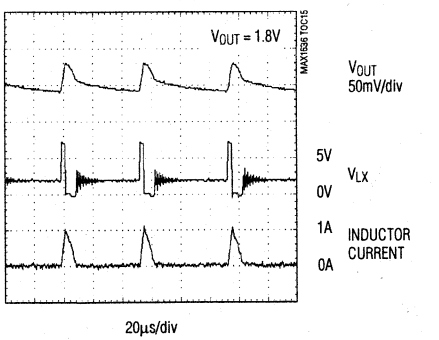
LOAD-TRANSIENT RESPONSE (1.8V, PWM MODE)



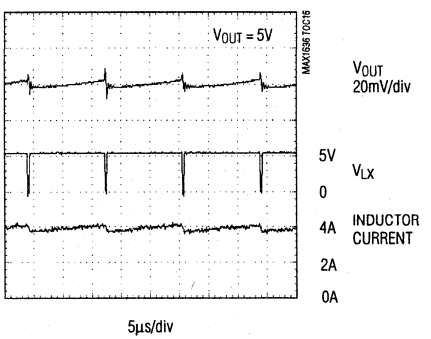
SWITCHING WAVEFORMS (PWM MODE)



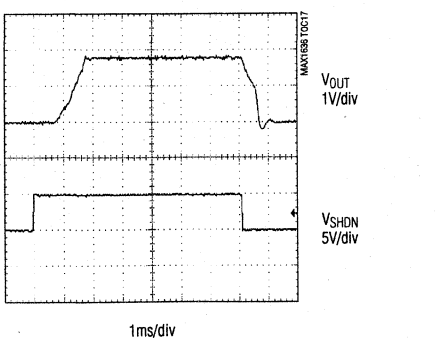
SWITCHING WAVEFORMS (PFM MODE)



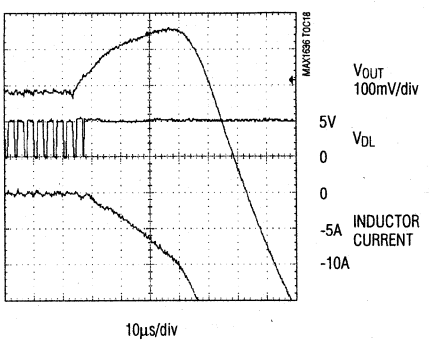
SWITCHING WAVEFORMS (DROPOUT OPERATION)



STANDBY AND STARTUP RESPONSE (V_{OUT} = 1.8V, NO LOAD)



OVERVOLTAGE-PROTECTION WAVEFORMS (V_{IN} SHORTED TO V_{OUT} THROUGH a 0.5Ω RESISTOR)



Low-Voltage, Precision Step-Down Controller for Portable CPU Power

Pin Description

PIN	NAME	FUNCTION
1	CSH	Current-Sense Input, High Side
2	CSL	Current-Sense Input, Low Side. Also serves as a feedback input in fixed output modes.
3	$\overline{RESET}$	Timed Reset Output. Low for at least 100ms after output voltage is valid, then goes high impedance (open drain).
4	$\overline{SHDN}$	Shutdown Control Input. Puts chip in shutdown or standby mode, depending on OVP (Table 5).
5	OVP	Overvoltage Protection Enable/Disable. Tie to GND to disable OVP; tie to V_{CC} to enable OVP.
6	CC	Compensation pin. Connect a small capacitor to GND to set the integration time constant.
7	REF	1.100V Reference Output. Capable of sourcing 50µA for external loads; bypass with a 0.22µF (min) capacitor.
8	SYNC	Oscillator Frequency Select and Synchronization Input. Tie to V_{CC} for 300kHz operation; tie to GND for 200kHz operation.
9, 10	GND	Analog Ground
11	FB	Feedback Input. Tie to GND for fixed 3.3V output; tie to V_{CC} for fixed 2.5V output; tie to resistor divider for adjustable mode.
12	V_{CC}	Main Supply Voltage Input. Powers the PWM controller, logic, and reference. Input range is +3.15V to +5.5V.
13	V+	5V VL Linear-Regulator Input. The VL linear regulator automatically shuts off if V+ is left open or shorted to V_L. Bypass V+ to GND with a 0.1µF capacitor close to the IC.
14	VL	5V Linear-Regulator Output. Powers the DL low-side gate driver. Bypass with a 2.2µF (min) capacitor.
15	DL	Low-Side Gate-Driver Output
16	PGND	Power Ground
17	BST	Boost-Capacitor Connection
18	DH	High-Side Gate-Driver Output
19	LX	Inductor Connection
20	$\overline{SKIP}$	Low-Noise Mode Control. Forces fixed-frequency PWM operation when high.

Standard Application Circuit

The basic MAX1636 buck converter (Figure 1) is easily adapted to meet a wide range of applications with inputs up to 30V by substituting components from Table 1. These circuits represent a good set of trade-offs between cost, size, and efficiency, while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current. Do not change the circuits' switching frequency without first recalculating component values (particularly inductance value at maximum battery voltage). Adding a Schottky rectifier across the synchronous rectifier improves circuit efficiency by approximately 1%. This rectifier is otherwise not needed because the MOSFET required typically incorporates a high-speed silicon diode from drain to source. Use a Schottky rectifier rated at a DC current equal to at least one-third of the load current.

Table 1. Component Selection for Standard Applications

COMPONENT	LOAD CURRENT				
	1A	4A	7A (EV KIT)	3A	3A
Input Voltage Range	7V to 22V	7V to 22V	7V to 22V	4.75V to 30V	6V to 30V
Output Voltage Range	1.8V	1.8V	1.25V to 2V	3.3V	5V
Application	CPU I/O	CPU Core	CPU Core		
Frequency	300kHz	300kHz	300kHz	300kHz	300kHz
Q1 High-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7403 or Siliconix Si9804DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY
Q2 Low-Side MOSFET	1/2 Si4902DY or 1/2 MMDF3NO3HD	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	Fairchild FDS6680 or Siliconix Si4420DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY	International Rectifier IRF7413, Fairchild NDS8410A, or Siliconix Si4410DY
C1 Input Capacitor	4.7µF, 25V ceramic Tokin C34Y5U1E475Z or Marcon/United Chemicon THCR40E1E475Z	2 x 10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR50E1E106ZT	4 x 10µF, 25V ceramic Tokin C34Y5U1E106Z or Marcon/United Chemicon THCR50E1E106ZT	2 x 22µF, 35V AVX TPSE226M035R0300 or Sprague 593D226X0035E2W	2 x 22µF, 35V AVX TPSE226M035R0300 or Sprague 593D226X0035E2W
C2 Output Capacitor	220µF, 6.3V tantalum Sprague 595D227X96R3C2	2 x 470µF, 4V low-ESR Sprague 594D477X0004R2T	4 x 390µF, 6.3V low-ESR, Sprague 594D397X06R3R2T, or 4 x 470µF, 4V Sprague 594D477X0004R2T	2x 220µF Sprague 594D 594D227X0010D2T	2x 220µF Sprague 594D 594D227X0010D2T
R1 Resistor	0.070Ω, 1% (1206) Dale WSL-1206-R070F	0.015Ω, 1% (2512) Dale WSL-2512-R015F	0.010Ω, 1% (2512) Dale WSL-2512-R010F	0.020Ω, 1% (2010) Dale WSL-2010-R020F	0.020Ω, 1% (2010) Dale WSL-2010-R020F
L1 Inductor	15µH Sumida CD54-150	4.6µH Panasonic ETQP1F4R6H, Sumida CDRH127-4R7, Coiltronics UP2-4R7, or Coilcraft DO3316P-472	2.2µH Panasonic P1F2R0HL, Sumida CDRH127-2R4, Coiltronics UP4-2R2, or Coilcraft DO5022P-222HC	10µH Sumida CDRH125-100, Coiltronics UP2-100, or Coilcraft DO3316-103	10µH Sumida CDRH125-100, Coiltronics UP2-100, or Coilcraft DO3316-103

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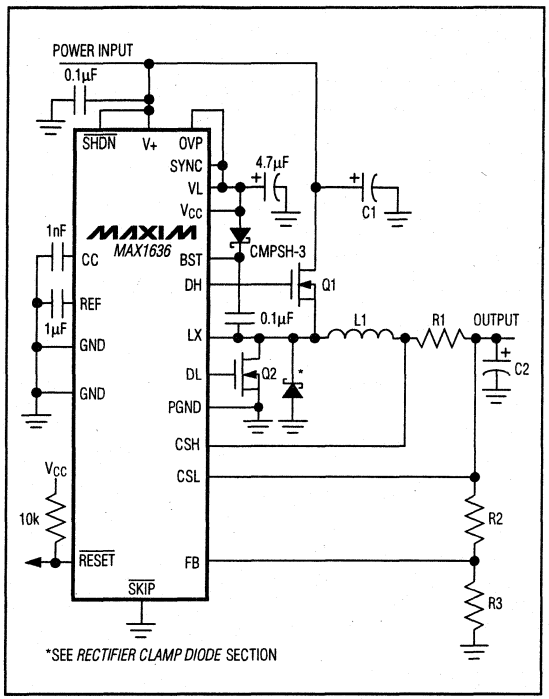

Figure 1. Standard Application Circuit

Table 2. Component Suppliers

COMPANY	FACTORY FAX (COUNTRY CODE)	USA PHONE
AVX	(1) 803-626-3123	(803) 946-0690
Central Semiconductor	(1) 516-435-1824	(516) 435-1110
Coilcraft	(1) 847-639-1469	(847) 639-6400
Coiltronics	(1) 561-241-9339	(561) 241-7876
Dale	(1) 605-665-1627	(605) 668-4131
Fairchild	(1) 408-721-1635	(408) 721-2181
International Rectifier (IR)	(1) 310-322-3332	(310) 322-3331
IRC	(1) 512-992-3377	(512) 992-7900
Marcon/United Chemi-Con	(1) 847-696-9278	(847) 696-2000
Matsuo	(1) 714-960-6492	(714) 969-2491
Motorola	(1) 602-994-6430	(602) 303-5454
Panasonic	(1) 714-373-7183	(714) 373-7939
Sanyo	(81) 7-2070-1174	(619) 661-6835
Siliconix	(1) 408-970-3950	(408) 988-8000
Sprague	(1) 603-224-1430	(603) 224-1961
Sumida	(81) 3-3607-5144	(847) 956-0666
TDK	(1) 847-390-4428	(847) 390-4373
Tokin	(1) 408-434-0375	(408) 432-8020

Detailed Description

The MAX1636 is a BiCMOS, switch-mode, power-supply controller designed primarily for buck-topology regulators in battery-powered applications where high efficiency and low quiescent supply current are critical. Light-load efficiency is enhanced by automatic Idle Mode operation, a variable-frequency, pulse-skipping mode that reduces transition and gate-charge losses. The step-down, power-switching circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter. The output voltage is the average AC voltage at the switching node, which is regulated by changing the duty cycle of the MOSFET switches. The gate-drive signal to the N-channel high-side MOSFET, which must exceed the battery voltage, is provided by a flying-capacitor boost circuit that uses a 100nF capacitor between BST and LX. The MAX1636 contains 10 major circuit blocks (Figure 2).

The pulse-width-modulation (PWM) controller consists of a Dual Mode™ feedback network and multiplexer, a multi-input PWM comparator, high-side and low-side gate drivers, and logic. The MAX1636 contains fault-protection circuits that monitor the PWM output for undervoltage and overvoltage. Bias generator blocks include the 5V (VL) linear regulator and the 1.1V precision reference. The PWM uses a 200kHz/300kHz synchronizable oscillator. The circuit blocks are powered from an internal IC power rail that receives power from either VL or V_{CC}. The synchronous-switch gate driver is powered directly from VL, while the high-side-switch gate driver is powered indirectly from VL via an external diode-capacitor boost circuit.

Dual Mode is a trademark of Maxim Integrated Products.

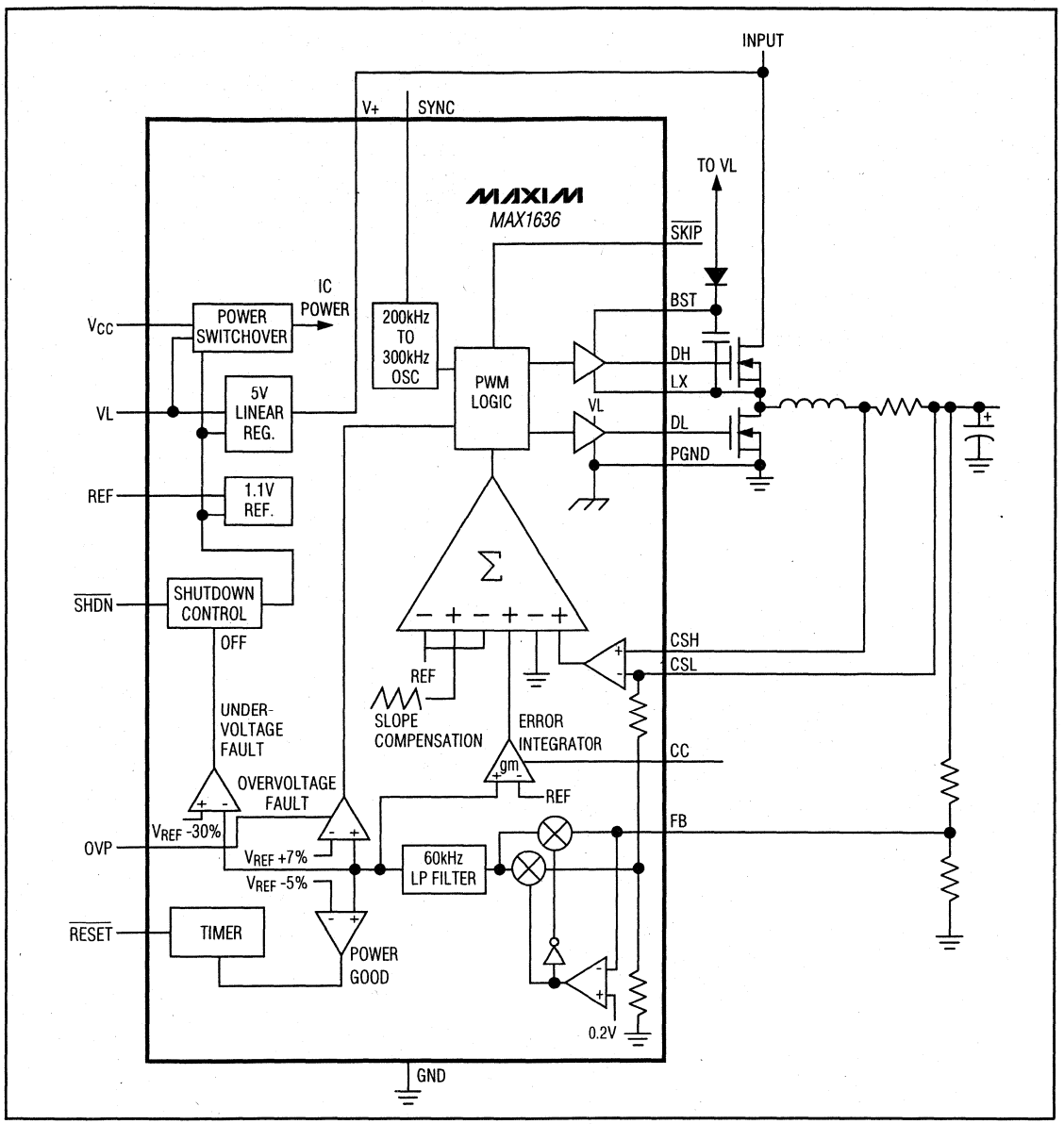

Figure 2. Functional Diagram

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Table 3. $\overline{SKIP}$ PWM Table

$\overline{SKIP}$	LOAD CURRENT	MODE	DESCRIPTION
Low	Light	Idle	Pulse-skipping, discontinuous inductor current
Low	Heavy	PWM	Constant-frequency PWM, continuous inductor current
High	Light	PWM	Constant-frequency PWM, continuous inductor current
High	Heavy	PWM	Constant-frequency PWM, continuous inductor current

PWM Controller

The heart of the current-mode PWM controller is a multi-input, open-loop comparator that sums four signals: the output voltage error signal with respect to the reference voltage, the current-sense signal, the integrated voltage-feedback signal, and the slope-compensation ramp (Figure 3).

The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage (Figure 4).

When $\overline{SKIP}$ = low, Idle Mode circuitry automatically optimizes efficiency throughout the load-current range. Idle Mode dramatically improves light-load efficiency

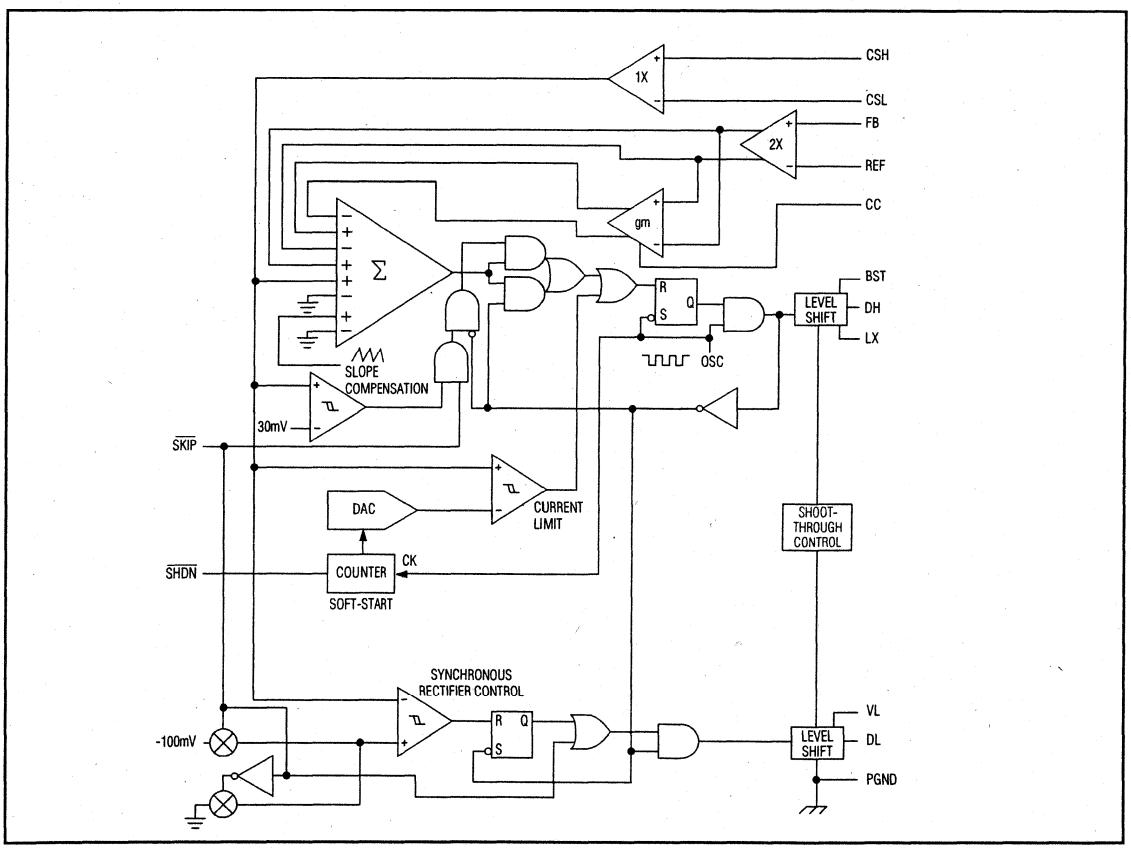

Figure 3. PWM Controller Functional Diagram

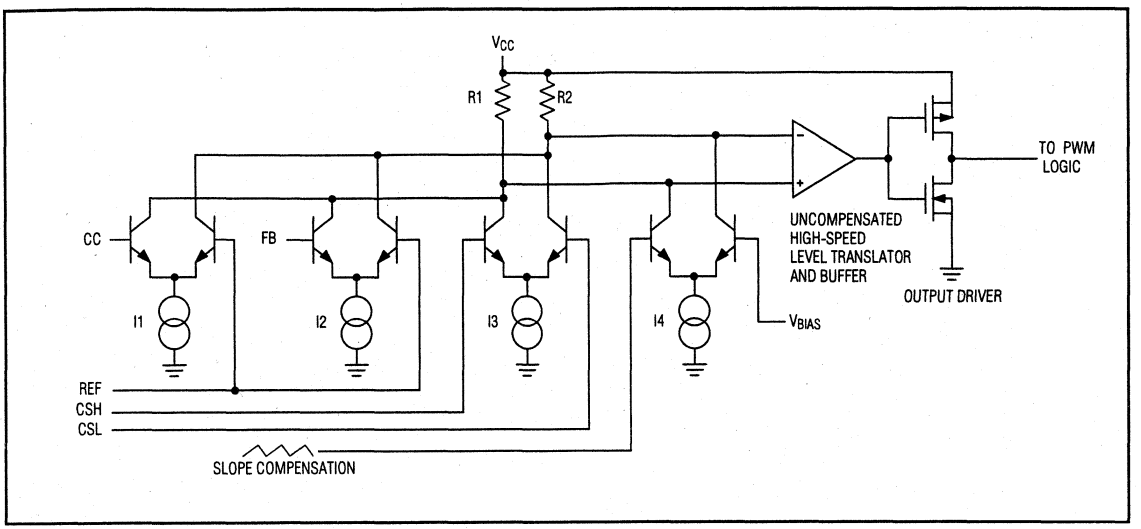

Figure 4. Main PWM Comparator Functional Diagram

by reducing the effective frequency, subsequently reducing switching losses. It forces the peak inductor current to ramp to 30% of the full current limit, delivering extra energy to the output and allowing subsequent cycles to be skipped. Idle Mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

With $\overline{SKIP}$ = high, the controller always operates in fixed-frequency PWM mode for lowest noise. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). As the high-side switch turns off, the synchronous rectifier latch sets; 60ns later, the low-side switch turns on. The low-side switch stays on until the beginning of the next clock cycle.

In PWM mode, the controller operates as a fixed-frequency, current-mode controller in which the duty factor is set by the input/output voltage ratio. The current-mode feedback system regulates the peak inductor current value as a function of the output voltage error signal. In continuous-conduction mode, the average inductor current is nearly the same as the peak current, so the circuit acts as a switch-mode transconductance amplifier. This pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current "staircasing," a slope-compensation ramp is summed into the main PWM comparator to make the apparent duty factor less than 50%.

The relative gains of the voltage-sense and current-sense inputs are weighted by the values of current sources that bias four differential input stages in the main PWM comparator (Figure 4). The voltage sense into the PWM has been conditioned by an integrated component of the feedback voltage, yielding excellent DC output voltage accuracy. See the *Output Voltage Accuracy* section for more information.

Synchronous Rectifier Driver (DL)

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky catch diode with a low-resistance MOSFET switch. Also, the synchronous rectifier ensures proper start-up of the boost gate-driver circuit. If the synchronous power MOSFET is omitted for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

If the circuit is operating in continuous-conduction mode, the DL drive waveform is simply the complement of the DH high-side-drive waveform (with controlled dead time to prevent cross-conduction or "shoot-through"). In discontinuous (light-load) mode, the synchronous switch is turned off as the inductor current falls through zero.

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Table 4. Powering the MAX1636

AVAILABLE POWER SOURCES	V_{CC} CONNECTS TO	V+ CONNECTS TO	VL CONNECTS TO	COMMENT
Battery, 3.3V, and 5V	3.3V	5V	5V	Most efficient
Battery and 5V	5V	5V	5V	
Battery and 3.3V	3.3V	Battery	Bypass capacitor only	
Battery only	VL	Battery	Bypass capacitor only	Least efficient

REF and VL Supplies and V_{CC} Input

The 1.1V reference (REF) is accurate to ±1% over temperature, making REF useful as a precision system reference. Bypass REF to GND with a 0.22µF (min) capacitor. REF can supply up to 50µA for external loads. Loading REF reduces the main output voltage slightly because of the reference load-regulation error. The 5V VL linear-regulator output can be tied to the system +5V supply in order to obtain gate-drive power from an efficient source. The two supply pins (V_{CC} and VL) are independent of each other (no protection diodes or sequencing requirements), allowing you to choose the most efficient sources for chip biasing from among existing system supply voltages without having to worry about sequencing or latch-up problems (Table 4).

The V_{CC} input runs the chip if the V_{CC} voltage is greater than 3.15V. Otherwise, the chip supply is powered from VL via the internal V_{CC}-VL switchover circuit. If a system supply between 3.3V and 5V is not available, tie V_{CC} directly to VL.

In shutdown mode, the VL regulator and reference are completely turned off. In standby mode, the VL regulator and DL stay alive so that the overvoltage-protection circuit can operate (Table 5).

Important: Ensure that VL and V_{CC} do not exceed 6V. Measure VL with the main output fully loaded. If it is pumped above 5.5V, either excessive boost-diode capacitance or excessive ripple at V+ is the probable cause. Use only small-signal diodes for the boost circuit (10mA to 100mA Schottky or 1N4148 are preferred) and bypass VL to PGND with a 4.7µF capacitor directly at the package pins.

Shutdown and Standby Modes

Holding $\overline{SHDN}$ low puts the IC into its 3µA shutdown mode. $\overline{SHDN}$ is a logic input with a threshold of about 1V (the VTH of an internal N-channel MOSFET). For automatic start-up, tie $\overline{SHDN}$ to V+.

Standby operation is entered when $\overline{SHDN}$ = low and OVP = high (Table 5). In standby mode, the VL regulator stays active, and the DL output is forced high to provide overvoltage protection by clamping the output to GND. However, DL is not forced high until the output sags below V_{REF}, so that the output can be held high by external keep-alive supplies.

$\overline{RESET}$ Power-Good Voltage Monitor

The power-good monitor generates a system-reset signal. The $\overline{RESET}$ output is an open drain that needs to be pulled up to the appropriate logic supply. At first power-up, $\overline{RESET}$ is held low until output is in regulation. At this point, an internal timer begins counting oscillator pulses, and $\overline{RESET}$ continues to be held low until 32,000 cycles have elapsed. After this timeout period (107ms at 300kHz or 160ms at 200kHz), the $\overline{RESET}$ output is released.

Output Undervoltage Lockout

The output undervoltage-lockout circuit is similar to foldback current limiting but employs a timer rather than a variable current limit. The SMPS has an undervoltage-protection circuit that is activated 6144 clock cycles after the SMPS is enabled. If the SMPS output is under 70% of the nominal value, output is latched off and does not restart until $\overline{SHDN}$ is toggled or until V+ power is cycled below 1V. Note that undervoltage protection can make prototype troubleshooting difficult, since only 20ms or 30ms elapse before the SMPS is latched off.

The output undervoltage lockout circuit protects against heavy overloads and shorts to the main SMPS output. The circuit trips if the output is less than 70% of the nominal output value any time after the timeout has expired upon start-up. When the comparator trips, the output is turned off (the SMPS stops switching). This state is similar to thermal shutdown and can be exited by a power-on reset or by a rising edge on $\overline{SHDN}$. The overvoltage crowbar is disabled in output undervoltage or thermal shutdown modes.

Table 5. Operating Modes

MODE	$\overline{SHDN}$	OVP	HOW ENTERED	STATUS	NOTES
Run	High	High		All circuit blocks active	Normal operation
Standby	Low	High		VL = on REF = off DL = high $\overline{RESET}$ = high-Z (high state)	DL = high to enforce overvoltage protection
Shutdown	Low	Low		All circuit blocks inactive	Lowest possible quiescent consumption
Overvoltage (crowbar)	High	High	V_{OUT} > 7% too high	VL = on REF = off DL = high $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits crowbar.
Output UVLO	High	Don't care	V_{OUT} < 70% of nominal after 20–30ms timeout expires	VL = on REF = off DL = low $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits output UVLO.
Thermal Shutdown	High	High	T_J > +150°C	VL = on REF = off DL = high $\overline{RESET}$ = low	Cycling $\overline{SHDN}$ or a power-on reset exits thermal shutdown.
Thermal Shutdown	High	Low	T_J > +150°C	All circuit blocks inactive	Cycling $\overline{SHDN}$ or a power-on reset exits thermal shutdown.

Output Overvoltage Protection (OVP)

The overvoltage crowbar protection circuit is intended to blow a fuse in series with the battery if the main SMPS output rises significantly higher than its preset level. In normal operation, the output is compared to the internal precision reference voltage. If the output goes 7% above nominal, the synchronous rectifier MOSFET turns on 100% (the high-side MOSFET is simultaneously forced off) in order to draw massive amounts of battery current to blow the fuse. This safety feature does not protect the system against a failure of the controller IC itself but is intended primarily to guard against a short across the high-side MOSFET. A crowbar event is latched and can only be reset by a rising edge on $\overline{SHDN}$ (or by removal of the V+ supply voltage). The overvoltage-detection decision is made relative to the regulation point.

The overvoltage comparators are kept inactive in standby mode. Instead, the DL driver is simply left in the high state. However, DL does not turn on until the output has decayed to less than 1V. This prevents conflicts in systems where the output is held up by an external source in suspend or backup mode. The OVP pin has an internal pulldown resistor that is only turned on during the reset phase. The OVP pin's state is then sampled and stored internally. A floating OVP pin implies no overvoltage protection.

Boost High-Side Gate-Drive Supply (BST)

Gate-drive voltage for the high-side N-channel switch is generated by a flying-capacitor boost circuit (Figure 2). The capacitor between BST and LX is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate-source terminals.

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and charges the boost capacitor to 5V. On the second half-cycle, the SMPS turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary enhancement voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above the battery voltage.

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Ringing at the high-side MOSFET gate (DH) in discontinuous-conduction mode (light loads) is a natural operating condition. It is caused by residual energy in the tank circuit, formed by the inductor and stray capacitance at the switching node, LX. The gate-drive negative rail is referred to LX, so any ringing there is directly coupled to the gate-drive output.

Current-Limiting and Current-Sense Inputs (CSH and CSL)

The current-limit circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL exceeds 100mV. This limiting is effective for both current flow directions, putting the threshold limit at ±100mV. The tolerance on the positive current limit is ±20%, so the external low-value sense resistor (R1) must be sized for 80mV/I_{PEAK}, where I_{PEAK} is the required peak inductor current to support the full load current. Components must be designed to withstand continuous current stresses of 120mV/R1.

For breadboarding or for very high current applications, it may be useful to wire the current-sense inputs with a twisted pair rather than PC traces (two pieces of wrapped wire twisted together are sufficient.) This reduces the noise picked up at CSH and CSL, which can cause unstable switching and reduced output current.

Oscillator Frequency and Synchronization (SYNC)

The SYNC input controls the oscillator frequency. Low selects 200kHz; high selects 300kHz. SYNC can also be used to synchronize with an external 5V CMOS or TTL clock generator. SYNC has a guaranteed 240kHz to 340kHz capture range. A high-to-low transition on SYNC initiates a new cycle.

Operation at 300kHz optimizes the application circuit for component size and cost. Operation at 200kHz provides increased efficiency, lower dropout, and improved load-transient response at low input-output voltage differences (see the *Low-Voltage Operation* section).

Output Voltage Accuracy (GND, CC)

Output voltage error is guaranteed to be within ±1% over all conditions of line, load, and temperature. The DC load regulation is typically better than 0.1% due to the integrator amplifier. Transient response is optimized by providing a feedback signal that has a direct path from the output to the main summing PWM comparator. The integrated feedback signal is also summed into the PWM comparator, with the gain weighted so that the integrated signal has only enough gain to correct the DC inaccuracies. The integrator's response time is determined by the time constant set by the capacitor placed on the CC pin. The time constant should not be so fast that the integrator responds to the normal V_{OUT} ripple or too slow to negate the integrator's effect. A 470pF to 1500pF CC capacitor is sufficient for 200kHz to 300kHz frequencies.

Figure 5 shows the output voltage response to a 0A to 3A load transient with and without the integrator. With the integrator, the output voltage returns to within 0.1% of its no-load value with only a small AC excursion. Without the integrator, the typical load-transient response with the AC and DC output voltage changes. Asymmetrical clamping at the integrator output prevents worsening of load transients during pulse-skipping mode.

Internal Digital Soft-Start Circuit

Soft-start allows a gradual increase of the internal current-limit level at start-up to reduce input surge currents. The SMPS contains an internal digital soft-start circuit controlled by a counter, a digital-to-analog converter (DAC), and a current-limit comparator. In shutdown or standby mode, the soft-start counter is reset to zero. When the SMPS is enabled, its counter starts counting oscillator pulses, and the DAC begins incrementing the comparison voltage applied to the current-limit comparator. The DAC output increases from 0mV to 100mV in five equal steps as the count increases to 512 clocks. As a result, the main output capacitor charges up relatively slowly. The exact time of the output rise depends on output capacitance and load current, but it is typically 1ms with a 300kHz oscillator.

Overload and Dropout Operation

Dropout (low input-output differential) operation is enhanced by stretching the clock pulse width to increase the maximum duty factor. The algorithm follows: If the output voltage (V_{OUT}) drops out of regulation without the current limit having been reached, the SMPS skips an off-time period (extending the on-time). At the end of the cycle, if the output is still out of regulation, the SMPS skips another off-time period. This action can continue until three off-time periods are skipped, effectively dividing the clock frequency by as much as four. This behavior also slightly improves load-transient response. Dividing the clock frequency by four raises the maximum duty factor to above 98%. The typical PWM minimum off-time is 300ns, regardless of the operating frequency.

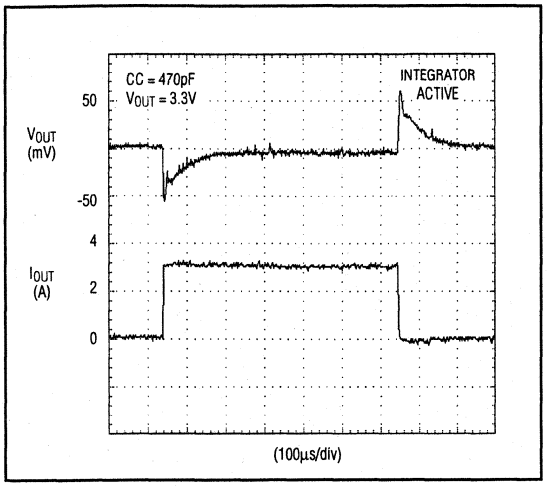

Figure 5a. Load-Transient Response with Integrator Active

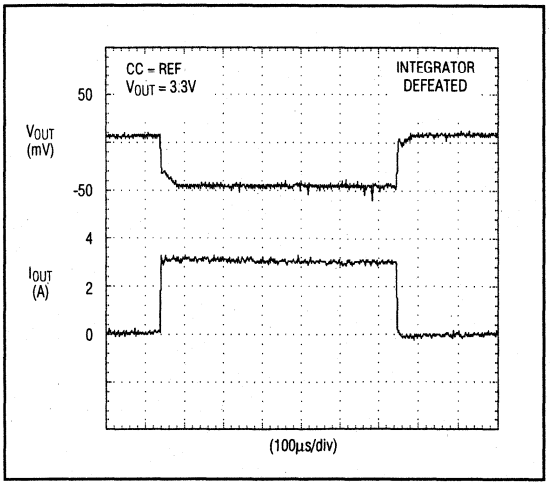

Figure 5b. Load-Transient Response with Integrator Defeated

Adjustable-Output Feedback (Dual-Mode FB)

A fixed, preset output voltage of 2.5V and 3.3V is selected when FB is connected to V_{CC} or ground. In this mode, internal resistors monitor the voltage on CSL. For voltages other than the fixed-output options, adjust the output voltage through a resistor divider connected to FB (Figure 2). Calculate the output voltage with the following formula:

$$V_{OUT} = V_{REF} (1 + R1 / R2)$$

where V_{REF} = 1.1V nominal. Recommended normal values for R2 range from 5kΩ to 100kΩ. To achieve a 1.1V nominal output, simply connect FB directly to CSL.

Remote output voltage sensing is not possible in fixed output mode due to the combined nature of the voltage-sense and current-sense inputs (CSL). It is, however, easy to do in adjustable mode by using the top of the external resistor divider as the remote sense point.

Low-Noise Operation (PWM Mode)

PWM mode ($\overline{SKIP}$ = high) minimizes RF and audio interference in noise-sensitive applications such as hi-fi multimedia-equipped systems, cellular phones, RF communicating computers, and electromagnetic pen-entry systems. See the summary of operating modes in Table 5. $\overline{SKIP}$ can be driven from an external logic signal.

PWM mode forces a constant switching frequency, reducing interference due to switching noise by concentrating the emissions at a known frequency outside the system audio or IF bands. Choose an oscillator frequency for which switching frequency harmonics do not overlap a sensitive frequency band. If necessary, synchronize the oscillator to a tight-tolerance external clock generator. To extend the output voltage-regulation range, constant operating frequency is not maintained under overload or dropout conditions (see the *Overload and Dropout Operation* section).

PWM mode ($\overline{SKIP}$ = high) forces two changes on the PWM controller. First, it disables the minimum-current comparator, ensuring fixed-frequency operation. Second, it changes the detection threshold for reverse-current limit from 0mV to -100mV, allowing the inductor current to reverse at light loads. This results in fixed-frequency operation and continuous inductor-current flow. PWM mode eliminates discontinuous-mode inductor ringing and improves cross-regulation of transformer-coupled, multiple-output supplies.

In most applications, tie $\overline{SKIP}$ to GND to minimize quiescent supply current. VL supply current with $\overline{SKIP}$ high is typically 20mA, depending on external MOSFET gate capacitance and switching losses.

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

Design Procedure

The five predesigned standard application circuits (Figure 1 and Table 1) contain ready-to-use solutions for common application needs. Use the following design procedure to optimize these basic schematics for different voltage or current requirements. But before beginning a design, firmly establish the following:

- Maximum input (battery) voltage, $V_{IN(MAX)}$. This value should include the worst-case conditions, such as no-load operation when a battery charger or AC adapter is connected but no battery is installed. $V_{IN(MAX)}$ must not exceed 30V.
- Minimum input (battery) voltage, $V_{IN(MIN)}$. This should be taken at full load under the lowest battery conditions. If $V_{IN(MIN)}$ is less than 4.5V, use an external circuit to externally hold VL above the VL undervoltage lockout threshold. If the minimum input-output difference is less than 1.5V, the filter capacitance required to maintain good AC load regulation increases (see *Low-Voltage Operation* section).

Inductor Value

The exact inductor value is not critical and can be freely adjusted to make trade-offs between size, cost, and efficiency. Lower inductor values minimize size and cost but reduce efficiency due to higher peak-current levels. The smallest inductor is achieved by lowering the inductance until the circuit operates at the border between continuous and discontinuous mode. Further reducing the inductor value below this crossover point results in discontinuous-conduction operation even at full load. This helps lower output filter capacitance requirements, but efficiency suffers due to high I^2R losses. On the other hand, higher inductor values mean greater efficiency, but resistive losses due to extra wire turns eventually exceed the benefit gained from lower peak-current levels. Also, high inductor values can affect load-transient response (see the V_{SAG} equation in the *Low-Voltage Operation* section). The equations in this section are for continuous-conduction operation.

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant, LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows smaller inductance but results in higher losses and higher ripple. A good compromise between size and losses is a 30% ripple-current to load-current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times higher than the DC load current.

$$L = V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (V_{IN(MIN)} \times f \times I_{OUT} \times LIR)$$

where f = switching frequency, normally 200kHz or 300kHz, and I_{OUT} = maximum DC load current. The peak current can be calculated by:

$$I_{PEAK} = I_{LOAD} + [V_{OUT}(V_{IN(MAX)} - V_{OUT}) / (2 \times f \times L \times V_{IN(MAX)})]$$

The inductor's DC resistance should be low enough that $R_{DC} \times I_{PEAK} < 100mV$, as it is a key parameter for efficiency performance. If a standard, off-the-shelf inductor is not available, choose a core with an LI^2 rating greater than $L \times I_{PEAK}^2$ and wind it with the largest diameter wire that fits the winding area. For 300kHz applications, ferrite-core material is strongly preferred; for 200kHz applications, Kool-Mu® (aluminum alloy) or even powdered iron is acceptable. If light-load efficiency is unimportant (in desktop PC applications, for example), then low-permeability iron-powder cores may be acceptable, even at 300kHz. For high-current applications, shielded-core geometries, such as toroidal or pot core, help keep noise, EMI, and switching-waveform jitter low.

Current-Sense Resistor Value

The current-sense resistor value is calculated according to the worst-case, low-current-limit threshold voltage (from the *Electrical Characteristics* table) and the peak inductor current:

$$R_{SENSE} = 80mV / I_{PEAK}$$

Use I_{PEAK} from the second equation in the *Inductor Value* section. Use the calculated value of R_{SENSE} to size the MOSFET switches and specify inductor saturation-current ratings according to the worst-case high-current-limit threshold voltage:

$$I_{PEAK} = 120mV / R_{SENSE}$$

Low-inductance resistors, such as surface-mount metal film, are recommended.

Input Capacitor Value

Connect low-ESR bulk capacitors directly to the drain on the high-side MOSFET. The bulk input filter capacitor is usually selected according to input ripple current requirements and voltage rating, rather than capacitor value. Electrolytic capacitors with low enough equivalent series resistance (ESR) to meet the ripple-current requirement invariably have sufficient capacitance values. Aluminum electrolytic capacitors, such as Sanyo OS-CON or Nichicon PL, are superior to tantalum types, which risk power-up surge-current failure, especially when connecting to robust AC adapters or low-impedance batteries. RMS input ripple current (I_{RMS}) is

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determined by the input voltage and load current, with the worst case occurring at $V_{IN} = 2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} \times \sqrt{V_{OUT}(V_{IN} - V_{OUT})} / V_{IN}$$

Therefore, when V_{IN} is $2 \times V_{OUT}$:

$$I_{RMS} = I_{LOAD} / 2$$

Output Filter Capacitor Value

The output filter capacitor values are generally determined by the ESR and voltage-rating requirements rather than actual capacitance requirements for loop stability. In other words, the low-ESR electrolytic capacitor that meets the ESR requirement usually has more output capacitance than is required for AC stability. Use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. To ensure stability, the capacitor must meet both minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > V_{REF}(1 + V_{OUT} / V_{IN(MIN)}) / V_{OUT} \times R_{SENSE} \times f$$

$$R_{ESR} < R_{SENSE} \times V_{OUT} / V_{REF}$$

where R_{ESR} can be multiplied by 1.5, as discussed below.

These equations are worst case, with 45 degrees of phase margin to ensure jitter-free, fixed-frequency operation, and provide a nicely damped output response for zero to full-load step changes. Some cost-conscious designers may wish to bend these rules with less-expensive capacitors, particularly if the load lacks large step changes. This practice is tolerable if some bench testing over temperature is done to verify acceptable noise and transient response.

No well-defined boundary exists between stable and unstable operation. As phase margin is reduced, the first symptom is timing jitter, which shows up as blurred edges in the switching waveforms where the scope does not quite sync up. Technically speaking, this jitter (usually harmless) is unstable operation, since the duty factor varies slightly. As capacitors with higher ESRs are used, the jitter becomes more pronounced, and the load-transient output voltage waveform starts looking ragged at the edges. Eventually, the load-transient waveform has enough ringing on it that the peak noise levels exceed the allowable output voltage tolerance. Note that even with zero phase margin and gross instability, the output voltage noise never gets much worse than $I_{PEAK} \times R_{ESR}$ (under constant loads).

Designers of RF communicators or other noise-sensitive analog equipment should be conservative and stay within the guidelines. Designers of notebook computers and similar commercial-temperature-range digital systems can multiply the R_{ESR} value by a factor of 1.5 without hurting stability or transient response.

The output voltage ripple, which is usually dominated by the filter capacitor's ESR, can be approximated as $I_{RIPPLE} \times R_{ESR}$. There is also a capacitive term, so the full equation for ripple in continuous-conduction mode is $V_{NOISE(p-p)} = I_{RIPPLE} \times [R_{ESR} + 1 / (2 \times p \times f \times C_{OUT})]$. In Idle Mode, the inductor current becomes discontinuous, with high peaks and widely spaced pulses, so the noise can actually be higher at light load (compared to full load). In Idle Mode, calculate the output ripple as follows:

$$V_{NOISE(p-p)} = \frac{0.02 \times R_{ESR}}{R_{SENSE}} + \frac{0.0003 \times L \times \left[1/V_{OUT} + 1/(V_{IN} - V_{OUT})\right]}{(R_{SENSE})^2 \times C_F}$$

Selecting Other Components

MOSFET Switches

The high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at VGS = 4.5V. Lower gate-threshold specifications are better (i.e., 2V max rather than 3V max). Drain-source breakdown voltage ratings must at least equal the maximum input voltage, preferably with a 20% derating factor. The best MOSFETs have the lowest on-resistance per nanocoulomb of gate charge. Multiplying $R_{DS(ON)}$ by Q_G provides a good figure of merit for comparing various MOSFETs. Newer MOSFET process technologies with dense cell structures generally perform best. The internal gate drivers tolerate >100nC total gate charge, but 70nC is a more practical upper limit to maintain best switching times.

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. I^2R losses are distributed between Q1 and Q2 according to duty factor as shown in the equations below. Generally, switching losses affect only the upper MOSFET, since the Schottky rectifier usually clamps the switching node before the synchronous rectifier turns on. Gate-charge losses are dissipated by the driver and do not heat the MOSFET. Calculate the temperature rise according to package thermal-resistance specifications to ensure

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

that both MOSFETs are within their maximum junction temperature at high ambient temperature. The worst-case dissipation for the high-side MOSFET occurs at both extremes of input voltage, and the worst-case dissipation for the low-side MOSFET occurs at maximum input voltage.

$$Duty = (V_{OUT} + V_{Q2}) / (V_{IN} - V_{Q1})$$

$$PD\ (upper\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times Duty + V_{IN} \times I_{LOAD} \times f \times [(V_{IN} \times C_{RSS}) / I_{GATE} + 20ns]$$

$$PD\ (lower\ FET) = I_{LOAD}^2 \times R_{DS(ON)} \times (1 - Duty)$$

where on-state voltage drop $V_Q = I_{LOAD} \times R_{DS(ON)}$, C_{RSS} = MOSFET reverse transfer capacitance, I_{GATE} = DH driver peak output current capability (1A typ), and 20ns = DH driver inherent rise/fall time. The MAX1636's output undervoltage shutdown protects the synchronous rectifier under output short-circuit conditions. To reduce EMI, add a 0.1µF ceramic capacitor from the high-side switch drain to the low-side switch source.

Rectifier Clamp Diode

The rectifier is a clamp across the low-side MOSFET that catches the negative inductor swing during the 60ns dead time between turning one MOSFET off and each low-side MOSFET on. The latest generations of MOSFETs incorporate a high-speed silicon body diode, which serves as an adequate clamp diode if efficiency is not of primary importance. A Schottky diode can be placed in parallel with the body diode to reduce the forward voltage drop, typically improving efficiency 1% to 2%. Use a diode with a DC current rating equal to one-third of the load current; for example, use an MBR0530 (500mA-rated) type for loads up to 1.5A, a 1N5819 type for loads up to 3A, or a 1N5822 type for loads up to 10A. The rectifier's rated reverse-breakdown voltage must be at least equal to the maximum input voltage, preferably with a 20% derating factor.

Boost-Supply Diode

A signal diode such as a 1N4148 works well in most applications. If the input voltage can go below +6V, use a small (20mA) Schottky diode for slightly improved efficiency and dropout characteristics. Do not use large power diodes, such as 1N5817 or 1N4001, since high junction capacitance can pump up VL to excessive voltages.

Low-Voltage Operation

Low input voltages and low input-output differential voltages each require extra care in their design. Low absolute input voltages can cause the VL linear regulator to enter dropout and eventually shut itself off. Low V_{IN} - V_{OUT} differentials can cause the output voltage to sag when the load current changes abruptly. The sag's amplitude is a function of inductor value and maximum duty factor (D_{MAX}, an *Electrical Characteristics* parameter, 98% guaranteed over temperature at f = 200kHz) as follows:

$$V_{SAG} = \frac{(I_{STEP})^2 \times L}{2 \times C_F \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

Table 6 is a low-voltage troubleshooting guide. The cure for low-voltage sag is to increase the output capacitor's value. For example, at V_{IN} = +5.5V, V_{OUT} = 5V, L = 10µH, f = 200kHz, and I_{STEP} = 3A, a total capacitance of 660µF keeps the sag less than 200mV. Note that only the capacitance requirement increases; the ESR requirements do not change. Therefore, the added capacitance can be supplied by a low-cost bulk capacitor in parallel with the normal low-ESR capacitor.

Applications Information

Heavy-Load Efficiency Considerations

The major efficiency-loss mechanisms under loads are as follows, in the usual order of importance:

- P(I^2R) = I^2R losses
- P(tran) = transition losses
- P(gate) = gate-charge losses
- P(diode) = diode-conduction losses
- P(cap) = capacitor ESR losses
- P(IC) = losses due to the IC's operating supply current

Inductor core losses are fairly low at heavy loads because the inductor's AC current component is small. Therefore, they are not accounted for in this analysis. Ferrite cores are preferred, especially at 300kHz, but powdered cores, such as Kool-Mu, can also work well.

$$Efficiency = P_{OUT} / P_{IN} \times 100\%$$

$$= P_{OUT} / (P_{OUT} + P_{TOTAL}) \times 100\%$$

$$P_{TOTAL} = P(I^2R) + P(tran) + P(gate) + P(diode) + P(cap) + P(IC)$$

$$P = (I^2R) = (I_{LOAD})^2 \times (R_{DC} + R_{DS(ON)} + R_{SENSE})$$

Table 6. Low-Voltage Troubleshooting Chart

SYMPTOM	CONDITION	ROOT CAUSE	SOLUTION
Sag or droop in V_{OUT} under step-load change	Low V_{IN}-V_{OUT} differential, <1.5V	Limited inductor-current slew rate per cycle.	Increase bulk output capacitance per formula (see *Low-Voltage Operation* section). Reduce inductor value.
Dropout voltage is too high (V_{OUT} follows V_{IN} as V_{IN} decreases)	Low V_{IN}-V_{OUT} differential, <1V	Maximum duty-cycle limits exceeded.	Reduce operation to 200kHz. Reduce MOSFET on-resistance and coil DCR.
Unstable—jitters between different duty factors and frequencies	Low V_{IN}-V_{OUT} differential, <0.5V	Normal function of internal low-dropout circuitry.	Increase the minimum input voltage or ignore.
Poor efficiency	Low input voltage, <5V	VL linear regulator is going into dropout and isn't providing good gate-drive levels.	Use a small 20mA Schottky diode for boost diode. Supply VL from an external source.
Won't start under load or quits before battery is completely dead	Low input voltage, <4.5V	VL output is so low that it hits the VL UVLO threshold.	Supply VL from an external source other than V_{IN}, such as the system +5V supply.

where R_{DC} is the DC resistance of the coil, $R_{DS(ON)}$ is the MOSFET on-resistance, and R_{SENSE} is the current-sense resistor value. The $R_{DS(ON)}$ term assumes identical MOSFETs for the high-side and low-side switches because they time-share the inductor current. If the MOSFETs are not identical, their losses can be estimated by averaging the losses according to duty factor.

$$PD(tran) = \text{transition loss} = V_{IN} \times I_{LOAD} \times f \times 3/2 \times [(V_{IN} C_{RSS} / I_{GATE}) + 20ns]$$

where C_{RSS} is the reverse transfer capacitance of the high-side MOSFET (a data-sheet parameter), I_{GATE} is the DH gate-driver peak output current (1.5A typ), and 20ns is the rise/fall time of the DH driver (20ns typ).

$$P(gate) = Q_g \times f \times VL$$

where VL is the internal logic-supply voltage (+5V), and Q_g is the sum of the gate-charge values for low-side and high-side switches. For matched MOSFETs, Q_g is twice the data-sheet value of an individual MOSFET. If V_{OUT} is set to less than 4.5V, replace VL in this equation with V_{BATT}. In this case, efficiency can be improved by connecting VL to an efficient 5V source, such as the system +5V supply.

$$P(diode) = \text{diode conduction losses} = I_{LOAD} \times V_{FWD} \times t_D \times f$$

where t_D is the diode-conduction time (120ns typ), and V_{FWD} is the forward voltage of the diode. This power is dissipated in the MOSFET body diode if no external Schottky diode is used.

$$P(cap) = \text{input capacitor ESR loss} = I_{RMS}^2 \times R_{ESR}$$

where I_{RMS} is the input ripple current as calculated in the *Input Capacitor Value* section.

Light-Load Efficiency Considerations

Under light loads, the PWM operates in discontinuous mode, where the inductor current discharges to zero at some point during the switching cycle. This makes the inductor current's AC component high compared to the load current, which increases core losses and I^2R losses in the output filter capacitors. For best light-load efficiency, use MOSFETs with moderate gate-charge levels and use ferrite, MPP, or other low-loss core material. Avoid powdered-iron cores; even Kool-Mu (aluminum alloy) is not as good as ferrite.

PC Board Layout Considerations

Good PC board layout is required in order to achieve specified noise, efficiency, and stable performance. The PC board layout artist must be given explicit instructions, preferably a pencil sketch showing the placement of power-switching components and high-current routing. See the PC board layout in the MAX1636 evaluation kit manual for examples. A ground plane is essential for optimum performance. In most applications, the circuit will be located on a multi-layer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current

Low-Voltage, Precision Step-Down Controller for Portable CPU Power

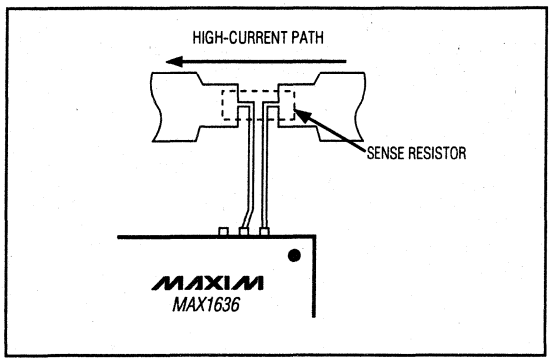


Figure 6. Kelvin Connections for the Current-Sense Resistors

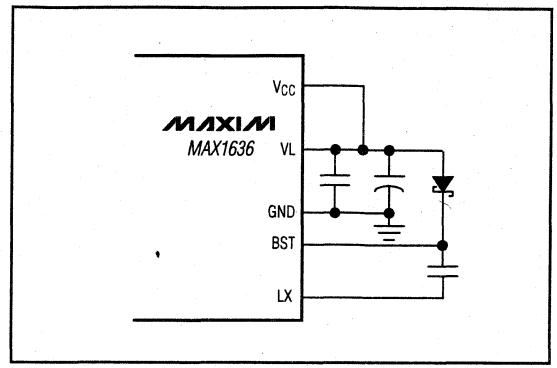


Figure 7. Capacitor Placement

connections, the bottom layer for quiet connections (REF, CC, GND), and the inner layers for an uninterrupted ground plane. Use the following step-by-step guide:

1) Place the high-power components (C1, C2, Q1, Q2, D1, L1, and R1) first, with their grounds adjacent.
   - *Minimize current-sense resistor trace lengths* and ensure accurate current sensing with Kelvin connections (Figure 6).
   - *Minimize ground trace lengths* in the high-current paths.
   - *Minimize other trace lengths* in the high-current paths.
     - — Use >5mm-wide traces.
     - — CIN to high-side MOSFET drain: 10mm max length
     - — Rectifier diode cathode to low side
     - — MOSFET: 5mm max length
     - — LX node (MOSFETs, rectifier cathode, inductor): 15mm max length

Ideally, surface-mount power components are butted up to one another with their ground terminals almost touching. These high-current grounds are then connected to each other with a wide, filled zone of top-layer copper so they do not go through vias. The resulting top-layer subground plane is connected to the normal inner-layer ground plane at the output ground terminals, which ensures that the IC's analog ground is sensing at the supply's output terminals without interference from IR drops and ground noise. Other high-current paths should also be minimized, but focusing primarily on short ground and current-sense connections eliminates about 90% of all PC board layout problems (see the PC board layouts in the MAX1636 evaluation kit manual for examples).

2) Place the IC and signal components. Keep the main switching nodes (LX nodes) away from sensitive analog components (current-sense traces and REF capacitor). Place the IC and analog components on the opposite side of the board from the power-switching node. **Important**: The IC must be no further than 10mm from the current-sense resistors. Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm and route them away from CSH, CSL, and REF. Place ceramic bypass capacitors close to the IC. The bulk capacitors can be placed further away. If using VL to power V_{CC}, minimize noise by placing a 0.1µF capacitor close to the V_{CC} pin and placing the 4.7µF capacitor further away, but closer than the boost diode (Figure 7).
3) Use a single-point star ground where the input ground trace, power ground (subground plane), and normal ground plane meet at the supply's output ground terminal. Connect both IC ground pins and all IC bypass capacitors to the normal ground plane.

Chip Information

TRANSISTOR COUNT: 3472

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Low-Voltage, Precision, Step-Down Controller for Portable CPU Power in a QSOP

General Description

The MAX1637 is a synchronous buck switch-mode power-supply controller that generates the CPU supply voltage in battery-powered systems. This device is a bare-bones MAX1636 in a 16-pin QSOP package. It achieves excellent DC-voltage output accuracy from the internal integrator and 2% AC-voltage accuracy including line and load regulation. Other features are low-voltage operation (3.15V) and excellent load-transient response needed by upcoming generations of dynamic-clock CPUs.

Up to 95% efficiency is achieved through synchronous rectification. Efficiency is greater than 80% over a 1000:1 load-current range, which extends battery life in system-suspend or standby mode. Excellent dynamic response corrects output load transients caused by the latest dynamic-clock CPUs within five 300kHz clock cycles. Strong, 1A on-board gate drivers ensure fast external N-channel MOSFET switching.

The MAX1637 features a logic-controlled and synchronizable, fixed-frequency, pulse-width-modulation (PWM) operating mode. This reduces noise and RF interference in sensitive mobile communications and pen-entry applications. Holding $\overline{SKIP}$ high forces fixed-frequency mode, for lowest noise under all load conditions.

For a stand-alone device that includes a 5V linear regulator, refer to the MAX1636 data sheet.

Applications

Notebook Computers

Subnotebook Computers

Handy-Terminals, PDAs

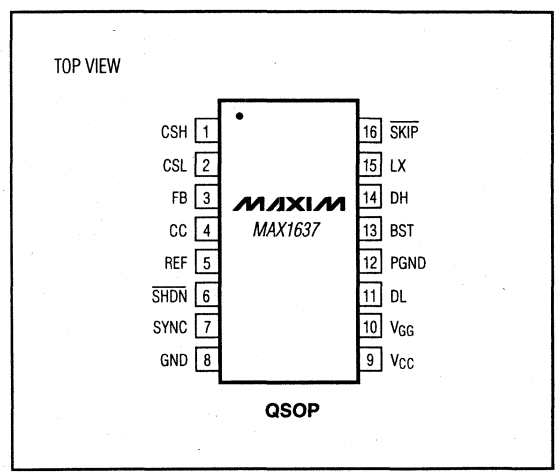
Features

- ♦ **±2% DC Accuracy**
- ♦ **On-Board Integrator Error Amplifier**
- ♦ **Up to 350kHz Adjustable Switching Frequency**
- ♦ **Low-Dropout Operation**
- ♦ **Idle Mode™ Pulse-Skipping Operation**
- ♦ **1A Gate Drivers**
- ♦ **1.1V to 5.5V Adjustable Output Voltage**
- ♦ **100mV, ±20mV Current-Limit Threshold**
- ♦ **3.15V Minimum Chip-Supply Voltage (at V_{CC} pin)**
- ♦ **Internal Digital Soft-Start**
- ♦ **1.1V, ±2% Reference Output**
- ♦ **1µA (typ) Total Shutdown Current**
- ♦ **Output Overvoltage Crowbar Protection**
- ♦ **Output Undervoltage Shutdown**
- ♦ **16-pin QSOP Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1637EEE	-40°C to +85°C	16 QSOP

Pin Configuration



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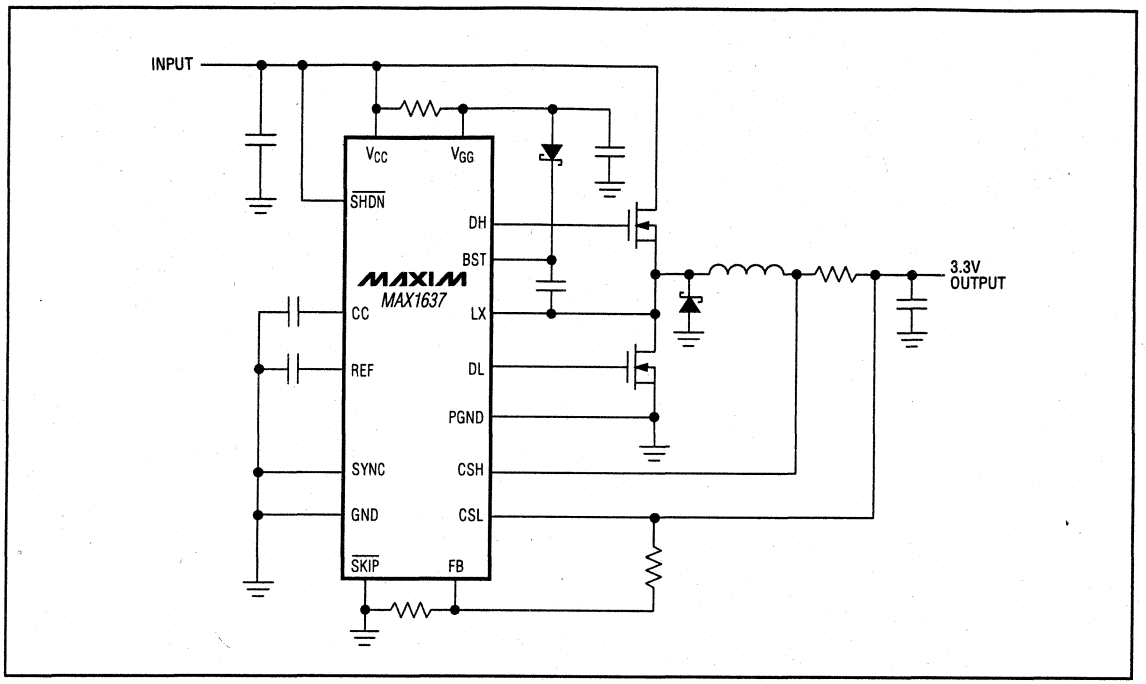
Low-Voltage, Precision, Step-Down Controller for Portable CPU Power in a QSOP

Typical Operating Circuit



ADVANCE INFORMATION
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8/97

MAXIM

High-Speed, Step-Down Controllers with Synchronous Rectification for CPU Power

General Description

The MAX1638/MAX1639 are ultra-high-performance, step-down DC-DC controllers for CPU power in high-end computer systems. Designed for demanding applications in which output voltage precision and good transient response are critical for proper operation, they deliver over 35A from 1.1V to 3.5V with ±1% total accuracy from a +5V ±10% supply. Excellent dynamic response corrects output transients caused by the latest dynamically clocked CPUs. These controllers achieve over 90% efficiency by using synchronous rectification. Flying-capacitor bootstrap circuitry drives inexpensive, external N-channel MOSFETs.

The switching frequency is pin selectable for 300kHz, 600kHZ, or 1MHz. High switching frequencies allow the use of a small, surface-mount inductor and decrease output filter capacitor requirements, reducing board area and system cost.

The MAX1638 is available in a 24-pin SSOP and offers additional features such as a digitally programmable output; adjustable transient response; selectable 0.5%, 1%, or 2% AC load regulation; and gate drive for an instant current-boost MOSFET. The MAX1639 is resistor adjustable and comes in a 16-pin narrow SO package. Other features in both controllers include internal digital soft-start, a power-good output, and a 3.5V ±1% reference output.

Applications

Pentium Pro™, Pentium II™, PowerPC™, Alpha™, and K6™ Systems
Desktop Computers
LAN Servers
Industrial Computers
GTL Bus Termination

Features

- ♦ **Better than ±1% Output Accuracy Over Line and Load**
- ♦ **Intel VRM-Specification Compatible**
- ♦ **90% Efficiency**
- ♦ **Excellent Transient Response**
- ♦ **Over 35A Output Current**
- ♦ **Digitally Programmable Output from 1.3V to 3.5V (MAX1638)**
- ♦ **Resistor-Adjustable Output down to 1.1V (MAX1639)**
- ♦ **Remote Sensing**
- ♦ **Adjustable AC-Loop Gain (MAX1638)**
- ♦ **GlitchCatcher™ Circuit for Fast Load-Transient Response (MAX1638)**
- ♦ **Power-Good (PWROK) Output**
- ♦ **Current-Mode Control**
- ♦ **Digital Soft-Start**
- ♦ **2A Gate-Drive Outputs**
- ♦ **Current-Limited Output**
- ♦ **Switching Frequency to 1MHz**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1638EAG	-40°C to +85°C	24 SSOP
MAX1638EEG	-40°C to +85°C	24 QSOP
MAX1639ESE	-40°C to +85°C	16 Narrow SO

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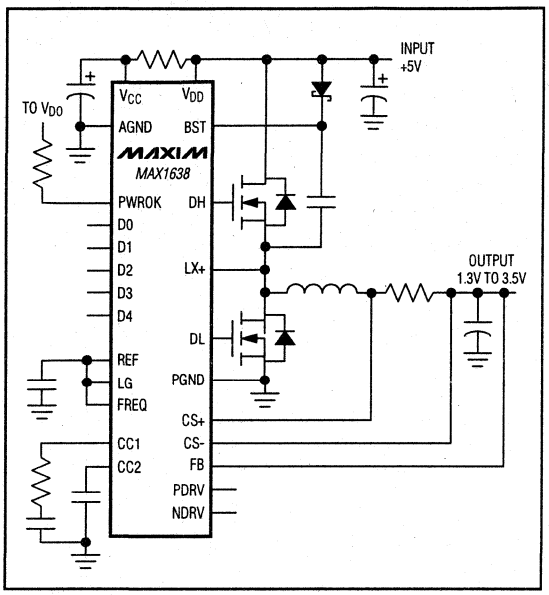
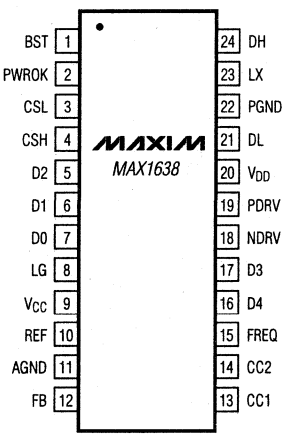
High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Typical Operating Circuit

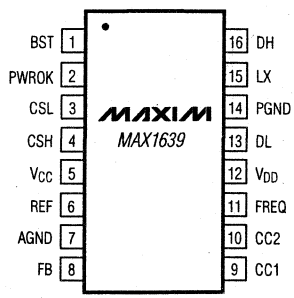


Pin Configuration

TOP VIEW



SSOP



Narrow SO

19-1245; Rev 0; 7/97

EVALUATION KIT AVAILABLE

MAXIM

Adjustable-Output, Switch-Mode Current Sources with Synchronous Rectifier

General Description

The MAX1640/MAX1641 CMOS, adjustable-output, switch-mode current sources operate from a +5.5V to +26V input, and are ideal for microprocessor-controlled battery chargers. Charging current, maximum output voltage, and pulse-trickle charge are programmed with external resistors. Programming the off-time modifies the switching frequency, suppressing undesirable harmonics in noise-sensitive circuits. The MAX1640's high-side current sensing allows the load to connect directly to ground, eliminating ground-potential errors. The MAX1641 incorporates a low-side current sense.

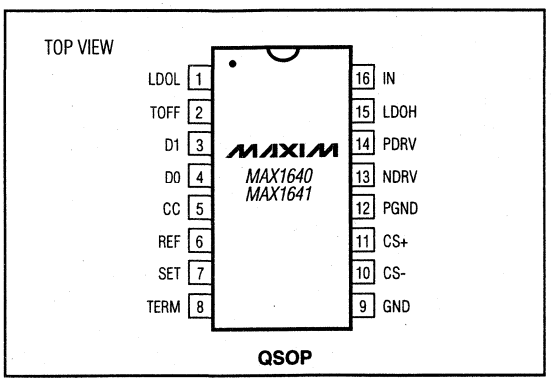
The MAX1640/MAX1641 step-down pulse-width-modulation (PWM) controllers use an external P-channel MOSFET switch and an optional, external N-channel MOSFET synchronous rectifier for increased efficiency. An internal low-dropout linear regulator provides power for the internal reference and circuitry as well as the gate drive for the N-channel synchronous rectifier.

The MAX1640/MAX1641 are available in space-saving, 16-pin narrow QSOP packages.

Applications

- Battery-Powered Equipment
  - Laptop, Notebook, and Palmtop Computers
  - Handy Terminals
- Portable Consumer Products
  - Cordless Phones
  - Cellular Phones
  - PCS Phones
- Backup Battery Charger

Pin Configuration



Features

- ♦ **95% Efficiency**
- ♦ **+5.5V to +26V Input Supply Range**
- ♦ **2V to 24V Adjustable-Output Voltage Range**
- ♦ **100% Maximum Duty Cycle (Low Dropout)**
- ♦ **Up to 500kHz PWM Operation**
- ♦ **Optional Synchronous Rectifier**
- ♦ **16-Pin QSOP Package**
- ♦ **Current-Sense Accuracy: 2% (MAX1641)**
  5.3% (MAX1640)

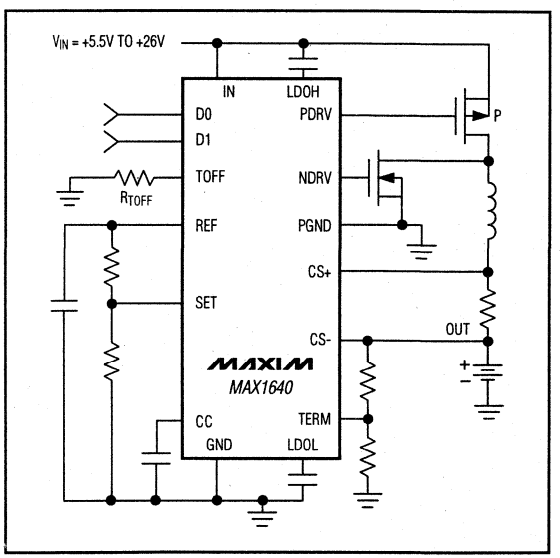
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1640C/D	0°C to +70°C	Dice*
MAX1640EEE	-40°C to +85°C	16 QSOP
MAX1641C/D	0°C to +70°C	Dice*
MAX1641EEE	-40°C to +85°C	16 QSOP

Dice are specified at T_A = +25°C, DC parameters only.

4

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-0.3V to +28V
LDOH to IN .....+0.3V to -6V
LDOL to GND .....-0.3V to +6V
PDRV to GND ..... (V_{LDOH} - 0.3V) to (V_{IN} + 0.3V)
NDRV to GND .....-0.3V to (V_{LDOL} + 0.3V)
TOFF, REF, SET, TERM, CC to GND .....-0.3V to (V_{LDOL} + 0.3V)
D0, D1 to GND .....-0.3V to +6V
CS+, CS- to GND .....-0.3V to +28V
PGND to GND .....±0.3V
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.30mW/°C above +70°C) 667mW
Operating Temperature Range
MAX164_EEE .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 2, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}			5.5		26	V
Linear-Regulator Output Voltage, V_{IN} Referenced	V_{LDOH}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA		V_{IN} - 5.5	V_{IN} - 5.0	V_{IN} - 4.5	V
Linear-Regulator Output Voltage, Ground Referenced	V_{LDOL}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA		4.5	5.0	5.5	V
Full-Scale Current-Sense Threshold		MAX1640		142	150	158	mV
		MAX1641		147	150	153	
Quarter-Scale Current-Sense Threshold		MAX1640		36	42	48	mV
		MAX1641		34	37.5	41	
Current-Sense Line Regulation		V_{IN} = V_{OUT} + 0.5V to 26V			0.03		%/V
Output Current Compliance		V_{OUT} = 2V to 24V	MAX1640		0.1	0.4	%/V
			MAX1641		0.1		
Quiescent V_{IN} Supply Current		D0 or D1 = high			2	4	mA
		D0 = D1 = low (off mode)			500		µA
Output Current in Off Mode		D0 = D1 = low				1	µA
V_{LDOL} Undervoltage Lockout				4.05	4.20	4.35	V
Reference Voltage	V_{REF}			1.96	2.00	2.04	V
Reference Load Regulation		I_{REF} = 0 to 50µA			4	10	mV
V_{SET} Input Current						1	µA
FET Drive Output Resistance		PFET and NFET drive				12	Ω
Off-Time Range				1		10	µs
Off-Time Accuracy		R_{TOFF} = 62kΩ		1.7	2.2	2.7	µs
Pulse-Trickle Mode Duty-Cycle Period		D0 = low, D1 = high, R_{TOFF} = 100kΩ		27	33	40	ms
Pulse-Trickle Mode Duty Cycle (Note 1)		D0 = low, D1 = high, R_{TOFF} = 100kΩ			12.5		%

Note 1: This ratio is generated by a 1:8 clock divider and is not an error source for current calculations.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 2, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM Maximum Duty Cycle			100			%
Input Low Voltage	V_{IL}	D0, D1			0.8	V
Input High Voltage	V_{IH}	D0, D1	2.4			V
Input Leakage Current	I_{IN}	D0, D1			±1	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = +12V, V_{OUT} = 6V, Circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted.)

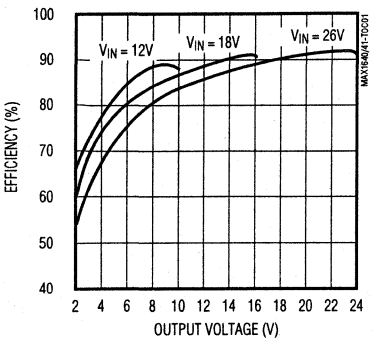
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		5.5		26	V
Linear-Regulator Output Voltage, V_{IN} Referenced	V_{LDOH}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA	V_{IN} - 5.5		V_{IN} - 4.5	V
Linear-Regulator Output Voltage, Ground Referenced	V_{LDOL}	V_{IN} = 5.5V to 26V, I_{LOAD} = 0 to 20mA	4.5		5.5	V
Full-Scale Current-Sense Threshold		MAX1640	141		159	mV
		MAX1641	146		154	
Quarter-Scale Current-Sense Threshold		MAX1640	34		48	mV
		MAX1641	33		42	
Output Current Compliance		V_{OUT} = 2V to 24V (MAX1640)			0.4	%/V
Quiescent V_{IN} Supply Current		D0 or D1 = high			4	mA
Output Current in Off Mode		D0 = D1 = low			1	µA
V_{LDOL} Undervoltage Lockout			4.0		4.4	V
Reference Voltage	V_{REF}		1.94		2.06	V
Reference Load Regulation		I_{REF} = 0 to 50µA			10	mV
V_{SET} Input Current					1	µA
FET Drive Output Resistance					12	Ω
Off-Time Range			1.5		8	µs
Off-Time Accuracy		R_{TOFF} = 62kΩ	1.5		2.5	µs
Pulse-Trickle Mode Duty-Cycle Period		D0 = low, D1 = high, R_{TOFF} = 50kΩ	25		42	ms
PWM Maximum Duty Cycle			100			%
Input Low Voltage	V_{IL}	D0, D1			0.8	V
Input High Voltage	V_{IH}	D0, D1	2.4			V
Input Leakage Current	I_{IN}	D0, D1			±1	µA

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

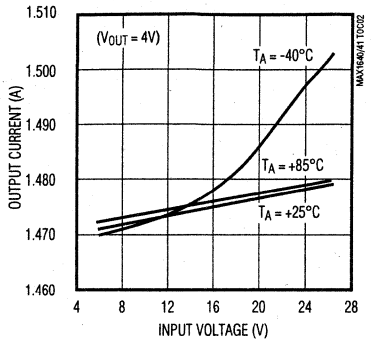
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

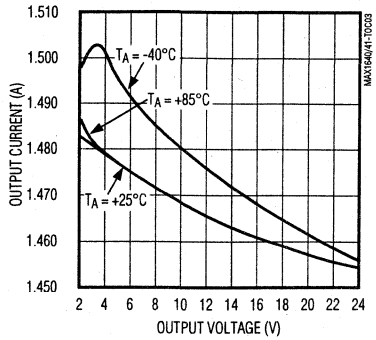
EFFICIENCY vs. OUTPUT VOLTAGE



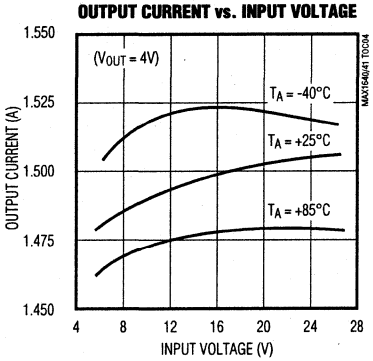
MAX1640
OUTPUT CURRENT vs. INPUT VOLTAGE



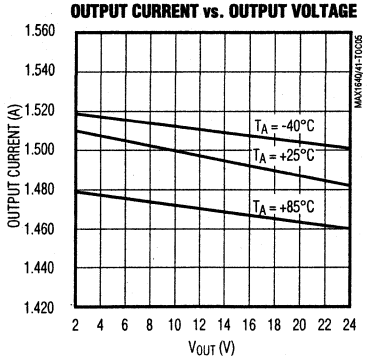
MAX1640
OUTPUT CURRENT vs. OUTPUT VOLTAGE



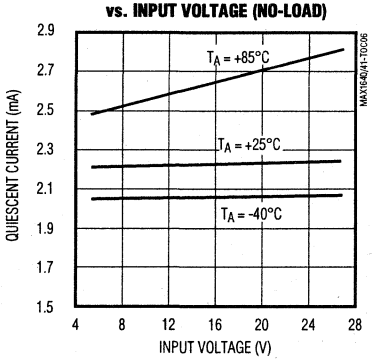
MAX1641
OUTPUT CURRENT vs. INPUT VOLTAGE



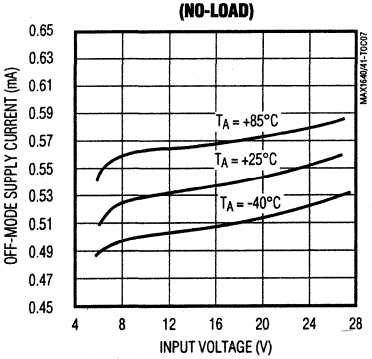
MAX1641
OUTPUT CURRENT vs. OUTPUT VOLTAGE



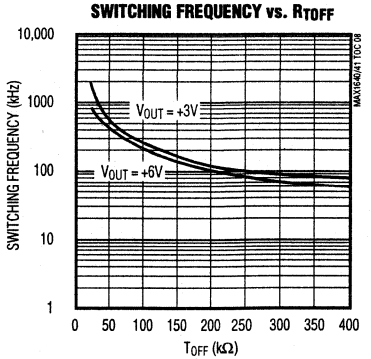
QUIESCENT CURRENT
vs. INPUT VOLTAGE (NO-LOAD)



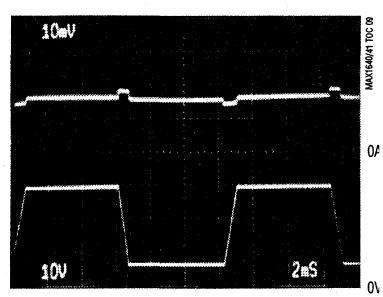
OFF-MODE SUPPLY CURRENT
(NO-LOAD)



SWITCHING FREQUENCY vs. R_{TOFF}



LINE-TRANSIENT RESPONSE



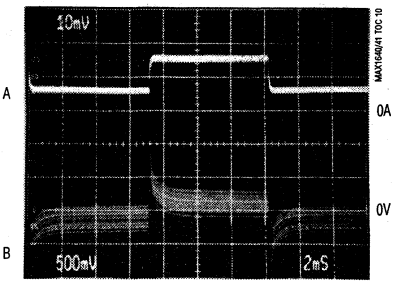
VLOAD = 3V 2ms/div
A: OUTPUT CURRENT, D1 = D0 = 1 1A/div
B: INPUT VOLTAGE, 10V/div

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

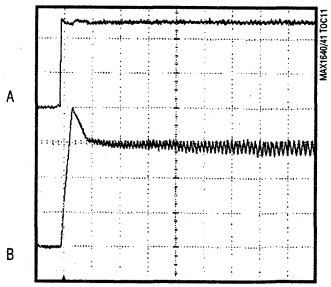
CURRENT-MODE CHANGE RESPONSE TIME



2ms/div

V_{IN} = 12V, V_{SET} = 1V, R_{LOAD} = 4Ω, NO OUTPUT CAPACITOR
A: OUTPUT CURRENT, D0 = D1 = 0 1A/div
B: LOAD VOLTAGE, AC coupled, 500mV/div

EXITING OFF MODE



20µs/div

V_{IN} = 12V, R_{LOAD} = 4Ω
A: D0 = D1 = 1 2V/div
B: OUTPUT CURRENT, 0.5A/div

Pin Description

PIN	NAME	FUNCTION
1	LDOL	Internal, Ground-Referenced Low-Dropout Linear Regulator Output. Bypass with a 0.1µF capacitor in parallel with a 4.7µF capacitor to GND.
2	TOFF	Off-Time Select Input. A resistor (R_{TOFF}) connected from this pin to GND programs the off-time for the hysteretic PWM step-down converter. This resistor also sets the period in duty-cycle mode. See *Duty-Cycle Mode and Programming the Off-Time.*
3, 4	D1, D0	Digital Inputs. Select mode of operation (Table 1).
5	CC	Constant-Current Loop Compensation Input. Bypass with a 0.01µF capacitor to GND.
6	REF	Reference Voltage Output (V_{REF} = 2V). Bypass with a 0.1µF capacitor to GND.
7	SET	Current Select Input. Program the desired current level by applying a voltage at SET between 0V and V_{REF}, ($I = V_{SET} / 13.3R_{SENSE}$). See Figure 3.
8	TERM	Maximum Output Voltage Termination Input. When V_{TERM} exceeds the reference voltage, the comparator resets the internal PWM latch, shutting off the external P-channel FET.
9	GND	Ground
10	CS-	Negative Current-Sense Comparator Input
11	CS+	Positive Current-Sense Comparator Input
12	PGND	High-Current Ground Return for the output drivers
13	NDRV	Gate Drive for an optional N-channel FET synchronous rectifier
14	PDRV	Gate Drive for the P-channel FET
15	LDOH	Internal, Input-Referenced Low-Dropout Linear Regulator Output. Bypass with a 0.33µF capacitor to IN.
16	IN	Power-Supply Input. Input of the internal, low-dropout linear regulators.

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

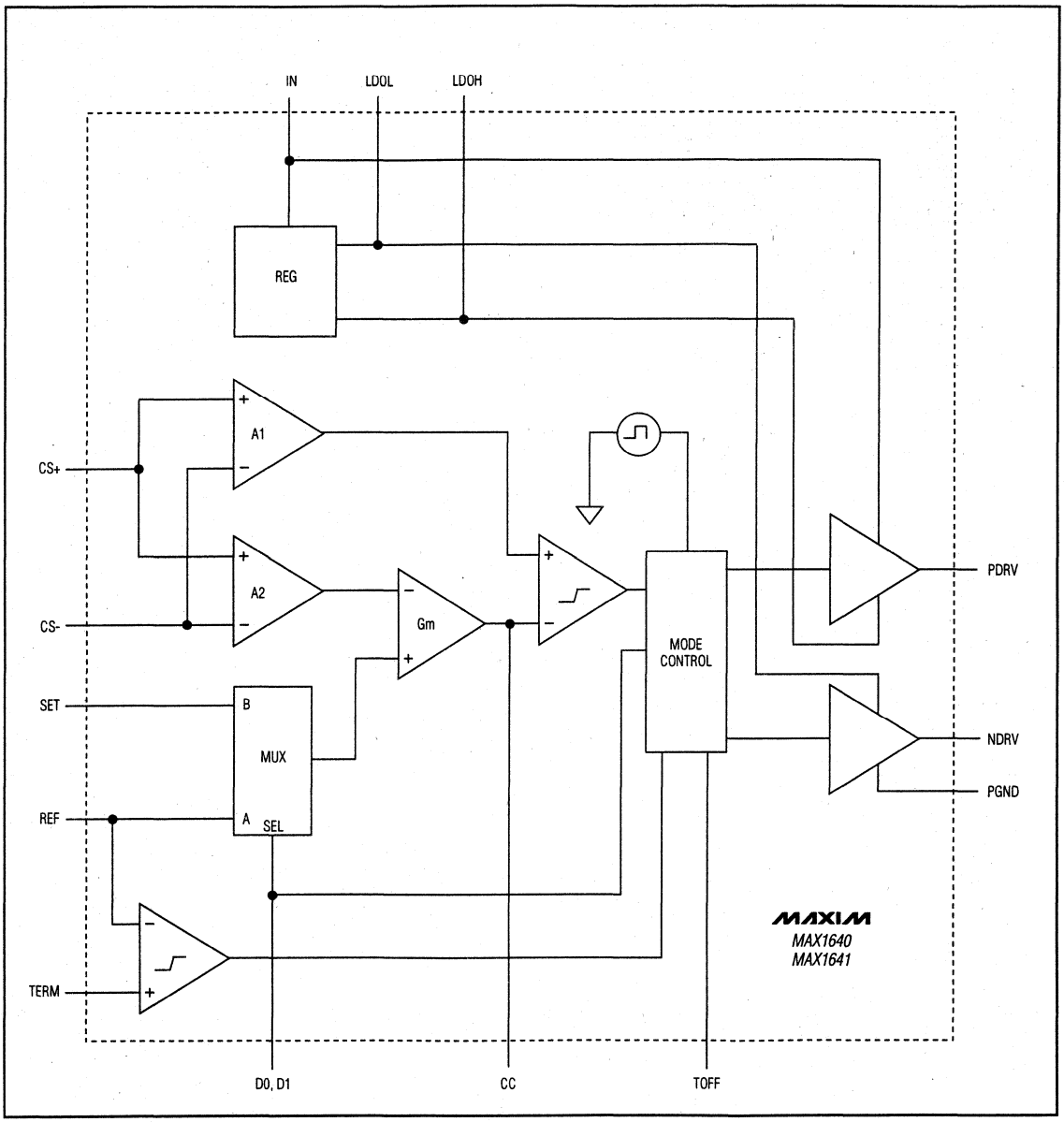


Figure 1. MAX1640/MAX1641 Functional Diagram

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

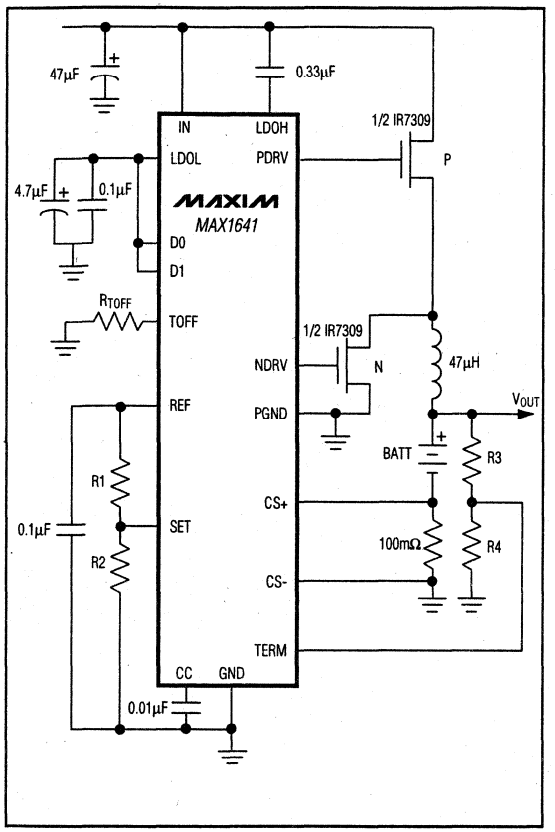


Figure 2a. Standard Application Circuit

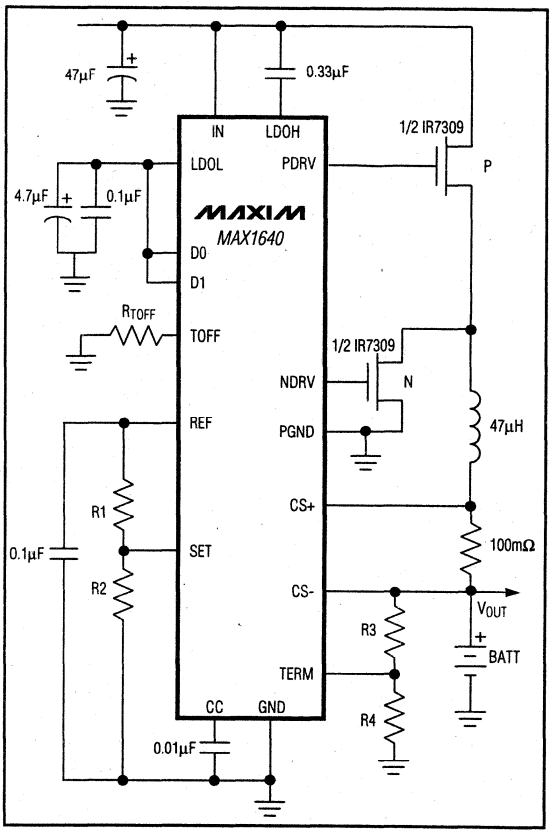


Figure 2b. Standard Application Circuit

Detailed Description

The MAX1640/MAX1641 switch-mode current sources utilize a hysteretic, current-mode, step-down pulse-width-modulation (PWM) topology with constant off-time. Internal comparators control the switching mechanism. These comparators monitor the current through a sense resistor (R_{SENSE}) and the voltage at TERM. When inductor current reaches the current limit [(V_{CS+} - V_{CS-}) / R_{SENSE}], the P-channel FET turns off and the N-channel FET synchronous rectifier turns on. Inductor energy is delivered to the load as the current ramps down. This ramp rate depends on R_{TOFF} and inductor values. When off-time expires, the P-channel FET turns back on and the N-channel FET turns off.

Two digital inputs, D0 and D1, select between four possible current levels (Table 1). In pulse-trickle mode, the part operates for 12.5% of the period set by R_{TOFF}, resulting in a lower current for pulse-trickle charging. Figure 1 is the MAX1640/MAX1641 functional diagram. Figure 2 shows the standard application circuits.

Charge Mode: Programming the Output Currents

The sense resistor, R_{SENSE}, sets two charging current levels. Choose between these two levels by holding D0 high, and toggling D1 either high or low (Table 1). The fast-charge current level equals V_{CS} / R_{SENSE} where V_{CS} is the full-scale current-sense voltage of 150mV. Alternatively, calculate this current by V_{REF} / (13.3R_{SENSE}). The top-off current equals V_{SET} / (13.3R_{SENSE}). A resistor-divider from REF to GND programs the voltage at SET (Figure 3).

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

The voltage at SET is given by:

$$R1 = R2 (V_{REF} / V_{SET} - 1); 10k\Omega < R2 < 300k\Omega$$

where V_{REF} = 2V and V_{SET} is proportional to the desired output current level.

Table 1. Selecting Output Current Levels

D1	D0	MODE	OUTPUT CURRENT (A)
0	0	OFF	0
0	1	Top-Off	$V_{SET} / (13.3R_{SENSE})$
1	0	Pulse-Trickle	$V_{SET} / (13.3R_{SENSE})$ 12.5% duty cycle
1	1	Fast Charge	$V_{SET} / (13.3R_{SENSE})$

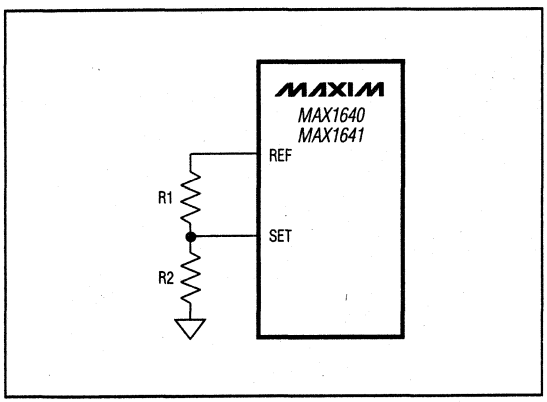


Figure 3. Adjusting the Output Current Level

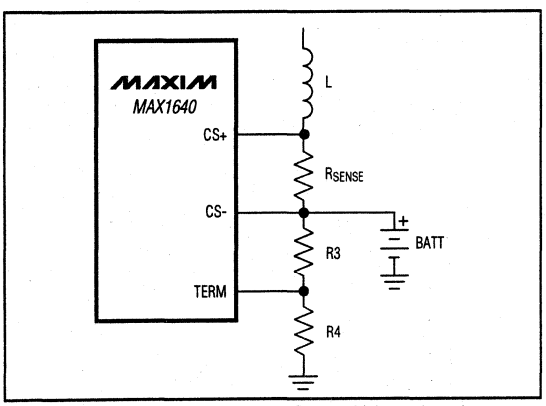


Figure 4a. Setting the Maximum Output Voltage Level

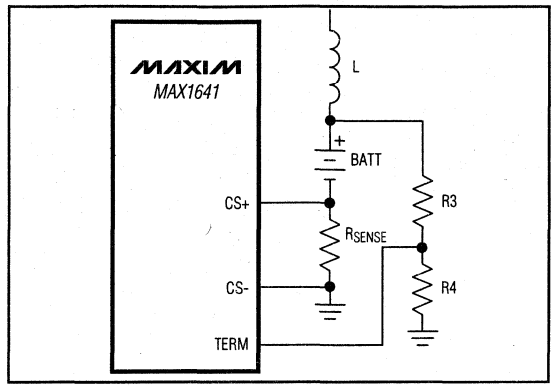


Figure 4b. Setting the Maximum Output Voltage Level

The MAX1640/MAX1641 are specified for V_{SET} between 0V and V_{REF}. For $V_{SET} > V_{REF}$, output current increases linearly (with reduced accuracy) until it clamps at $V_{SET} \approx 4V$.

Pulse-Trickle Mode: Selecting the Pulse-Trickle Current

Pulling D0 low and D1 high selects pulse-trickle mode. This current equals $V_{SET} / (13.3R_{SENSE})$ and remains on for 12.5% of the period set by R_{TOFF}. Pulse-trickle current maintains full charge across the battery and can slowly charge a cold battery before fast charging commences.

$$PERIOD = 3.2 \times 10^{-7} \times R_{TOFF}(sec)$$

Off Mode: Turning Off the Output Current

Pulling D0 and D1 low turns off the P-channel FET and hence the output current flow. This mode also controls end of charge and protects the battery against excessive temperatures.

Setting the Maximum Output Voltage Level

The maximum output voltage should be programmed to a level higher than the output/battery voltage ($I_{LOAD} \times R_{LOAD}$). An external resistor-divider between the output and ground (Figure 4) sets the voltage at TERM. Once the voltage at TERM exceeds the reference, the internal comparator turns off the P-channel FET, terminating current flow. Select R4 in the 10kΩ to 500kΩ range. R3 is given by:

$$R3 = R4 (V_{OUT} / V_{TERM}) - 1$$

where V_{TERM} = 2V and V_{OUT} is the desired output voltage.

Programming the Off-Time

When programming the off-time, consider such factors as maximum inductor current ripple, maximum output voltage, inductor value, and inductor current rating. The output current ripple is less than the inductor current ripple and depends heavily on the output capacitor's size.

Perform the following steps to program the off-time:

1) Select the maximum output current ripple. I_R(A)
2) Select the maximum output voltage. V_{OUT}(MAX)(V)
3) Calculate the inductor value range as follows:

   $L_{MIN} = (V_{OUTMAX} \times 1\mu s) / I_R$

   $L_{MAX} = (V_{OUTMAX} \times 10\mu s) / I_R$
4) Select an inductor value in this range.
5) Calculate t_{OFF} as follows:

$$t_{OFF} = \frac{L \times I_R}{V_{OUTMAX}}$$

6) Program t_{OFF} by selecting R_{TOFF} from:

$$R_{TOFF} = (29.3 \times 10^9) \times t_{OFF}$$

7) Calculate the switching frequency by:

$$fs = 1 / (t_{ON} + t_{OFF})$$

   where $t_{ON} = (I_R \times L) / (V_{IN} - V_{OUT})$ and $I_R = (V_{OUT} \times t_{OFF}) / L$. L is the inductor value, V_{IN} is the input voltage, V_{OUT} is the output voltage, and I_R is the output peak-to-peak current ripple.

Note that R_{TOFF} sets both the off-time and the pulse-trickle charge period.

Reference

The on-chip reference is laser trimmed for a precise 2V at REF. REF can source no more than 50µA. Bypass REF with a 0.1µF capacitor to ground.

Constant-Current Loop: AC Loop Compensation

The constant-current loop's output is brought out at CC. To reduce noise due to variations in switching currents, bypass CC with a 1nF to 100nF capacitor to ground. A large capacitor value maintains a constant average output current but slows the loop response to changes in switching current. A small capacitor value speeds up the loop response to changes in switching current, generating increased ripple at the output. Select C_{CC} to optimize the ripple vs. loop response.

Synchronous Rectification

Synchronous rectification reduces conduction losses in the rectifier by shunting the Schottky diode with a low-resistance MOSFET switch. In turn, efficiency increases by about 3% to 5% at heavy loads. To prevent cross-conduction or "shoot-through," the synchronous rectifier turns on shortly after the P-channel power MOSFET turns off. The synchronous rectifier remains off for 90% of the off-time. In low-cost designs, the synchronous rectifier FET may be replaced by a Schottky diode.

Table 2. Component Manufacturers

COMPONENT	MANUFACTURER	
Inductor	Sumida	CDRH125 series
	Coilcraft	D03316P series
	Coiltronics	UP2 series
MOSFETs	International Rectifier	IRF7309
	Siliconix	S14539DY
Sense Resistor	Dale	WSL-2010 series
	IRC	LR2010-01 series
Capacitors	AVX	TPS series
	Sprague	595D series
Rectifier	Motorola	MBAR5340t3
		IN5817-IN5822
	Nihon	NSQ03A04

Component Selection

External Switching Transistors

The MAX1640/MAX1641 drive an enhancement-mode P-channel MOSFET and a synchronous-rectifier N-channel MOSFET (Table 2).

When selecting a P-channel FET, some important parameters to consider are on-resistance ($r_{DS(ON)}$), maximum drain-to-source voltage (V_{DS} max), maximum gate-to-source voltage (V_{GS} max), and minimum threshold voltage (V_{TH} min).

In high-current applications, MOSFET package power dissipation often becomes a dominant design factor. I^2R power losses are the greatest heat contributor for both high-side and low-side MOSFETs. Switching losses affect the upper MOSFET only (P-channel), since the Schottky rectifier or the N-FET body diode clamps the switching node before the synchronous rectifier turns on.

Rectifier Diode

If an N-channel MOSFET synchronous rectifier is not used, a Schottky rectifier is needed. The MAX1640/

Adjustable-Output, Switch-Mode Current Source with Synchronous Rectifier

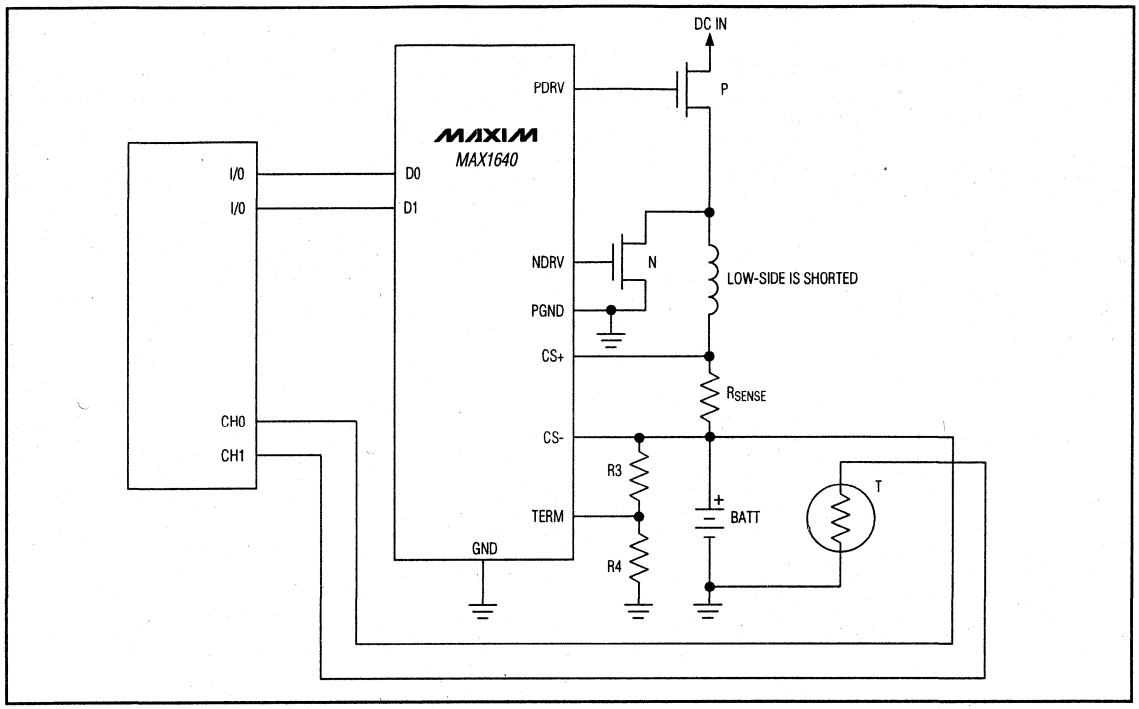


Figure 5. Microcontroller Battery Charger

MAX1641's high switching frequency demands a high-speed rectifier (Table 2). Schottky diodes such as the 1N5817–1N5822 are recommended. Make sure the Schottky diode's average current rating exceeds the peak current limit and that its breakdown voltage exceeds the output voltage (V_{OUT}). For high-temperature applications, Schottky diodes may be inadequate due to their high leakage current; high-speed silicon diodes such as the MUR105 or EC11FS1 can be used instead. At heavy loads and high temperatures, the benefits of a Schottky diode's low forward voltage may outweigh the disadvantage of high leakage current. If the application uses an N-channel MOSFET synchronous rectifier, a parallel Schottky diode is usually unnecessary except with very high charge current (> 3 amps). Best efficiency is achieved with both an N-channel MOSFET and a Schottky diode.

Inductor Value

Refer to the section *Programming the Off-Time* to select the proper inductor value. There is a trade-off between inductor value, off-time, output current ripple, and switching frequency.

Applications Information

All-Purpose Microcontroller Battery Charger: NiCd, NiMH

In applications where a microcontroller is available, the MAX1640/MAX1641 can be used as a low-cost battery charger (Figure 5). The controller takes over fast charge, pulse-trickle charge, charge termination, and other smart functions. By monitoring the output voltage at V_{OUT}, the controller initiates fast charge (set D0 and D1 high), terminates fast charge and initiates top-off (set D0 high and D1 low), enters trickle charge (set D0 low and D1 high), or shuts off and terminates current flow (set D0 and D1 low).

Layout and Grounding

Due to high current levels and fast switching waveforms, proper PC board layout is essential. High-current ground paths should be connected in a star

configuration to PGND. These traces should be wide to reduce resistance and as short as possible to reduce stray inductance. All low-current ground paths should be connected to GND. Place the input bypass capacitor as close as possible to the IN pin. See MAX1640 EV kit for layout example.

Chip Information

TRANSISTOR COUNT: 1233

19-1183; Rev 0; 6/97

EVALUATION KIT AVAILABLE

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

General Description

The MAX1642/MAX1643 are high-efficiency, low-voltage, step-up DC-DC converters intended for devices powered by a single alkaline cell. They feature low quiescent supply currents and are supplied in the ultra-small µMAX package, which is only 1.1mm high. The guaranteed start-up voltage is 0.88V.

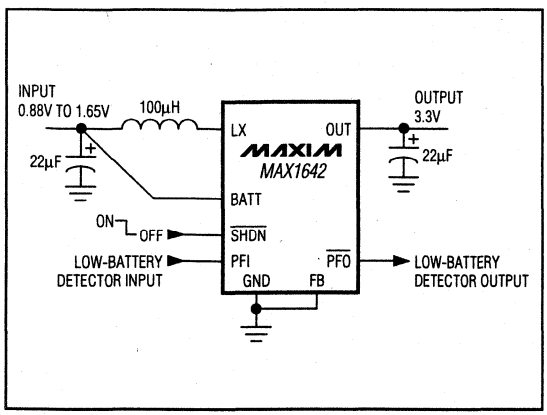
Each device consists of an internal 1Ω, N-channel MOSFET power switch; a built-in synchronous rectifier that acts as the catch diode; an oscillator; a reference; and pulse-frequency-modulation (PFM) control circuitry. Both devices feature an independent undervoltage comparator (PFI/$\overline{PFO}$). The MAX1642 also includes a 2µA logic-controlled shutdown mode. The MAX1643 offers a dedicated low-battery detector ($\overline{BATTLO}$) in lieu of shutdown.

The output voltage for each device is preset to 3.3V ±4%, or can be adjusted from +2V to +5.2V using only two resistors.

Applications

Pagers
Remote Controls
Pointing Devices
Personal Medical Monitors
Single-Cell Battery-Powered Devices

Typical Operating Circuit



Features

- ♦ **Built-In Synchronous Rectifier**
- ♦ **0.88V Guaranteed Start-Up**
- ♦ **Ultra-Small µMAX Package: 1.1mm High**
- ♦ **83% Efficiency**
- ♦ **4µA Quiescent Supply Current into BATT Pin**
- ♦ **2µA Logic-Controlled Shutdown (MAX1642)**
- ♦ **Two Undervoltage Detectors (MAX1643)**
- ♦ **2V to 5.2V Output Range**
- ♦ **20mA Output Current at 1.2V Input**
- ♦ **Reverse Battery Protection**

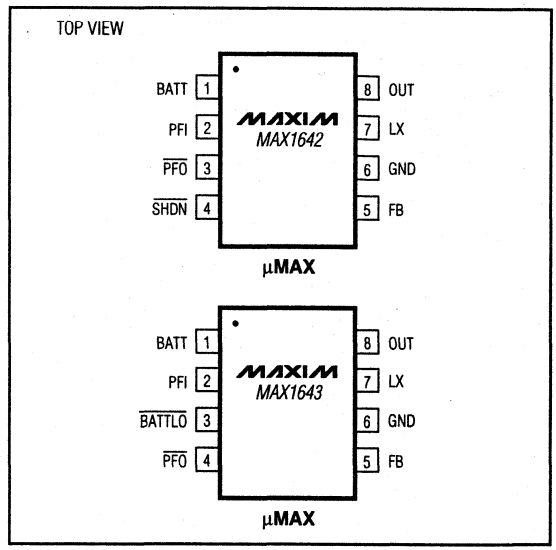
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1642C/D	0°C to +70°C	Dice*
MAX1642EUA	-40°C to +85°C	8 µMAX
MAX1643C/D	0°C to +70°C	Dice*
MAX1643EUA	-40°C to +85°C	8 µMAX

*Dice are tested at T_A = +25°C.

Note: To order these devices shipped in tape and reel, add a -T to the part number.

Pin Configurations



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For small orders, phone 408-737-7600 ext. 3468.

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

ABSOLUTE MAXIMUM RATINGS

BATT to GND .....-0.3V to 6.0V
BATT Forward Current 0.5A
OUT to GND .....-0.3V to 6.0V
OUT, LX Current 1A
LX to GND .....-0.3V to 6.0V
$\overline{SHDN}$, FB, $\overline{BATTLO}$, $\overline{PFO}$ to GND .....-0.3V to 6.0V
PFI to GND .....-0.3V to V_{BATT}
Reverse Battery Current (T_A = +25°C) (Note 1) 220mA

Continuous Power Dissipation
μMAX (derate 4.1mW/°C above 70°C) 330mW
Operating Temperature Range
MAX1642EUA/MAX1643EUA .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: The reverse battery current is measured from the *Typical Operating Circuit's* input terminal to GND when the battery is connected backward. A reverse current of 220mA will not exceed package dissipation limits but, if left for an extended time (more than 10 minutes), may degrade performance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Operating Input Voltage	$V_{BATT(MIN)}$			0.7		V
Maximum Operating Input Voltage					1.65	V
Start-Up Voltage (Note 2)		R_L = 3kΩ, T_A = +25°C	0.88			V
Start-Up Voltage Tempco				-2		mV/°C
Output Voltage	V_{OUT}	V_{FB} < 0.1V	3.16	3.30	3.44	V
Output Voltage Range		External feedback	2.0		5.2	V
FB Set Voltage	V_{FB}	External feedback	1.18	1.225	1.27	V
N-Channel On-Resistance		V_{OUT} = 3.3V		1	1.5	Ω
P-Channel On-Resistance		V_{OUT} = 3.3V		1.5	2.2	Ω
P-Channel Catch-Diode Voltage		I_{DIODE} = 100mA, P-channel switch off		0.8		V
On-Time Constant	K	0.9V < V_{BATT} < 1.5V (t_{ON} = K / V_{BATT})	17	25	35	V-μs
Off-Time Tracking Ratio (Note 3)	RATIO	0.9V < V_{BATT} < 1.5V, V_{OUT} = 3.3V	1		1.5	
Quiescent Current into OUT	I_{QOUT}	V_{OUT} = 3.5V		11	18	μA
Quiescent Current into BATT	I_{QBATT}			4	6.5	μA
Shutdown Current into OUT	$I_{SHDN,OUT}$	V_{OUT} = 3.5V (MAX1642)		0.1	1	μA
Shutdown Current into BATT	$I_{SHDN,BATT}$	V_{BATT} = 1.0V (MAX1642)		2	3.5	μA
Efficiency	η	I_{LOAD} = 20mA		80		%
FB Input Current		V_{FB} = 1.3V			10	nA
PFI Trip Voltage		Falling PFI, hysteresis = 1%	590	614	632	mV
PFI Input Current		V_{PFI} = 650mV			10	nA
$\overline{PFO}$, $\overline{BATTLO}$ Low Output Voltage	V_{OL}	V_{PFI} = 0V, V_{OUT} = 3.3V, I_{SINK} = 1mA			0.4	V
$\overline{PFO}$, $\overline{BATTLO}$ Leakage Current		V_{PFI} = 650mV, $V_{\overline{PFO}}$ = 6V			1	μA
$\overline{BATTLO}$ Trip Voltage		V_{OUT} = 3.3V, hysteresis = 2% (MAX1643)	0.96	1.0	1.04	V
$\overline{SHDN}$ Input Low Voltage	V_{IL}	% of V_{BATT} (MAX1642)			20	%
$\overline{SHDN}$ Input High Voltage	V_{IH}	% of V_{BATT} (MAX1642)	80			%
$\overline{SHDN}$ Input Current		(MAX1642)			10	nA

ELECTRICAL CHARACTERISTICS

(V_{BATT} = $V_{\overline{SHDN}}$ = 1.3V, I_{LOAD} = 0mA, FB = GND, **T_A = -40°C to +85°C,** unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output Voltage	V_{OUT}	V_{FB} < 0.1V	2.99	3.56	V
FB Set Voltage	V_{FB}	External feedback	1.11	1.32	V
N-Channel On-Resistance		V_{OUT} = 3.3V		1.5	Ω
P-Channel On-Resistance		V_{OUT} = 3.3V		2.2	Ω
On-Time Constant	K	0.9V < V_{BATT} < 1.5V (t_{ON} = K / V_{BATT})	12.4	38.2	V-µs
Quiescent Current into OUT	I_{QOUT}	V_{OUT} = 3.5V		18	µA
Quiescent Current into BATT	I_{QBATT}			6.5	µA
Shutdown Current into OUT	$I_{SHDN,OUT}$	V_{OUT} = 3.5V (MAX1642)		1	µA
Shutdown Current into BATT	$I_{SHDN,BATT}$	V_{BATT} = 1.0V (MAX1642)		3.5	µA
PFI Trip Voltage		Falling PFI, hysteresis = 1%	550	662	mV
$\overline{BATTLO}$ Trip Voltage		Falling V_{BATT}, V_{OUT} = 3.3V, hysteresis = 2% (MAX1643)	0.93	1.06	V

Note 2: Start-up guaranteed by correlation to measurements of device parameters (i.e., switch on-resistance, on-times, off-times, and output voltage trip points).

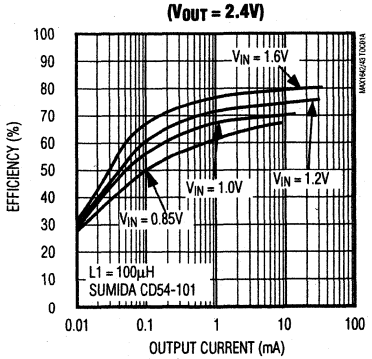
Note 3: $t_{OFF} = \left[\frac{t_{ON} \times V_{BATT}}{V_{OUT} - V_{BATT}}\right]$ x RATIO. This guarantees discontinuous conduction.

Note 4: Specifications to -40°C are guaranteed by design, not production tested.

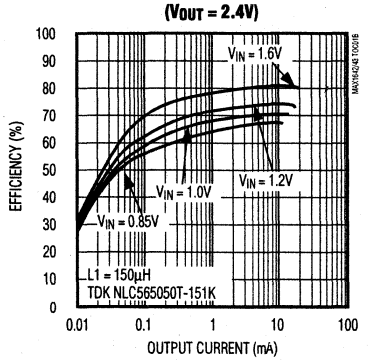
Typical Operating Characteristics

(Circuit of Figure 4, V_{BATT} = 1.2V, R1 + R2 = 1MΩ, T_A = +25°C, unless otherwise noted.)

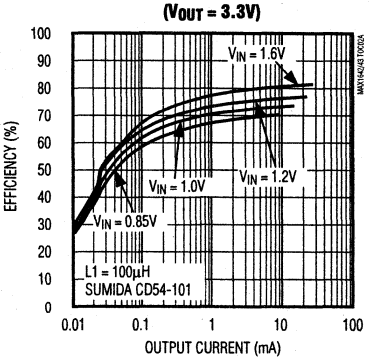
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 2.4V)



EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 2.4V)



EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)

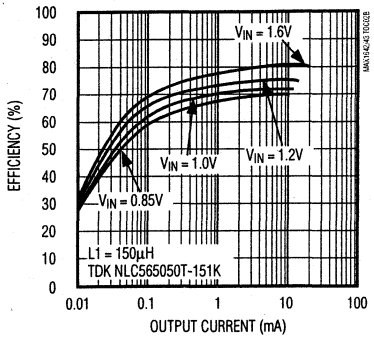


High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

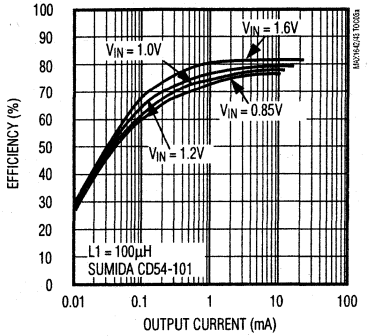
Typical Operating Characteristics (continued)

(Circuit of Figure 4, V_{BATT} = 1.2V, R1 + R2 = 1MΩ, T_A = +25°C, unless otherwise noted.)

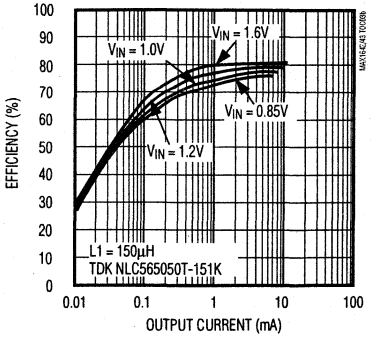
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 3.3V)



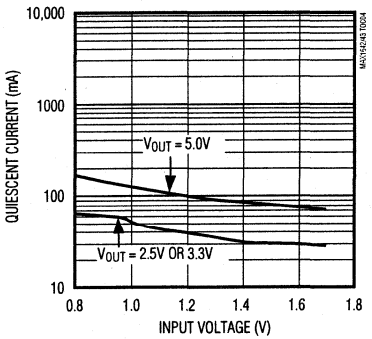
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5.0V)



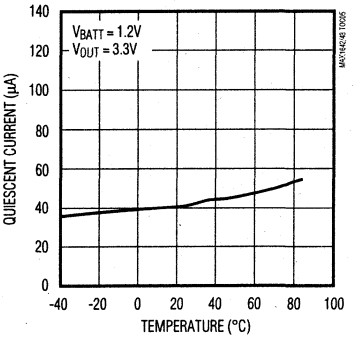
EFFICIENCY vs. OUTPUT CURRENT (V_{OUT} = 5.0V)



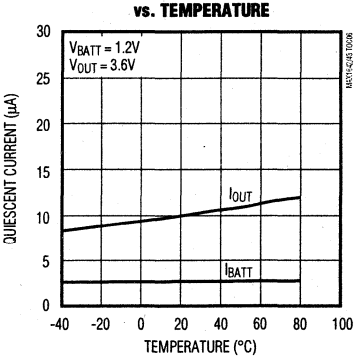
NO-LOAD BATTERY CURRENT vs. INPUT VOLTAGE



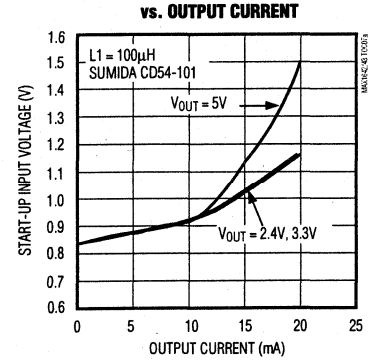
NO-LOAD BATTERY CURRENT vs. TEMPERATURE



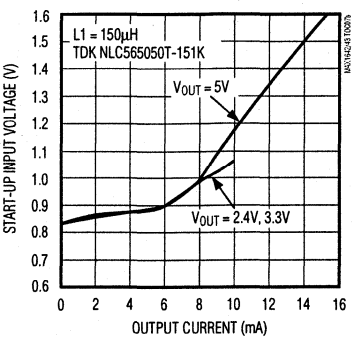
BATT AND OUT PIN QUIESCENT CURRENTS vs. TEMPERATURE



MINIMUM START-UP INPUT VOLTAGE vs. OUTPUT CURRENT



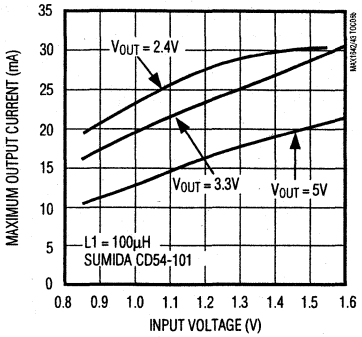
MINIMUM START-UP INPUT VOLTAGE vs. OUTPUT CURRENT



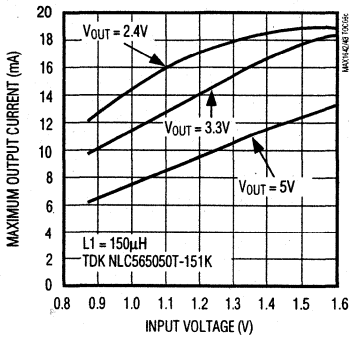
Typical Operating Characteristics (continued)

(Circuit of Figure 4, V_{BATT} = 1.2V, R1 + R2 = 1MΩ, T_A = +25°C, unless otherwise noted.)

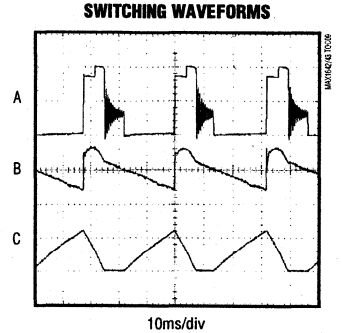
MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE

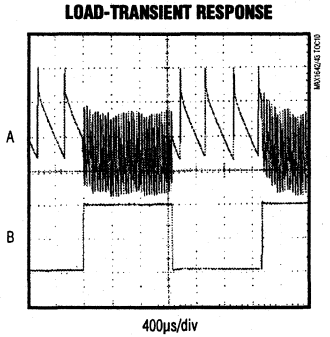


SWITCHING WAVEFORMS



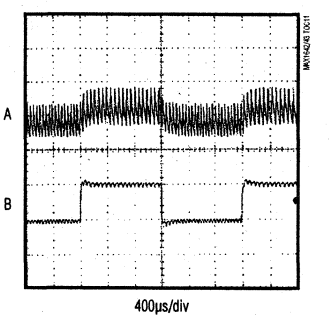
V_{OUT} = 3.3V, V_{IN} = 1.2V, I_{OUT} = 12mA
A: LX, 2V/div, L1 = TDK NLC565050T-151K
B: OUT, 20mV/div, 3.3V DC OFFSET
C: INDUCTOR CURRENT, 100mA/div

LOAD-TRANSIENT RESPONSE



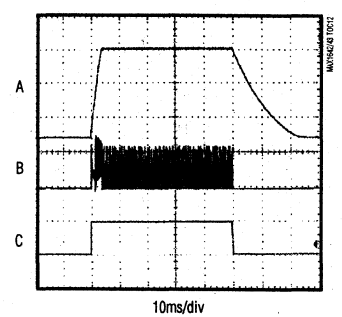
V_{OUT} = 3.3V, V_{BATT} = 1.2V
A: OUT, 20mV/div, 3.3V DC OFFSET
B: LOAD, 2mA to 20mA, 10mA/div

LINE-TRANSIENT RESPONSE



V_{OUT} = 3.3V, LOAD = 15mA
A: OUT, 50mV/div, 3.3V DC OFFSET
B: V_{BATT}, 1V to 1.5V, 500mV/div

SHUTDOWN RESPONSE AND INDUCTOR CURRENT



V_{OUT} = 3.3V, V_{BATT} = 1.2V, I_{OUT} = 5mA
A: OUT, 1V/div
B: INDUCTOR CURRENT, 200mA/div
C: $\overline{SHDN}$, 2V/div

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

Pin Description

PIN		NAME	FUNCTION
MAX1642	MAX1643		
1	1	BATT	IC Battery-Power Input. Sense input for $\overline{\text{BATTLO}}$ comparator (MAX1643 only).
2	2	PFI	Power-Fail Input. When the voltage on PFI drops below 614mV, $\overline{\text{PFO}}$ sinks current.
—	3	$\overline{\text{BATTLO}}$	Open-Drain Battery-Low Output. When the voltage at BATT drops below 1V, $\overline{\text{BATTLO}}$ sinks current.
3	4	$\overline{\text{PFO}}$	Open-Drain Power-Fail Output. Sinks current when PFI drops below 614mV.
4	—	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Connect to BATT for normal operation.
5	5	FB	Feedback Input for adjustable-output operation. Connect FB to an external resistor voltage divider between OUT and GND. Connect to GND for fixed-output operation.
6	6	GND	Ground
7	7	LX	N-Channel MOSFET Switch Drain and P-Channel Synchronous-Rectifier Drain
8	8	OUT	Power Output. Feedback input for fixed 3.3V operation and IC power input. Connect filter capacitor close to OUT.

Detailed Description

The MAX1642/MAX1643 each consist of an internal 1Ω, N-channel MOSFET power switch, a built-in synchronous rectifier that acts as the catch diode, an oscillator, a reference, and PFM control circuitry (Figure 1).

These devices are optimized for applications with power-management features that operate from one alkaline cell, such as pagers, remote controls, and battery-powered instruments. They are designed to meet the specific demands of the operating states characteristic of such systems:

1) *Primary battery is good and the load is active:* In this state, the system draws tens of milliamperes, and the MAX1642/MAX1643 typically offer 80% efficiency.
2) *Primary battery is good and the load is sleeping:* In this state, the load is drawing hundreds of microamperes, and the DC-DC converter IC draws very low quiescent current. In many applications, the load is expected to be in this state most of the time.

Operating Principle

The MAX1642/MAX1643 employ a proprietary pulse-frequency-modulation (PFM) control scheme that combines the ultra-low quiescent current traditional of pulse-skipping PFM converters with the high-load efficiency of pulse-width-modulation (PWM) converters. The on-time and minimum off-times are varied as a function of the input and output voltages:

$$t_{ON} = \frac{K}{V_{BATT}}$$

$$t_{OFF(MIN)} = \frac{1.2 \times K}{V_{OUT} - V_{BATT}}$$

where K is typically 25V-µs. This enables the MAX1642/MAX1643 to maintain high efficiency over a wide range of loads and input/output voltages. The DC-DC converter is powered from the OUT pin.

When the error comparator detects that the output voltage is too low, it turns on the internal N-channel MOSFET switch until the on-time is satisfied (see Figure 1 and the Standard Application Circuits, Figures 2 and 3). During the on-time, current ramps up in the inductor, storing energy in a magnetic field. When the MOSFET turns off, during the second half of each cycle, the magnetic field collapses, causing the inductor voltage to force current through the synchronous rectifier, transferring the stored energy to the output filter capacitor and load. The output filter capacitor stores charge while current from the inductor is high, then holds up the output voltage until the second half of the next switching cycle, smoothing power flow to the load.

Bootstrap DC-DC Block

The bootstrap block contains a low-voltage start-up oscillator. This oscillator pumps up the output voltage to approximately 1.7V, where the main DC-DC converter can operate. The oscillator is powered from the BATT input and drives an NPN switch. During start-up, the P-channel synchronous rectifier remains off and either its body diode or an external diode is used as an output rectifier. Reduce the load as needed to allow start-up with input voltages below 2V (see *Typical Operating Characteristics*).

Shutdown (MAX1642)

Pulling $\overline{SHDN}$ low places the MAX1642 in shutdown mode (I_{SHDN} = 2µA typical). In shutdown, the internal switching MOSFET turns off, $\overline{PFO}$ goes high-impedance, and the synchronous rectifier turns off to prevent reverse current from flowing from the output back to the input. However, there is still a forward current path through the synchronous-rectifier body diode from the input to the output. Thus, in shutdown, the output remains one diode drop below the battery voltage (V_{BATT}). To disable the shutdown feature, connect $\overline{SHDN}$ (a logic input) to BATT.

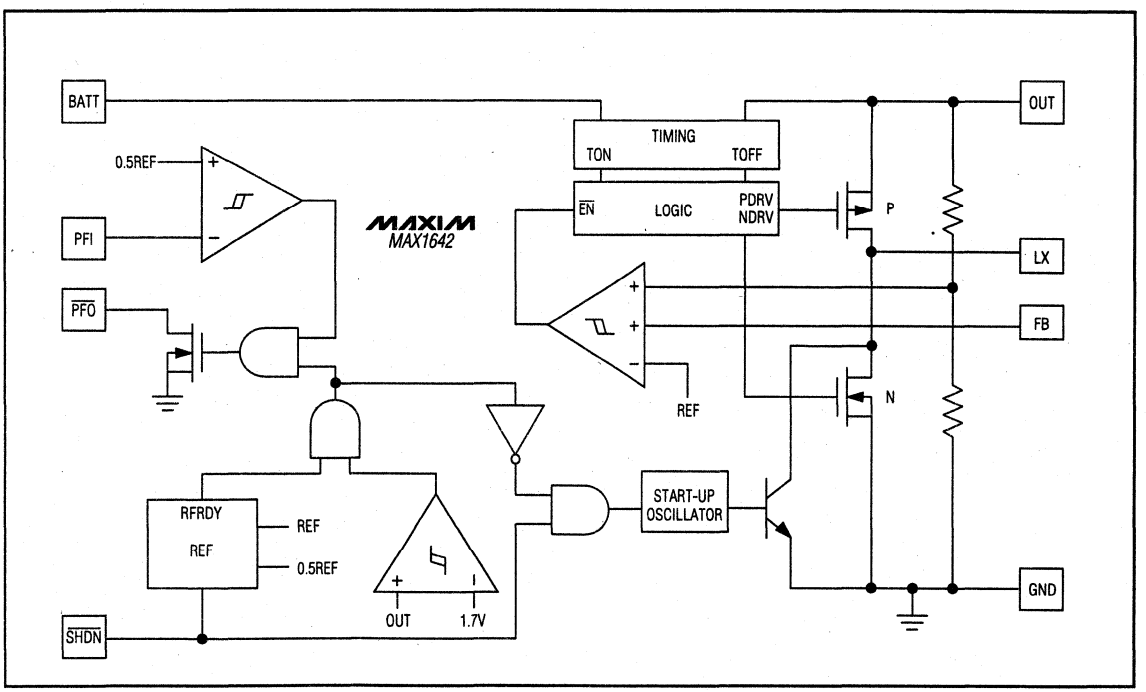


Figure 1. MAX1642 Functional Diagram

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

$\overline{\text{BATTLO}}$ (MAX1643)

The MAX1643 contains an on-chip comparator for low-battery detection. If the voltage at BATT drops below 1V, $\overline{\text{BATTLO}}$ sinks current. $\overline{\text{BATTLO}}$ is an open-drain output. In combination with PFI/$\overline{\text{PFO}}$, this allows monitoring of both the input and output voltages.

Reverse-Battery Protection

The MAX1642/MAX1643 can sustain/survive single-cell battery reversal up to the package power-dissipation limit. An internal 5Ω resistor in series with a diode limits reverse current to less than 220mA, which prevents damage to the MAX1642/MAX1643. Prolonged operation above 220mA reverse-battery current can degrade the devices' performance.

Design Information

Output Voltage Selection

The MAX1642/MAX1643 operate with a 3.3V ±4% or adjustable output. To select fixed-voltage operation, connect FB to GND. For an adjustable output between 2V and 5.2V, connect FB to a resistor voltage divider between OUT and GND (Figure 4). FB regulates to 1.23V.

Since FB leakage is 10nA max, select feedback resistor R2 in the 100kΩ to 1MΩ range. R1 is given by:

$$R1 = R2\left(\frac{V_{OUT}}{V_{REF}} - 1\right)$$

where V_{REF} = 1.23V.

Power-Fail Detection

The MAX1642/MAX1643 have an on-chip comparator for power-fail detection. This comparator can detect loss of power at the input or output. If the voltage at PFI falls below 614mV, the $\overline{\text{PFO}}$ output sinks current to GND. Hysteresis at the power-fail input is 1%. The power-fail monitor's threshold is set by two resistors: R3 and R4 (Figure 5). Set the threshold using the following equation:

$$R3 = R4\left(\frac{V_{TH}}{V_{PFI}} - 1\right)$$

where V_{TH} is the desired threshold of the power-fail detector, and V_{PFI} is the 614mV reference of the power-fail comparator. Since PFI leakage is 10nA max, select feedback resistor R4 in the 100kΩ to 1MΩ range.

Low-Battery Start-Up

The MAX1642/MAX1643 are bootstrapped circuits with a low-voltage start-up oscillator. They can start under low-load conditions at lower battery voltages than at full load. Once started, the output can maintain the load as the battery voltage decreases below the start-up voltage (see *Typical Operating Characteristics*).

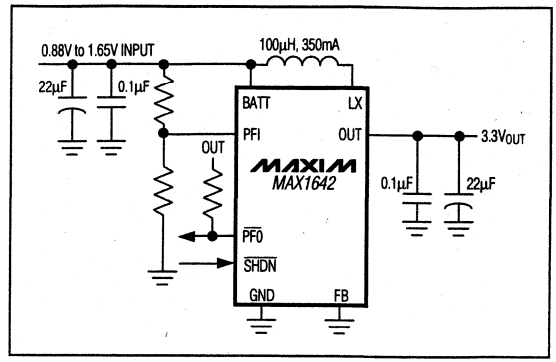


Figure 2. MAX1642 3.3V Standard Application Circuit

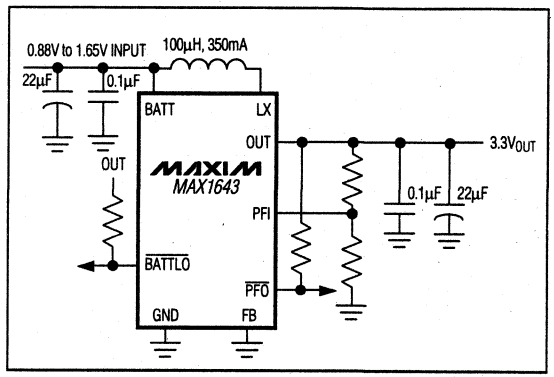


Figure 3. MAX1643 3.3V Standard Application Circuit

Inductor Selection

A 100µH inductor is recommended for most applications. The use of lower inductor values (down to 68µH) increases maximum output current. Higher values (up to 220µH) reduce peak inductor current and consequent ripple and noise. The inductor's saturation-current rating must exceed the peak current limit synthesized by the MAX1642/MAX1643's timing algorithms:

$$I_{PEAK} = \frac{K_{MAX}}{L_{MIN}}$$

where K_{MAX} = 35V-µs. The maximum recommended I_{PEAK} is 350mA. For best efficiency, inductor series resistance should be less than 1Ω.

Capacitor Selection

Choose input and output capacitors to service input and output peak currents with acceptable voltage ripple. A 22µF, 6V, low-ESR, surface-mount tantalum output filter capacitor typically provides 60mV output ripple when stepping up from 1.3V to 3.3V at 20mA. The input filter capacitor (C_{IN}) also reduces peak currents drawn from the battery and improves efficiency.

Low equivalent series resistance (ESR) capacitors are recommended. Capacitor ESR is a major contributor to output ripple (usually more than 60%). Ceramic capacitors have the lowest ESR, but low-ESR tantalums represent a good balance between cost and performance. Low-ESR aluminum electrolytic capacitors are tolerable, and standard aluminum electrolytic capacitors should be avoided. Do not exceed tantalum capacitors' ripple-current ratings; select capacitors with a rating exceeding the peak inductor current (I_{PEAK}).

PC Board Layout and Grounding

High switching frequencies and large peak currents make PC board layout an important part of design. Poor design can result in excessive EMI on the feedback paths and voltage gradients in the ground plane. Both of these factors can result in instability or regulation errors. The OUT pin must be bypassed directly to GND as close to the IC as possible (within 0.2 in. or 5mm).

Place power components—such as the MAX1642/MAX1643, inductor, input filter capacitor, and output filter capacitor—as close together as possible. Keep their traces short, direct, and wide (≥50 mil or 1.25mm), and place their ground pins close together in a star-ground configuration. Keep the extra copper on the board and integrate it into ground as a pseudo-ground plane. On multilayer boards, route the star ground using component-side copper fill, then connect it to the internal ground plane using vias.

Place the external voltage-feedback network very close to the FB pin (within 0.2 in. or 5mm). Noisy traces, such as from the LX pin, should be kept away from the voltage-feedback network and separated from it using grounded copper. The evaluation kit manual shows an example PC board layout, routing, and pseudo-ground plane.

Noise and Voltage Ripple

EMI and output voltage ripple can be minimized by following a few simple design rules.

1) Place the DC-DC converter and digital circuitry on an opposite corner of the PC board, away from sensitive RF and analog input stages.

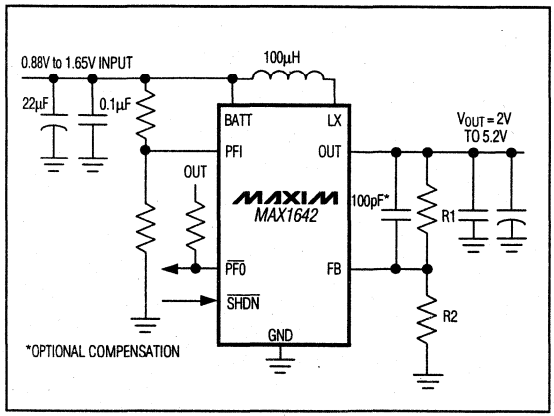


Figure 4. Adjustable-Output Circuit

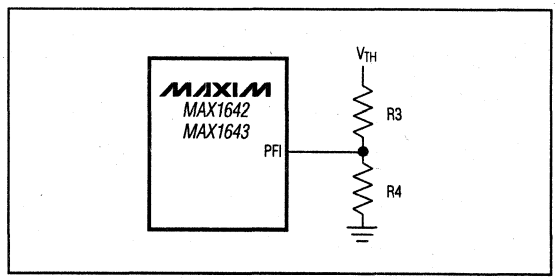


Figure 5. Power-Fail Detection Circuit

2) Use a closed-core inductor, such as toroid or shielded bobbin, to minimize fringe magnetic fields.
3) Choose the largest inductor value that satisfies the load requirement to minimize peak switching current and resulting ripple and noise.
4) Use low-ESR input and output filter capacitors.
5) Follow sound circuit-board layout and grounding rules (see the *PC Board Layout and Grounding* section).
6) Where necessary, add LC pi filters, linear post-regulators such as the MAX8863 and MAX8864 (SOT23 package), or shielding. The LC pi filter's cutoff frequency should be at least a decade or two below the DC-DC converter's switching frequency for the specified load and input voltage.

High-Efficiency, Step-Up DC-DC Converters for 1V Inputs

Table 1. Component Suppliers

SUPPLIER		PHONE	FAX
AVX	USA	(803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA	(847) 639-6400	(847) 639-1469
Coiltronics	USA	(561) 241-7876	(561) 241-9339
Dale	USA	(605) 668-4131	(605) 665-1627
Nichicon	USA Japan	(847) 843-7500 81-7-5231-8461	(847) 843-2798 81-7-5256-4158
Sanyo	USA Japan	(619) 661-6835 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sprague	USA	(603) 224-1961	(603) 224-1430
Sumida	USA Japan	(847) 956-0666 81-3-3607-5111	(847) 956-0702 81-3-3607-5144
TDK	USA	(847) 390-4373	(847) 390-4428

Chip Information

TRANSISTOR COUNT: 594

SUBSTRATE CONNECTED TO GND

Table 2. Surface-Mount Inductor Information

INDUCTANCE (µH)	VENDOR/PART	INDUCTOR SPECIFICATION	
		RESISTANCE (Ω)	I_{SAT} (mA)
68	Coilcraft DO1608-683	0.75	400
	Sumida CD54-680	0.46	610
100	Coilcraft DO1608-104	1.1	310
	Sumida CD54-101	0.7	520
	TDK NLC565050T-101K	1.6	250
150	Coilcraft DO1608-154	1.7	270
	Sumida CD54-151	1.1	400
	TDK NLC565050T-151K	2.2	210
220	Coilcraft DO1608-224	2.3	220
	Sumida CD54-221	1.57	350

19-1158; Rev 0; 12/96

MAXIM

Chemistry-Independent Battery Chargers

General Description

The MAX1647/MAX1648 provide the power control necessary to charge batteries of any chemistry. In the MAX1647, all charging functions are controlled via the Intel System Management Bus (SMBus™) interface. The SMBus 2-wire serial interface sets the charge voltage and current, and provides thermal status information. The MAX1647 functions as a level 2 charger, compliant with the Duracell/Intel Smart Battery Charger Specification. The MAX1648 omits the SMBus serial interface, and instead sets the charge voltage and current proportional to the voltage applied to external control pins.

In addition to the feature set required for a level 2 charger, the MAX1647 generates interrupts to signal the host when power is applied to the charger or a battery is installed or removed. Additional status bits allow the host to check whether the charger has enough input voltage, and whether the voltage on or current into the battery is being regulated. This allows the host to determine when lithium-ion batteries have completed charge without interrogating the battery.

The MAX1647 is available in a 20-pin SSOP with a 2mm profile height. The MAX1648 is available in a 16-pin SO package.

Applications

Notebook Computers

Personal Digital Assistants

Charger Base Stations

Phones

Features

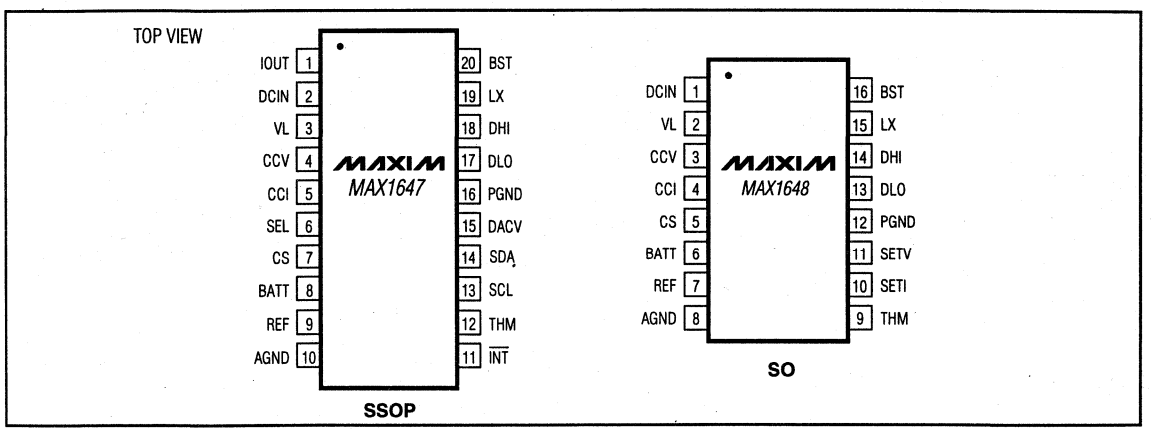
- ♦ **Charges Any Battery Chemistry: Li-Ion, NiCd, NiMH, Lead Acid, etc.**
- ♦ **Intel SMBus 2-Wire Serial Interface (MAX1647)**
- ♦ **Intel/Duracell Level 2 Smart Battery Compliant (MAX1647)**
- ♦ **4A, 2A, or 1A Maximum Battery-Charge Current**
- ♦ **11-Bit Control of Charge Current**
- ♦ **Up to 18V Battery Voltage**
- ♦ **10-Bit Control of Voltage**
- ♦ **±0.75% Voltage Accuracy with External ±0.1% Reference**
- ♦ **Up to 28V Input Voltage**
- ♦ **Battery Thermistor Fail-Safe Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1647EAP	-40°C to +85°C	20 SSOP
MAX1648ESE	-40°C to +85°C	16 Narrow SO

4

Pin Configurations



SMBus is a trademark of Intel Corp.

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For small orders, phone 408-737-7600 ext. 3468.

Chemistry-Independent Battery Chargers

ABSOLUTE MAXIMUM RATINGS

DCIN to AGND .....-0.3V to 30V
DCIN to IOUT .....-0.3V to 7.5V
BST to AGND .....-0.3V to 36V
BST, DHI to LX .....-0.3V to 6V
LX to AGND .....-0.3V to 30V
THM, CCI, CCV, DACV, REF,
DLO to AGND .....-0.3V to (VL + 0.3V)
VL, SEL, $\overline{INT}$, SDA, SCL to AGND (MAX1647) .....-0.3V to 6V
SETV, SETI to AGND (MAX1648).....-0.3V to 6V
BATT, CS+ to AGND.....-0.3V to 20V
PGND to AGND .....-0.3V to +0.3V
SDA, $\overline{INT}$ Current 50mA
VL Current.....50mA
Continuous Power Dissipation (T_A = +70°C)
16-Pin SO (derate 8.7mW/°C above +70°C).....696mW
20-Pin SSOP (derate 8mW/°C above +70°C) 640mW
Operating Temperature Range
MAX1647EAP, MAX1648ESE .....-40°C to +85°C
Storage Temperature.....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = 18V, V_{REF} = 4.096V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
DCIN Input Voltage Range		7.5		28	V
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V, logic inputs = VL		4	6	mA
VL Output Voltage	7.5V < V_{DCIN} < 28V, no load	5.15	5.4	5.65	V
VL Load Regulation	I_{LOAD} = 10mA			100	mV
VL AC_PRESENT Trip Point	MAX1647	3.20	4	5.15	V
REF Output Voltage	0µA < I_{SOURCE} < 500µA	3.74	3.9	4.07	V
REF Overdrive Input Current				700	µA
SWITCHING REGULATOR					
Oscillator Frequency		200	250	300	kHz
DHI Maximum Duty Cycle		89	93		%
DHI On-Resistance	High or low		4	7	Ω
DLO On-Resistance	High or low		6	14	Ω
BATT Input Current (Note 1)	VL < 3.2V, V_{BATT} = 12V		1	5	µA
	VL < 5.15V, V_{BATT} = 12V		350	500	
CS Input Current (Note 1)	VL < 3.2V, V_{CS} = 12V		1	5	µA
	VL < 5.15V, V_{CS} = 12V		170	400	
BATT, CS Input Voltage Range		0		19	V
CS to BATT Single-Count Current-Sense Voltage	MAX1647, SEL = open, ChargingCurrent( ) = 0x0020		2.94		mV
CS to BATT Full-Scale Current-Sense Voltage	MAX1647, SEL = open, ChargingCurrent( ) = 0x07F0; MAX1648, V_{SETI} = 1.024V	170	185	200	mV
Voltage Accuracy	MAX1647, ChargingVoltage( ) = 0x1060, ChargingVoltage( ) = 0x3130; MAX1648, V_{SETV} = 3.15V, V_{SETV} = 1.05V	-0.65		0.65	%

ELECTRICAL CHARACTERISTICS (continued)

(V_{DCIN} = 18V, V_{REF} = 4.096V, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ERROR AMPLIFIERS						
GMV Amplifier Transconductance				1.4		mA/V
GMI Amplifier Transconductance				0.2		mA/V
GMV Amplifier Maximum Output Current				±80		µA
GMI Amplifier Maximum Output Current				±200		µA
CCI Clamp Voltage with Respect to CCV	1.1V < V_{CCV} < 3.5V		25	80	200	mV
CCV Clamp Voltage with Respect to CCI	1.1V < V_{CCI} < 3.5V		25	80	200	mV
TRIP POINTS AND LINEAR CURRENT SOURCES						
BATT POWER_FAIL Trip Point	MAX1647		86.5	89	91.5	% of V_{DCIN}
THM THERMISTOR_OR Over-Range Trip Point	MAX1647		89.5	91	92.5	% of V_{REF}
THM THERMISTOR_COLD Trip Point			74	75.5	77	% of V_{REF}
THM THERMISTOR_HOT Trip Point			22	23.5	25	% of V_{REF}
THM THERMISTOR_UR Under-Range Trip Point	MAX1647		3	4.5	6	% of V_{REF}
IOUT Output Current	MAX1647, V_{DCIN} = 7.5V, V_{IOUT} = 0V	ChargingCurrent( ) = 0x001F	25	31	35	mA
		ChargingCurrent( ) = 0x0000			10	µA
IOUT Operating Voltage Range	With respect to DCIN voltage		-7.5		-1.0	V
CURRENT- AND VOLTAGE-SETTING DACs (MAX1647)						
CDAC Current-Setting DAC Resolution	Guaranteed monotonic		6			bits
VDAC Voltage-Setting DAC Resolution	Guaranteed monotonic		10			bits
SETV, SETI (MAX1648)						
SETV Input Bias Current					1	µA
SETI Input Bias Current					5	µA
SETV Input Voltage Range			0		4.2	V
SETI Input Voltage Range			0		1.024	V
LOGIC LEVELS (MAX1647)						
SDA, SCL Input Low Voltage					0.8	V
SDA, SCL Input High Voltage			2.8			V
SDA, SCL Input Bias Current			-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V		6			mA

Note 1: When DCIN is less than 4V, VL is less than 3.2V, causing the battery current to be typically 2µA (CS plus BATT input current).

Chemistry-Independent Battery Chargers

ELECTRICAL CHARACTERISTICS

(V_{DCIN} = 18V, V_{REF} = 4.096V, **T_A = -40°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY AND REFERENCE					
DCIN Quiescent Current	7.5V < V_{DCIN} < 28V, logic inputs = VL		4	6	mA
VL Output Voltage	7.5V < V_{DCIN} < 28V, no load	5.15	5.4	5.65	V
REF Output Voltage	0µA < I_{SOURCE} < 500µA	3.74	3.9	4.07	V
SWITCHING REGULATOR					
Oscillator Frequency		200	250	310	kHz
DHI Maximum Duty Cycle		89			%
DHI On-Resistance	High or low		4	7	Ω
DLO On-Resistance	High or low		6	14	Ω
BATT Input Current	VL < 3.2V, V_{BATT} = 12V			5	µA
CS Input Current	VL < 3.2V, V_{CS} = 12V			5	µA
CS to BATT Full-Scale Current-Sense Voltage	MAX1647, SEL = open, ChargingCurrent( ) = 0x07F0; MAX1648, V_{SETI} = 1.024V	160	185	200	mV
Voltage Accuracy	MAX1647, ChargingVoltage( ) = 0x1060, ChargingVoltage( ) = 0x3130; MAX1648, V_{SETV} = 3.15V, V_{SETV} = 1.05V	-0.65		0.65	%
ERROR AMPLIFIERS					
GMV Amplifier Transconductance			1.4		mA/V
GMI Amplifier Transconductance			0.2		mA/V
GMV Amplifier Maximum Output Current			±130		µA
GMI Amplifier Maximum Output Current			±320		µA
TRIP POINTS AND LINEAR CURRENT SOURCES					
THM THERMISTOR_OR Over-Range Trip Point	MAX1647	89.5	91	92.5	% of V_{REF}
THM THERMISTOR_COLD Trip Point		74	75.5	77	% of V_{REF}
THM THERMISTOR_HOT Trip Point		22	23.5	25	% of V_{REF}
THM THERMISTOR_UR Under-Range Trip Point	MAX1647	3	4.5	6	% of V_{REF}
SETV, SETI (MAX1648)					
SETV Input Bias Current				1	µA
SETI Input Bias Current				5	µA
LOGIC LEVELS (MAX1647)					
SDA, SCL Input Low Voltage				0.8	V
SDA, SCL Input High Voltage		2.8			V
SDA, SCL Input Bias Current		-1		1	µA
SDA Output Low Sink Current	V_{SDA} = 0.6V	6			mA

TIMING CHARACTERISTICS—MAX1647

(T_A = 0°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

TIMING CHARACTERISTICS—MAX1647

(T_A = -40°C to +85°C, unless otherwise noted. Limits over this temperature range are guaranteed by design.)

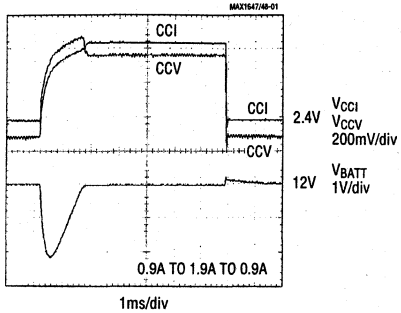
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Serial-Clock High Period	t_{HIGH}		4			µs
SCL Serial-Clock Low Period	t_{LOW}		4.7			µs
Start-Condition Setup Time	$t_{SU:STA}$		4.7			µs
Start-Condition Hold Time	$t_{HD:STA}$		4			µs
SDA Valid to SCL Rising-Edge Setup Time, Slave Clocking in Data	$t_{SU:DAT}$		250			ns
SCL Falling Edge to SDA Transition	$t_{HD:DAT}$		0			ns
SCL Falling Edge to SDA Valid, Master Clocking in Data	t_{DV}				1	µs

Chemistry-Independent Battery Chargers

Typical Operating Characteristics

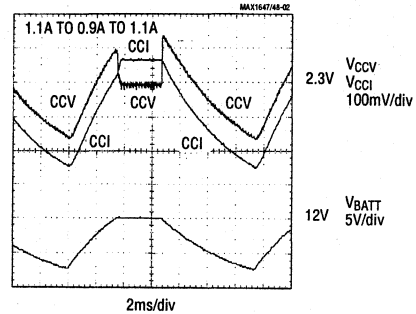
(Circuit of Figure 3, T_A = +25°C, unless otherwise noted.)

MAX1647
BATT LOAD TRANSIENT



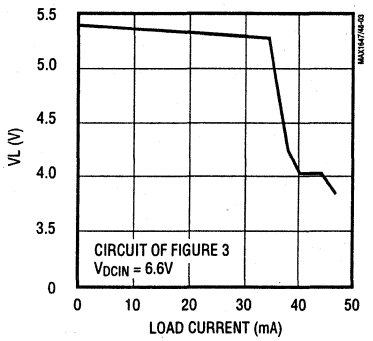
ChargingVoltage( ) = 0x2EE0 = 12000mV
ChargingCurrent( ) = 0xFFFF = MAX VALUE
ACDCIN = 18.0V, SEL = OPEN, R1 = 0.1Ω
R2 = 10kΩ, C1 = 68µF, C2 = 0.1µF, C3 = 47nF
L1 = 22µH, V_{REF} = 4.096V

MAX1647
BATT LOAD TRANSIENT

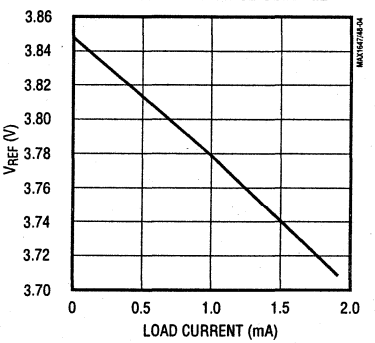


ChargingVoltage( ) = 0x2EE0 = 12000mV
ChargingCurrent( ) = 0x03E8 = 1000mA
ACDCIN = 18.0V, SEL = OPEN, C1 = 68µF,
C2 = 0.1µF, C3 = 47nF, R1 = 0.1Ω
R2 = 10kΩ, L1 = 22µH, V_{REF} = 4.096V

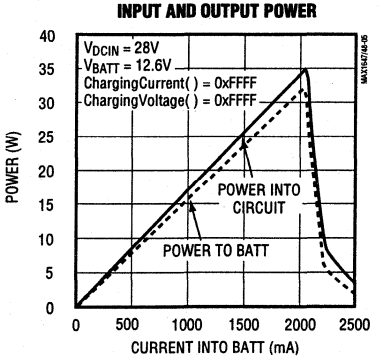
VL VOLTAGE vs. LOAD CURRENT



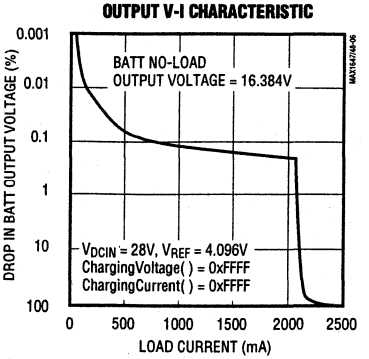
INTERNAL REFERENCE VOLTAGE



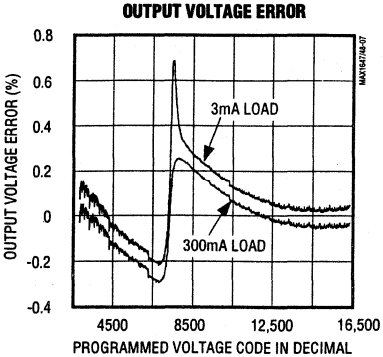
INPUT AND OUTPUT POWER



MAX1647
OUTPUT V-I CHARACTERISTIC



OUTPUT VOLTAGE ERROR



Pin Description

PIN		NAME	FUNCTION
MAX1647	MAX1648		
1	—	IOUT	Linear Current-Source Output
2	1	DCIN	Input Voltage for Powering Charger
3	2	VL	Chip Power Supply. 5.4V linear regulator output from DCIN.
4	3	CCV	Voltage-Regulation-Loop Compensation Point
5	4	CCI	Current-Regulation-Loop Compensation Point
6	—	SEL	Current-Range Selector. Tying SEL to VL sets a 4A full-scale current. Leaving SEL open sets a 2A full-scale current. Tying SEL to AGND sets a 1A full-scale current.
7	5	CS	Current-Sense Positive Input
8	6	BATT	Battery Voltage Input and Current-Sense Negative Input
9	7	REF	3.9V Reference Voltage Output or External Reference Input
10	8	AGND	Analog Ground
—	10	SETI	Current-Regulation-Loop Set Point
11	—	$\overline{INT}$	Open-Drain Interrupt Output
—	11	SETV	Voltage-Regulation-Loop Set Point
12	9	THM	Thermistor Sense Voltage Input
13	—	SCL	Serial Clock
14	—	SDA	Serial Data
15	—	DACV	Voltage DAC Output
16	12	PGND	Power Ground
17	13	DLO	Low-Side Power MOSFET Driver Output
18	14	DHI	High-Side Power MOSFET Driver Output
19	15	LX	Power Connection for the High-Side Power MOSFET Driver
20	16	BST	Power Connection for the High-Side Power MOSFET Driver

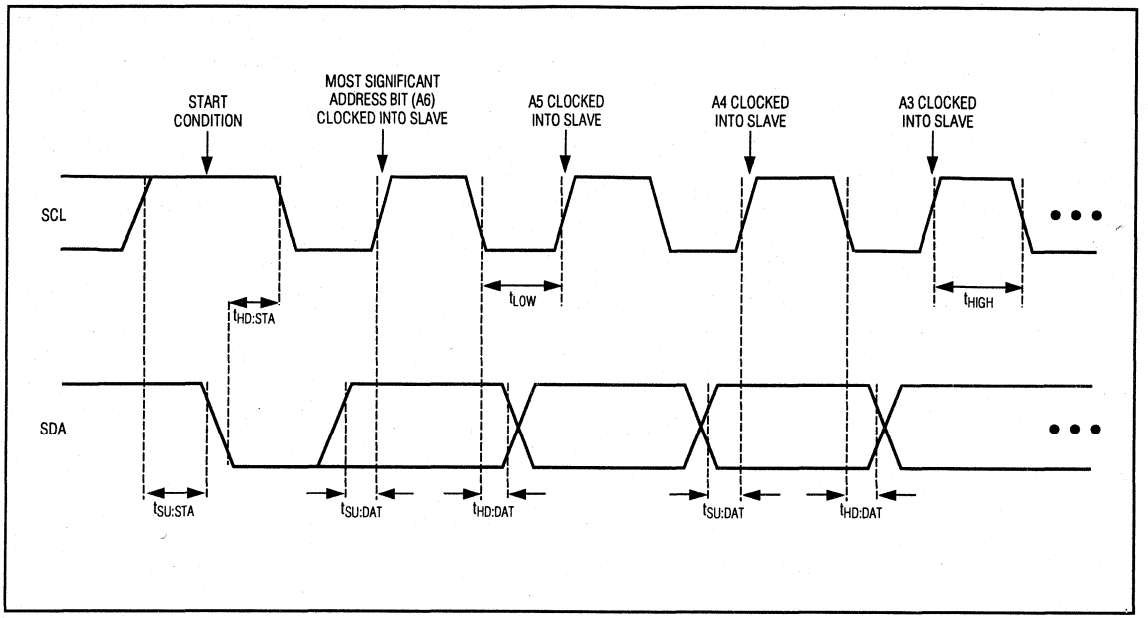


Figure 1. SMBus Serial Interface Timing—Address

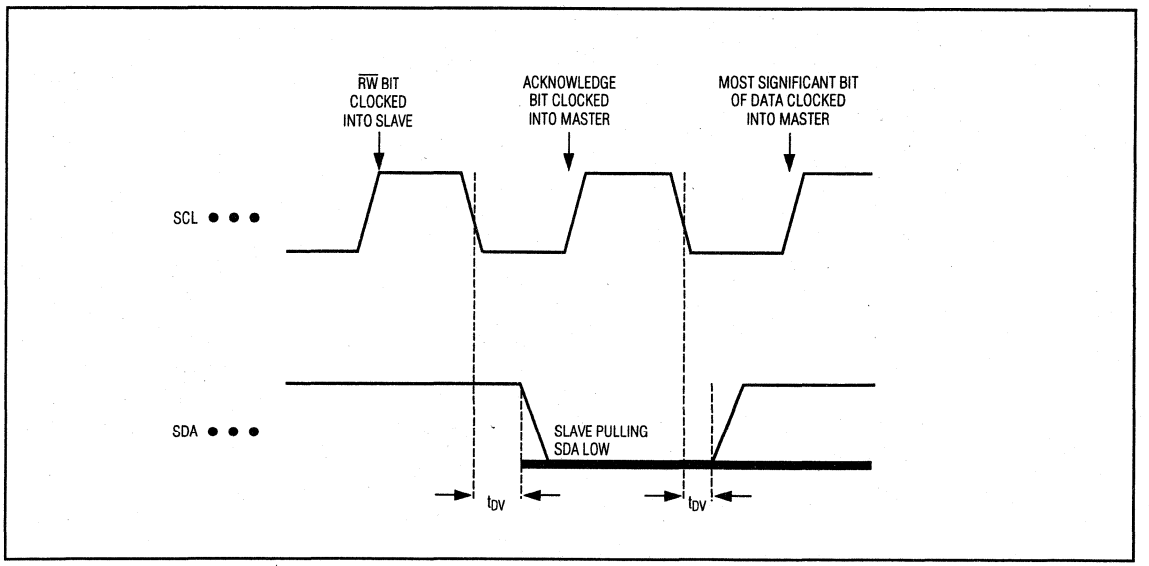


Figure 2. SMBus Serial Interface Timing—Acknowledge

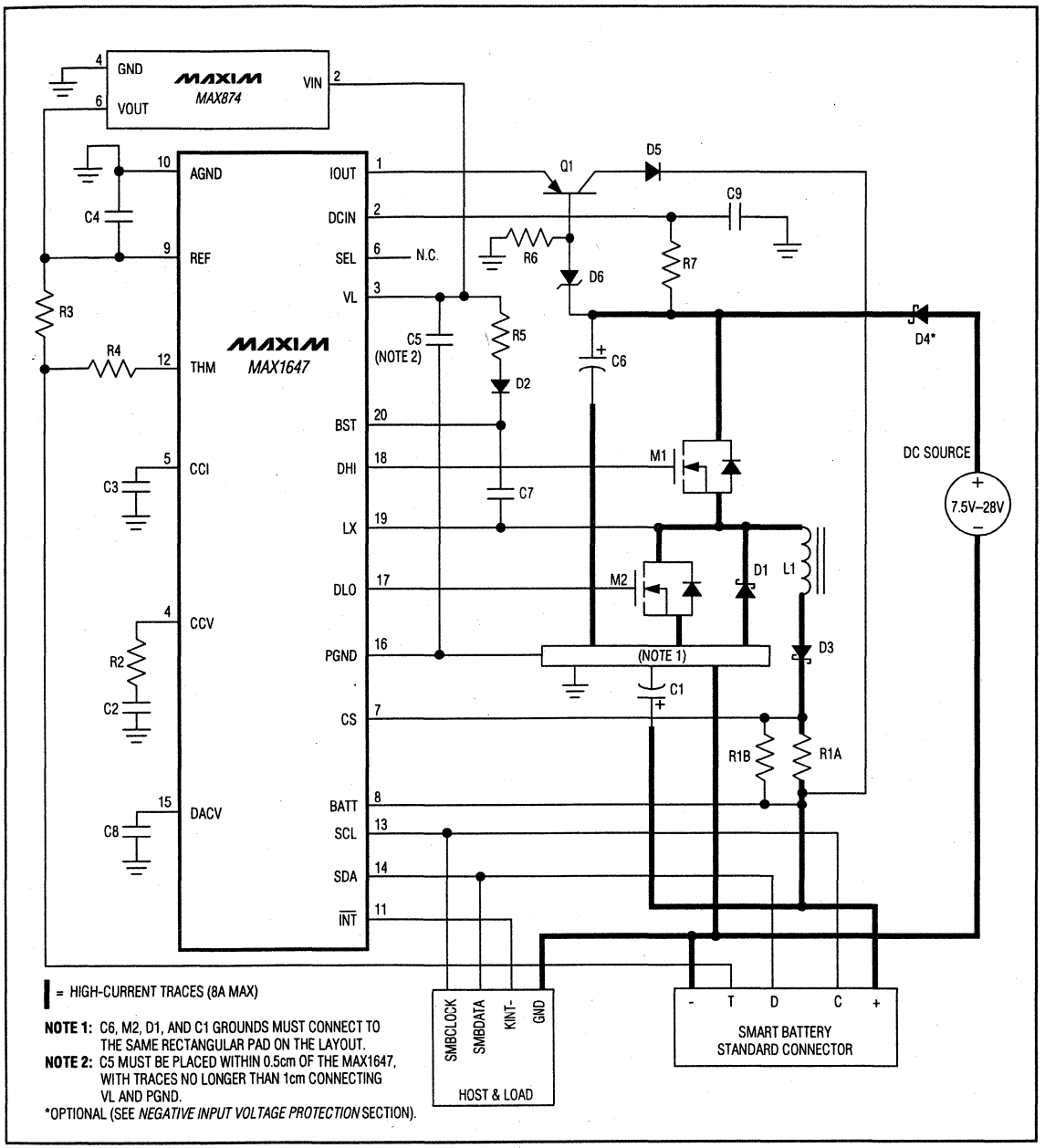


Figure 3. MAX1647 Typical Application Circuit

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Table 1a. Component Selection for Figure 3 Circuit (Also Use for Figure 4)

DESIGNATION	QTY	UNITS	NOTES	SOURCE/TYPE
C1	47	µF	20V, ESR at 250kHz ≤ 0.4Ω	Sprague, 595D476X0020D7T, D case AVX, TPSE476M020R0150, E case
C2, C4, C7, C9	0.1	µF		
C3	47	nF		
C5	1	µF	10V, ceramic or low ESR	
C6	22	µF	35V	
C8	22	nF	10V	
D1, D3, D4			3A I_{DC}, 30V Schottky diode, P_D > 0.8W, 1N5821 equivalent	NIEC, NSQ03A04, FLAT-PAK (SMC) NIEC, 30VQ04F, TO-252AA (SMD) Motorola, MBRS340T3, SMC Motorola, MBRD340T4, DPAK Diodes Inc., SK33, SMC IR, 30BQ040, SMC
D2, D5			50mA I_{DC}, 40V fast-recovery diode, 1N4150 equivalent	
D6			4.3V zener diode, 1N4731 or equivalent	
L1	22	µH	±20%, 3A I_{SAT} Note: size in L x W x H	Sumida, RCH-110/220M, 10mm x 10mm x 10mm Coiltronics, UP2-220, 0.541" x 0.345" x 0.231" Coilcraft, DO3340P-223, 0.510" x 0.370" x 0.450" Coilcraft, DO5022P-223, 0.730" x 0.600" x 0.280"
M1			$R_{DS, ON}$ ≤ 0.1Ω, V_{DSS} ≥ 30V, P_D > 0.5W, logic level, N-channel power MOSFET	Motorola, MMSF5N03HD, SO-8 Motorola, MMDF3N03HD, SO-8 Motorola, MTD20N03HDL, DPAK IR, IRF7201, SO-8 IR, IRF7303, SO-8 IR, IRF7603, Micro8 Siliconix, Si9410DY, SO-8 Siliconix, Si9936DY, SO-8 Siliconix, Si6954DQ, TSSOP-8
M2			$R_{DS, ON}$ ≤ 10Ω, V_{DSS} ≥ 30V, logic level, N-channel power MOSFET, 2N7002 equivalent	Motorola, 2N7002LT1, SOT23 Motorola, MMBF170LT1, SOT23 Diodes Inc., 2N7002, SOT23 Diodes Inc., BS870, SOT23 Zetex, ZVN3306F, SOT23 Central Semiconductor, 2N7002, SOT23
Q1			$V_{CE, MAX}$ ≤ -30V, 50mA $I_{C, CONT}$, 2N3906 equivalent	
R1A	100	mΩ	±1%, 1W	IRC, CHP1100R100F13, 2512 IRC, LR251201R100F, 2512 Dale, WSL-2512/0.1Ω/±1%, 2512
R1B	1	Ω	±5%, 1/8W	
R2, R4	10	kΩ	±5%, 1/16W	
R3	10	kΩ	±1%, 1/16W	
R5, R7	10	Ω	±5%, 1/16W	
R6	10	kΩ	±5%, 1/8W	

Table 1b. Component Suppliers

MANUFACTURER	PHONE	FAX
AVX	(803) 946-0690	(803) 626-3123
Central Semiconductor	(516) 435-1110	(516) 435-1824
Coilcraft	(847) 639-6400	(847) 639-1469
Coiltronics	(561) 241-7876	(561) 241-9339
Dale	(605) 668-4131	(605) 665-1627
IR	(310) 322-3331	(310) 322-3332
IRC	(512) 992-7900	(512) 992-3377
NIEC	(805) 867-2555	(805) 867-2698
Siliconix	(408) 988-8000	(408) 970-3950
Sprague	(603) 224-1961	(603) 224-1430
Sumida	(847) 956-0666	(847) 956-0702
Zetex	(516) 543-7100	(516) 864-7630

Detailed Description

Output Characteristics

The MAX1647/MAX1648 contain both a voltage-regulation loop and a current-regulation loop. Both loops operate independently of each other. The voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set point (V0). The current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current-limit set point (I0). The current-regulation loop is in control as long as BATT voltage is below V0. When BATT voltage reaches V0, the current loop no longer regulates, and the voltage-regulation loop takes over. Figure 5 shows the V-I characteristic at the BATT pin.

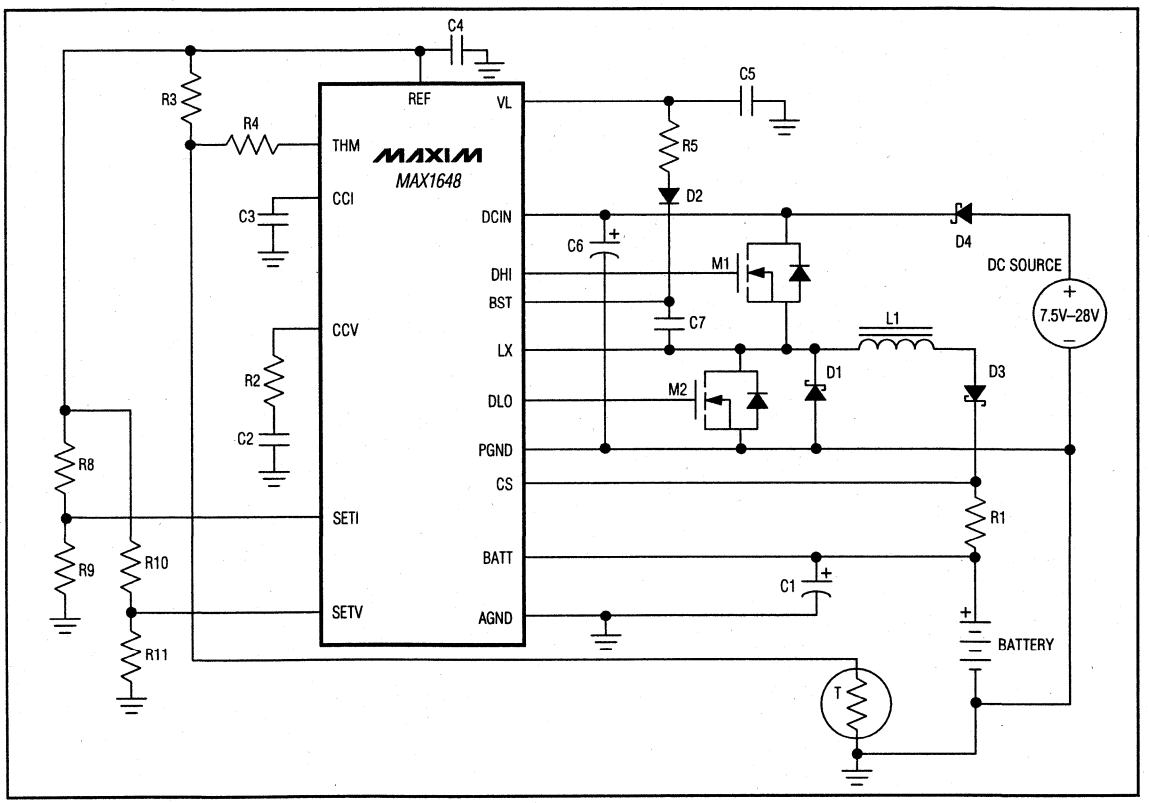

Figure 4. MAX1648 Typical Operating Circuit

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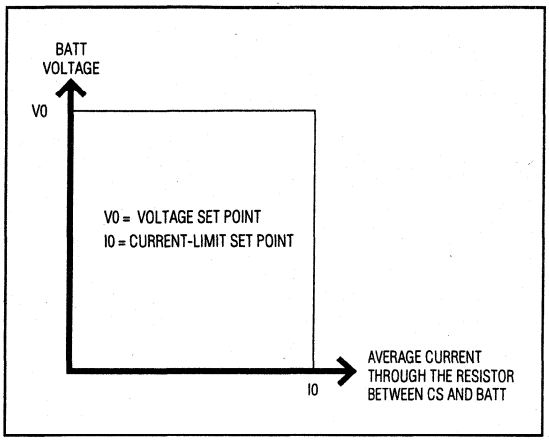

Figure 5. Output V-I Characteristic

Setting V0 and I0 (MAX1647)

Set the MAX1647's voltage and current-limit set points via the Intel System Management Bus (SMBus™) 2-wire serial interface. The MAX1647's logic interprets the serial-data stream from the SMBus interface to set internal digital-to-analog converters (DACs) appropriately. See the *MAX1647 Logic* section for more information.

Setting V0 and I0 (MAX1648)

Set the MAX1648's voltage- and current-limit set points (V0 and I0, respectively) using external resistive dividers. Figure 6b is the MAX1648 block diagram. V0 equals four times the voltage on the SETV pin. I0 equals the voltage on SETI divided by 5.5, divided by R1 (Figure 4).

Analog Section

The MAX1647/MAX1648 analog section consists of a current-mode PWM controller and two transconductance error amplifiers: one for regulating current and the other for regulating voltage. The MAX1647 uses DACs to set the current and voltage level, which are controlled via the SMBus interface. The MAX1648 eliminates the DACs and controls the error amplifiers directly from SETI (for current) and SETV (for voltage). Since separate amplifiers are used for voltage and current control, both control loops can be compensated separately for optimum stability and response in each state. The following discussion relates to the MAX1647; however, MAX1648 operation can easily be inferred from the MAX1647.

Whether the MAX1647 is controlling the voltage or current at any time depends on the battery's state. If the battery has been discharged, the MAX1647's output reaches the current-regulation limit before the voltage limit, causing the system to regulate current. As the battery charges, the voltage rises until the voltage limit is reached, and the charger switches to regulating voltage. The transition from current to voltage regulation is done by the charger, and need not be controlled by the host.

Voltage Control

The internal GMV amplifier controls the MAX1647's output voltage. The voltage at the amplifier's noninverting input amplifier is set by a 10-bit DAC, which is controlled by a ChargingVoltage( ) command on the SMBus (see the *MAX1647 Logic* section for more information). The battery voltage is fed to the GMV amplifier through a 4:1 resistive voltage divider. With an external 4.096V reference, the set voltage ranges between 0 and 16.38V with 16mV resolution.

This poses a challenge for charging four lithium-ion cells in series: because the lithium-ion battery's typical per-cell voltage is 4.2V maximum, 16.8V is required. A larger reference voltage can be used to circumvent this. Under this condition, the maximum battery voltage no longer matches the programmed voltage. The solution is to use a 4.2V reference and host software. Contact Maxim's applications department for more information.

The GMV amplifier's output is connected to the CCV pin, which compensates the voltage-regulation loop. Typically, a series-resistor/capacitor combination can be used to form a pole-zero couplet. The pole introduced rolls off the gain starting at low frequencies. The zero of the couplet provides sufficient AC gain at mid-frequencies. The output capacitor then rolls off the mid-frequency gain to below 1, to guarantee stability before encountering the zero introduced by the output capacitor's equivalent series resistance (ESR). The GMV amplifier's output is internally clamped to between one-fourth and three-fourths of the voltage at REF.

Current Control

The internal GMI amplifier and an internal current source control the battery current while the charger is regulating current. Since the regulator current's accuracy is not adequate to ensure full 11-bit accuracy, an internal linear current source is used in conjunction with the PWM regulator to set the battery current. The current-control DAC's five least significant bits set the

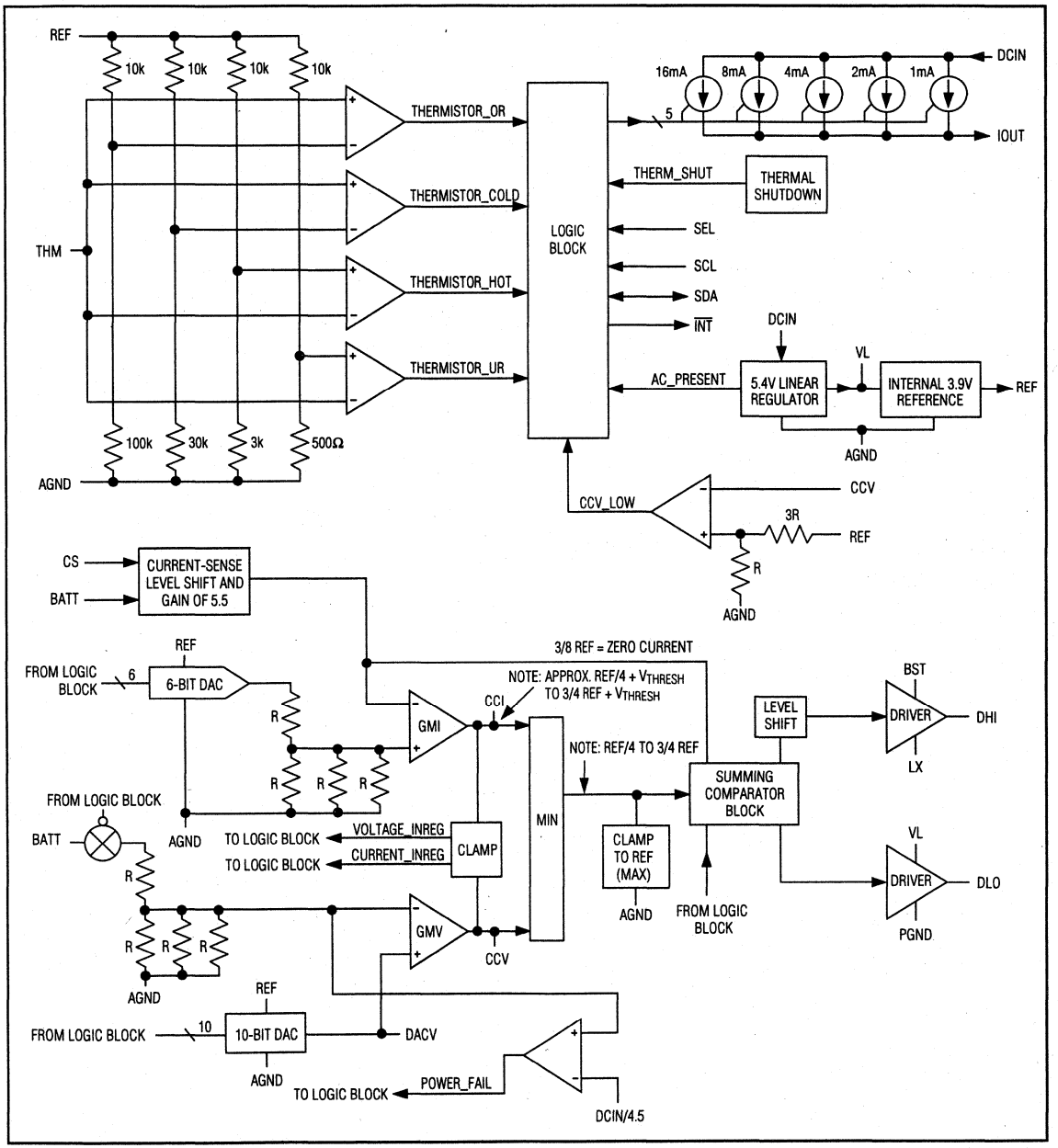

Figure 6a. MAX1647 Block Diagram

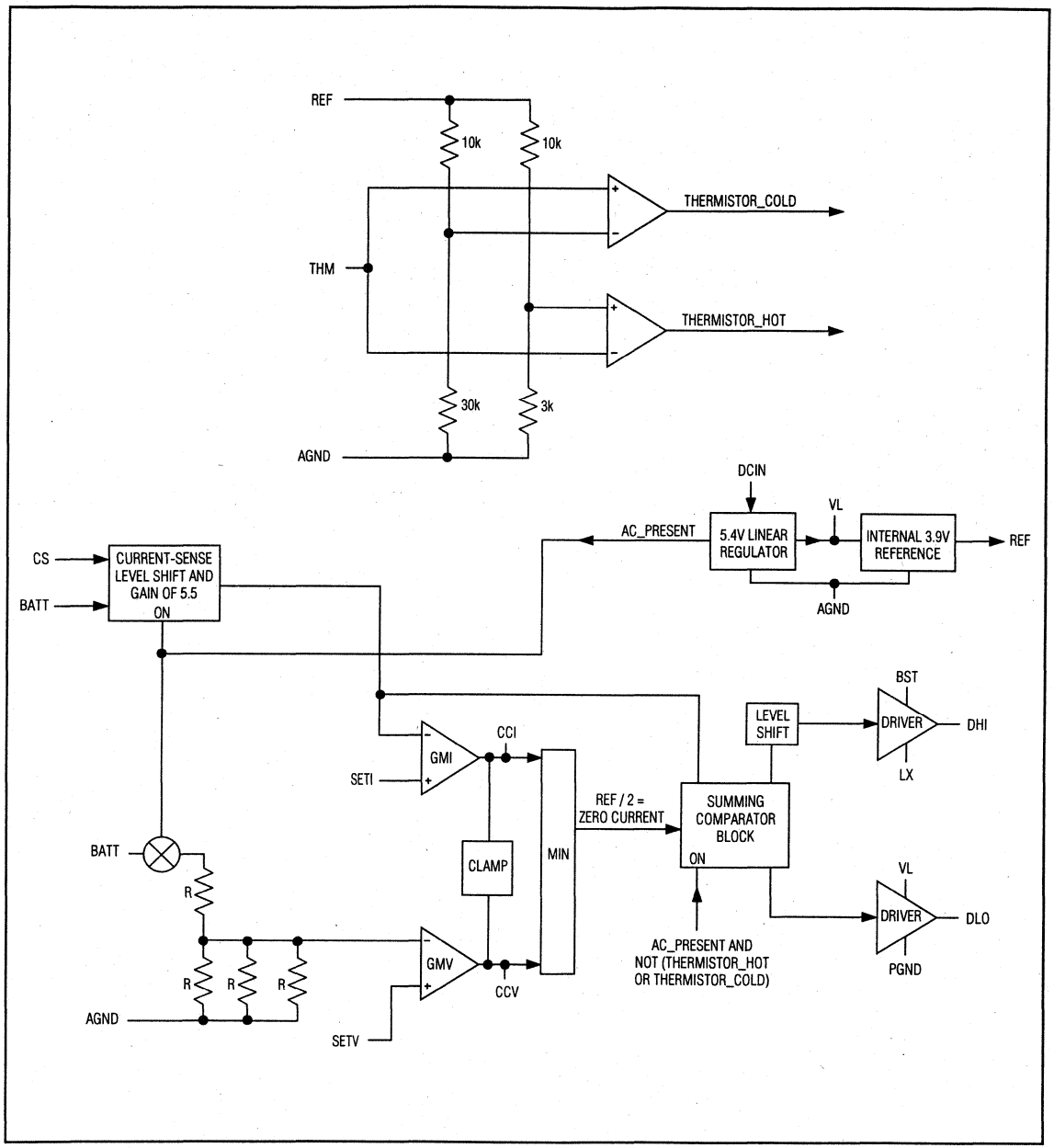

Figure 6b. MAX1648 Block Diagram

internal current sources' state, and the six most significant bits control the switching regulator's current. The internal current source supplies 1mA resolution to the battery to comply with the smart-battery specification. When the current is set to a number greater than 32, the internal current source remains at 31mA. This guarantees that battery-current setting is monotonic regardless of current-sense resistor choice and current-sense amplifier offset.

The GMI amplifier's noninverting input is driven by a 4:1 resistive voltage divider, which is driven by the 6-bit DAC. If an external 4.096V reference is used, this input is approximately 1.0V at full scale, and the resolution is 16mV. The current-sense amplifier drives the inverting input to the GMI amplifier. It measures the voltage across the current-sense resistor (R_{SEN}) (which is between the CS and BATT pins), amplifies it by approximately 5.45, and level shifts it to ground. The full-scale current is approximately 0.2V / R_{SEN}, and the resolution is 3.2mV / R_{SEN}.

The current-regulation-loop is compensated by adding a capacitor to the CCI pin. This capacitor sets the current-feedback loop's dominant pole. The GMI amplifier's output is clamped to between approximately one-fourth and three-fourths of the REF voltage. While the current is in regulation, the CCV voltage is clamped to within 80mV of the CCI voltage. This prevents the battery voltage from overshooting when the DAC voltage setting is updated. The converse is true when the voltage is in regulation and the current is not at the current DAC setting. Since the linear range of CCI or CCV is about 1.5V to 3.5V or about 2V, the 80mV clamp results in a relatively negligible overshoot when the loop switches from voltage to current regulation or vice versa.

PWM Controller

The battery voltage or current is controlled by the current-mode, pulse-width-modulated (PWM), DC-DC converter controller. This controller drives two external N-channel MOSFETs, which switch the voltage from the input source. This switched voltage feeds an inductor, which filters the switched rectangular wave. The controller sets the pulse width of the switched voltage so that it supplies the desired voltage or current to the battery.

The heart of the PWM controller is the multi-input comparator. This comparator sums three input signals to determine the pulse width of the switched signal, setting the battery voltage or current. The three signals are the current-sense amplifier's output, the GMV or GMI error amplifier's output, and a slope-compensation signal, which ensures that the controller's internal current-control loop is stable.

The PWM comparator compares the current-sense amplifier's output to the higher output voltage of either the GMV or the GMI amplifier (the error voltage). This current-mode feedback corrects the duty ratio of the switched voltage, regulating the peak battery current and keeping it proportional to the error voltage. Since the average battery current is nearly the same as the peak current, the controller acts as a transconductance amplifier, reducing the effect of the inductor on the output filter LC formed by the output inductor and the battery's parasitic capacitance. This makes stabilizing the circuit easy, since the output filter changes from a complex second-order RLC to a first-order RC. To preserve the inner current-control loop's stability, slope compensation is also fed into the comparator. This damps out perturbations in the pulse width at duty ratios greater than 50%.

At heavy loads, the PWM controller switches at a fixed frequency and modulates the duty cycle to control the battery voltage or current. At light loads, the DC current through the inductor is not sufficient to prevent the current from going negative through the synchronous rectifier (Figure 3, M2). The controller monitors the current through the sense resistor R_{SEN}; when it drops to zero, the synchronous rectifier turns off to prevent negative current flow.

MOSFET Drivers

The MAX1647 drives external N-channel MOSFETs to regulate battery voltage or current. Since the high-side N-channel MOSFET's gate must be driven to a voltage higher than the input source voltage, a charge pump is used to generate such a voltage. The capacitor C7 (Figure 3) charges to approximately 5V through D2 when the synchronous rectifier turns on. Since one side of C7 is connected to the LX pin (the source of M1), the high-side driver (DHI) can drive the gate up to the voltage at BST, which is greater than the input voltage, when the high-side MOSFET turns on.

The synchronous rectifier behaves like a diode, but with a smaller voltage drop to improve efficiency. A small dead time is added between the time that the high-side MOSFET turns off and the synchronous rectifier turns on, and vice versa. This prevents crowbar currents (currents that flow through both MOSFETS during the brief time that one is turning on and the other is turning off). Connect a Schottky rectifier from ground to LX (across the source and drain of M2) to prevent the synchronous rectifier's body diode from conducting. The body diode typically has slower switching-recovery times, so allowing it to conduct would degrade efficiency.

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The synchronous rectifier may not be completely replaced by a diode because the BST capacitor charges while the synchronous rectifier is turned on. Without the synchronous rectifier, the BST capacitor may not fully charge, leaving the high-side MOSFET with insufficient gate drive to turn on. However, the synchronous rectifier may be replaced with a small MOSFET, such as a 2N7002, to guarantee that the BST capacitor is allowed to charge. In this case, most of the current at high currents is carried by the diode and not by the synchronous rectifier.

Internal Regulator and Reference

The MAX1647 uses an internal low-dropout linear regulator to create a 5.4V power supply (VL), which powers its internal circuitry. VL can supply up to 20mA. A portion of this current powers the internal circuitry, but the remaining current can power the external circuitry. The current used to drive the MOSFETs comes from this supply, which must be considered when calculating how much power can be drawn. To estimate the current required to drive the MOSFETs, multiply the total gate charge of each MOSFET by the switching frequency (typically 250kHz). The internal circuitry requires as much as 6mA from the VL supply. To ensure VL stability, bypass the VL pin with a 1µF or greater capacitor.

The MAX1647 has an internal ±2% accurate 3.9V reference voltage. An external reference can be used to increase the charger's accuracy. Use a 4.096V reference, such as the MAX874, for compliance with the Intel/Duracell smart-battery specification. Voltage-setting accuracy is ±0.65%, so the total voltage accuracy is the accuracy added to the reference accuracy. For 1% total voltage accuracy, use a reference with ±0.35% or greater accuracy. If the internal reference is used, bypass it with a 0.1µF or greater capacitor.

MAX1647 Logic

The MAX1647 uses serial data to control its operation. The serial interface complies with the SMBus specification (see *System Management Bus Specification*, from Intel Architecture Labs; http://www.intel.com/IAL/power-mgm.html; Intel Architecture Labs: 800-253-3696). Charger functionality complies with the Intel/Duracell Smart Charger Specification for a level 2 charger.

The MAX1647 uses the SMBus Read-Word and Write-Word protocols to communicate with the battery it is charging, as well as with any host system that monitors the battery to charger communications. The MAX1647 never initiates communication on the bus; it only receives commands and responds to queries for status information. Figure 7 shows examples of the SMBus Write-Word and Read-Word protocols.

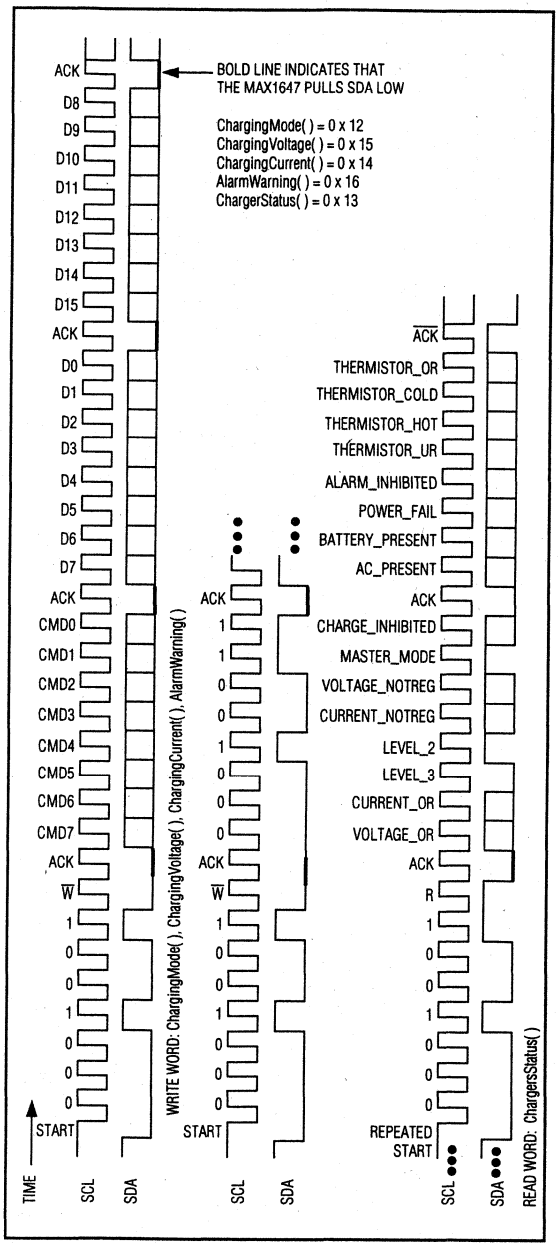

Figure 7. Write-Word and Read-Word Examples

Each communication with the MAX1647 begins with a start condition that is defined as a falling edge on SDA with SCL high. The device address follows the start condition. The MAX1647 device address is 0b0001001 (0b indicates a binary number), which may also be denoted as 0x12 (0x indicates a hexadecimal number) for Write-Word commands, or 0x13 in hexadecimal for Read-Word commands (note that the address is only seven bits, and the hexadecimal representation uses R/$\overline{W}$ as its least significant bit).

ChargerMode( )

The ChargerMode( ) command uses Write-Word protocol. The command code for ChargerMode( ) is 0x12; thus the CMD7–CMD0 bits in Write-Word protocol should be 0b00010010. Table 2 describes the functions of the 16 different data bits (D0–D15). Bit 0 refers to the D0 bit in the Write-Word protocol (Figure 7).

Whenever the BATTERY_PRESENT status bit is clear, the HOT_STOP bit is set, regardless of any previous ChargerMode( ) command. To charge a battery that has a thermistor impedance in the HOT range (i.e., THERMISTOR_HOT = 1 and THERMISTOR_UR = 0), the host must use the ChargerMode( ) command to clear HOT_STOP **after** the battery is inserted. The HOT_STOP bit returns to its default power-up condition ('1') whenever the battery is removed.

ChargingVoltage( )

The ChargingVoltage( ) command uses Write-Word protocol. The command code for ChargingVoltage( ) is 0x15; thus, the CMD7–CMD0 bits in Write-Word protocol should be 0b00010101. The 16-bit binary number formed by D15–D0 represents the voltage set point (V0) in millivolts; however, since the MAX1647 has only 16mV resolution in setting V0, the D0, D1, D2, and D3 bits are ignored. For D15 = D14 = 0:

$$VOLTAGE_OR = 0 \text{ and } V0\,(\text{in Volts}) = 4 \times REF \times \frac{VDAC}{2^{10}}$$

In equation 1, VDAC is the decimal equivalent of the binary number represented by bits D13, D12, D11, D10, D9, D8, D7, D6, D5, and D4 programmed with the ChargingVoltage( ) command. For example, if D4–D13 are all set, VDAC is the decimal equivalent of 0b1111111111 (1023). If either D15 or D14, or both D15 and D14, are set, all the bits in the voltage DAC (Figure 6a) are set, regardless of D13–D0, and the status register's VOLTAGE_OR bit is set. For D15 = 1 and/or D14 = 1:

$$VOLTAGE_OR = 1 \text{ and } V0\,(\text{in Volts}) = 4 \times REF \times \frac{2^{10}-1}{2^{10}}$$

Table 2. ChargerMode( ) Bit Functions

BIT NAME	BIT POSITION*	POR VALUE**	FUNCTION
INHIBIT_CHARGE	0	0	0 = Allow normal operation; clear the CHG_INHIBITED status bit. 1 = Turn the charger off; set the CHG_INHIBITED status bit.
ENABLE_POLLING	1	—	Not implemented. Write 0 into this bit.
POR_RESET	2	—	0 = No change in any non-ChargerMode( ) settings. 1 = Change the voltage and current settings to 0xFFFF and 0x00C0 respectively; clear the THERMISTOR_HOT and ALARM_INHIBITED bits.
RESET_TO_ZERO	3	—	Not implemented. Write 0 into this bit.
N/A	4, 7, 8, 9, 11–15	—	Not implemented. Write 1 into this bit.
BATTERY_PRESENT_MASK	5	0	0 = Interrupt on either edge of the BATTERY_PRESENT status bit. 1 = Do not interrupt because of a BATTERY_PRESENT bit change.
POWER_FAIL_MASK	6	1	0 = Interrupt on either edge of the POWER_FAIL status bit. 1 = Do not interrupt because of a POWER_FAIL bit change.
HOT_STOP	10	1	0 = The THERMISTOR_HOT status bit does not turn the charger off. 1 = THERMISTOR_HOT turns the charger off.

**Bit position in the D15–D0 data.* ***Power-on reset value.*

N/A = Not available.

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Figure 8 shows the mapping between V0 (the voltage-regulation-loop set point) and the ChargingVoltage( ) data.

The power-on reset value for the ChargingVoltage( ) register is 0xFFF0; thus, the first time a MAX1647 is powered on, the BATT voltage regulates to 16.368V with V_{REF} = 4.096V. Any time the BATTERY_PRESENT status bit is clear, the ChargingVoltage( ) register returns to its power-on reset state.

ChargingCurrent( )

The ChargingCurrent( ) command uses Write-Word protocol. The command code for ChargingCurrent( ) is 0x14; thus, the CMD7–CMD0 bits in Write-Word protocol should be 0b00010100. The 16-bit binary number formed by D15–D0 represents the current-limit set point (I0) in milliamps. Tying SEL to AGND selects a 1.023A maximum setting for I0. Leaving SEL open selects a 2.047A maximum setting for I0. Tying SEL to VL selects a 4.095A maximum setting for I0.

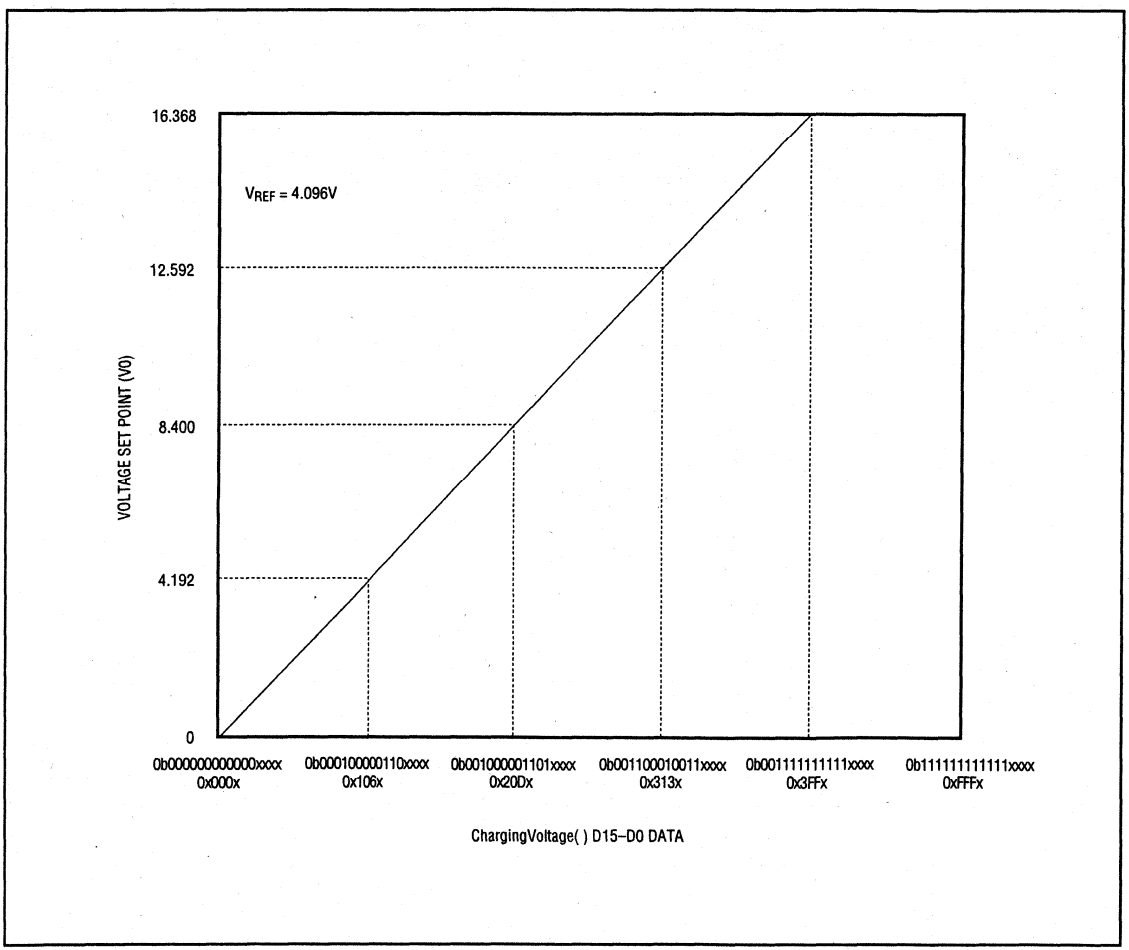

Figure 8. ChargingVoltage( ) Data to Voltage Mapping

Two sources of current in the MAX1647 charge the battery: a binary-weighted linear current source sources from IOUT, and a switching regulator controls the current flowing through the current-sense resistor (R1). IOUT provides a small maintenance charge current to compensate for battery self-discharge, while the switching regulator provides large currents for fast charging.

IOUT sources from 1mA to 31mA. Table 3 shows the relationship between the value programmed with the ChargingCurrent( ) command and IOUT source current. The CCV_LOW comparator checks to see if the output voltage is too high by comparing CCV to REF / 4. If CCV_LOW = 1 (when CCV < REF / 4), IOUT shuts off, preventing the output voltage from exceeding the voltage set point specified by the ChargingVoltage( ) register. VOLTAGE_NOTREG = 1 whenever the internal clamp pulls down on CCV. (The internal clamp pulls down on CCV to keep its voltage close to CCI's voltage.)

Table 3. Relationship Between IOUT Source Current and ChargingCurrent( ) Value

CHARGE_ INHIBITED	(NOTE 1)	ALARM_ INHIBITED	ChargingVoltage( )	ChargingCurrent( )	CCV_LOW	VOLTAGE_ NOTREG	IOUT OUTPUT CURRENT
0	0	0	0x0010–0xFFFF	0x0001–0x001F	0	x	1mA–31mA
0	0	0	0x0010–0xFFFF	0x0001–0x001F	1	0	0mA
0	0	0	0x0010–0xFFFF	0x0001–0x001F	1	1	1mA–31mA
0	0	0	0x0010–0xFFFF	0x0020–0xFFFF	0	x	31mA
0	0	0	0x0010–0xFFFF	0x0020–0xFFFF	1	0	0mA
0	0	0	0x0010–0xFFFF	0x0020–0xFFFF	1	1	31mA
0	0	0	x	0x0000	x	x	0mA
0	0	0	0x0000–0x000F	x	x	x	0mA
0	x	1	x	x	x	x	0mA
0	1	x	x	x	x	x	0mA
1	x	x	x	x	x	x	0mA

Note 1: Logical AND of THERMISTOR_HOT, HOT_STOP, NOT(THERMISTOR_UR).

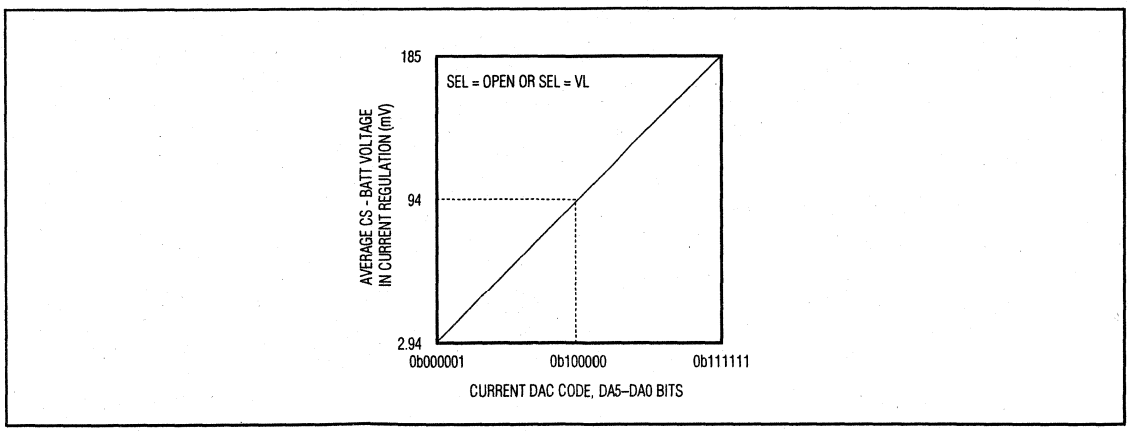

Figure 9. Average Voltage Between CS and BATT vs. Current DAC Code

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Table 4. Relationship Between Current DAC Code and the ChargingCurrent( ) Value

CHARGE_ INHIBITED	(NOTE 1)	ALARM_ INHIBITED	ChargingVoltage( )	SEL	ChargingCurrent( )	CURRENT DAC CODE	SW REG ON?	(NOTE 2)
0	0	0	0x0010–0xFFFF	0V	0x0001–0x001F	0	No	0
0	0	0	0x0010–0xFFFF	0V	0x0020–0x003F	2	Yes	0
0	0	0	0x0010–0xFFFF	0V	0x0040–0x03DF	4–60	Yes	0
0	0	0	0x0010–0xFFFF	0V	0x03E0–0x03FF	62	Yes	0
0	0	0	0x0010–0xFFFF	0V	0x0400–0xFFFF	62	Yes	1
0	0	0	0x0010–0xFFFF	open	0x0001–0x001F	0	No	0
0	0	0	0x0010–0xFFFF	open	0x0020–0x003F	1	Yes	0
0	0	0	0x0010–0xFFFF	open	0x0040–0x07DF	2–62	Yes	0
0	0	0	0x0010–0xFFFF	open	0x07E0–0x07FF	63	Yes	0
0	0	0	0x0010–0xFFFF	open	0x0800–0xFFFF	63	Yes	1
0	0	0	0x0010–0xFFFF	VL	0x0001–0x001F	0	No	0
0	0	0	0x0010–0xFFFF	VL	0x0020–0x003F	1	Yes	0
0	0	0	0x0010–0xFFFF	VL	0x0040–0x007F	1	Yes	0
0	0	0	0x0010–0xFFFF	VL	0x0080–0x0F9F	2–62	Yes	0
0	0	0	0x0010–0xFFFF	VL	0x0FA0–0x0FBF	63	Yes	0
0	0	0	0x0010–0xFFFF	VL	0x0FC0–0x0FFF	63	Yes	0
0	0	0	0x0010–0xFFFF	VL	0x0001–0xFFFF	63	Yes	1
0	0	0	x	x	0x0000	0	No	0
0	0	0	0x0010–0xFFFF	x	x	N/C	No	N/C
0	x	1	x	x	x	N/C	No	N/C
0	1	x	x	x	x	N/C	No	N/C
1	x	x	x	x	x	N/C	No	N/C

Note 1: Logical AND of THERMISTOR_HOT, HOT_STOP, NOT(THERMISTOR_UR).
Note 2: Value of CURRENT_OR bit in the ChargerStatus( ) register.
N/C = No change

Table 5. Effect of SEL Pin-Strapping on the ChargingCurrent( ) Data Bits

SEL	R1 (mΩ)	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
AGND	181	0	0	0	0	0	0	DA5	DA4	DA3	DA2	DA1	I4	I3	I2	I1	I0
Open	90	0	0	0	0	0	DA5	DA4	DA3	DA2	DA1	DA0	I4	I3	I2	I1	I0
VL	45	0	0	0	0	DA5	DA4	DA3	DA2	DA1	DA0	*	I4	I3	I2	I1	I0

**When SEL = VL, D5 = 1 forces DA0 to be 1 regardless of the D6 bit value.*

With the switching regulator on, the current through R1 (Figure 3) is regulated by sensing the average voltage between CS and BATT. A 6-bit current DAC controls the current-limit set point. DA5–DA0 denote the bits in the current DAC code. Figure 9 shows the relationship between the current DAC code and the average voltage between CS and BATT.

When the switching regulator is off, DHI is forced to LX and DLO is forced to ground. This prevents current from flowing through inductor L1. Table 4 shows the relationship between the ChargingCurrent( ) register value and the switching regulator current DAC code.

With SEL = AGND, R1 should be as close as possible to 0.185 / 1.023 = 181mΩ to ensure that the actual output current matches the data value programmed with the ChargingCurrent( ) command. With SEL = open, R1 should be as close as possible to 90mΩ. With SEL = VL, R1 should be as close as possible to 45mΩ. Table 5 summarizes how SEL affects the R1 value and the meaning of data bits D15–D0 in the ChargingCurrent( ) command. DA5–DA0 denote the current DAC code bits, and I4–I0 denote the IOUT linear-current source binary weighting bits. Note that whenever any current DAC bits are set, the linear-current source is set to full scale (31mA).

The power-on reset value for the ChargingCurrent( ) register is 0x000C. Irrespective of the SEL pin setting, the MAX1647 powers on with I0 set to 12mA (i.e., DA5–DA0, I1, and I0 all equal to zero, and only I3 and I2 set). Anytime the BATTERY_PRESENT status bit is clear (battery removed), the ChargingCurrent( ) register returns to its power-on reset state. This ensures that upon insertion of a battery, the initial charging current is 12mA.

AlarmWarning( )

The AlarmWarning( ) command uses Write-Word protocol. The command code for AlarmWarning( ) is 0x16; thus the CMD7–CMD0 in Write-Word protocol should be 0b00010110. The AlarmWarning( ) command sets the ALARM_INHIBITED status bit in the MAX1647 if D15, D14, or D12 of the Write-Word protocol data equals 1. Table 6 summarizes the AlarmWarning( ) command's function. The ALARM_INHIBITED status bit remains set until BATTERY_PRESENT = 0 (battery removed) or a ChargerMode() command is written with the POR_RESET bit set. As long as ALARM_INHIBITED = 1, the MAX1647 switching regulator and IOUT current source remain off.

ChargerStatus( )

The ChargerStatus( ) command uses Read-Word protocol. The command code for ChargerStatus( ) is 0x13; thus, the CMD7–CMD0 bits in Write-Word protocol should be 0b00010011. The ChargerStatus( ) command returns information about thermistor impedance and the MAX1647's internal state. The Read-Word protocol returns D15–D0 (Figure 7). Table 7 describes the meaning of the individual bits. The latched bits, THERMISTOR_HOT and ALARM_INHIBITED, are cleared whenever BATTERY_PRESENT = 0 or ChargerMode( ) is written with POR_RESET = 1.

Interrupts and the Alert-Response Address

An interrupt is triggered ($\overline{INT}$ goes low) whenever power is applied to DCIN, the BATTERY_PRESENT bit changes, or the POWER_FAIL bit changes. BATTERY_PRESENT and POWER_FAIL have interrupt masks that can be set or cleared via the ChargerMode( ) command. $\overline{INT}$ stays low until the interrupt is cleared. There are two methods for clearing the interrupt: issuing a ChargerStatus( ) command, and using the Receive Byte protocol with a 0x19 Alert-Response address. The MAX1647 responds to the Alert-Response address with the 0x89 byte.

Applications Information

Using the MAX1647 with Duracell Smart Batteries

The following pseudo-code describes an interrupt routine that is triggered by the MAX1647 $\overline{INT}$ output going low. This interrupt routine keeps the host informed of any changes in battery-charger status, such as DCIN power detection, or battery removal and insertion.

DOMAX1647:
{ This is the beginning of the routine that handles MAX1647 interrupts. }

{ Check the status of the MAX1647. }
TEMPWORD = ReadWord(SMBADDR = 0b00010011 = 0x13, COMMAND = 0x13)

{ Check for the normal power-up case without a battery installed. THERMISTOR_OR = 1, BATTERY_PRESENT = 0. Use 0b1011111011111111 = 0xBEFF as the mask. }

IF (TEMPWORD OR 0xBEFF) = 0xBFFF THEN GOTO NOBATT:

{ Check to see if the battery is installed. BATTERY_PRESENT = 1. Use 0b1011111111111111 = 0xBFFF as the mask. }

Table 6. Effect of the AlarmWarning( ) Command

AlarmWarning( ) WRITE-WORD PROTOCOL DATA																RESULT
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED
x	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED
x	x	x	1	x	x	x	x	x	x	x	x	x	x	x	x	Set ALARM_INHIBITED

Chemistry-Independent Battery Chargers

IF (TEMPWORD OR 0xBEFF) = 0xFFFF THEN GOTO HAVEBATT:
GOTO ENDINT:
HAVEBATT:
{ A battery is installed. Turn the battery's broadcast mode off to monitor the charging process. Using the BatteryMode( ) command, make sure the CHARGER_MODE bit is set. }
WriteWord(SMBADDR = 0b00010110 = 0x16, COMMAND = 0X03, DATA = 0x4000)
GOTO ENDINT:
NOBATT:
{ Notify the system that AC power is present, but no battery is present. }
GOTO ENDINT:
ENDINT:
{ This is the end of the interrupt routine. }

The following pseudo-code describes a polling routine that queries the battery for its desired charge voltage and charge current, checks to make sure that the requested charge current and charge voltage are valid, and instructs the MAX1647 to comply with the request.

DOPOLLING:
{ This is the beginning of the polling routine. }
{ Ask the battery what voltage it wants using the battery's ChargingVoltage( ) command. }
TEMPVOLTAGE = ReadWord(SMBADDR = 0b00010111 = 0x17, COMMAND = 0x15)
{ Ask the battery what current it wants using the battery's ChargingCurrent( ) command. }
TEMPCURRENT = ReadWord(SMBADDR = 0b00010111 = 0x17, COMMAND = 0x14)
{ Now the routine can check that the TEMPVOLTAGE and TEMPCURRENT values make sense and that the battery is not malfunctioning. }
{ With valid TEMPVOLTAGE and TEMPCURRENT values, instruct the MAX1647 to comply with the request. }
WriteWord(SMBADDR = 0b00010010 = 0x12 , COMMAND = 0x15, DATA = TEMPVOLTAGE)
WriteWord(SMBADDR = 0b00010010 = 0x12 , COMMAND = 0x14, DATA = TEMPCURRENT)
ENDPOL:
{ This is the end of the polling routine. }

Negative Input Voltage Protection

In most portable equipment, the DC power to charge batteries enters via a two-conductor cylindrical power jack. It is easy for the end user to add an adapter to switch the DC power's polarity. Polarized capacitor C6 would be destroyed if a negative voltage were applied. Diode D4 in Figure 3 prevents this from happening.

If reverse-polarity protection for the DC input power is not necessary, diode D4 can be omitted. This eliminates the power lost due to the voltage drop on diode D4.

Selecting External Components for the MAX1647 4A Application

The MAX1647 can be configured to charge at a maximum current of 4A (instead of 2A, as shown in Figure 3) by changing the external power components and tying SEL to REF. The following paragraphs discuss the selection requirements for each component in Figure 3 that must be changed to accommodate the 4A application.

Diode D4 in Figure 3 has to support both the charge current and the current required to operate the host load (i.e., what the batteries normally power when not charging). This means that the continuous current flowing through D4 exceeds 4A. One possible choice for D4 is the Motorola MBRD835L 8A Schottky barrier diode in a DPAK surface-mount package. Care must be taken in thermal management of the circuit board when using the 4A application circuit, by mounting D4 on a three-square-inch piece of copper.

Motorola's MBRD835L can also be used for D3. The Siliconix Si4410DY is a good choice for M1 and M2 in the 4A application. Changing M2 from a 2N7002 (Table 1) to a Si4410DY increases the power dissipated by the MAX1647's 20-pin SSOP.

High-current inductors are difficult to find in surface-mount packages. Low-cost solutions use toroidal powdered-iron cores with exposed windings of heavy-gauge wire. The Coiltronics CTX20-5-52 20µH 5A inductor provides a high-efficiency solution.

R1A must also dissipate more power in the 4A application circuit than in the circuit of Figure 3. R1A's value decreases to 50mΩ in the 4A application. IRC's LR2512-01-R050-F meets this requirement with a 1W maximum power-dissipation rating.

Table 7. ChargerStatus( ) Bit Descriptions

NAME	BIT POSITION	LATCHED?	DESCRIPTION
CHARGE_INHIBITED	0	Yes	0 = Ready to charge a smart battery 1 = Charger is off; IOUT current = 0mA; DLO = PGND; DHI = LX
MASTER_MODE	1	N/A	Always returns '0'
VOLTAGE_NOTREG	2	No	0 = BATT voltage is limited at the voltage set point (BATT = V0). 1 = BATT voltage is less than the voltage set point (BATT < V0).
CURRENT_NOTREG	3	No	0 = Current through R1 is at its limit (I_{BATT} = I0). 1 = Current through R1 is less than its limit (I_{BATT} < I0).
LEVEL_2	4	N/A	Always returns 1
LEVEL_3	5	N/A	Always returns 0
CURRENT_OR	6	No	0 = ChargingCurrent( ) value is valid for MAX1647. 1 = ChargingCurrent( ) value exceeds what MAX1647 can actually deliver.
VOLTAGE_OR	7	No	0 = ChargingVoltage( ) value is valid for MAX1647. 1 = ChargingVoltage( ) value exceeds what MAX1647 can actually deliver.
THERMISTOR_OR	8	No	0 = THM voltage < 91% of REF voltage 1 = THM voltage > 91% of REF voltage
THERMISTOR_COLD	9	No	0 = THM voltage < 75% of REF voltage 1 = THM voltage > 75% of REF voltage
THERMISTOR_HOT	10	Yes	This bit reports the state of an internal SR flip-flop (denoted THERMISTOR_HOT flip-flop). The THERMISTOR_HOT flip-flop is set whenever THM is below 23% of REF. It is cleared whenever BATTERY_PRESENT = 0 or ChargerMode( ) is written with POR_RESET = 1.
THERMISTOR_UR	11	No	0 = THM voltage > 5% of REF voltage 1 = THM voltage < 5% of REF voltage
ALARM_INHIBITED	12	Yes	This bit reports the state of an internal SR flip-flop (denoted ALARM_INHIBITED flip-flop). The ALARM_INHIBITED flip-flop is set whenever the AlarmWarning( ) command is written with D15, D14, or D12 set. The ALARM_INHIBITED flip-flop is cleared whenever BATTERY_PRESENT = 0 or ChargerMode( ) is written with POR_RESET = 1.
POWER_FAIL	13	No	0 = BATT voltage < 89% of DCIN voltage 1 = BATT voltage > 89% of DCIN voltage
BATTERY_PRESENT	14	No	0 = No battery is present (THERMISTOR_OR = 1). 1 = A battery is present (THERMISTOR_OR = 0).
AC_PRESENT	15	No	0 = VL voltage < 4V 1 = VL voltage > 4V

**Bit position in the D15-D0 data*
N/A = Not applicable

Chip Information

TRANSISTOR COUNT: 3612

SUBSTRATE CONNECTED TO AGND

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

High-Efficiency, PWM, Step-Down DC-DC Controllers in QSOP Packages

General Description

The MAX1652–MAX1655 are high-efficiency, pulse-width-modulated (PWM), step-down DC-DC controllers in small QSOP packages. The MAX1653/MAX1655 also come in 16-pin narrow SO packages that are pin-compatible upgrades to the popular MAX797. Improvements include higher duty-cycle operation for better dropout, lower quiescent supply currents for better light-load efficiency, and a lower output voltage range.

The MAX1652–MAX1655 achieve up to 96% efficiency and deliver up to 10A using a unique Idle Mode™ synchronous-rectified PWM control scheme. These devices automatically switch between PWM operation at heavy loads and pulse-frequency-modulated (PFM) operation at light loads to optimize efficiency over the entire output current range. Both external power switches are inexpensive n-channel MOSFETs, which provide low resistance while saving space and reducing cost.

The MAX1653/MAX1655 permit the user to override the automatic PWM/PFM setting with a logic signal for noise-sensitive applications. All devices operate with a selectable 150kHz/300kHz switching frequency, which can also be adjusted from 190kHz to 340kHz with an external clock signal.

The MAX1652/MAX1654 have an additional feedback pin, which permits regulation of a low-cost second output tapped from a transformer winding. The MAX1652 provides an additional positive output. The MAX1654 provides an additional negative output.

The MAX1652–MAX1654 have a 4.5V to 28V input range. The MAX1652/MAX1653/MAX1654's output range is 2.5V to 5.5V. The MAX1655's output range extends down to 1V. The MAX1653EVKIT is available to speed designs.

Applications

Notebook Computers
PDAs
Cellular Phones
Hand-Held Computers
Handy-Terminals
Mobile Communicators
Distributed Power

Features

- **96% Efficiency**
- **Small, 16-Pin QSOP Package (half the size of a 16-pin narrow SO)**
- **Pin-Compatible with MAX797 (MAX1653/MAX1655)**
- **Output Voltage Down to 1V (MAX1655)**
- **4.5V to 28V Input Range**
- **98% Duty Cycle for Lower Dropout**
- **170µA Quiescent Supply Current**
- **3µA Logic-Controlled Shutdown**
- **Dual, N-Channel, Synchronous-Rectified Control**
- **Fixed 150kHz/300kHz PWM Switching (or synched from 190kHz to 340kHz)**
- **Programmable Soft Start**
- **Low-Cost Secondary Outputs (MAX1652/MAX1654)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1652C/D	0°C to +70°C	Dice*
MAX1652EEE	-40°C to +85°C	16 QSOP
MAX1653C/D	0°C to +70°C	Dice*
MAX1653ESE	-40°C to +85°C	16 Narrow SO
MAX1653EEE	-40°C to +85°C	16 QSOP
MAX1654C/D	0°C to +70°C	Dice*
MAX1654EEE	-40°C to +85°C	16 QSOP
MAX1655C/D	0°C to +70°C	Dice*
MAX1655ESE	-40°C to +85°C	16 Narrow SO
MAX1655EEE	-40°C to +85°C	16 QSOP

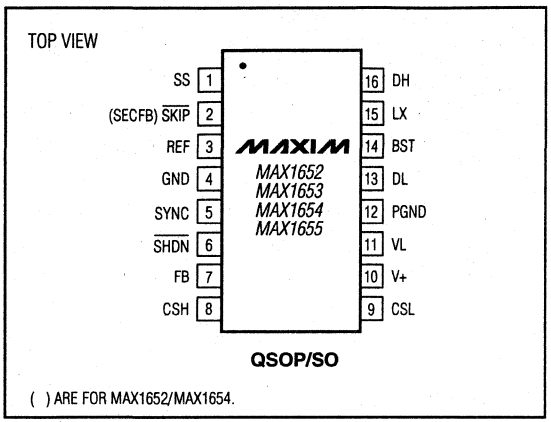
**Contact factory for dice specifications.*

Idle Mode is a trademark of Maxim Integrated Products.

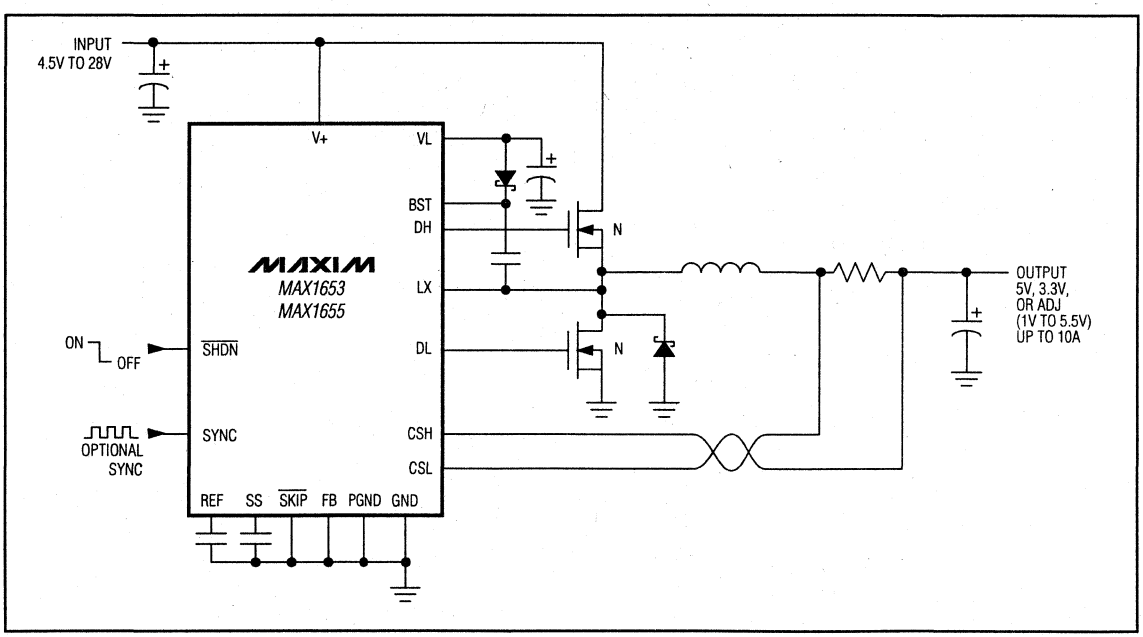
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

High-Efficiency, PWM, Step-Down DC-DC Controllers in QSOP Packages

Pin Configuration



Typical Operating Circuit



19-1263; Rev 0; 7/97

MAXIM

350mA, 16.5V Input, Low-Dropout Linear Regulators

General Description

The MAX1658/MAX1659 linear regulators maximize battery life by combining ultra-low supply currents and low dropout voltages. They feature Dual Mode™ operation, which presets the output to 3.3V (MAX1658) or 5V (MAX1659), or permits it to be adjusted between 1.25V and 16V. The regulator supplies up to 350mA, with a typical dropout of 650mV for the MAX1658 and 490mV for the MAX1659. With their P-channel MOSFET pass transistor, these devices maintain a low quiescent current from zero output current to the full 350mA, even in dropout. They support input voltages ranging from 2.7V to 16.5V.

The MAX1658/MAX1659 feature a 1µA shutdown mode, reverse battery protection, short-circuit protection, and thermal shutdown. They are available in a special high-power (1.2W), 8-pin SO package designed specifically for compact applications.

Applications

Digital Cordless Phones
PCS Phones
Cellular Phones
PCMCIA Cards
Modems
Hand-Held Instruments
Palmtop Computers
Electronic Planners

Features

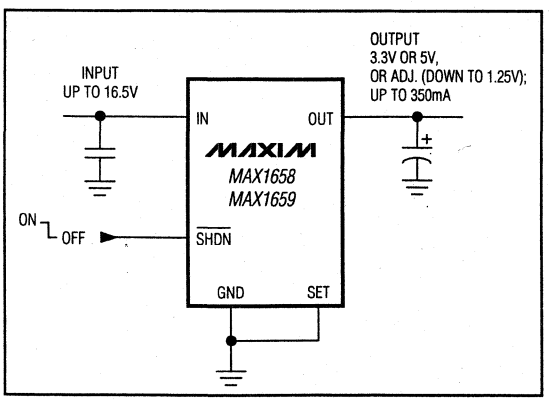
- ♦ **Wide Input Voltage Range: 2.7V to 16.5V**
- ♦ **Low, 490mV Dropout at 350mA Output Current (MAX1659)**
- ♦ **30µA Supply Current**
- ♦ **1µA Max Shutdown Current**
- ♦ **High-Power (1.2W) 8-Pin SO Package**
- ♦ **Dual Mode Operation Output:**
  Fixed 3.3V (MAX1658)
  Fixed 5.0V (MAX1659)
  or Adjustable (1.25V to 16V)
- ♦ **Thermal Overload Protection**
- ♦ **Current-Limit Protection**
- ♦ **Reverse Battery Protection**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1658C/D	0°C to +70°C	Dice*
MAX1658ESA	-40°C to +85°C	8 SO
MAX1659C/D	0°C to +70°C	Dice*
MAX1659ESA	-40°C to +85°C	8 SO

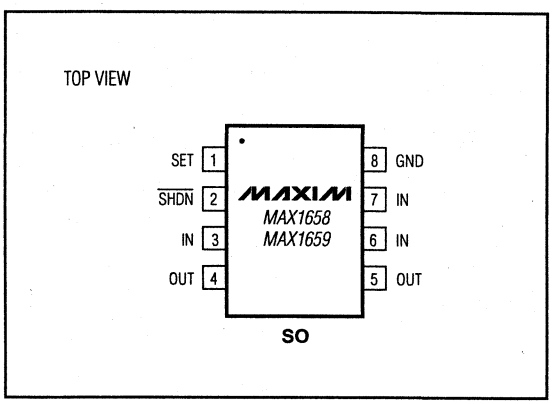
**Dice are tested at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



Dual Mode is a trademark of Maxim Integrated Products.

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

350mA, 16.5V Input, Low-Dropout Linear Regulators

ABSOLUTE MAXIMUM RATINGS

IN to GND .....-17V to +17V
Continuous Output Current 500mA
Output Short-Circuit Duration .....Infinite
SET, $\overline{SHDN}$ to GND .....-17V to +17V
OUT to GND .....-0.3V to (VIN + 0.3V)
Continuous Power Dissipation (Note 1)
SO (derate 14.5mW/°C above +70°C) 1.2W

Operating Temperature Range
MAX1658ESA/MAX1659ESA .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature Range (soldering, 10sec).....+300°C

Note 1: See *Operating Region and Power Dissipation* section.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5V (MAX1658), V_{IN} = 6V (MAX1659); C_{OUT} = 10µF; $\overline{SHDN}$ = IN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	SET = OUT		2.7		16.5	V
Output Voltage	V_{OUT}	SET = GND, 0mA < I_{LOAD} < 350mA	MAX1658, 5V ≤ V_{IN} ≤ 16.5V	3.20	3.30	3.40	V
			MAX1659, 6V ≤ V_{IN} ≤ 16.5V	4.85	5.00	5.15	
Regulated Output Voltage Range		(Note 3)		1.25		16	V
Maximum Output Current	$I_{OUT(MAX)}$			350			mA
Current Limit	I_{LIM}				900		mA
Supply Current	I_Q				30	60	µA
Dropout Voltage (Note 4)	ΔV_{DO}	I_{OUT} = 1mA			2		mV
		I_{OUT} = 350mA	MAX1658		650	1500	
			MAX1659		490	875	
Line Regulation	ΔV_{LNR}	MAX1658, V_{IN} = 5V to 16.5V			0.03		%/V
		MAX1659, V_{IN} = 6V to 16.5V			0.05		
Load Regulation	ΔV_{LDR}	I_{OUT} = 0mA to 350mA			0.003		%/mA
Startup Overshoot	V_{OSH}				0		$\%V_{OUT}$
Output Noise	e_n	10Hz to 100kHz			2.5		mVp-p
SHUTDOWN							
Logic-Low Input	$V_{INL\overline{SHDN}}$	2.7V ≤ V_{IN} ≤ 16.5V				0.4	V
Logic-High Input Threshold	$V_{INH\overline{SHDN}}$	2.7V ≤ V_{IN} ≤ 16.5V		2.0			V
Shutdown Input Bias Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND or $\overline{SHDN}$ = IN			0.1		µA
Shutdown Supply Current	$I_{Q\overline{SHDN}}$	$\overline{SHDN}$ ≤ 0.4V			0.1	1	µA
Shutdown Exit Time	t_{START}	V_{OUT} = 5.0V			120		µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 5V (MAX1658), V_{IN} = 6V (MAX1659); C_{OUT} = 10µF; $\overline{SHDN}$ = IN; T_A = T_{MIN} to T_{MAX}; unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

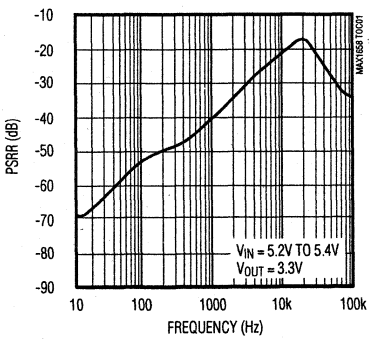
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SET INPUT						
SET Reference Voltage	V_{SET}	I_{OUT} = 10µA (Note 3)	1.174	1.210	1.246	V
SET Input Leakage Current	I_{SET}	T_A = +25°C (Note 3)		0.01	0.025	µA
		T_A = +85°C (Note 3)		0.1		
THERMAL PROTECTION						
Thermal Shutdown Temperature	T_{SD}			165		°C
Thermal Shutdown Hysteresis	ΔT_{SD}			10		°C

Note 2: Specifications to -40°C are guaranteed by design, not production tested.
Note 3: Adjustable configuration only. V_{IN} = 16.5V.
Note 4: The dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 2V.

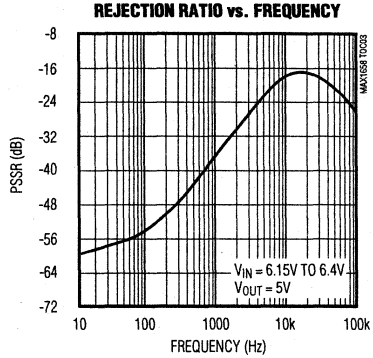
Typical Operating Characteristics

(V_{IN} = 5V (MAX1658), V_{IN} = 6V (MAX1659); $\overline{SHDN}$ = IN; SET = GND; C_{IN} = 0.1µF; C_{OUT} = 10µF tantalum; T_A = +25°C; unless otherwise noted.)

MAX1658
POWER-SUPPLY
REJECTION RATIO vs. FREQUENCY



MAX1659
POWER-SUPPLY
REJECTION RATIO vs. FREQUENCY

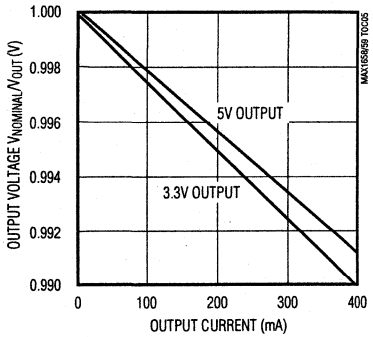


350mA, 16.5V Input, Low-Dropout Linear Regulators

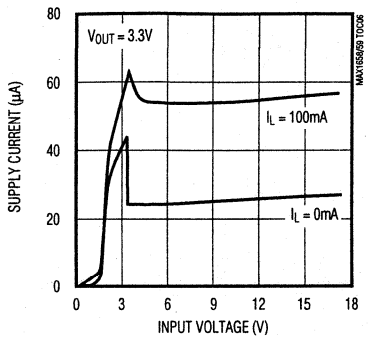
Typical Operating Characteristics (continued)

(V_{IN} = 5V (MAX1658), V_{IN} = 6V (MAX1659); $\overline{SHDN}$ = IN; SET = GND; C_{IN} = 0.1µF; C_{OUT} = 10µF tantalum; T_A = +25°C; unless otherwise noted.)

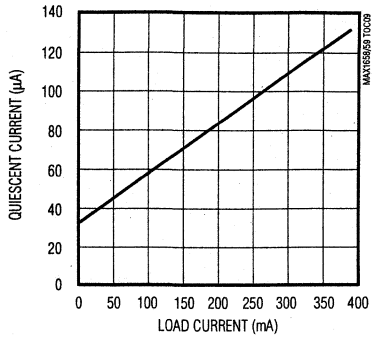
NORMALIZED OUTPUT VOLTAGE vs. LOAD CURRENT



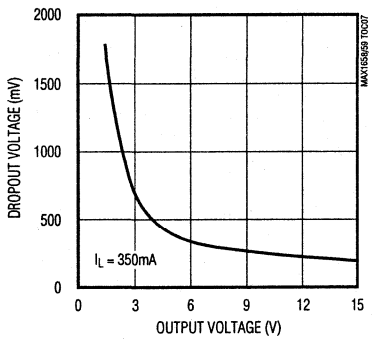
MAX1658 SUPPLY CURRENT vs. INPUT VOLTAGE



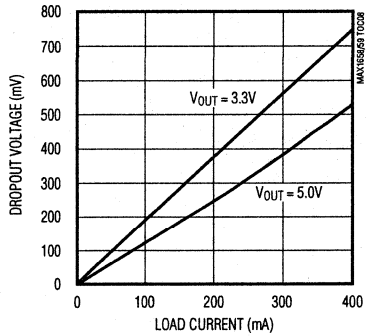
QUIESCENT CURRENT vs. LOAD CURRENT



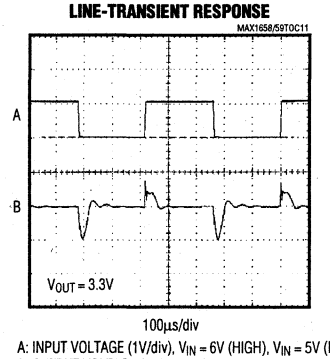
DROPOUT VOLTAGE vs. OUTPUT VOLTAGE



DROPOUT VOLTAGE vs. LOAD CURRENT

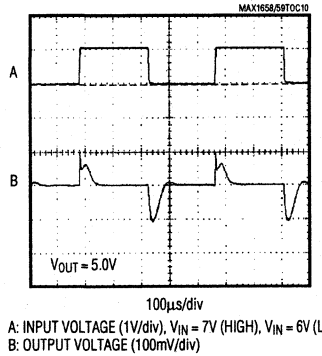


MAX1658 LINE-TRANSIENT RESPONSE



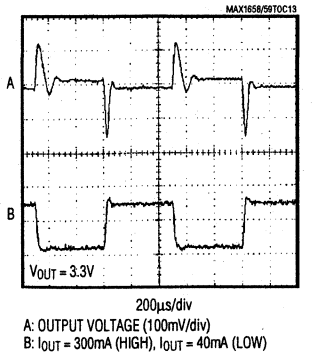
A: INPUT VOLTAGE (1V/div), V_{IN} = 6V (HIGH), V_{IN} = 5V (LO\
B: OUTPUT VOLTAGE (100mV/div)

MAX1659 LINE-TRANSIENT RESPONSE



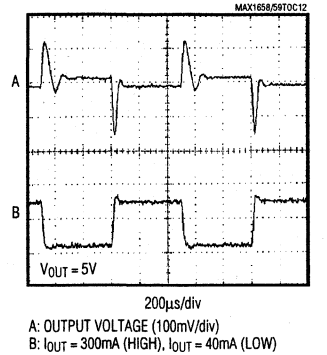
A: INPUT VOLTAGE (1V/div), V_{IN} = 7V (HIGH), V_{IN} = 6V (LOW)
B: OUTPUT VOLTAGE (100mV/div)

MAX1658 LOAD-TRANSIENT RESPONSE



A: OUTPUT VOLTAGE (100mV/div)
B: I_{OUT} = 300mA (HIGH), I_{OUT} = 40mA (LOW)

MAX1659 LOAD-TRANSIENT RESPONSE

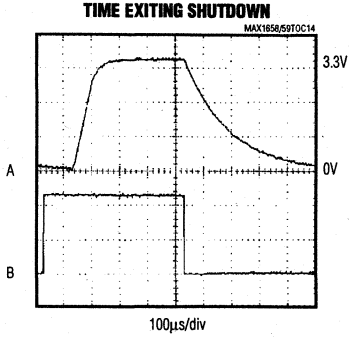


A: OUTPUT VOLTAGE (100mV/div)
B: I_{OUT} = 300mA (HIGH), I_{OUT} = 40mA (LOW)

Typical Operating Characteristics (continued)

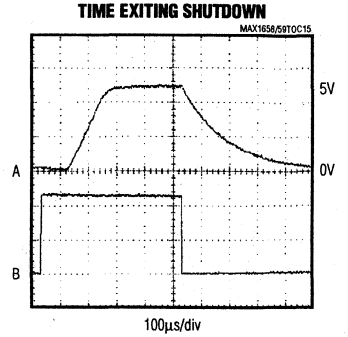
(V_{IN} = 5V (MAX1658), V_{IN} = 6V (MAX1659); $\overline{SHDN}$ = IN; SET = GND; C_{IN} = 0.1µF; C_{OUT} = 10µF tantalum; T_A = +25°C; unless otherwise noted.)

MAX1658 OVERSHOOT AND TIME EXITING SHUTDOWN



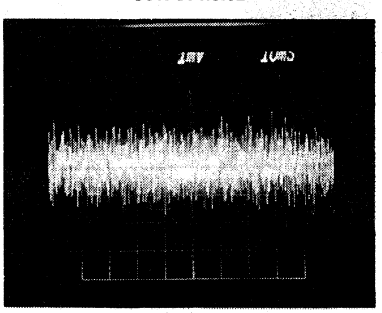
A: OUTPUT VOLTAGE (1V/div)
B: $\overline{SHDN}$ PIN VOLTAGE (2V/div)

MAX1659 OVERSHOOT AND TIME EXITING SHUTDOWN



A: OUTPUT VOLTAGE (2V/div)
B: $\overline{SHDN}$ PIN VOLTAGE (2V/div)

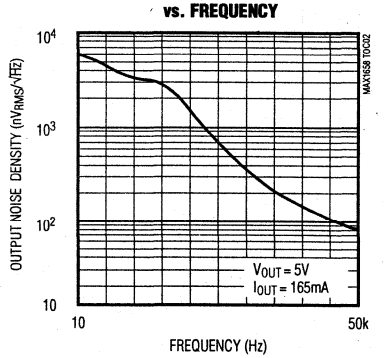
OUTPUT NOISE



10ms/div

10Hz TO 100kHz NOISE, V_{OUT} = 5V (1mV/div), I_{OUT} = 165mA

OUTPUT NOISE DENSITY vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	SET	Output Voltage Input. Connecting SET to ground selects the factory-preset 3.3V (MAX1658) or 5V (MAX1659) output voltage. For an adjustable output voltage, connect SET to a resistive voltage divider from OUT to GND.
2	$\overline{SHDN}$	Shutdown Input. When $\overline{SHDN}$ is low, the device turns off and typically draws 0.1µA of supply current.
3, 6, 7	IN	Unregulated Input Supply Voltage, 2.7V to 16.5V input range. The IN pins also serve as heatsinks. Connect to a copper plane to achieve maximum thermal dissipation.
4, 5	OUT	Regulated Output Voltage. Fixed or adjustable from 1.25V to 16V. Sources up to 350mA. For stable operation, bypass with a 10µF, low-ESR (<0.2Ω) capacitor from OUT to GND. For improved load-transient response, use a larger low-ESR capacitor.
8	GND	Ground

350mA, 16.5V Input, Low-Dropout Linear Regulators

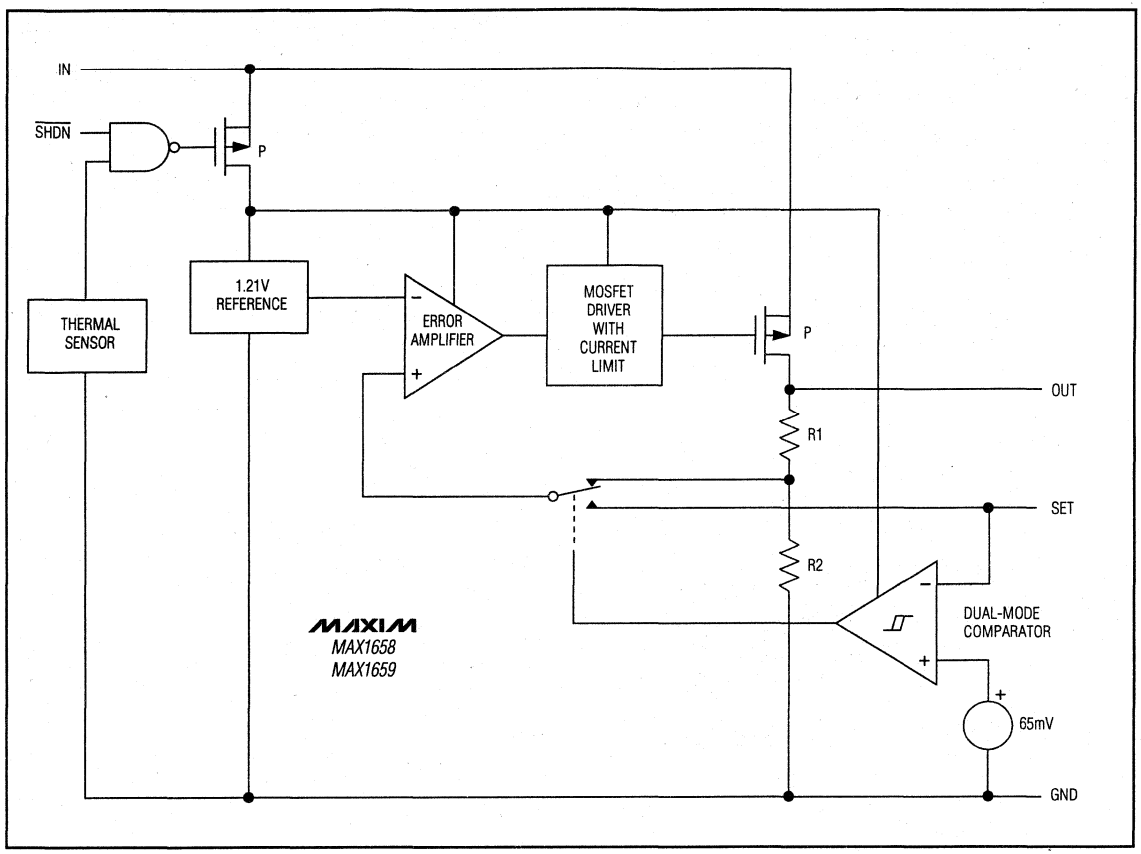


Figure 1. Functional Diagram

Detailed Description

The MAX1658/MAX1659 are micropower, low-dropout linear regulators featuring Dual Mode™ operation, which allows them to deliver an adjustable (1.25V to 16.5V) or preset (3.3V for the MAX1658, 5V for MAX1659) output. They supply up to 350mA while requiring only 120µA of supply current (typically 30µA with no load). The devices include thermal shutdown circuitry, output current limiting, a P-channel pass transistor, a Dual Mode comparator, and a feedback voltage divider. Figure 1 shows the functional diagram.

The 1.21V reference is connected to the amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The error signal applies the drive to the P-channel pass transistor. If the feedback voltage is lower than the reference voltage, the transistor's gate is pulled lower, increasing output current.

The output voltage is fed back through an internal resistor network or an external user-selected network. The Dual Mode comparator examines the voltage at the SET pin and selects either the internal or external feedback path. If SET is below 65mV, internal feedback sets the MAX1658's output voltage to 3.3V and the MAX1659's to 5V. Otherwise, external feedback is used for an adjustable output between 1.25V and 16.5V. Additional features include internal current limiting, reverse battery protection, thermal-overload protection, and a 1µA shutdown mode.

350mA, 16.5V Input, Low-Dropout Linear Regulators

P-Channel Pass Transistor

The MAX1658/MAX1659 feature an internal P-channel MOSFET pass transistor. Using a MOSFET provides several advantages over similar PNP designs, including lower dropout voltage and extended battery life. Unlike bipolar transistors, MOSFETs reduce quiescent current, because they require no base current, particularly at heavy loads and in dropout. As a result, the MAX1658/MAX1659 operate at a low quiescent current even in dropout.

Output Voltage Selection

Dual Mode operation allows the MAX1658/MAX1659 to operate at either a preset or a user-adjustable output voltage. The device compares the SET pin voltage with an internal 65mV reference. If the voltage is lower than 65mV (typically achieved by grounding SET), the device switches to an internal resistor-divider feedback network that sets the output voltage. The MAX1658's preset output voltage is 3.3V and the MAX1659's is 5V (Figure 2).

If the SET pin is not below 65mV, the device switches to external feedback and SET becomes a feedback input. The feedback network can be configured to produce an output between 16V and the voltage reference (nominally 1.21V). Under regulation, the feedback mechanism adjusts the error signal such that the voltage at the SET pin equals the reference voltage. Therefore, to achieve the minimum output, connect SET directly to OUT. For other voltages, a resistive voltage-divider network is necessary. Figure 3 shows the topology of a typical circuit operating in adjustable mode. The output voltage is set by the following equation:

$$V_{OUT} = V_{SET}\left(1 + \frac{R1}{R2}\right)$$

where V_{SET} = 1.21V. Solving for R1 yields:

$$R1 = R2\left(\frac{V_{OUT}}{V_{SET}} - 1\right)$$

The input leakage current of the SET input is less than 25nA. This allows the use of large resistors in the feedback network to minimize output current loss without compromising accuracy. R2 can be as high as 500kΩ in most applications.

Shutdown

A logic low on the $\overline{SHDN}$ pin places the MAX1658/MAX1659 in shutdown. This mode deactivates all functions, including the pass transistor. The device consumes less than 1µA of supply current in shutdown, and its output becomes high impedance. The MAX1658/MAX1659 exit shutdown in 100µs.

Output Current Limit

The MAX1658/MAX1659 include current-limiting circuitry that monitors and controls the pass transistor and limits output current to around 900mA. The output can be shorted to ground indefinitely without damaging the device.

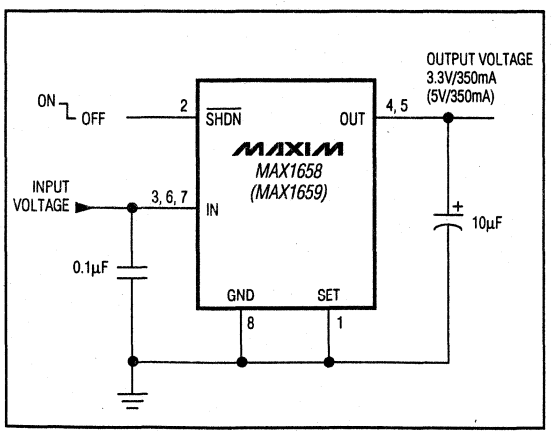


Figure 2. Preset Output Configuration

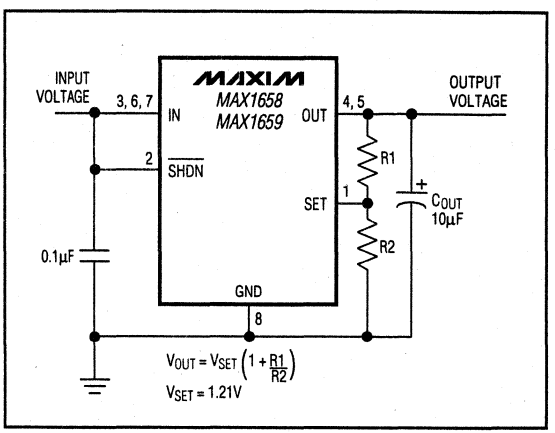


Figure 3. Adjustable Output Configuration Using External Feedback Resistors

350mA, 16.5V Input, Low-Dropout Linear Regulators

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1658/MAX1659. When the junction temperature exceeds T_J = +165°C, the pass transistor deactivates, allowing the IC to cool. Once it has cooled by 10°C, the control logic will enable operation. Under thermal overload, the output of the device will pulse as the die heats up and then cools to operational levels. Prolonged operation under these conditions is not recommended.

Operating Region and Power Dissipation

Maximum power dissipation of the MAX1658/MAX1659 depends on the thermal resistance of the package and circuit board, the temperature difference between the die and ambient air, and the rate of air flow. The power dissipation by the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The maximum power dissipation is:

$$P_{MAX} = \left(\frac{(T_J - T_A)}{(\theta_{JB} + \theta_{BA})} \right)$$

where $(T_J - T_A)$ is the temperature difference between MAX1658/MAX1659 die junction and the surrounding air, θ_{JB} is the thermal resistance of the package, and θ_{BA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air. The 8-pin SO package for the MAX1658/MAX1659 features a special lead frame with a lower thermal resistance and higher allowable power dissipation than a standard SO-8. The thermal resistance of this package is θ_{JB} = 69°C/W, compared with θ_{JB} = 170°C/W for an SO-8.

The IN pins of the MAX1658/MAX1659 package perform the dual function of providing an electrical connection to IN and channeling heat away. Connect all IN pins to the input voltage using a large pad or power plane on the surface. Where this is impossible, connect to a copper plane on an adjacent layer. The pad should meet the dimensions specified in Figure 4.

Figure 4 assumes the IC is soldered directly to the pad, has a +125°C maximum junction temperature and a +25°C ambient air temperature, and has no other heat sources. Use larger pad sizes for lower junction temperatures, higher ambient temperatures, or conditions where the IC is not soldered directly to a heat-sinking IN pad.

The MAX1658/MAX1659 can regulate currents up to 350mA and operate with input voltages up to 16.5V, but not simultaneously. High output currents can only be sustained when input-output differential voltage is low,

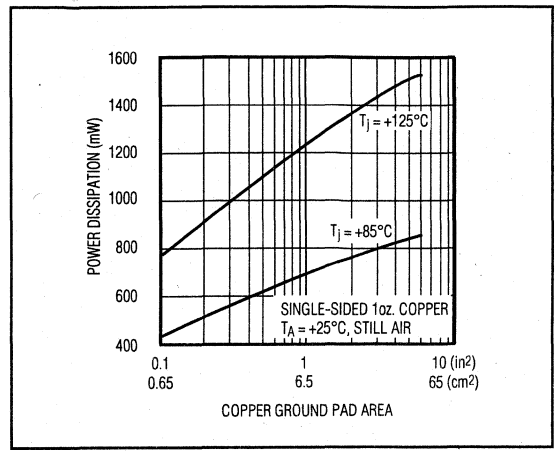


Figure 4. Typical Maximum Power Dissipation vs. Ground Pad Area

as shown in the following equation. Maximum power dissipation depends on packaging, board layout, temperature, and air flow. The maximum output current is:

$$I_{OUT(MAX)} = \frac{P_{MAX} \times (125°C - T_A)}{(V_{IN} - V_{OUT}) \times 100°C}$$

where P_{MAX} is derived from the T_J = 125°C curve of Figure 4.

Reverse Battery Protection

The MAX1658/MAX1659 feature reverse battery protection. Under normal operation, a P-channel MOSFET connects the substrate of the device to IN. When the input voltage falls below ground (implying reverse battery conditions), the P-channel switch turns off and disconnects the substrate from IN, disabling the device. The maximum reverse battery voltage allowed is -17V. $\overline{SHDN}$ also withstands reverse battery conditions and can be connected directly to IN with no loss of protection.

Polarized input bypass capacitors will be damaged under reverse battery conditions. To ensure circuit reliability, use a non-polarized capacitor at the input.

The MAX1658/MAX1659 do not provide reverse current protection. If V_{OUT} is greater than V_{IN} by more than 300mV, reverse current will flow. Reverse current protection can be added by connecting a Schottky diode in series with IN.

Applications Information

Output Capacitor Selection and Stability

To maintain stability, connect a ≥10µF capacitor with less than 200mΩ equivalent series resistance (ESR) from OUT to GND. Larger output capacitors improve load-transient response. Currents lower than 350mA make the use of smaller output capacitors possible. Table 1 shows the maximum output current typically achieved using various output capacitors. Output voltages higher than 3.3V require less output capacitance to remain stable.

Table 1. Typical Load Current Capabilities

OUTPUT CAPACITOR	LOAD CURRENT RANGE
2.2µF tantalum	0mA to 120mA
4.7µF tantalum	0mA to 250mA
10µF tantalum	0mA to 350mA

Input Bypass Capacitor

The use of a 0.1µF to 10µF input bypass capacitor is recommended. Larger capacitors provide better supply-noise rejection and line-transient response, as well as improved performance when the supply has a high AC impedance. Polarized input bypass capacitors will be damaged under reverse battery conditions. If reverse input voltages are expected, use a non-polarized capacitor at the input.

Noise and PSRR

The MAX1658/MAX1659 exhibit 2.5mVp-p of noise during normal operation. This noise level is negligible in most applications.

The MAX1658/MAX1659 are designed to maintain excellent power-supply rejection (55dB) at 50Hz/60Hz (or 50dB at 120Hz). These regulators are ideal for wall-cube applications that may contain significant ripple. Larger input and output capacitors will further improve the circuit's AC response. See the Power-Supply Rejection Ratio vs. Frequency graphs in the *Typical Operating Characteristics*.

Chip Information

TRANSISTOR COUNT: 207

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Digitally Controlled Fuel-Gauge Interface

General Description

The MAX1660 digitally controlled fuel-gauge interface executes two essential functions for rechargeable battery-pack management: fuel gauging and pack overcurrent protection. It accurately monitors a battery pack's charge and discharge current flow, and records each using two independent, on-board coulomb counters. Each counter's contents are externally accessible via a System Management Bus (SMBus™)-compliant 2-wire serial interface. An optional third wire interrupts the microcontroller (µC) when the charge or discharge counters reach a preset value or when an overcurrent condition (charge or discharge) occurs. In the event of an overcurrent or short-circuit condition, the MAX1660 disconnects the load and alerts its host. The MAX1660's flexibility allows accurate fuel gauging for any battery chemistry, using any desired control algorithm.

The MAX1660 operates with battery voltages from +4V to +28V and provides two micropower shutdown modes, increasing battery lifetime. To minimize total parts count, the device integrates a precision 2.00V system-reference output, a 3.3V linear-regulator output that can supply up to 5mA to power external circuitry, and a power-on reset output for the system µC. The MAX1660 is available in a 16-pin QSOP package.

Features

- ♦ **1% Accuracy over a 600µA to 4A Current Range (R_{SENSE} = 30mΩ)**
- ♦ **SMBus 2-Wire (plus optional interrupt) Serial Interface**
- ♦ **2.00V Precision System Reference Output**
- ♦ **3.3V Linear-Regulator Output Powers External Circuitry**
- ♦ **Two Micropower Shutdown Modes**
- ♦ **Independent Charge and Discharge Coulomb Counters**
- ♦ **Battery-Overcharge/Overdischarge Protection**
- ♦ **Battery Short-Circuit/Overcurrent Protection**
- ♦ **On-Board Power MOSFET Drivers**
- ♦ **80µA Quiescent Current**
- ♦ **<1µA Shutdown Current**
- ♦ **Small 16-Pin QSOP Package (same board area as 8-pin SO)**

Applications

Smart-Battery Packs

Battery-Pack Fuel Gauging

Battery-Pack Overcurrent Protection

Digital Current-Sense Instrumentation

Industrial-Control System Interfaces

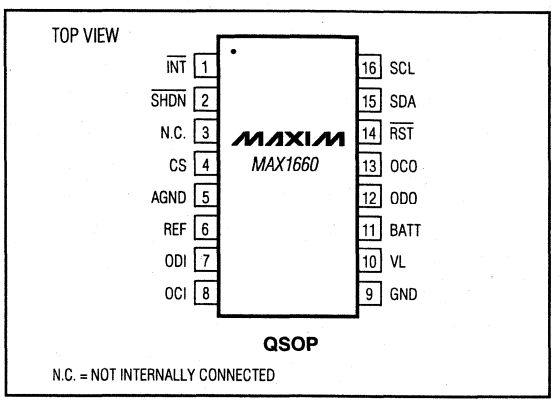
Analog-to-Digital Conversion

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1660C/D	0°C to +70°C	Dice*
MAX1660EEE	-40°C to +85°C	16 QSOP

**Contact factory for dice specifications.*

Pin Configuration



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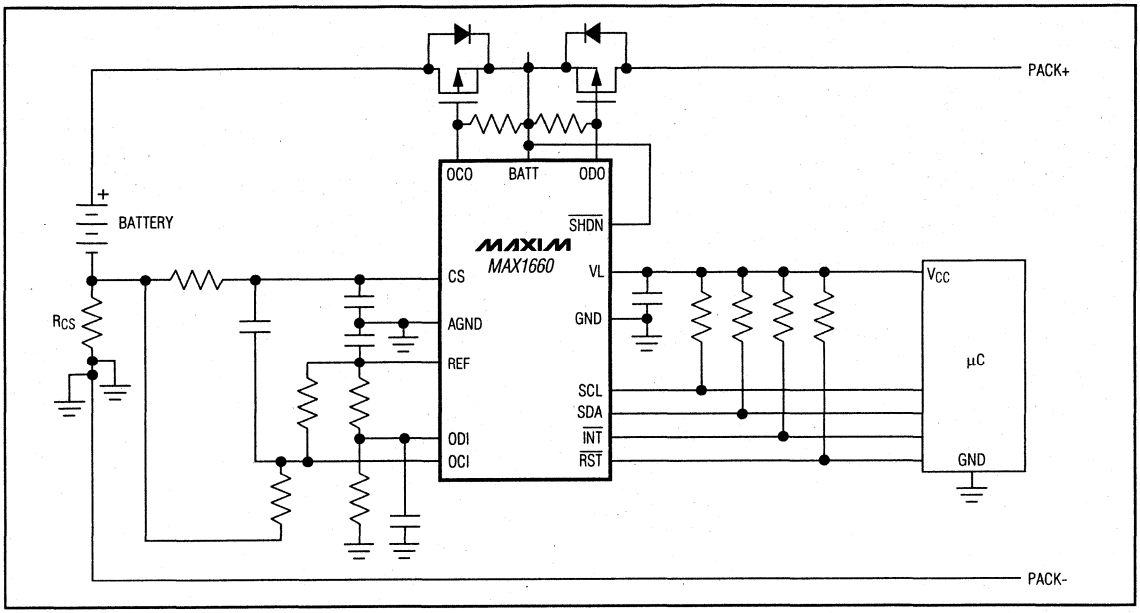
Digitally Controlled Fuel-Gauge Interface

Typical Operating Circuit



ADVANCE INFORMATION
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MAXIM

Serial-to-Parallel/Parallel-to-Serial Converters and Load-Switch Controllers with SMBus Interface

General Description

The MAX1661/MAX1662/MAX1663 are serial-to-parallel/parallel-to-serial converters intended to control external power MOSFETs in power-plane switching applications. These small, low-cost devices can be used on a system motherboard to manage point-of-load switching from a 2-wire SMBus™ serial interface. Each device has three high-voltage, open-drain outputs that double as TTL-level logic inputs, giving them bidirectional capabilities. The I/O pins can withstand 28V and are therefore capable of controlling battery-voltage distribution switches in notebook computers.

There are two basic device types: the MAX1661 is intended for N-channel MOSFETs, while the MAX1662/MAX1663 are intended for P-channel MOSFETs. The MAX1661's outputs are low, whereas the MAX1662/MAX1663's outputs become high upon power-up. This ensures that the MOSFETs are off at power up so that the system can enforce power-plane sequencing.

The $\overline{\text{SMBSUS}}$ control input selects between control data previously written to two separate data registers. This feature allows the system to select asynchronously between two different power-plane configurations, eliminating latencies introduced by the serial bus. Other features include thermal-overload and overcurrent protection, ultra-low supply current, and hardware/software-interrupt capability.

Applications

Point-of-Load Power-Bus Switching
Notebook and Subnotebook Computers
Power-Plane Switching
Smart Batteries
Desktop Computers

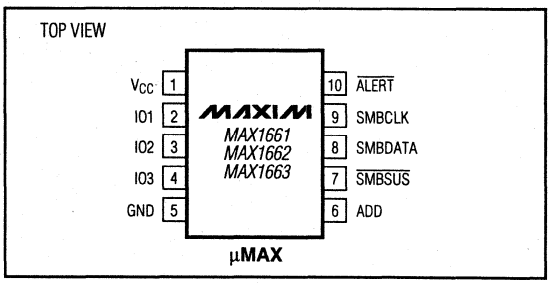
Features

- ♦ **Performs Serial-to-Parallel or Parallel-to-Serial Conversions**
- ♦ **Three General-Purpose Digital Input/Output Pins**
- ♦ **SMBus 2-Wire Serial Interface**
- ♦ **Supports $\overline{\text{SMBSUS}}$ Asynchronous Suspend**
- ♦ **3µA Typical Supply Current**
- ♦ **+2.7V to +5.5V Supply Range**
- ♦ **I/Os Can Withstand +28V**
- ♦ **Available in a Space-Saving, Low-Cost, 10-Pin µMAX Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1661EUB	-40°C to +85°C	10 µMAX
MAX1662EUB	-40°C to +85°C	10 µMAX
MAX1663EUB	-40°C to +85°C	10 µMAX

Pin Configuration



Selector Guide

PART	POWER-ON RESET STATE	APPLICATION	SMBus ADDRESS	
			ADDRESS PIN	ADDRESS
MAX1661	Outputs low	N-channel MOSFETs	GND	0100000
			High-Z	0111100
			VCC	1001000
MAX1662	Outputs high	P-channel MOSFETs	GND	0100001
			High-Z	0111101
			VCC	1001001
MAX1663	Outputs high	P-channel MOSFETs	GND	0100010
			High-Z	0111110
			VCC	1001010

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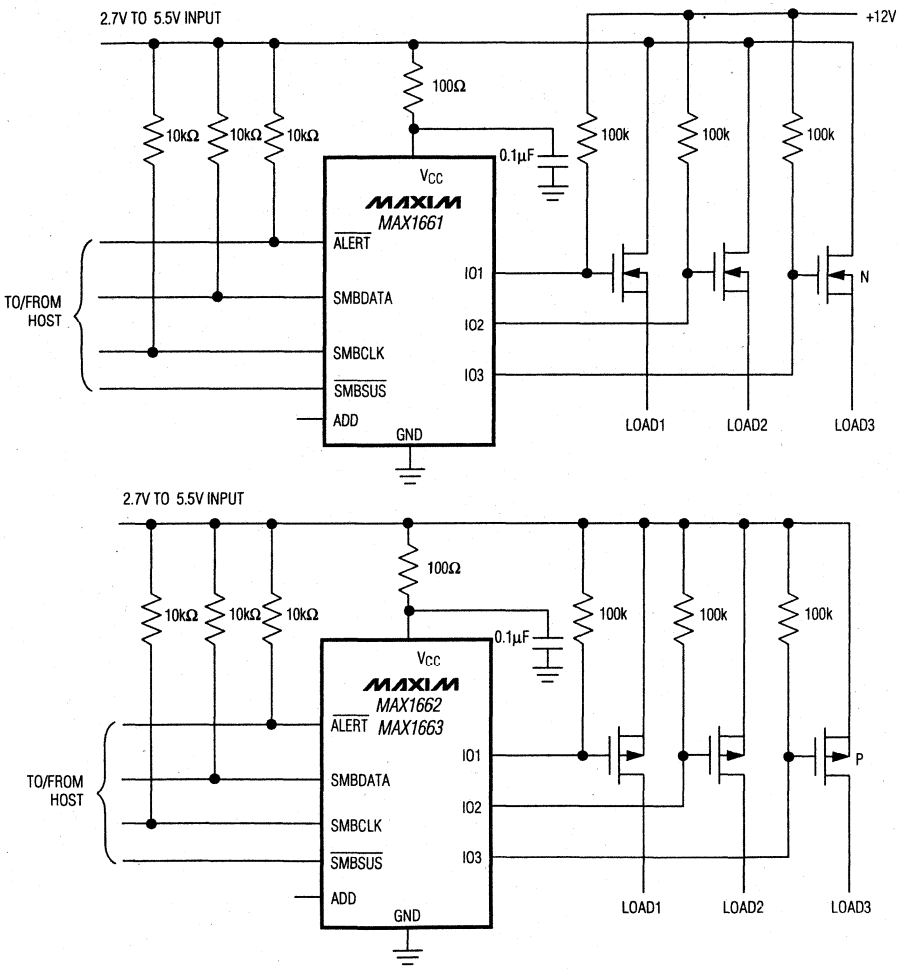
Serial-to-Parallel/Parallel-to-Serial Converters and Load-Switch Controllers with SMBus Interface

Typical Operating Circuits



ADVANCE INFORMATION

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MAXIM

Step-Up/Down DC-DC Converter in QSOP Package

General Description

The MAX1672 integrates a step-up DC-DC converter with a linear regulator to provide step-up/down voltage conversion. This device provides a constant output voltage for inputs that vary above and below the output voltage. It has a 1.8V to 11V input range and a preset 3.3V or 5V output. The output can also be set from 1.25V to 5.5V using two resistors. Typical efficiency is 85%.

The MAX1672's step-up/linear regulator configuration permits the use of a smaller inductor than can be used with competing SEPIC and flyback configurations. The MAX1672 uses only one inductor that is half the size of the competing solutions (because the one-half LI^2 requirements of a step-up converter are one-half those of SEPIC and flyback converters). Switch current is also selectable, permitting the use of smaller inductors. The linear regulator also acts as a filter to reduce output ripple voltage.

The MAX1672 has a low 100µA quiescent supply current, which is further reduced to 1µA in logic-controlled shutdown. The output voltage is disconnected from the input in shutdown. The MAX1672 also has an PGI/$\overline{PGO}$ power-good detector.

The MAX1672 comes in a 16-pin QSOP package (same size as a standard 8-pin SO). For a larger device that delivers more output current, refer to the MAX710/MAX711. The preassembled MAX1672 evaluation kit is available to speed designs.

Features

- **Step-Up/Down Voltage Conversion**
- **1.8V to 11V Input Range**
- **Adjustable Output Range (or preset 3.3V and 5V output)**
- **Output Power:**
  150mA at 5V with V_{IN} = 2V
- **100µA Quiescent Supply Current**
- **Smaller Inductor than SEPIC and Flybacks**
- **Load Disconnected from Input in Shutdown**
- **Supply Current from Battery:**
  200µA No-Load
  0.2µA when Off
- **PGI/$\overline{PGO}$ Power-Good Comparator**
- **16-Pin QSOP Package (same footprint as 8-pin SO)**
- **No External FETS Required**

Applications

Single-Cell, Lithium-Powered Portable Devices

2-Cell to 4-Cell AA Alkaline Hand-Held Equipment

3.3V and Other Low-Voltage Systems

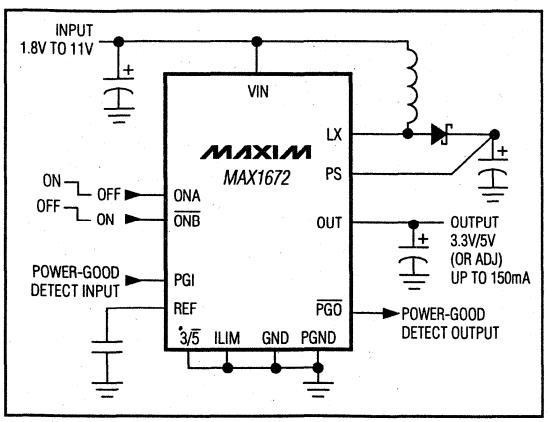
Battery-Powered Devices with AC Input Adapters

Digital Cameras

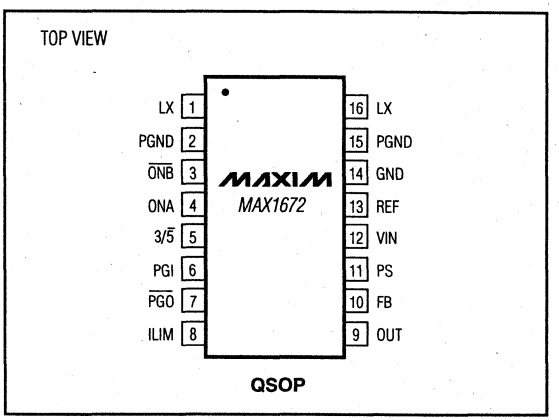
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1672C/D	0°C to +70°C	Dice
MAX1672EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Regulated, 125mA-Output, Charge-Pump DC-DC Inverter

General Description

The MAX1673 charge-pump inverter provides a low-cost and compact means of generating a regulated negative output from a positive input at up to 125mA. Its equivalent output resistance is only 6Ω. The MAX1673 comes in an 8-pin SO and requires only three small capacitors and two resistors to set its output voltage. The input range is 2V to 5.5V. The regulated output can be set from (-1 x V_{IN}) to 0V in skip mode or from (-1 x V_{IN}) to -1.5V in linear mode.

The MAX1673 can be configured to regulate in one of two ways: in skip mode or in linear mode. In skip mode, the MAX1673 regulates by varying its switching frequency as a function of the load current. This patented on-demand switching gives the MAX1673 two advantages: very small capacitors and very low quiescent supply current. For example, at heavy loads, it transfers energy from the input to the output by switching at up to 350kHz, requiring only small 2.2µF capacitors. At light loads, it switches more slowly, using only 45µA quiescent supply current.

In linear mode, the MAX1673 switches at a constant 350kHz and regulates its output by controlling the current-path resistance. The output ripple's constant frequency allows it to be easily filtered for low-noise applications.

The MAX1673 also features a 1µA logic-controlled shutdown. For a smaller device that delivers about 30mA and fits in a smaller package, refer to the MAX868.

Applications

Hard Disk Drives

Analog Signal-Processing Applications

Measurement Instruments

Modems

Camcorders

Digital Cameras

Features

- **Regulated Negative Output Voltage (Up to -1 x V_{IN})**
- **125mA Output Current (6Ω output impedance)**
- **45µA Quiescent Supply Current (skip-mode regulation)**
- **350kHz Fixed-Frequency, Low-Noise Output (linear mode)**
- **2V to 5.5V Input Range**
- **1µA Logic-Controlled Shutdown**

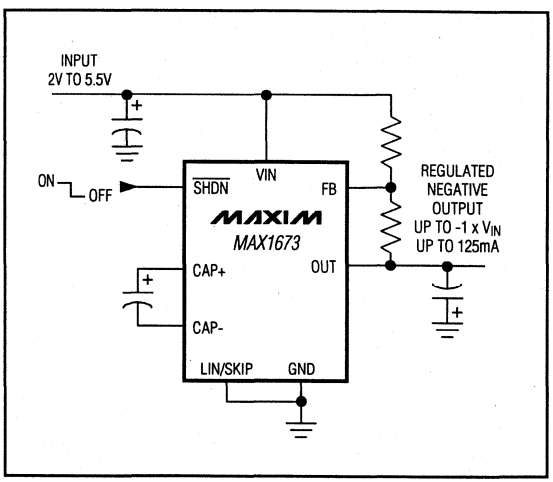
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1673C/D	0°C to +70°C	Dice*
MAX1673ESA	-40°C to +85°C	8 SO

**Dice are tested at T_A = +25°C, DC parameters only.*

4

Typical Operating Circuit



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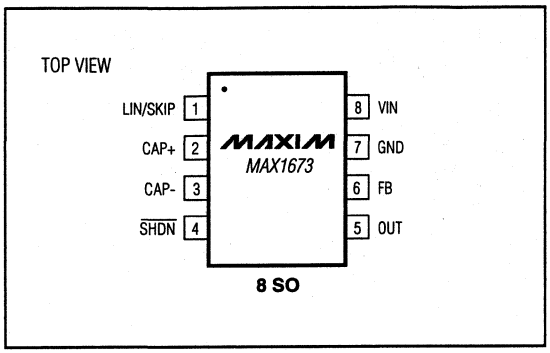
Regulated, 125mA-Output Charge-Pump DC-DC Inverter

Pin Configuration



19-1247; Rev 0; 7/97

MAXIM

125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

General Description

The MAX1680/MAX1681 inductorless switched-capacitor voltage converters either invert an input voltage of +2.0V to +5.5V or double it while supplying up to 125mA output current. They have a selectable-frequency option that allows the use of small capacitors: 4.7µF (MAX1680), 1µF (MAX1681). With their high output current capability, these charge-pump devices are suitable replacements for inductor-based regulators, which require more expensive external components and additional board space.

The devices' equivalent output resistance (typically 3.5Ω) allows them to deliver as much as 125mA with only a 440mV drop. A shutdown feature reduces quiescent current to less than 1µA. The MAX1680/MAX1681 are available in 8-pin SO packages. For devices that deliver up to 50mA in smaller µMAX packages, refer to the MAX860/MAX861 data sheet.

Features

- ♦ **Selectable Switching Frequencies:**
  125kHz/250kHz (MAX1680)
  500kHz/1MHz (MAX1681)
- ♦ **Allow Use of Small Capacitors**
  (1µF for the MAX1681)
- ♦ **125mA Output Current**
- ♦ **3.5Ω Output Impedance**
- ♦ **1µA Logic-Controlled Shutdown**
- ♦ **Configurable as Voltage Inverters or Doublers**
- ♦ **+2.0V to +5.5V Input Voltage Range**
- ♦ **Available in 8-Pin SO Packages**
- ♦ **90% Efficiency**

Applications

Local Negative Supplies

Interface Power Supplies

Op-Amp Power Supplies

MOSFET Bias

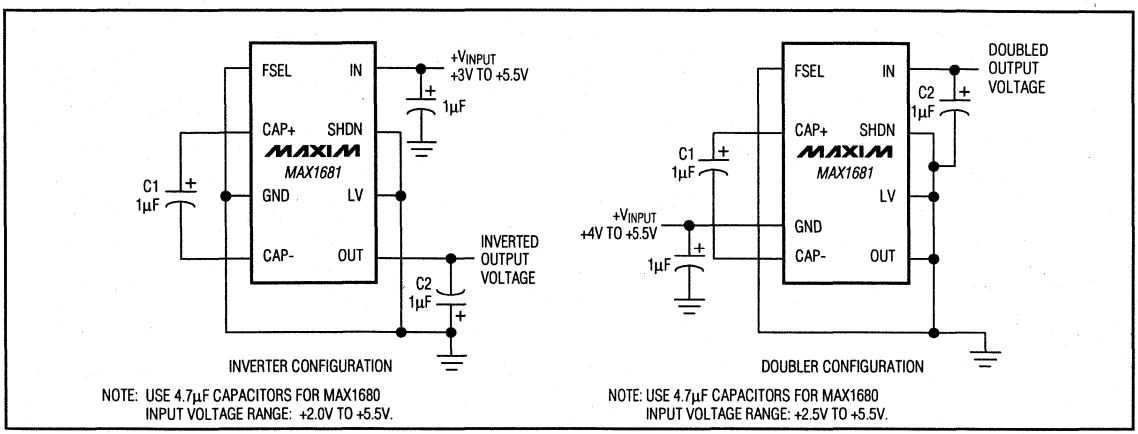
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1680C/D	0°C to +70°C	Dice*
MAX1680ESA	-40°C to +85°C	8 SO
MAX1681C/D	0°C to +70°C	Dice*
MAX1681ESA	-40°C to +85°C	8 SO

Contact factory for dice specifications.

Pin Configuration appears at end of data sheet.

Typical Operating Circuits



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125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

ABSOLUTE MAXIMUM RATINGS

IN .....-0.3V to +6V
LV .....(V_{OUT} - 0.3V) to (V_{IN} + 0.3V)
CAP+ .....-0.3V to (V_{IN} + 0.3V)
SHDN, FSEL .....(V_{LV} - 0.3V) to (V_{IN} + 0.3V)
OUT, CAP- .....-6V to 0.3V
Continuous Output Current 135mA
Output Short-Circuit Duration to GND (Note 1) 1sec

Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Shorting OUT to IN may damage the device and should be avoided.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuits* (inverter configuration), FSEL = LV = GND, V_{IN} = 5V, C1 = C2 = 10µF (MAX1680), C1 = C2 = 2.2µF (MAX1681), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Inverter configuration, R_L = 1kΩ, LV = GND		MAX1680	2.0		5.5	V
				MAX1681	3.0		5.5	
		Doubler configuration, R_L = 1kΩ, LV = OUT		MAX1680	2.5		5.5	
				MAX1681	4.0		5.5	
Supply Current	I+	MAX1680	FSEL = IN (125kHz)	T_A = +25°C		2.5	4.5	mA
							5.4	
			FSEL = LV (250kHz)	T_A = +25°C		5	9	
							10.8	
		MAX1681	FSEL = IN (500kHz)	T_A = +25°C		10	18	
							21.6	
			FSEL = LV (1MHz)	T_A = +25°C		20	36	
							43.2	
Output Voltage Under Load (Note 2)	V_{LOAD}	I_{LOAD} = 125mA			-3.75	-4.56		V
Output Resistance (Note 2)	R_{OUT}	FSEL = IN or LV				3.5	10	Ω
Output Resistance to Ground in Shutdown	$R_{OUT(SHUT)}$	SHDN = IN				1	5	Ω
Shutdown Current	I+SHDN	OUT = GND, SHDN = IN					1	µA
Input Bias Current (SHDN)	I_{SHDN}				-1		1	µA
Input Bias Current (FSEL)	I_{FSEL}				-1		1	µA
Shutdown, FSEL Thresholds	V_{IL}	LV = GND (Note 3)					1	V
	V_{IH}				4			
Switching Frequency	f_{OSC}	MAX1680	FSEL = LV	T_A = +25°C	187	250	313	kHz
					157		348	
			FSEL = IN	T_A = +25°C	94	125	156	
					79		174	
		MAX1681	FSEL = LV	T_A = +25°C	750	1000	1250	
					570		1490	
			FSEL = IN	T_A = +25°C	375	500	625	
					285		745	

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuits* (inverter configuration), FSEL = LV = GND, V_{IN} = 5V, C1 = C2 = 10µF (MAX1680), C1 = C2 = 2.2µF (MAX1681), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Efficiency		R_L = 100Ω to GND, FSEL = IN	MAX1680		90		%
			MAX1681		80		

ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuits* (inverter configuration), FSEL = LV = GND, V_{IN} = 5V, C1 = C2 = 10µF (MAX1680), C1 = C2 = 2.2µF (MAX1681), **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}	Inverter configuration, R_L = 1kΩ, LV = GND	MAX1680	2.0		5.5	V
			MAX1681	3.0		5.5	
		Doubler configuration, R_L = 1kΩ, LV = OUT	MAX1680	2.5		5.5	
			MAX1681	4.0		5.5	
Supply Current	I+	MAX1680	FSEL = IN (125kHz)			5.4	mA
			FSEL = LV (250kHz)			10.8	
		MAX1681	FSEL = IN (500kHz)			21.6	
			FSEL = LV (1MHz)			43.2	
Output Voltage Under Load (Note 2)	V_{LOAD}	I_{LOAD} = 125mA		-3.75			V
Output Resistance (Note 2)	R_{OUT}	FSEL = IN or LV				10	Ω
Output Resistance in Shutdown	$R_{OUT(SHUT)}$	SHDN = IN				5	Ω
Shutdown Current	$I+_{SHDN}$	OUT = GND, SHDN = IN				1	µA
Input Bias Current (SHDN)	I_{SHDN}					1	µA
Input Bias Current (FSEL)	I_{FSEL}			-1		1	µA
Shutdown, FSEL Thresholds	V_{IL}	LV = GND (Note 3)		-1		1	V
	V_{IH}			4			
Switching Frequency	f_{OSC}	MAX1680	FSEL = LV	157		348	kHz
			FSEL = IN	79		174	
		MAX1681	FSEL = LV	570		1490	
			FSEL = IN	285		745	

Note 2: C1 and C2 are low-ESR (<0.2Ω) capacitors. Capacitor ESR adds to the circuit's output resistance. Using capacitors with higher ESR reduces output voltage and efficiency. The specified output resistance includes the C1 and C2 0.2Ω ESR.

Note 3: The typical threshold for V_{INPUT} other than +5V is $0.35V_{INPUT}$ (V_{IL} = V_{IH}).

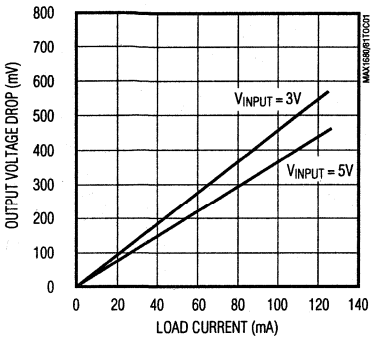
Note 4: Specifications to -40°C are guaranteed by design, not production tested.

125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

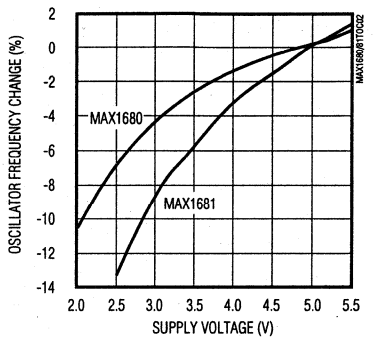
Typical Operating Characteristics

(All curves generated using the inverter configuration shown in the *Typical Operating Circuits* with LV = GND, FSEL = IN or LV, C1 = C2 = 10µF (MAX1680), C1 = C2 = 2.2µF (MAX1681), and T_A = +25°C, unless otherwise noted. Test results are also valid for the doubler configuration with LV = OUT and T_A = +25°C.)

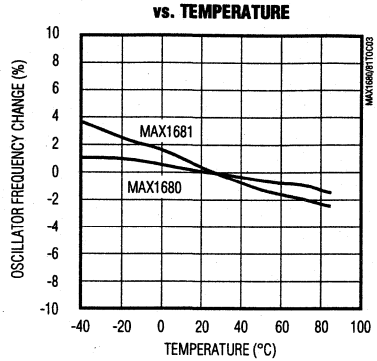
OUTPUT VOLTAGE DROP vs. LOAD CURRENT



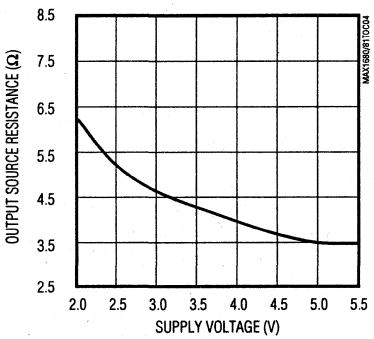
OSCILLATOR FREQUENCY CHANGE vs. SUPPLY VOLTAGE



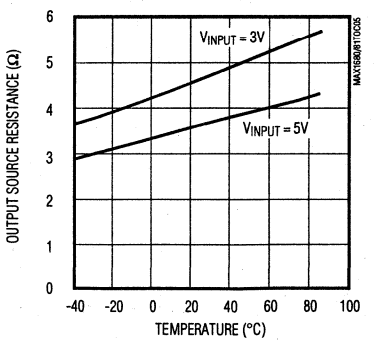
OSCILLATOR FREQUENCY CHANGE vs. TEMPERATURE



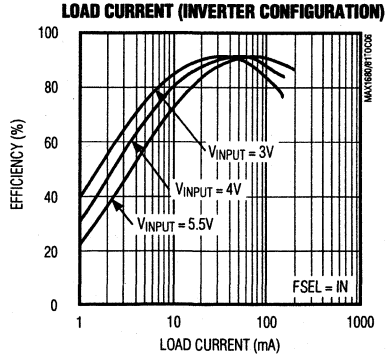
OUTPUT SOURCE RESISTANCE vs. SUPPLY VOLTAGE



OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



MAX1680 EFFICIENCY vs. LOAD CURRENT (INVERTER CONFIGURATION)

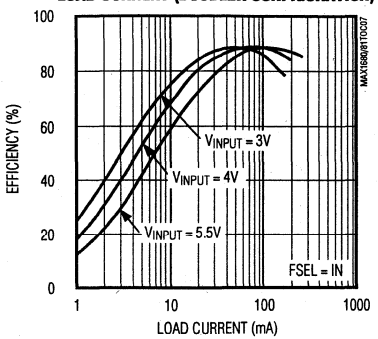


125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

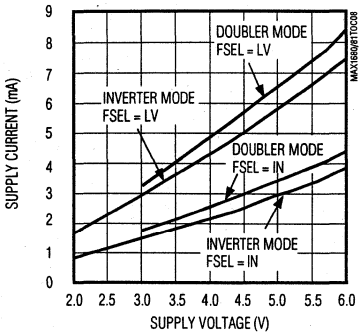
Typical Operating Characteristics (continued)

(All curves generated using the inverter configuration shown in the *Typical Operating Circuits* with LV = GND, FSEL = IN or LV, C1 = C2 = 10µF (MAX1680), C1 = C2 = 2.2µF (MAX1681), and T_A = +25°C, unless otherwise noted. Test results are also valid for the doubler configuration with LV = OUT and T_A = +25°C.)

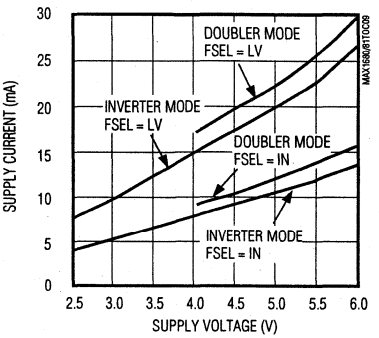
MAX1681 EFFICIENCY vs. LOAD CURRENT (DOUBLER CONFIGURATION)



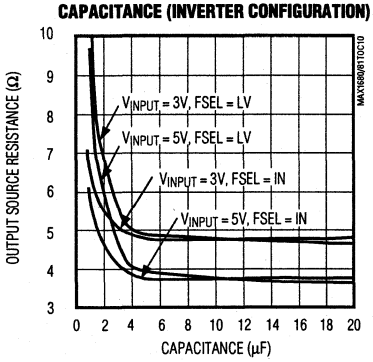
MAX1680 SUPPLY CURRENT vs. SUPPLY VOLTAGE



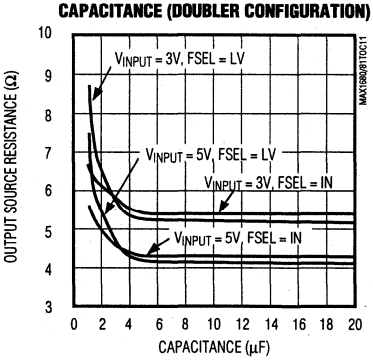
MAX1681 SUPPLY CURRENT vs. SUPPLY VOLTAGE



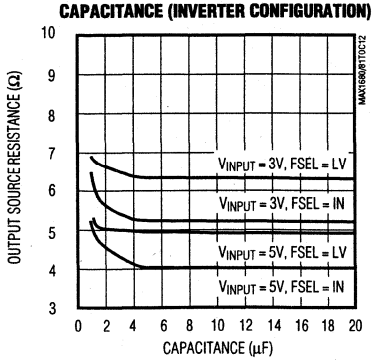
MAX1680 OUTPUT SOURCE RESISTANCE vs. CAPACITANCE (INVERTER CONFIGURATION)



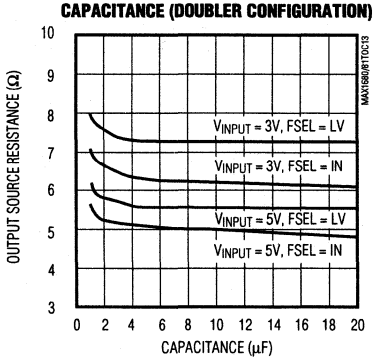
MAX1680 OUTPUT SOURCE RESISTANCE vs. CAPACITANCE (DOUBLER CONFIGURATION)



MAX1681 OUTPUT SOURCE RESISTANCE vs. CAPACITANCE (INVERTER CONFIGURATION)



MAX1681 OUTPUT SOURCE RESISTANCE vs. CAPACITANCE (DOUBLER CONFIGURATION)



125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

Pin Description

PIN	NAME	FUNCTION	
		INVERTER	DOUBLER
1	FSEL	Selects operating frequency. MAX1680: 250kHz when FSEL is low, 125kHz when FSEL is high. MAX1681: 1MHz when FSEL is low, 500kHz when FSEL is high.	
2	CAP+	Positive Charge-Pump Capacitor Connection	
3	GND	Power-Supply Ground Input	Power-Supply Positive Voltage Input
4	CAP-	Negative Charge-Pump Capacitor Connection	
5	OUT	Negative Voltage Output	Power-Supply Ground Connection
6	LV	Logic Voltage Input. Connect LV to GND.	Connect LV to OUT.
7	SHDN	Shutdown Input. Driving SHDN high disables the charge pump, and the output goes to 0V. SHDN is a CMOS input.	Not available; connect to OUT.
8	IN	Power-Supply Positive Voltage Input	Positive Voltage Output

Detailed Description

The MAX1680/MAX1681 switched-capacitor voltage converters either invert or double the input voltage. They have low output resistance (3.5Ω) and can deliver up to 125mA output current. These devices operate at one of two selectable frequencies: 125kHz/250kHz (MAX1680) and 500kHz/1MHz (MAX1681). This provides the flexibility to optimize capacitor size, operating supply current, and overall circuit efficiency. Frequency selection also allows for minimizing coupling into other sensitive circuits. These devices contain no internal divider; the oscillator frequency equals the switching frequency. The devices can easily be cascaded to produce a higher output voltage, or paralleled to deliver more current.

The MAX1680/MAX1681 feature a shutdown mode that reduces supply current to <1µA (SHDN = high). OUT, in the inverter configuration, pulls to ground in shutdown mode. Shutdown is not available in the doubler configuration; connect SHDN to OUT.

Applications Information

Voltage Inverter

A simple voltage inverter is the most common MAX1680/MAX1681 application. It requires three external capacitors (including the input bypass capacitor) as shown in the *Typical Operating Circuits* (inverter configuration). Although the output is not regulated, low output resistance produces a typical drop of only 0.44V with a 125mA load. This low output resistance makes the devices fairly insensitive to changes in load (see the graphs for Output Source Resistance vs. Temperature and Supply Voltage in the *Typical Operating Characteristics* section).

Voltage Doubler

The MAX1680/MAX1681 can be configured as a voltage doubler with two external capacitors as shown in the *Typical Operating Circuits* (doubler configuration). When loaded, the output voltage drop is similar to that of the voltage inverter. The minimum input supply range is slightly higher than in the inverter configuration. Calculate ripple voltage using the equation in the *Capacitor Selection* section.

Frequency Control

A frequency-control pin, FSEL, provides design flexibility. Each device has two selectable frequencies: 125kHz/250kHz (MAX1680) and 500kHz/1MHz (MAX1681). This allows optimization of capacitor size and supply current for a given output load. Table 1 summarizes the frequency options .

Table 1. Nominal Switching Frequencies

FSEL CONNECTION	FREQUENCY (kHz)	
	MAX1680	MAX1681
FSEL = LV	250	1000
FSEL = IN	125	500

125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

Operating Frequency Trade-Offs

It is important to recognize the trade-offs between switching frequency, power consumption, noise, cost, and performance. Higher frequency switching reduces capacitor size while maintaining the same output impedance, thus saving capacitor cost and board space. Lower frequency designs use less supply current. Table 2 summarizes the relative trade-offs.

Table 2. Switching-Frequency Trade-Offs

ATTRIBUTE	LOWER FREQUENCY	HIGHER FREQUENCY
Output Ripple	Larger	Smaller
C1, C2 Values	Larger	Smaller
Supply Current	Smaller	Larger

Capacitor Selection

The MAX1680/MAX1681 are tested with capacitor values of 10µF and 2.2µF, respectively. Capacitor size and switching speed determine output resistance. Larger C1 values decrease the output resistance until the internal switch resistance (3.5Ω typ) becomes the dominant term. Low-ESR capacitors minimize output resistance and ripple voltage. The entire circuit's output resistance can be approximated by the following equation:

$$R_{OUT} \cong R_O + 4 \times ESR_{C1} + ESR_{C2} + [1 / (f_{OSC} \times C1)] + [1 / (f_{OSC} \times C2)]$$

where R_O is the device's internal effective switch resistance and f_{OSC} is the switching frequency. Output resistance is a critical circuit component, as it determines the voltage drop that will occur at the output from the ideal value of $-V_{INPUT}$ (or $2V_{INPUT}$ when doubling).

To optimize performance, minimize overall resistance in the system. In particular, equivalent series resistance (ESR) in the capacitors produces significant losses as large currents flow through them. Therefore, choose a low-ESR capacitor for highest efficiency. Table 3 lists recommended capacitors and their suppliers.

Calculate the output ripple voltage as follows:

$$V_{RIPPLE} = [(I_{OUT}) / (2 \times f_{OSC} \times C2)] + 2 \times (I_{OUT} \times ESR_{C2})$$

where I_{OUT} is the load current, f_S is the charge pump's operating frequency, C2 is the output capacitor, and ESR_{C2} is the output capacitor's ESR.

Table 4 lists the minimum recommended capacitances that allow for the maximum output current. The output capacitor, C2, is normally equal to or greater than the charge-pump capacitor, C1. Capacitor values can be scaled directly proportional to the input voltage, frequency, and load current. For example, for V_{INPUT} = 5V, I_{LOAD} = 125mA at f_{OSC} = 125kHz, a 6.4µF minimum capacitor is recommended. For an output of only 62.5mA, a 3.2µF capacitor is recommended. C1's value can be estimated as follows:

$$C1 = 6.4\mu F \times (V_{INPUT} / 5.0V) \times (125kHz / f_{OSC}) \times (I_{LOAD} / 125mA)$$

where f_{OSC} is the switching frequency (kHz) and I_{LOAD} is the output current (mA) required.

Table 3. Low-ESR Capacitor Suppliers

SUPPLIER	PHONE	FAX	DEVICE TYPE
AVX	(803) 946-0690 (800) 282-4975	(803) 626-3123	Surface mount, TPS series
Marcon/United Chemi-Con	(847) 696-2000	(847) 696-9278	Ceramic capacitors
Matsuo	(714) 969-2491	(714) 960-6492	Surface mount, 267 series
Nichicon	USA: (847) 843-7500 Japan: 81-7-5231-8461	USA: (847) 843-2798 Japan: 81-7-5256-4158	Through-hole, PL series
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	USA: (619) 661-1055 Japan: 81-7-2070-1174	Through-hole, OS-CON series
Sprague	(603) 224-1961	(603) 224-1430	Surface mount, 595D series
TDK	(847) 390-4373	(847) 390-4428	Ceramic capacitors
United Chemi-Con	(714) 255-9500	(714) 255-9400	Through-hole, LXF series
Vishay/Vitramon	(203) 268-6261	(203) 452-5670	SMT ceramic chip capacitors

125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

Table 4. Minimum Recommended Capacitances for Maximum Output Current

fosc (kHz)	CAPACITANCE (µF) (C1 = C2)			
	V_{IN} = 2V	V_{IN} = 3V	V_{IN} = 4V	V_{IN} = 5V
125	2.5	3.8	5.1	6.4
250	1.2	1.9	2.5	3.2
500	0.6	0.9	1.2	1.6
1000	0.3	0.4	0.6	0.8

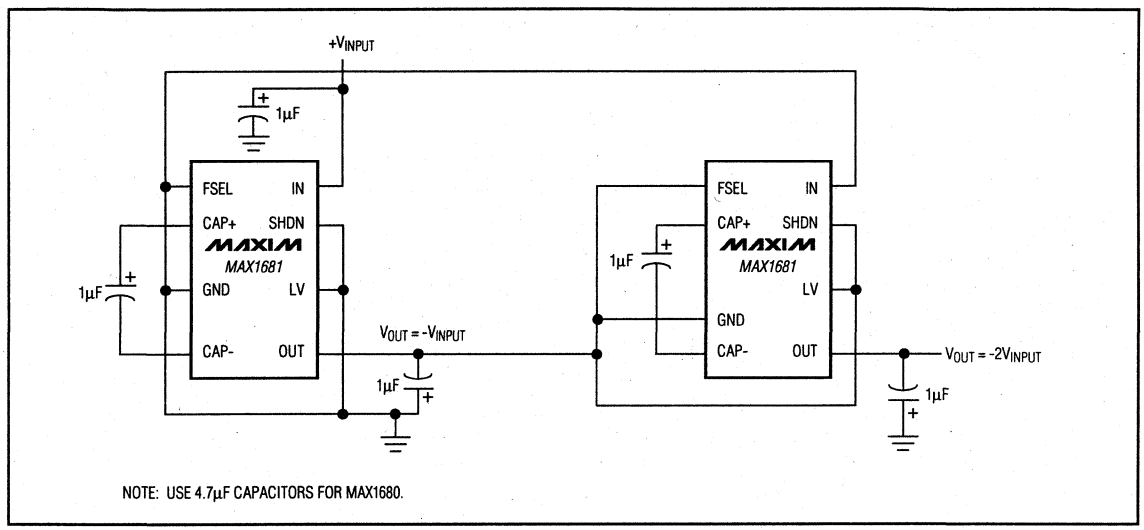


Figure 1. Cascading MAX1680/MAX1681s to Increase Output Voltage

Bypass Capacitor

Bypass the input voltage to reduce AC impedance and to prevent internal switching noise. Bypassing depends on the source impedance location. The AC ripple current is 2 x I_{OUT} for the doubler and the inverter. Use a large bypass capacitor (equal to C1) if the supply has high AC impedance.

Cascading Devices

To produce larger negative voltages, cascade two devices (Figure 1). For two devices, the unloaded output voltage is approximately -2 x V_{INPUT}, but this value is reduced slightly by the first device's output resistance multiplied by the second device's quiescent current. The effective output resistance for a cascaded device is larger than that for an individual device (20Ω for two devices). Cascading several devices increases output resistance and reduces efficiency. If a large negative voltage is required for several stages, an inductive inverting switching regulator such as the MAX629 or MAX774 may offer more advantages.

Paralleling Devices

Parallel two or more MAX1680/MAX1681s to reduce output resistance voltage drop under a given load. With reduced output resistance, paralleled devices deliver higher load currents. Figure 2 shows two MAX1680/MAX1681s connected in parallel. Output resistance is inversely proportional to the number of devices.

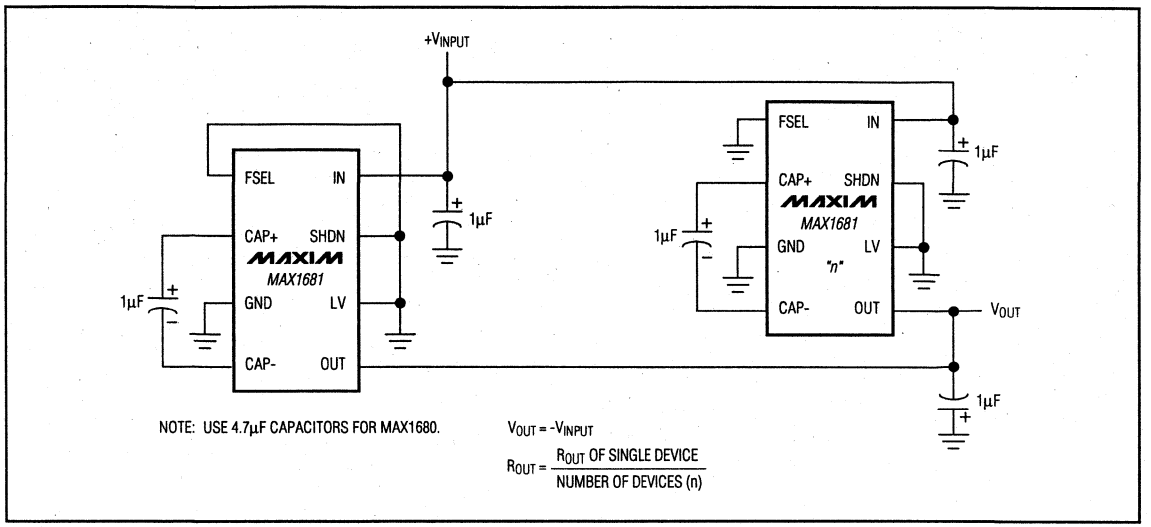


Figure 2. Paralleling MAX1680/MAX1681s to Increase Output Current

Combined Doubler and Inverter

Figure 3 shows a single MAX1680/MAX1681 as an inverter and a doubler. The maximum output current is the sum of the loads on the two outputs and is still limited to 125mA. As the device is loaded, the output voltages move toward ground. In this particular configuration, connect LV to GND (inverter). The diodes used in the circuit cause a drop of approximately 0.7V in the doubler's output voltage, impacting efficiency.

Compatibility with the MAX660 and MAX860/MAX861

The MAX1680/MAX1681 can be used in place of the MAX860/MAX861, except for the SHDN and FSEL pins. The MAX1680/MAX1681 shut down with a high input voltage, compared with the MAX860/MAX861. The MAX1680/MAX1681 have only two frequency choices.

Replacing the MAX660 with the MAX1680/MAX1681 involves a wiring change, as the external oscillator pin is replaced by the shutdown feature. Table 5 compares the devices.

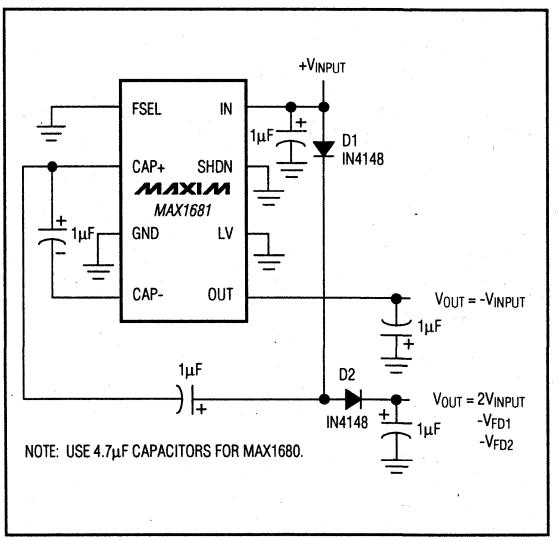


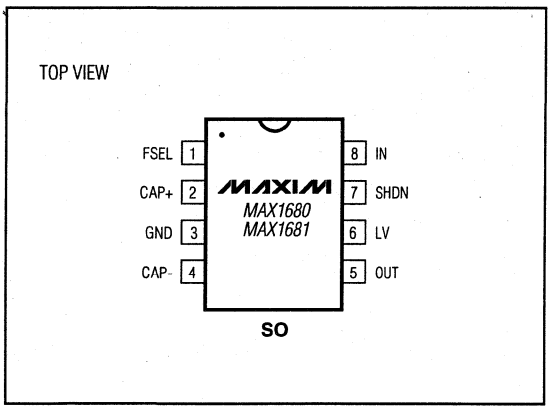
Figure 3. Combined Doubler and Inverter

125mA, Frequency-Selectable, Switched-Capacitor Voltage Converters

Table 5. Device Comparison

PART NUMBER	TYPICAL QUIESCENT CURRENT (mA)	OUTPUT CURRENT (mA)	OUTPUT RESISTANCE (Ω)	SWITCHING FREQUENCY (kHz)
MAX660	0.12/1.0	100	6.5	5/40
MAX665	0.20/1.0	100	6.5	5/40
MAX860	0.20/0.60/1.40	50	12	6/50/130
MAX861	0.30/1.10/2.50	50	12	13/100/250
MAX1680	2.5/5.0	125	3.5	125/250
MAX1681	10/20	125	3.5	500/1000
ICL7660	0.080	10	55	5

Pin Configuration



Chip Information

TRANSISTOR COUNT: 171

SUBSTRATE CONNECTED TO IN

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

General Description

The MAX1700/MAX1701 are high-efficiency, low-noise, step-up DC-DC converters. They are intended for use in battery-powered wireless applications. They use a synchronous-rectifier pulse-width-modulation (PWM) boost topology to generate 2.7V to 5V outputs from battery inputs such as one to three NiCd/NiMH cells or one Li-Ion cell. Both devices have an internal 5A, 100mΩ N-channel MOSFET switch and a 150mΩ P-channel synchronous rectifier.

With their internal synchronous rectifier, the MAX1700/MAX1701 deliver 5% better efficiency than similar non-synchronous converters. They also feature a pulse-frequency-modulation (PFM) standby mode to improve efficiency at light loads and a 5µA shutdown mode.

The MAX1700/MAX1701 come in 16-pin QSOP packages (which occupy the same space as an 8-pin SO). The MAX1701 includes two comparators to generate power-good and low-battery warning outputs. It also contains a linear-gain block that can be used to build a linear regulator using an external P-channel pass device.

For higher-power outputs, refer to the MAX1703. For dual outputs (step-up and linear regulator), refer to the MAX1705/MAX1706. For an on-board analog-to-digital converter, refer to the MAX848/MAX849.

The MAX1701EVKIT evaluation kit is available to speed designs.

Applications

Digital Cordless Phones
PCS Phones
Wireless Handsets
Two-Way Pagers
Personal Communicators
Palmtop Computers
Hand-Held Instruments

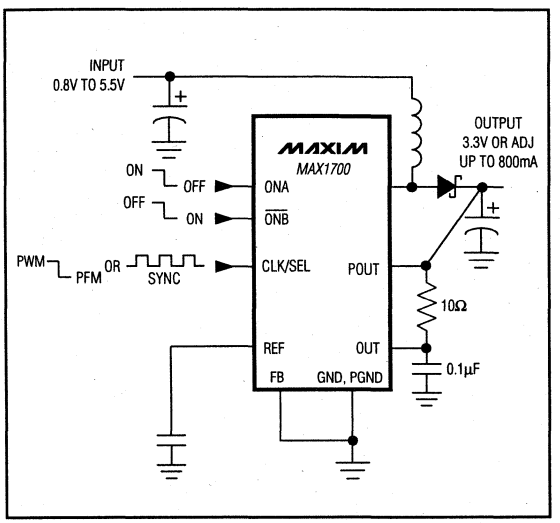
Features

- **Up to 96% Efficiency**
- **$1V_{IN}$ Guaranteed Start-Up**
- **0.8V to 5.5V Input Range**
- **Up to 800mA Output**
- **Step-Up Output (adjustable from 2.7V to 5.5V)**
- **PWM/PFM Synchronous-Rectified Topology**
- **External Clock or Internal 300kHz Oscillator (guaranteed ±14%)**
- **5µA Logic-Controlled Shutdown**
- **Power-Good Output (MAX1701)**
- **Low-Battery Comparator (MAX1701)**
- **Multi-Use Uncommitted Gain Block (MAX1701)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1700C/D	0°C to +70°C	Dice
MAX1700EEE	-40°C to +85°C	16 QSOP
MAX1701C/D	0°C to +70°C	Dice
MAX1701EEE	-40°C to +85°C	16 QSOP

Typical Operating Circuit



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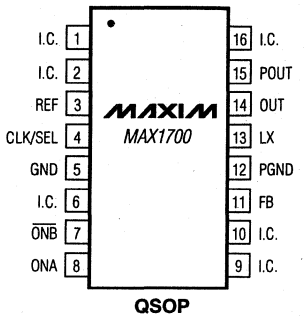
For small orders, phone 408-737-7600 ext. 3468.

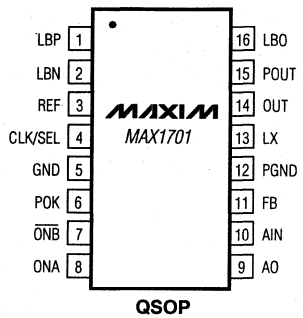
1-Cell to 3-Cell, High-Power (1A), Low-Noise, Step-Up DC-DC Converters

Pin Configurations

TOP VIEW



QSOP



QSOP

I.C. = INTERNAL CONNECTION. DO NOT CONNECT TO THIS PIN.

MAXIM

1-Cell to 3-Cell, High-Power (2A), Low-Noise Step-Up DC-DC Converter

General Description

The MAX1703 is a high-efficiency, low-noise, step-up DC-DC converter. This device is intended for use in battery-powered wireless applications. It uses a synchronous-rectifier pulse-width-modulation (PWM) boost topology to generate a 2.7V to 5V output from battery inputs such as one to three NiCd/NiMH cells or one Li-Ion cell. It has an internal 2A, 50mΩ, N-channel MOSFET switch and a 100mΩ, P-channel synchronous rectifier.

With its internal synchronous rectifier, the MAX1703 delivers 5% better efficiency than similar nonsynchronous converters. It also features a pulse-frequency-modulation (PFM) standby mode to improve efficiency at light loads, and a 1µA shutdown mode.

The MAX1703 comes in a 16-pin narrow SO package and includes an uncommitted comparator to generate a power-good or low-battery warning output. It also contains a linear-gain block that can be used to build a linear regulator using an external P-channel pass device.

For lower-power outputs and a smaller package, refer to the MAX1700/MAX1701. For dual outputs (step-up plus linear regulator), refer to the MAX1705/MAX1706. For an on-board analog-to-digital converter, refer to the MAX848/MAX849.

The MAX1703 evaluation kit is available to speed designs.

Features

- **92% Efficiency from 3V Input to 5V Output**
- **Guaranteed 1A Output at 5V from 3V Input**
- **Up to 1.5A Output**
- **Fixed 5V or Adjustable Step-Up Output (2.7V to 5V)**
- **0.8V to 5.5V Input Range**
- **Low-Power (300µW) Standby Mode**
- **Low-Noise, Constant-Frequency Mode (300kHz)**
- **Switching Frequency Synchronizable (200kHz to 400kHz)**
- **1µA Logic-Controlled Shutdown**
- **Power-Good Comparator**
- **Uncommitted Op-Amp Gain Block**

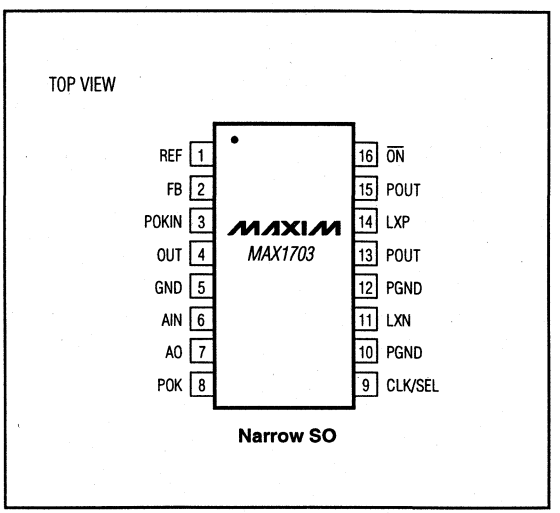
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1703C/D	0°C to +70°C	Dice
MAX1703ESE	-40°C to +85°C	16 Narrow SO

Applications

Digital Cordless Phones
PCS Phones
Wireless Handsets
Two-Way Pagers
Personal Communicators
Palmtop Computers
Hand-Held Instruments

Pin Configuration



Narrow SO

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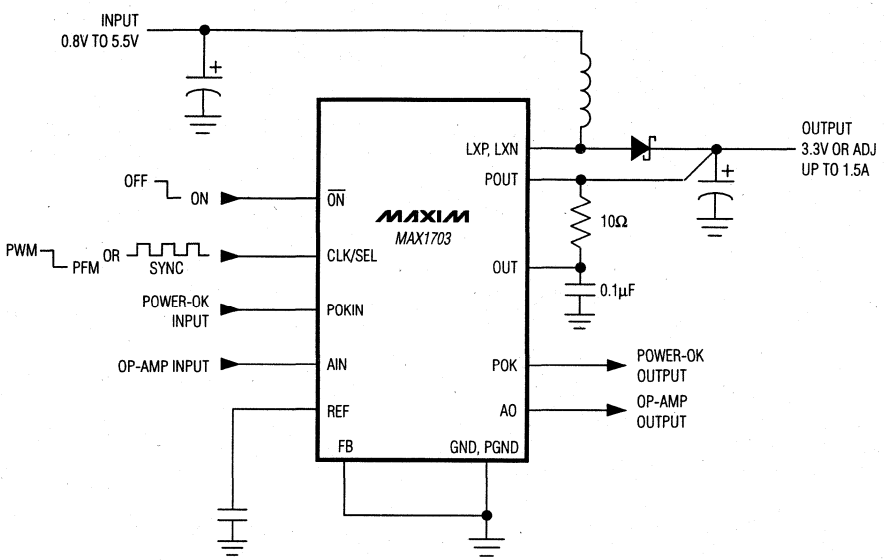
1-Cell to 3-Cell, High-Power (2A), Low-Noise Step-Up DC-DC Converter

Typical Operating Circuit



19-1198; Rev 0; 4/97

EVALUATION KIT AVAILABLE

MAXIM

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

General Description

The MAX1705/MAX1706 are high-efficiency, low-noise, step-up DC-DC converters with an auxiliary linear-regulator output. These devices are intended for use in battery-powered wireless applications. They use a synchronous rectifier pulse-width-modulation (PWM) boost topology to generate 2.5V to 5.5V outputs from battery inputs, such as 1 to 3 NiCd/NiMH cells or 1 Li-Ion cell. The MAX1705 has an internal 1A N-channel MOSFET switch. The MAX1706 has a 0.5A switch. Both devices also have a built-in low-dropout linear regulator that delivers up to 200mA.

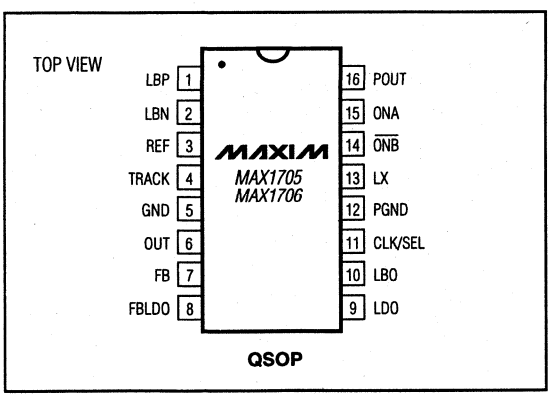
With an internal synchronous rectifier, the MAX1705/MAX1706 deliver 5% better efficiency than similar non-synchronous converters. They also feature a pulse-frequency-modulation (PFM) standby mode to improve efficiency at light loads, and a 1µA shutdown mode. An efficiency-enhancing track mode reduces the step-up DC-DC converter output to 300mV above the linear-regulator output.

Both devices come in a 16-pin QSOP package, which occupies the same space as an 8-pin SO. Other features include two shutdown-control inputs for push-on/push-off control, and an uncommitted comparator for use as a voltage monitor.

Applications

Digital Cordless Phones
Personal Communicators
Palmtop Computers
Hand-Held Instruments
PCS Phones
Wireless Handsets
Two-Way Pagers

Pin Configuration



Features

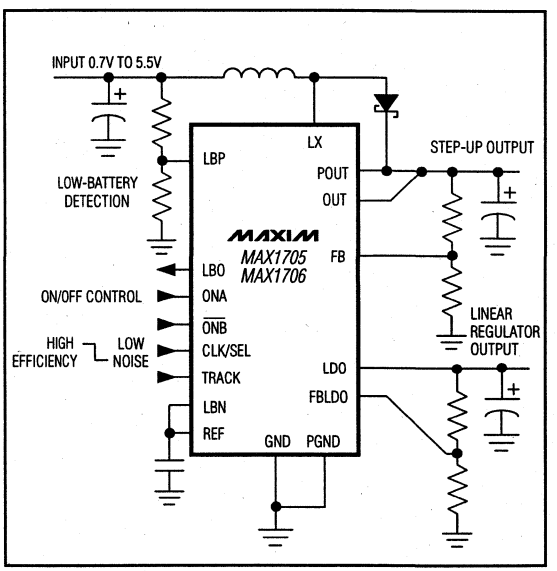
- ♦ **Up to 96% Efficiency**
- ♦ **1.1V_{IN} Guaranteed Start-Up**
- ♦ **Up to 850mA Output (MAX1705)**
- ♦ **Step-Up Output (2.5V to 5.5V adjustable)**
- ♦ **Linear Regulator (1.25V to 5.0V adjustable)**
- ♦ **PWM/PFM Synchronous-Rectified Topology**
- ♦ **300kHz PWM Mode or Synchronizable**
- ♦ **1µA Shutdown Mode**
- ♦ **Voltage Monitor**
- ♦ **Pushbutton On/Off Control**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1705C/D	0°C to +70°C	Dice*
MAX1705EEE	-40°C to +85°C	16 QSOP
MAX1706C/D	0°C to +70°C	Dice*
MAX1706EEE	-40°C to +85°C	16 QSOP

*Dice are tested at T_A = +25°C, DC parameters only.

Typical Operating Circuit



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1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

ABSOLUTE MAXIMUM RATINGS

ONA, $\overline{ONB}$, FBLDO, OUT, POUT to GND .....-0.3V to 6V
PGND to GND .....±0.3V
POUT to OUT .....±0.3V
LX to PGND .....-0.3V to (V_{POUT} + 0.3V)
CLK/SEL, REF, FB, TRACK, LDO,
LBN, LBP, LBO to GND .....-0.3V to (V_{OUT} + 0.3V)
LDO Short Circuit .....Continuous

Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{OUT} = V_{POUT} = V_{LBP} = 3.6V, CLK/SEL = FB = LBN = LBO = ONA = $\overline{ONB}$ = TRACK = GND, REF = open (bypassed with 0.22µF), LX = open, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC CONVERTER							
Minimum Start-Up Voltage		T_A = +25°C, I_{LOAD} < 1mA, Figure 2			0.9	1.1	V
Minimum Operating Battery Voltage		(Note 1)			0.7		V
FB Regulation Voltage		CLK/SEL = OUT		1.219	1.233	1.247	V
FB Input Current		V_{FB} = 1.5V			0.01	50	nA
OUT Adjust Range				2.5		5.5	V
Load Regulation		MAX1705, 0A ≤ I_{LX} ≤ 0.5A; MAX1706, 0A ≤ I_{LX} ≤ 0.25A; CLK/SEL = OUT			0.65	1.25	%
OUT Voltage in Track Mode		TRACK = V_{LDO} > 2.3V		V_{LDO} + 0.2	V_{LDO} + 0.3	V_{LDO} + 0.4	V
Frequency in Start-Up Mode	f_{LX}	V_{POUT} = V_{OUT} = 1.5V		40	150	300	kHz
Start-Up to Normal Mode Transition Voltage		(Note 2)		2.00	2.15	2.30	V
Supply Current in Shutdown	I_{OUT}	ONA = GND, $\overline{ONB}$ = OUT, measure I_{OUT}			1	20	µA
Supply Current in Low-Power Mode	I_{OUT}	CLK/SEL = GND, V_{FB} = V_{FBLDO} = 1.5V, no load			100	190	µA
Supply Current in Low-Noise Mode	I_{OUT}	CLK/SEL = OUT	V_{FB} = V_{FBLDO} = 1.5V, no load		180	360	µA
			FB = GND (LX switching)		2.1		mA
REFERENCE							
Reference Output Voltage		I_{REF} = 0µA		1.238	1.250	1.262	V
Reference Load Regulation		-1µA < I_{REF} < 50µA			4	15	mV
Reference Supply Regulation		2.5V < V_{OUT} < 5.5V			0.2	5	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = V_{POUT} = V_{LBP} = 3.6V, CLK/SEL = FB = LBN = LBO = ONA = $\overline{ONB}$ = TRACK = GND, REF = open (bypassed with 0.22µF), LX = open, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC SWITCHES							
POUT Leakage Current		V_{LX} = 0V, $V_{\overline{ONB}}$ = V_{OUT} = 5.5V			0.1	20	µA
LX Leakage Current		V_{LX} = 0V, $V_{\overline{ONB}}$ = V_{OUT} = 5.5V			0.1	20	µA
Switch On-Resistance		N-channel, I_{LX} = 100mA	CLK/SEL = GND		0.23	0.45	Ω
			CLK/SEL = OUT		0.16	0.28	
		P-channel, I_{LX} = 100mA			0.27	0.50	
N-Channel MOSFET Current Limit	I_{LIM}	CLK/SEL = OUT	MAX1705	1000	1280	1550	mA
			MAX1706	550	750	950	
		CLK/SEL = GND	MAX1705	250	435	550	
			MAX1706	250	435	550	
P-Channel Synchronous-Rectifier Turn-Off Current		CLK/SEL = GND		20	70	120	mA
LINEAR REGULATOR							
FBLDO Regulation Voltage		FBLDO = LDO, I_{LOAD} = 1mA		1.238	1.250	1.262	V
FBLDO Input Current		V_{FBLDO} = 1.5V			0.01	50	nA
LDO Adjust Range				1.25		5.0	V
Short-Circuit Current Limit		FBLDO = GND		220	300	500	mA
Dropout Resistance		V_{FBLDO} = 1V, I_{LDO} = 200mA			0.5	1.2	Ω
Load Regulation		10µA < I_{LDO} < 200mA, FBLDO = LDO			0.4	1.2	%
Line Regulation		2.5V < V_{OUT} < 5.5V, FBLDO = LDO, I_{LDO} = 1mA			0.1	0.5	%
AC Power-Supply Rejection		f = 300kHz			38		dB
Thermal Shutdown		Hysteresis approximately 10°C			155		°C
LOW-BATTERY COMPARATOR							
LBN, LBP Offset		LBP falling		-5		5	mV
LBN, LBP Hysteresis		LBP rising			16		mV
LBN, LBP Common-Mode Input Range		V_{LBN} = 0.5V and 1.5V (at least one input must be within this range)		0.5		1.5	V
LBN, LBP Input Current		V_{LBN} = V_{LBP} = 1V			0.01	50	nA
LBO Output Low Voltage		I_{SINK} = 1mA, V_{OUT} = 2.5V, LBP = GND, LBN = OUT				0.4	V
LBO High Leakage		V_{LBO} = V_{OUT} = 5V				1	µA
CONTROL INPUTS							
Input Low Level		1.2V < V_{OUT} < 5.5V, ONA, $\overline{ONB}$ (Note 3)				0.2V_{OUT}	V
		V_{OUT} = 2.5V, CLK/SEL, TRACK				0.2V_{OUT}	
Input High Level		1.2V < V_{OUT} < 5.5V, ONA, $\overline{ONB}$ (Note 3)		0.8V_{OUT}			V
		V_{OUT} = 5.5V, CLK/SEL, TRACK		0.8V_{OUT}			
Input Leakage Current (CLK/SEL, ONA, $\overline{ONB}$, TRACK)						1	µA

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = V_{POUT} = V_{LBP} = 3.6V, CLK/SEL = FB = LBN = LBO = ONA = $\overline{ONB}$ = TRACK = GND, REF = open (bypassed with 0.22µF), LX = open, **T_A = 0°C to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal Oscillator Frequency		CLK/SEL = OUT	260	300	340	kHz
External Oscillator Synchronization Range			200		400	kHz
Oscillator Maximum Duty Cycle			80	86	90	%
Minimum CLK/SEL Pulse				200		ns
Maximum CLK/SEL Rise/Fall Time				100		ns

ELECTRICAL CHARACTERISTICS

(V_{OUT} = V_{POUT} = V_{LBP} = 3.6V, CLK/SEL = FB = LBN = LBO = ONA = $\overline{ONB}$ = TRACK = GND, REF = open (bypassed with 0.22µF), LX = open, **T_A = -40°C to +85°C,** unless otherwise noted, Note 4.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC-DC CONVERTER							
FB Regulation Voltage		CLK/SEL = OUT		1.215		1.251	V
OUT Voltage in Track Mode		TRACK = OUT, V_{LDO} > 2.3V		V_{LDO} + 0.2		V_{LDO} + 0.4	V
Start-Up to Normal Mode Transition Voltage				2.0		2.3	V
Supply Current in Shutdown	I_{OUT}	ONA = 0V, $\overline{ONB}$ = OUT, measure I_{OUT}				20	µA
Supply Current in Low-Power Mode	I_{OUT}	CLK/SEL = 0V, FB = FBLDO = 1.5V, no load				190	µA
Supply Current in Low-Noise Mode	I_{OUT}	CLK/SEL = OUT, V_{FB} = V_{FBLDO} = 1.5V, no load				360	µA
REFERENCE							
Reference Output Voltage		I_{REF} = 0µA		1.235		1.265	V
DC-DC CONVERTER							
Switch On-Resistance		N-channel, I_{LX} = 100mA	CLK/SEL = 0V			0.45	Ω
			CLK/SEL = OUT			0.28	
		P-channel, I_{LX} = 100mA	CLK/SEL = OUT			0.50	
N-Channel MOSFET Current Limit	I_{LIM}	CLK/SEL = OUT	MAX1705	1000		1700	mA
			MAX1706	550		950	
		CLK/SEL = 0V	MAX1705	250		570	
			MAX1706	250		570	
P-Channel Synchronous-Rectifier Turn-Off Current		CLK/SEL = 0V		20		120	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{OUT} = V_{POUT} = V_{LBP} = 3.6V, CLK/SEL = FB = LBN = LBO = ONA = $\overline{ONB}$ = TRACK = GND, REF = open (bypassed with 0.22µF), LX = open, **T_A = -40°C to +85°C,** unless otherwise noted, Note 4.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR						
FBLDO Regulation Voltage		FBLDO = LDO, I_{LOAD} = 1mA	1.233		1.268	V
FBLDO Input Current		V_{FBLDO} = 1.5V		0.01	50	nA
Short-Circuit Current Limit		FBLDO = LDO = GND	220		600	mA
Dropout Resistance		V_{FBLDO} = 1V, I_{LDO} = 200mA			1.2	Ω
LOW-BATTERY COMPARATOR						
LBN, LBP Offset		LBP falling	-5		5	mV
LBN, LBP Common-Mode Input Range		LBN = 0.5V and 1.5V (at least one input must be within this range)	0.5		1.5	V
LBO High Leakage		LBO = OUT = 5V			1	µA
CONTROL INPUTS						
Input Low Level		1.2V < V_{OUT} < 5.5V, ONA, $\overline{ONB}$ (Note 2)			0.15V_{OUT}	V
		V_{OUT} = 2.5V, CLK/SEL, TRACK			0.15V_{OUT}	
Input High Level		1.2V < V_{OUT} < 5.5V, ONA, $\overline{ONB}$ (Note 2)	0.85V_{OUT}			V
		V_{OUT} = 5.5V, CLK/SEL, TRACK	0.85V_{OUT}			
Internal Oscillator Frequency		CLK/SEL = OUT	260		340	kHz
External Oscillator Synchronization Range			200		400	kHz

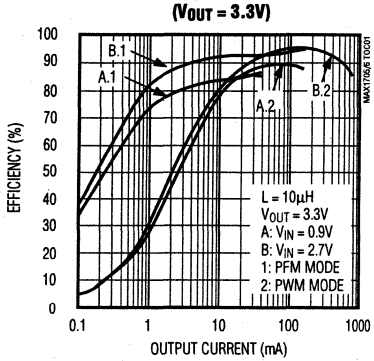
Note 1: Once the output is in regulation, the MAX1705/MAX1706 operate down to a 0.7V input voltage.
Note 2: The device is in start-up mode when V_{OUT} is below this value (see *Low-Voltage Start-Up Oscillator* section).
Note 3: ONA and $\overline{ONB}$ inputs have a hysteresis of approximately 0.15V_{OUT}.
Note 4: Specifications to -40°C to are guaranteed by design, not production tested.

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

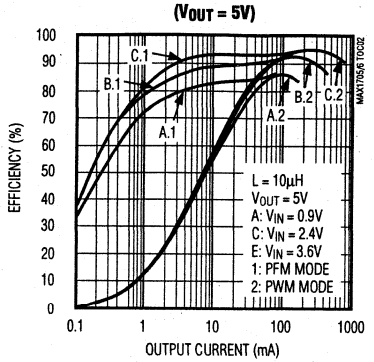
Typical Operating Characteristics

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

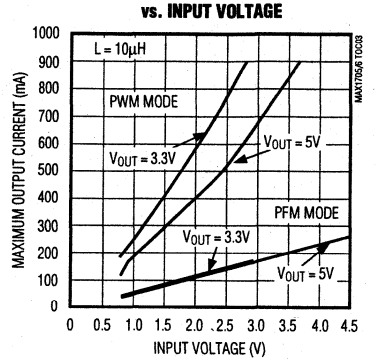
MAX1705
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 3.3V)



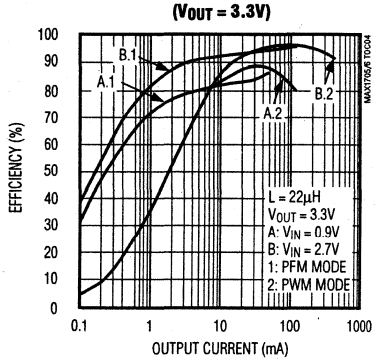
MAX1705
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 5V)



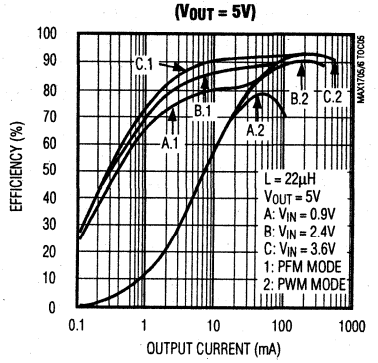
MAX1705
MAXIMUM OUTPUT CURRENT
vs. INPUT VOLTAGE



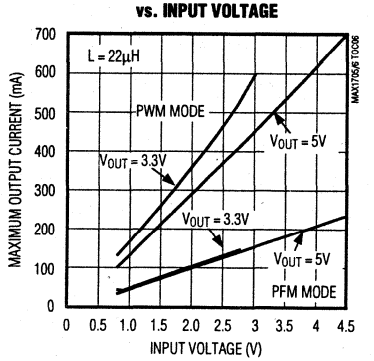
MAX1706
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 3.3V)



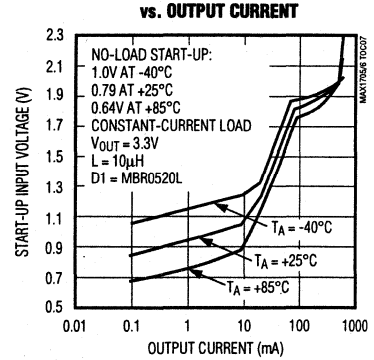
MAX1706
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 5V)



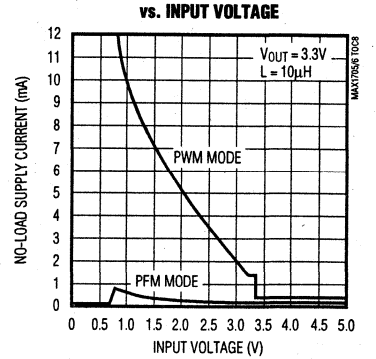
MAX1706
MAXIMUM OUTPUT CURRENT
vs. INPUT VOLTAGE



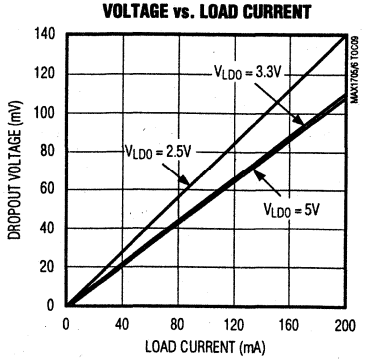
MAX1705
START-UP INPUT VOLTAGE
vs. OUTPUT CURRENT



NO-LOAD SUPPLY CURRENT
vs. INPUT VOLTAGE



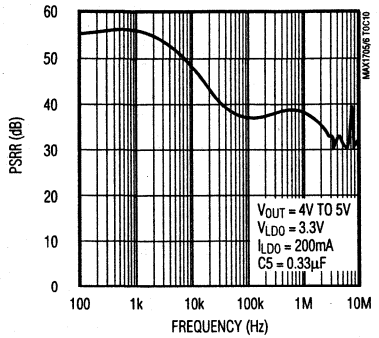
LINEAR-REGULATOR DROPOUT
VOLTAGE vs. LOAD CURRENT



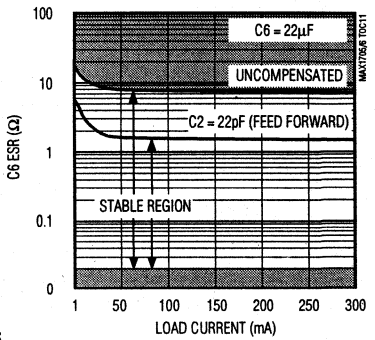
Typical Operating Characteristics (continued)

(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

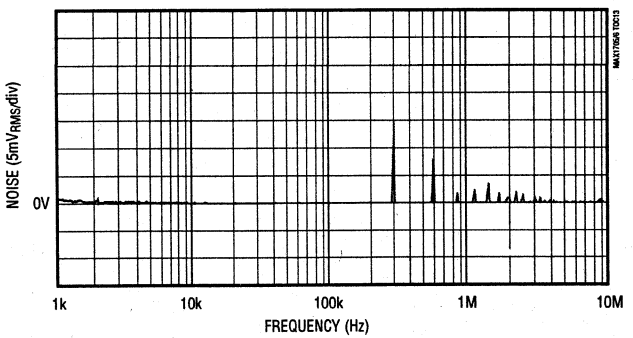
LINEAR-REGULATOR POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



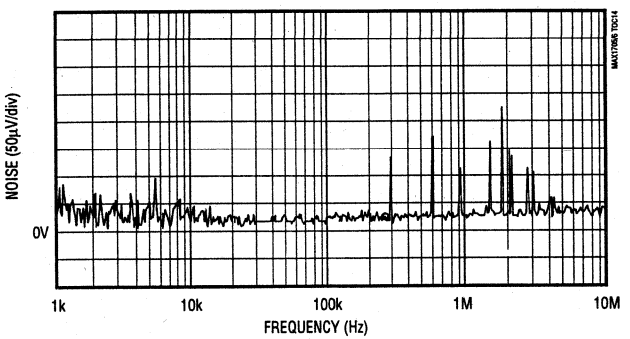
LINEAR-REGULATOR REGION OF STABLE C6 ESR vs. LOAD CURRENT



MAX1705
NOISE SPECTRUM AT POUT
(V_{OUT} = 4.5V, V_{IN} = 1.2V, 200mA LOAD)



MAX1705
LINEAR-REGULATOR OUTPUT NOISE SPECTRUM
(V_{LDO} = 3.3V, V_{OUT} = 4.5V, V_{IN} = 1.2V, I_{LDO} = 200mA)

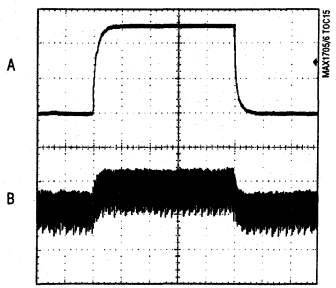


1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

Typical Operating Characteristics (continued)

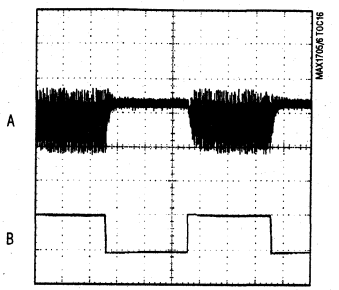
(Circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

MAX1705
LINE-TRANSIENT RESPONSE



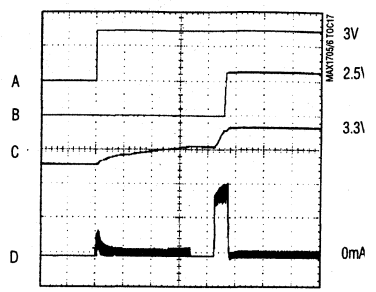
I_{OUT} = 0mA, V_{OUT} = 3.3V
A = V_{IN}, 1.5V TO 2.0V, 200mV/div
B = V_{OUT}, 10mV/div, 3.3V DC OFFSET

MAX1705
LOAD-TRANSIENT RESPONSE



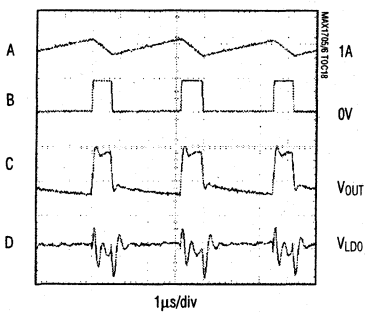
V_{IN} = 1.2V, V_{OUT} = 3.3V
A = V_{OUT}, 50mV/div, 3.3V DC OFFSET
B = I_{OUT}, 0mA TO 200mA, 200mA/div

MAX1705
POWER-ON DELAY
(PWM MODE)



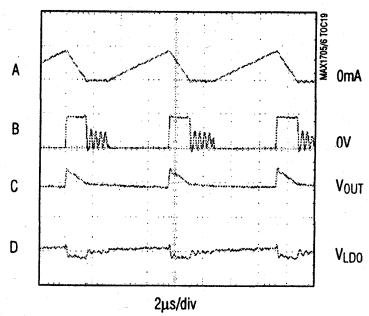
V_{IN} = 1.2V, LOAD = 1kΩ
A = ONA, 2V/div
B = V_{LDO}, 2V/div
C = V_{OUT}, 2V/div
D = INDUCTOR CURRENT, 500mA/div

MAX1705
PWM SWITCHING WAVEFORMS



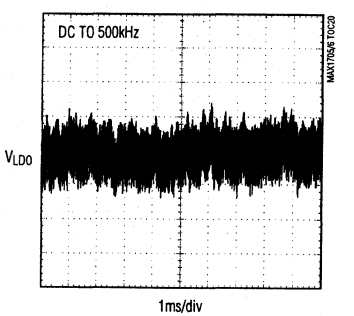
V_{IN} = 1.2V, V_{OUT} = 4.5V, V_{LDO} = 3.3V, I_{LDO} = 200mA
A = INDUCTOR CURRENT, 500mA/div
B = LX VOLTAGE, 5V/div
C = V_{OUT} RIPPLE, 50m/div AC COUPLED
D = V_{LDO} RIPPLE, 5m/div AC COUPLED
C5 = 0.33µF

MAX1705
PFM SWITCHING WAVEFORMS



V_{IN} = 1.2V, V_{OUT} = 4.5V, V_{LDO} = 3.3V, I_{LDO} = 40mA
A = INDUCTOR CURRENT, 500mA/div
B = LX VOLTAGE, 5V/div
C = V_{OUT} RIPPLE, 50mV/div AC COUPLED
D = V_{LDO} RIPPLE, 5mV/div AC COUPLED
C5 = 0.33µF

MAX1705
LINEAR-REGULATOR
OUTPUT NOISE



V_{LDO} IS AC COUPLED, 1mv/div
I_{LDO} = 200mA
C5 = 0.33µF

Pin Description

PIN	NAME	FUNCTION
1	LBP	Low-Battery Comparator Noninverting Input. Common-mode range is 0.5V to 1.5V.
2	LBN	Low-Battery Comparator Inverting Input. Common-mode range is 0.5V to 1.5V.
3	REF	1.250V Reference Output. Bypass REF with a 0.33µF capacitor to GND. REF can source up to 50µA.
4	TRACK	Track-Mode Control Input for DC-DC Converter. In track mode, the boost-converter output is sensed at OUT and set 0.3V above LDO to improve efficiency. Set TRACK to OUT for track mode. Connect TRACK to GND for normal operation.
5	GND	Ground
6	OUT	Step-Up Converter Feedback Input, used during track mode. IC power and low-dropout linear-regulator input. Bypass OUT to GND with a 0.1µF ceramic capacitor placed as close to the IC as possible.
7	FB	Step-Up DC-DC Converter Feedback Input. Connect FB to a resistor voltage divider between POUT and GND to set the output voltage between 2.5V and 5.5V. FB regulates to 1.233V.
8	FBLDO	Low-Dropout Linear-Regulator Feedback Input. Connect FBLDO to a resistor voltage divider between LDO to GND to set the output voltage from 1.25V to V_{OUT} - 0.3V (5.0V max). FBLDO regulates to 1.250V.
9	LDO	Low-Dropout Linear-Regulator Output. LDO sources up to 200mA. Bypass to GND with a 22µF capacitor.
10	LBO	Low-Battery Comparator Output. This open-drain, N-channel output is low when LBP < LBN. Input hysteresis is 16mV.
11	CLK/SEL	Switching-Mode Selection and External-Clock Synchronization Input: • CLK/SEL = low: low-power, low-quiescent-current PFM mode. • CLK/SEL = high: low-noise, high-power PWM mode. Switches at a constant frequency (300kHz). Full output power is available. • CLK/SEL = driven with an external clock: low-noise, high-power synchronized PWM mode. Synchronizes to an external clock (from 200kHz to 400kHz). Turning on the DC-DC converter with CLK/SEL = GND also serves as a soft-start function, since peak inductor current is reduced.
12	PGND	Power Ground for the source of the N-channel power MOSFET switch
13	LX	Inductor connection to the drains of the P-channel synchronous rectifier and N-channel switch
14	$\overline{ONB}$	Off Control Input. When $\overline{ONB}$ = high and ONA = low, the IC is off. Connect $\overline{ONB}$ to GND for normal operation (Table 2).
15	ONA	On Control Input. When ONA = high or $\overline{ONB}$ = low, the IC turns on. Connect ONA to OUT for normal operation (Table 2).
16	POUT	Boost DC-DC Converter Power Output. POUT is the source of the P-channel synchronous-rectifier MOSFET switch. Connect an external Schottky diode from LX to POUT. The output current available from POUT is reduced by the current drawn from the LDO linear-regulator output.

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

Detailed Description

The MAX1705/MAX1706 are designed to supply both power and low-noise circuitry in portable RF and data-acquisition instruments. They combine a linear regulator, step-up switching regulator, N-channel power MOSFET, P-channel synchronous rectifier, precision reference, and low-battery comparator in a single 16-pin QSOP package (Figure 1). The switching DC-DC converter boosts a 1- or 2-cell input to an adjustable output between 2.5V and 5.5V. The internal low-dropout regulator provides linear post-regulation for noise-sensitive circuitry, as well as outputs from 1.25V to 300mV below the switching-regulator output. The MAX1705/MAX1706 start from a low, 1.1V input and remain operational down to 0.7V.

These devices are optimized for use in cellular phones and other applications requiring low noise during full-power operation, as well as low quiescent current for maximum battery life during standby and shutdown. They feature constant-frequency (300kHz), low-noise pulse-width-modulation (PWM) operation with 300mA or 730mA output capability from one or two cells, respectively, with 3.3V output. A low-quiescent-current standby pulse-frequency-modulation (PFM) mode offers an output up to 60mA and 140µA, respectively, and reduces quiescent power consumption to 500µW. In shutdown mode, the quiescent current is further reduced to just 1µA. Figure 2 shows the standard application circuit for the MAX1705 configured in high-power PWM mode.

Additional features include synchronous rectification for high efficiency and improved battery life, and an uncommitted comparator for low-battery detection. A CLK/SEL input allows frequency synchronization to reduce interference. Dual shutdown controls allow shutdown using a momentary pushbutton switch and microprocessor control.

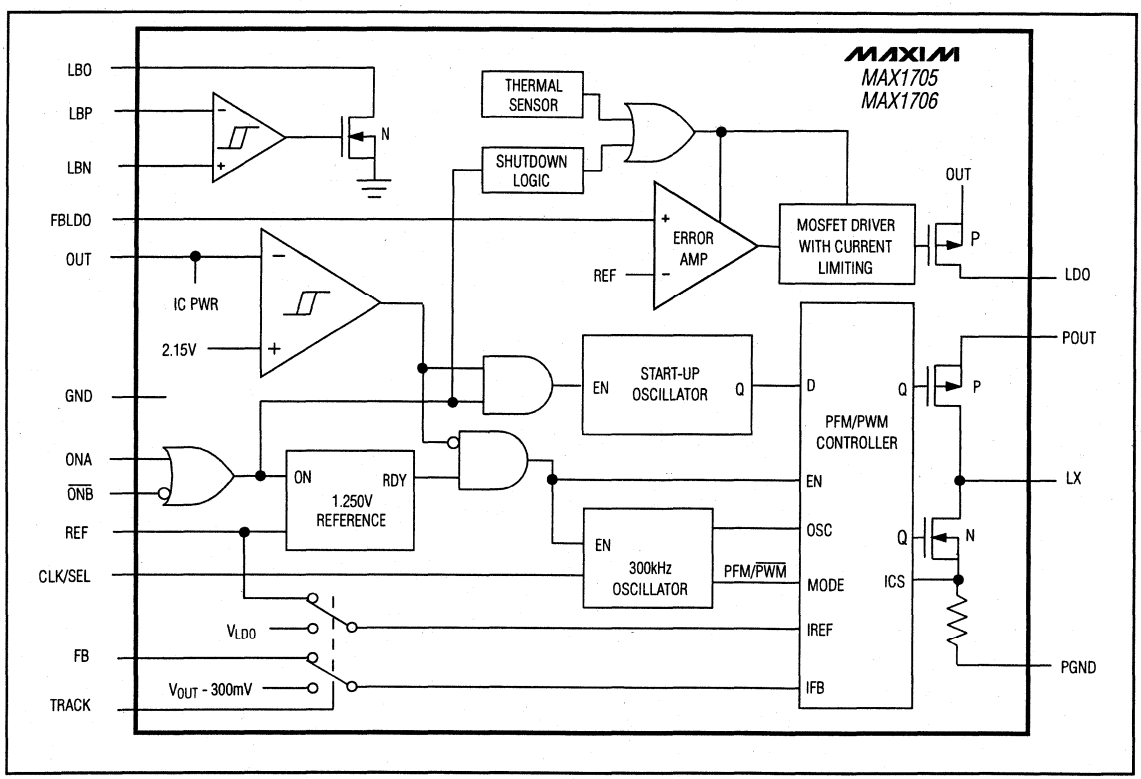


Figure 1. Functional Diagram

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

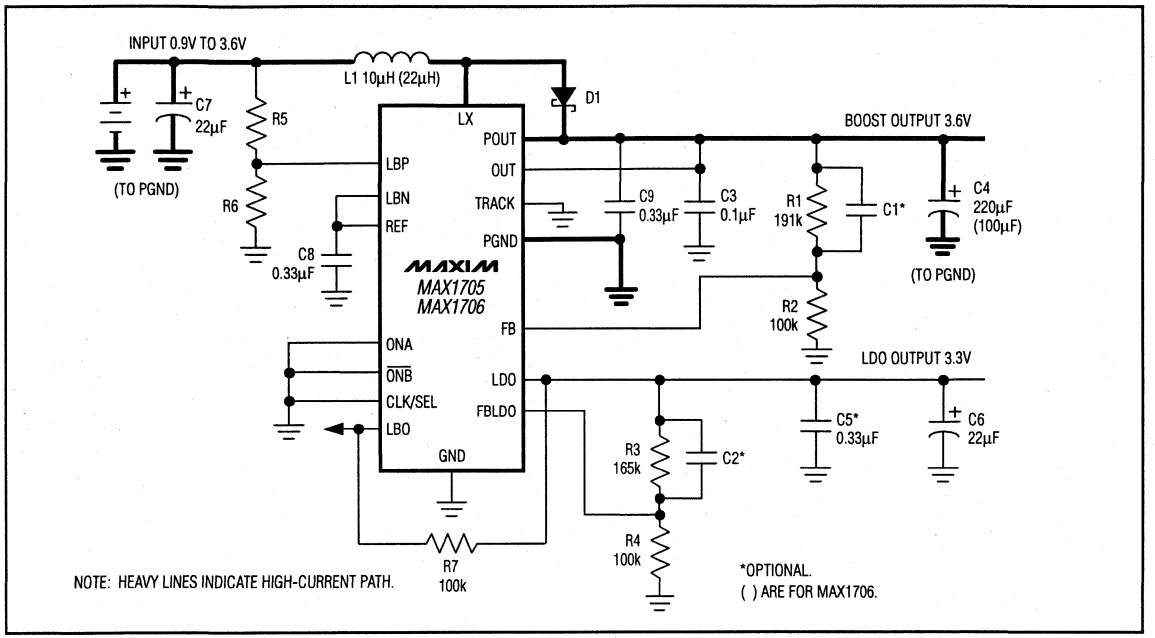


Figure 2. Typical Operating Circuit (PWM Mode)

Step-Up Converter

The step-up switching DC-DC converter generates an adjustable output to supply both power circuitry (such as RF power amplifiers) and the internal low-dropout linear regulator. During the first part of each cycle, the internal N-channel MOSFET switch is turned on. This allows current to ramp up in the inductor and store energy in a magnetic field. During the second part of each cycle, when the MOSFET is turned off, the voltage across the inductor reverses and forces current through the diode and synchronous rectifier to the output filter capacitor and load. As the energy stored in the inductor is depleted, the current ramps down, and the output diode and synchronous rectifier turn off. Voltage across the load is regulated using either PWM or PFM operation, depending on the CLK/SEL pin setting (Table 1).

Low-Noise, High-Power PWM Operation

When CLK/SEL is pulled high, the MAX1705/MAX1706 operate in a high-power, low-noise PWM mode. During PWM operation, they switch at a constant frequency (300kHz), and modulate the MOSFET switch pulse width to control the power transferred per cycle and regulate the voltage across the load. In PWM mode, the devices can output up to 850mA. Switching harmonics generated by fixed-frequency operation are consistent and easily filtered.

During PWM operation, each of the internal clock's rising edges sets a flip-flop, which turns on the N-channel MOSFET switch (Figure 3). The switch is turned off when the sum of the voltage-error and current-feedback signals trips a multi-input comparator and resets the flip-flop; the switch remains off for the rest of the cycle. When a change occurs in the output voltage error signal into the comparator, it shifts the level that the inductor current is allowed to ramp to during each cycle and modulates the MOSFET switch pulse width. A second comparator enforces a 1.55A (max) inductor-

Table 1. Selecting the Operating Mode

CLK/SEL	MODE	FEATURES
0	PFM	Low supply current
1	PWM	Low noise, high output current
External Clock (200kHz to 400kHz)	Synchronized PWM	Low noise, high output current

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

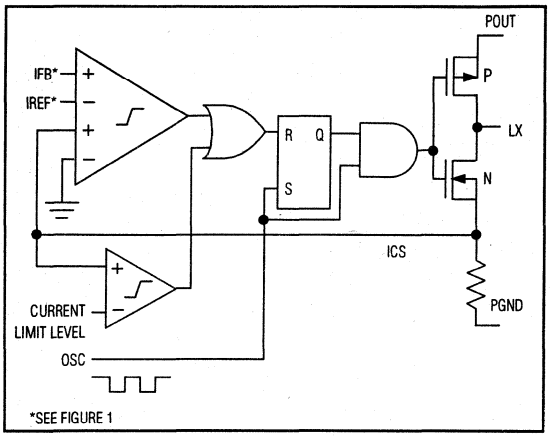


Figure 3. Simplified PWM Controller Block Diagram

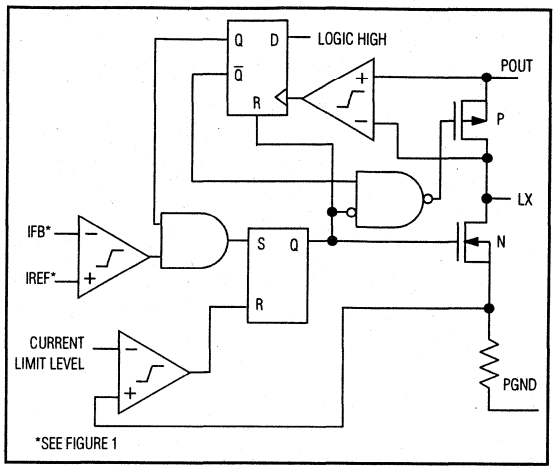


Figure 4. Controller Block Diagram in PFM Mode

current limit for the MAX1705, and 950mA (max) for the MAX1706. During PWM operation, the circuit operates with a continuous inductor current.

Synchronized PWM Operation

The MAX1705/MAX1706 can also be synchronized to a 200kHz to 400kHz frequency by applying an external clock to CLK/SEL. This allows the user to set the harmonics, to avoid IF bands in wireless applications. The synchronous rectifier is also active during synchronized PWM operation.

Low-Power PFM Operation

Pulling CLK/SEL low places the MAX1705/MAX1706 in low-power standby mode. During standby mode, PFM operation regulates the output voltage by transferring a fixed amount of energy during each cycle, and then modulating the switching frequency to control the power delivered to the output. The devices switch only as needed to service the load, resulting in the highest possible efficiency at light loads. Output current capability in PFM mode is 140mA (from 2.4V input to 3.3V output). The output is regulated at 1.3% above the PWM threshold.

During PFM operation, the error comparator detects output voltage falling out of regulation and sets a flip-flop, turning on the N-channel MOSFET switch (Figure 4). When the inductor current ramps to the PFM mode current limit (435mA) and stores a fixed amount of energy, the current-sense comparator resets a flip-flop. The flip-flop turns off the N-channel switch and turns on the P-channel synchronous rectifier. A second flip-flop, previously reset by the switch's "on" signal, inhibits the error comparator from initiating another cycle until the energy stored in the inductor is dumped into the output filter capacitor and the synchronous rectifier current ramps down to 70mA. This forces operation with a discontinuous inductor current.

Synchronous Rectifier

The MAX1705/MAX1706 feature an internal 270mΩ, P-channel synchronous rectifier to enhance efficiency. Synchronous rectification provides a 5% efficiency improvement over similar nonsynchronous step-up regulators. In PWM mode, the synchronous rectifier is turned on during the second half of each cycle. In PFM mode, an internal comparator turns on the synchronous rectifier when the voltage at LX exceeds the step-up converter output, and then turns it off when the inductor current drops below 70mA.

Linear Regulator

The internal low-dropout linear regulator steps down the output from the step-up converter and reduces switching ripple. It is intended to power noise-sensitive analog circuitry, such as low-noise amplifiers and IF stages in cellular phones and other instruments, and can deliver up to 200mA. However, in practice, the maximum output current is further limited by the current available from the boost converter and by the voltage differential between OUT and LDO. Use a 22µF capacitor with a 1Ω or less equivalent series resistance (ESR) at the output for stability (see the Linear Regulator Region of Stable C6 ESR vs. Load Current graph in the *Typical Operating Characteristics*). During power-up, the linear regulator remains off until the step-up converter goes into regulation for the first time.

The linear regulator in the MAX1705/MAX1706 features a 0.5Ω, P-channel MOSFET pass transistor. This provides several advantages, including longer battery life, over similar designs using a PNP pass transistor. The P-channel MOSFET requires no base-drive current, which reduces quiescent current considerably. PNP-based regulators tend to waste base-drive current in dropout when the pass transistor saturates. The MAX1705/MAX1706 eliminate this problem.

The linear-regulator error amplifier compares the output feedback sensed at the FBLDO input against the internal 1.250V reference, and amplifies the difference (Figure 1). The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback signal is lower than the reference, the pass-transistor gate is pulled lower, allowing more current to pass to the output, thereby increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output. Additional blocks include a current-limiting block and a thermal-overload protection block.

Low-Voltage Start-Up Oscillator

The MAX1705/MAX1706 use a CMOS, low-voltage start-up oscillator for a 1.1V guaranteed minimum start-up input voltage at +25°C. On start-up, the low-voltage oscillator switches the N-channel MOSFET until the output voltage reaches 2.15V. Above this level, the normal step-up converter feedback and control circuitry take over. Once the device is in regulation, it can operate down to a 0.7V input, since internal power for the IC is bootstrapped from the output using the OUT pin.

To reduce current loading during step-up, the linear regulator is kept off until the start-up converter goes into regulation. Minimum start-up voltage is influenced by load and temperature (see the *Typical Operating Characteristics*). To allow proper start-up, do not apply a full load at POUT until after the device has exited start-up mode and entered normal operation.

Shutdown

The MAX1705/MAX1706 feature a shutdown mode that reduces quiescent current to less than 1µA, preserving battery life when the system is not in use. During shutdown, the reference, the low-battery comparator, and all feedback and control circuitry are off. The step-up converter's output drops to one Schottky diode drop below the input, but the linear regulator output is turned off.

Entry into shutdown mode is controlled by logic input pins ONA and $\overline{ONB}$ (Table 2). Both inputs have trip points near $0.5V_{OUT}$ with $0.15V_{OUT}$ hysteresis.

Table 2. On/Off Logic Control

ONA	$\overline{ONB}$	MAX1705/MAX1706
0	0	On
0	1	Off
1	0	On
1	1	On

Tracking

Connecting TRACK to the step-up converter output implements a tracking mode that sets the step-up converter output to 300mV above the linear-regulator output, improving efficiency. In track mode, feedback for the step-up converter is derived from the OUT pin. When TRACK is low, the step-up converter and linear regulator are separately controlled by their respective feedback inputs, FB and FBLDO. TRACK is a logic input with a $0.5V_{OUT}$ threshold, and should be hard-wired or switched with a slew rate exceeding 1V/µs. V_{LDO} must be set above 2.3V for track mode to operate properly.

On power-up with TRACK = OUT, the step-up converter initially uses the FB input to regulate its output. After the step-up converter goes into regulation for the first time, the linear regulator turns on. When the linear regulator reaches 2.3V, track mode is enabled and the step-up converter is regulated to 300mV above the linear-regulator output.

Low-Battery Comparator

The internal low-battery comparator has uncommitted inputs and an open-drain output capable of sinking 1mA. To use it as a low-battery-detection comparator, connect the LBN input to the reference, and connect the LBP input to an external resistor divider between the positive battery terminal and GND (Figure 2). The resistor values are then as follows:

$$R5 = R6\left(\frac{V_{IN,TH}}{V_{LBN}} - 1\right)$$

where $V_{IN,TH}$ is the desired input voltage trip point and $V_{LBN} = V_{REF} = 1.25V$. Since the input bias current into LBP is less than 50nA, R6 can be a large value (such as 270kΩ or less) without sacrificing accuracy. Connect the resistor voltage divider as close to the IC as possible, within 0.2in. (5mm) of the LBP pin. The inputs have a 0.5V to 1.5V common-mode input range, and a 16mV input-referred hysteresis.

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

The low-battery comparator can also be used to monitor the output voltage, as shown in Figure 5.

To set the low-battery threshold to a voltage below the 1.25V reference, insert a resistor divider between REF and LBN, and connect the battery to the LBP input through a 10kΩ current-limiting resistor (Figure 6). The equation for setting the resistors for the low-battery threshold is then as follows:

$$R5 = R6\left(\frac{V_{REF}}{V_{IN,TH}} - 1\right)$$

Alternatively, the low-battery comparator can be used to check the output voltage or to control the load directly on POUT during start-up (Figure 7). Use the following equation to set the resistor values:

$$R5 = R6\left(\frac{V_{OUT,TH}}{V_{LBP}} - 1\right)$$

where $V_{OUT,TH}$ is the desired output voltage trip point and V_{LBP} is connected to the reference or 1.25V.

Reference

The MAX1705/MAX1706 have an internal 1.250V, 1% bandgap reference. Connect a 0.33µF bypass capacitor to GND within 0.2in. (5mm) of the REF pin. REF can source up to 50µA of external load current.

Design Procedure

Setting the Output Voltages

Set the step-up converter output voltage between 2.5V and 5.5V by connecting a resistor voltage-divider to FB from OUT to GND, as shown in Figure 8. The resistor values are then as follows:

$$R1 = R2\left(\frac{V_{POUT}}{V_{FB}} - 1\right)$$

where V_{FB}, the step-up regulator feedback setpoint, is 1.233V. Since the input bias current into FB is less than 50nA, R2 can have a large value (such as 270kΩ or less) without sacrificing accuracy. Connect the resistor voltage-divider as close to the IC as possible, within 0.2in. (5mm) of the FB pin.

Alternatively, set the step-up converter output to track the linear regulator by 300mV. To accomplish this, set TRACK to OUT.

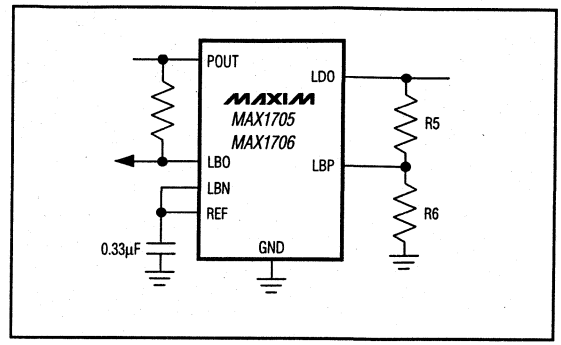


Figure 5. Using the Low-Battery Comparator to Sense the Output Voltage

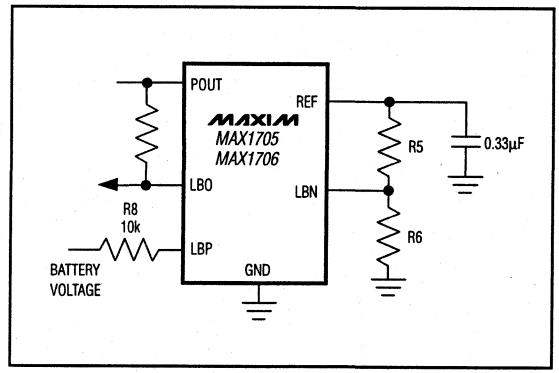


Figure 6. Detecting Battery Voltages Below 1.25V

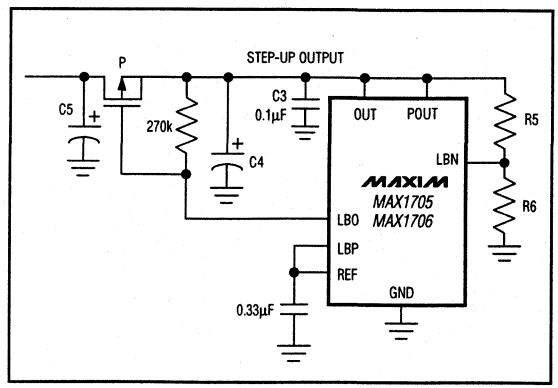


Figure 7. Using the Low-Battery Comparator for Load Control During Start-Up

To set the low-dropout linear-regulator output, use a resistor voltage-divider connected to FBLDO from LDO to GND. Set the output to a value at least 300mV less than the step-up converter output using the following formula:

$$R3 = R4\left(\frac{V_{LDO}}{V_{FBLDO}} - 1\right)$$

where V_{FBLDO}, the linear-regulator feedback trip point, is 1.250V. Since the input bias current into FBLDO is less than 50nA, R4 can be a large value (such as 270kΩ or less). Connect the resistor voltage-divider as close to the IC as possible, within 0.2in. (5mm) of the FBLDO pin.

Inductor Selection

The MAX1705/MAX1706's high switching frequency allows the use of a small surface-mount inductor. Use a 10µH inductor for the MAX1705 and a 22µH inductor for the MAX1706. Make sure the saturation-current rating exceeds the N-channel switch current limit of 1.55A for the MAX1705 and 950mA for the MAX1706. For high efficiency, chose an inductor with a high-frequency core material, such as ferrite, to reduce core losses. To minimize radiated noise, use a torroid, pot core, or shielded-bobbin inductor. See Table 3 for suggested parts and Table 4 for a list of inductor suppliers. Connect the inductor from the battery to the LX pin as close to the IC as possible.

Attaching the Output Diode

Use a Schottky diode, such as a 1N5817, MBR0520L, or equivalent. The Schottky diode carries current during start-up, and in PFM mode after the synchronous rectifier turns off. Thus, the current rating only needs to be 500mA. Attach the diode between the LX and POUT pins, as close to the IC as possible.

In high-temperature applications, some Schottky diodes may be unsuitable due to high reverse-leakage currents. Try substituting a Schottky diode with a higher reverse voltage rating, or use an ultra-fast silicon rectifier with reverse recover times less than 60ns (such as a MUR150 or EC11FS1). Do not use ordinary rectifier diodes, since slow switching speeds and long reverse recovery times compromise efficiency and load regulation.

Choose Input and Output Filter Capacitors

Choose input and output filter capacitors that service the input and output peak currents with acceptable voltage ripple. Choose input capacitors with working voltage ratings over the maximum input voltage, and output capacitors with working voltage ratings higher than the output.

A 100µF, 100mΩ, low-ESR tantalum capacitor is recommended at the MAX1706's step-up output. For the MAX1705, use two in parallel or a 220µF low-ESR tantalum capacitor. The input filter capacitor (C7) also reduces peak currents drawn from the input source and reduces input switching noise. The input voltage source impedance determines the size required for the input capacitor. When operating directly from one or two NiCd cells placed close to the MAX1705/MAX1706, use a 22µF, low-ESR input filter capacitor. When operating from a power source placed farther away, or

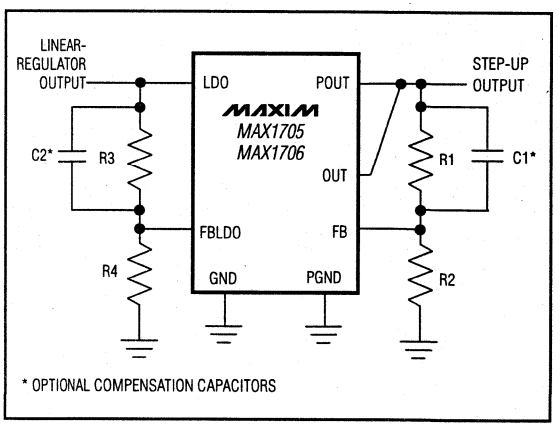


Figure 8. Feedback Connections for the MAX1705/MAX1706

Table 3. Component Selection Guide

PRODUCTION	INDUCTORS	CAPACITORS	DIODES
Surface Mount	Sumida CDR63B, CD73, CDR73B, CD74B series Coilcraft DO1608, DO3308, DT3316 series	Matsuo 267 series Sprague 595D series AVX TPS series	Motorola MBR0520L
Through Hole	Sumida RCH654 series	Sanyo OS-CON series Nichicon PL series	Motorola 1N5817

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

from higher-impedance batteries, consider using one or two 100µF, 100mΩ, low-ESR tantalum capacitors.

Low-ESR capacitors are recommended. Capacitor ESR is a major contributor to output ripple—often more than 70%.

Ceramic, Sanyo OS-CON, and Panasonic SP/CB-series capacitors offer the lowest ESR. Low-ESR tantalum capacitors are second best and generally offer a good trade-off between price and performance. Do not exceed the ripple-current ratings of tantalum capacitors. Avoid aluminum-electrolytic capacitors, since their ESR is too high.

Adding Bypass Capacitors

Several ceramic bypass capacitors are required for proper operation of the MAX1705/MAX1706. Bypass REF with a 0.33µF capacitor to GND. Connect a 0.1µF ceramic capacitor from OUT to GND and a 0.33µF ceramic capacitor from POUT to PGND. Place a 22µF, low-ESR capacitor and an optional 0.33µF ceramic capacitor from the linear-regulator output LDO to GND. An optional 22pF ceramic capacitor can be added to the linear-regulator feedback network to reduce noise (C2, Figure 2). Place each of these as close to their respective pins as possible, within 0.2in. (5mm) of the DC-DC converter IC. High-value, low-voltage, surface-mount ceramic capacitors are now readily available in small packages; see Table 4 for suggested suppliers.

Designing a PC Board

High switching frequencies and large peak currents make PC board layout an important part of design. Poor design can cause excessive EMI and ground-bounce, both of which can cause instability or regulation errors by corrupting voltage- and current-feedback signals. It is highly recommended that the PC board example of the MAX1705 evaluation kit (EV kit) be followed.

Power components—such as the inductor, converter IC, filter capacitors, and output diode—should be placed as close together as possible, and their traces should be kept short, direct, and wide. Place the LDO output capacitor as close to the LDO pin as possible. Make the connection between POUT and OUT very short. Keep the extra copper on the board, and integrate it into ground as a pseudo-ground plane.

On multilayer boards, do not connect the ground pins of the power components using vias through an internal ground plane. Instead, place them close together and route them in a star-ground configuration using component-side copper. Then connect the star ground to the internal ground plane using vias.

Keep the voltage-feedback networks very close to the MAX1705/MAX1706—within 0.2in. (5mm) of the FB and FBLDO pins. Keep noisy traces, such as from the LX pin, away from the reference and voltage-feedback networks, especially the LDO feedback, and separated from them using grounded copper. Consult the MAX1705/MAX1706 EV kit for a full PC board example.

Table 4. Component Suppliers

SUPPLIER	PHONE	FAX
AVX	USA: (803) 946-0690 (800) 282-4975	(803) 626-3123
Coilcraft	USA: (847) 639-6400	(847) 639-1469
Matsuo	USA: (714) 969-2491	(714) 960-6492
Motorola	USA: (602) 303-5454	(602) 994-6430
Sanyo	USA: (619) 661-6835 Japan: 81-7-2070-6306	(619) 661-1055 81-7-2070-1174
Sumida	USA: (847) 956-0666 Japan: 81-3-3607-5111	(847) 956-0702 81-3-3607-5144

Applications Information

Use in a Typical Wireless Phone Application

The MAX1705/MAX1706 are ideal for use in digital cordless and PCS phones. The power amplifier (PA) is connected directly to the step-up converter output for maximum voltage swing (Figure 9). The internal linear regulator is used for post-regulation to generate low-noise power for DSP, control, and RF circuitry. Typically, RF phones spend most of their life in standby mode and short periods in transmit/receive mode. During standby, maximize battery life by setting CLK/SEL = GND and TRACK = OUT; this places the IC in PFM and track modes (for lowest quiescent power consumption). In transmit/receive mode, set TRACK = GND and CLK/SEL = OUT to increase the PA supply voltage and initiate high-power, low-noise PWM operation. Table 5 lists the typical available output current when operating with one or more NiCd/NiMH cells or one Li-Ion cell.

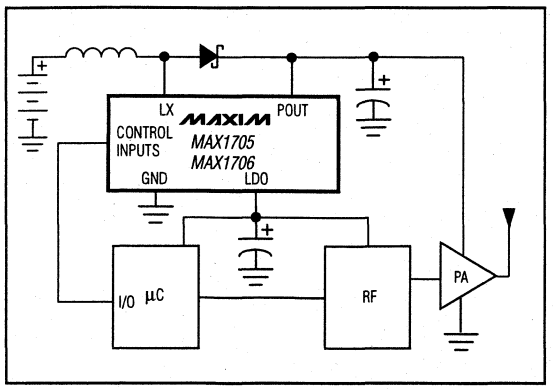


Figure 9. Typical Phone Application

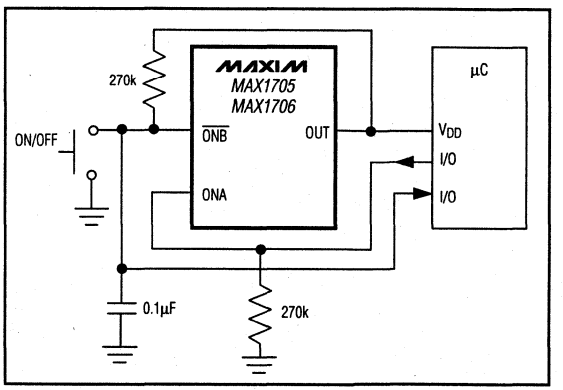


Figure 10. Momentary Pushbutton On/Off Switch

Table 5. Typical Available Output Current

NUMBER OF CELLS	INPUT VOLTAGE (V)	STEP-UP OUTPUT VOLTAGE: (PA POWER SUPPLY) (V)	TOTAL OUTPUT CURRENT (mA)	
			MAX1705	MAX1706
1 NiCd/NiMH	1.2	3.3	300	200
2 NiCd/NiMH	2.4	3.3	730	450
2 NiCd/NiMH	2.4	5.0	500	350
3 NiCd/NiMH or 1 Li-Ion	3.6	5.0	850	550

Implementing Soft-Start

To implement soft-start, set CLK/SEL low on power-up; this forces PFM operation and reduces the peak switching current to 435mA. Once the circuit is in regulation, CLK/SEL can be set high for full-power operation.

Adding a Manual Power Reset

A momentary pushbutton switch can be used to turn the MAX1705/MAX1706 on and off (Figure 10). ONA is pulled low and $\overline{ONB}$ is pulled high to turn the part off. When the momentary switch is pressed, $\overline{ONB}$ is pulled low and the regulator turns on. The switch must be pressed long enough for the microcontroller (µC) to exit reset (200ms) and drive ONA high. A small capacitor is added to help debounce the switch. The µC issues a logic high to ONA, which holds the part on regardless of the switch state. To turn the regulator off, press the switch again, allowing the µC to read the switch status and pull ONA low. When the switch is released, $\overline{ONB}$ is pulled high.

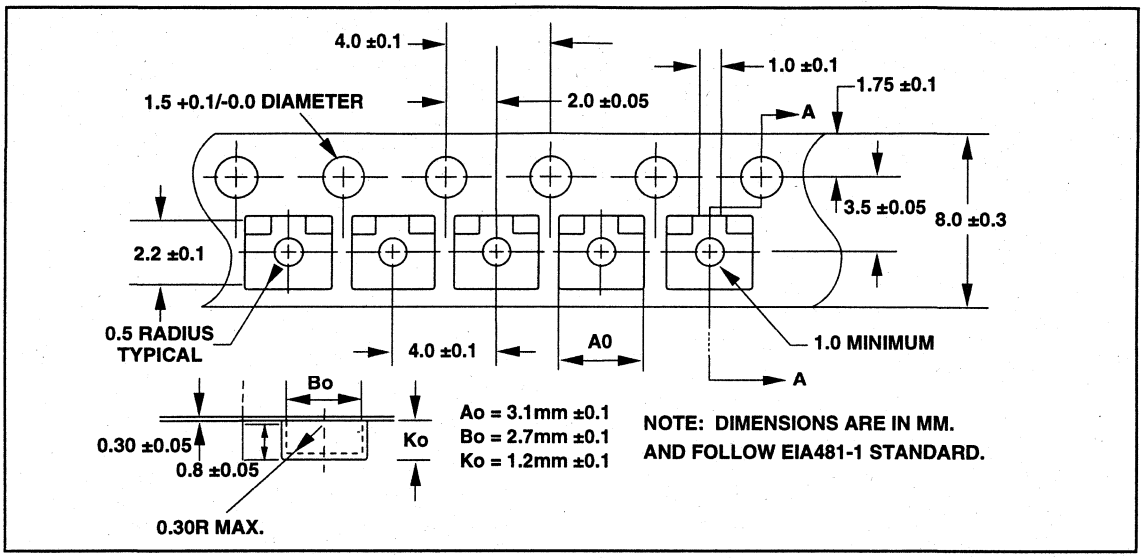
Chip Information

TRANSISTOR COUNT: 1649

SUBSTRATE CONNECTED TO GND

1- to 3-Cell, High-Current, Low-Noise, Step-Up DC-DC Converters with Linear Regulator

Tape-and-Reel Information



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Noise, Low-Dropout, 150mA Linear Regulators in SOT-23

General Description

The MAX8867/MAX8868 low-noise, low-dropout linear regulators operate from a 2.5V to 5.5V input and deliver up to 150mA. Typical output noise is 30μV_{RMS}. The output voltage is preset to common voltages from 2.5V to 5.0V in 100mV increments. Typical dropout is 110mV at 100mA. These devices are pin-compatible with the MAX8863/MAX8864.

The MAX8867/MAX8868 use an internal P-channel MOSFET pass transistor, which keeps the supply current at a low 90µA, independent of the load current and dropout voltage.

Other features include a 1µA logic-controlled shutdown, short-circuit and thermal-shutdown protection, and reverse battery protection. The MAX8868 also includes an auto-discharge function, which actively discharges the output voltage to ground when the device is placed in shutdown. Both devices come in a miniature 5-pin SOT23 package.

Applications

Cellular Telephones
Cordless Telephones
PCS Telephones
PCMCIA Cards
Modems
Hand-Held Instruments
Palmtop Computers
Electronic Planners

Features

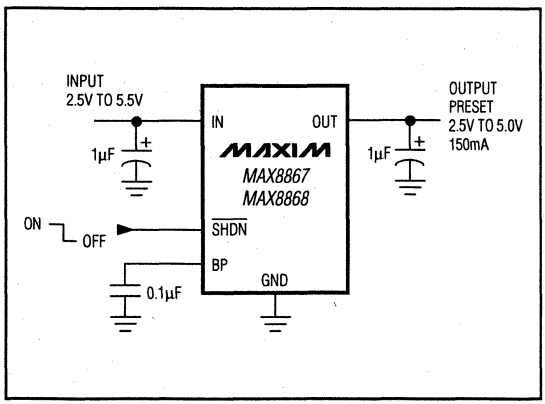
- ♦ **Low 30μV_{RMS} Output Noise**
- ♦ **Low 110mV Dropout at 100mA Output (165mV at 150mA Output)**
- ♦ **Low 90µA Operating Supply Current, Independent of Output Current and Dropout**
- ♦ **Thermal Overload and Short-Circuit Protection**
- ♦ **Reverse Battery Protection**
- ♦ **Output Current Limit**
- ♦ **Preset Output Voltages (±3.5%)**
- ♦ **1µA Logic-Controlled Shutdown**
- ♦ **Pin-Compatible with the MAX8863/MAX8864**

Ordering Information

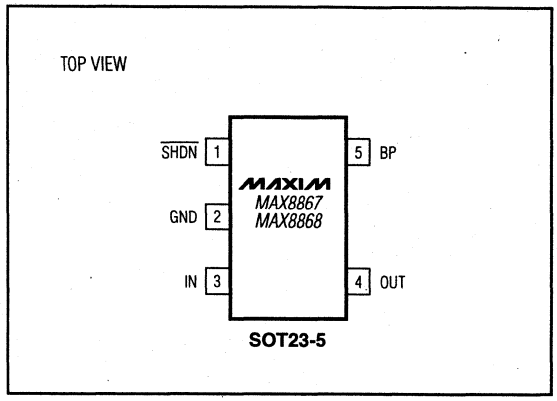
PART*	TEMP. RANGE	PIN-PACKAGE
MAX8867C/DXX	0°C to +70°C	Dice**
MAX8867EUKXX-T	-40°C to +85°C	SOT23-5
MAX8868C/DXX	0°C to +70°C	Dice**
MAX8868EUKXX-T	-40°C to +85°C	SOT23-5

**XX is the output voltage specification.*
***Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



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19-1257; Rev 0; 7/97

MAXIM

Low-Dropout, 120mA Linear Regulators

General Description

The MAX8873T/S/R and MAX8874T/S/R low-dropout linear regulators operate from a +2.5V to +5.5V input range and deliver up to 120mA. A PMOS pass transistor allows the low, 82µA supply current to remain independent of load, making these devices ideal for battery-operated portable equipment such as cellular phones and cordless phones.

The devices feature Dual Mode™ operation: their output voltage is preset (at 3.15V for the T versions, 2.84V for the S versions, or 2.80V for the R versions) or can be adjusted with an external resistor divider. Total error on the output is ±3.5%. Output voltages are set on the low side of popular ranges so that power drain is minimized for longer battery life. Other features include low-power shutdown, short-circuit protection, thermal shutdown protection, and reverse battery protection. The MAX8874 also includes an auto-discharge function, which actively discharges the output voltage to ground when the device is placed in shutdown mode. Both devices come in a miniature 5-pin SOT23 package.

For dual versions, refer to the MAX8865/MAX8866 data sheet. For low-noise versions with 30µV_{RMS} output noise, refer to the MAX8877/MAX8878.

Applications

Cordless Telephones	Modems
PCS Telephones	Hand-Held Instruments
Cellular Telephones	Palmtop Computers
PCMCIA Cards	Electronic Planners

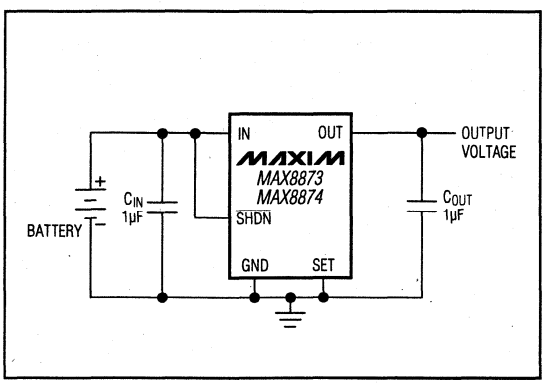
Features

- **LP2980 Pin-Compatible SOT23 Package**
- **Low, 55mV Dropout Voltage at 50mA I_{OUT} (130mV at 120mA)**
- **Low, 73µA No-Load Supply Current**
  Low, 82µA Operating Supply Current (even in dropout)
- **Miniature External Components**
- **Thermal Overload Protection**
- **Output Current Limit**
- **Reverse Battery Protection**
- **Dual Mode Operation: Fixed or Adjustable (1.25V to 5.5V) Output**
- **Low-Power Shutdown**

Ordering Information

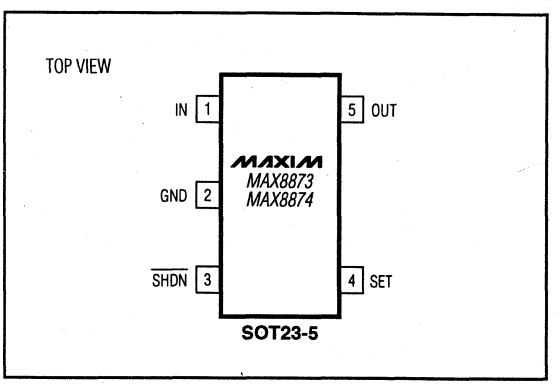
PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX8873TEUK-T	-40°C to +85°C	5 SOT23-5	ABZH
MAX8873SEUK-T	-40°C to +85°C	5 SOT23-5	ABZI
MAX8873REUK-T	-40°C to +85°C	5 SOT23-5	ABZL
MAX8874TEUK-T	-40°C to +85°C	5 SOT23-5	ABZJ
MAX8874SEUK-T	-40°C to +85°C	5 SOT23-5	ABZK
MAX8874REUK-T	-40°C to +85°C	5 SOT23-5	ABZM

Typical Operating Circuit



Dual Mode is a trademark of Maxim Integrated Products.

Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

Low-Dropout, 120mA Linear Regulators

ABSOLUTE MAXIMUM RATINGS

V_{IN} to GND ..... -6V to 6V
Output Short-Circuit Duration ..... Infinite
SET to GND ..... -0.3V to 6V
$\overline{SHDN}$ to GND ..... -6V to 6V
$\overline{SHDN}$ to IN ..... -6V to 0.3V
OUT to GND ..... -0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
SOT23-5 (derate 7.1mW/°C above +70°C) 571mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
θ_{JA} ..... 140°C/W
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage (Note 2)	V_{IN}			2.5		5.5	V
Output Voltage	V_{OUT}	0mA ≤ I_{OUT} ≤ 50mA, SET = GND	MAX887_T	3.05	3.15	3.25	V
			MAX887_S	2.75	2.84	2.93	
			MAX887_R	2.70	2.80	2.88	
Adjustable Output Voltage Range (Note 3)	V_{OUT}			V_{SET}		5.5	V
Maximum Output Current				120			mA
Current Limit (Note 4)	I_{LIM}				280		mA
Ground Pin Current	I_Q	SET = GND	I_{OUT} = 0mA		73	150	µA
			I_{OUT} = 50mA		82		
Dropout Voltage (Note 5)		I_{OUT} = 1mA			1.1		mV
		I_{OUT} = 50mA			55	120	
Line Regulation	ΔV_{LNR}	V_{IN} = 2.5V to 5.5V, SET tied to OUT, I_{OUT} = 1mA		-0.10	0	0.10	%/V
Load Regulation	ΔV_{LDR}	I_{OUT} = 0mA to 50mA	SET = GND		0.011	0.030	%/mA
			SET tied to OUT		0.006		
Output Voltage Noise		10Hz to 1MHz	C_{OUT} = 1µF		350		μV_{RMS}
			C_{OUT} = 100µF		220		
SHUTDOWN							
$\overline{SHDN}$ Input Threshold	V_{IH}			2.0			V
	V_{IL}					0.4	
$\overline{SHDN}$ Input Bias Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$ = V_{IN}	T_A = +25°C		0	100	nA
			T_A = T_{MAX}		0.05		
Shutdown Supply Current	I_{QSHDN}	V_{OUT} = 0V	T_A = +25°C		0.0001	1	µA
			T_A = T_{MAX}		0.02		
Shutdown to Output Discharge Delay (MAX8874)		C_{OUT} = 1µF, no load			1		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

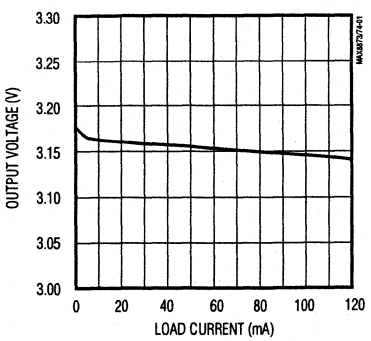
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SET INPUT							
SET Reference Voltage (Note 3)	V_{SET}	V_{IN} = 2.5V to 5.5V, I_{OUT} = 1mA	T_A = +25°C	1.225	1.25	1.275	V
			T_A = T_{MIN} to T_{MAX}	1.215	1.25	1.285	
SET Input Leakage Current (Note 3)	I_{SET}	V_{SET} = 1.3V	T_A = +25°C		0.015	2.5	nA
			T_A = T_{MAX}		0.5		
THERMAL PROTECTION							
Thermal Shutdown Temperature	T_{SHDN}				170		°C
Thermal Shutdown Hysteresis	ΔT_{SHDN}				20		°C

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.
Note 2: Guaranteed by line-regulation test.
Note 3: Adjustable mode only.
Note 4: For design purposes, the current limit should be considered 120mA minimum to 420mA maximum.
Note 5: The dropout voltage is defined as (V_{IN} - V_{OUT}) when V_{OUT} is 100mV below the value of V_{OUT} for V_{IN} = V_{OUT} + 2V.

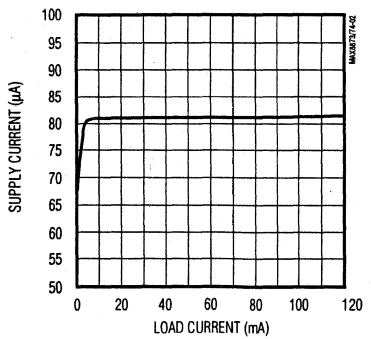
Typical Operating Characteristics

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, MAX887_T, T_A = +25°C, unless otherwise noted.)

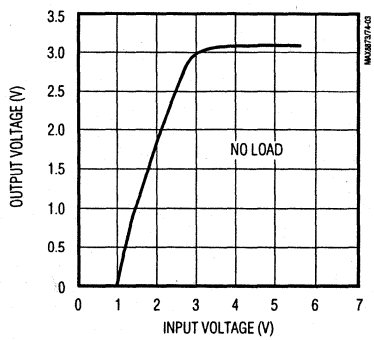
OUTPUT VOLTAGE vs. LOAD CURRENT



SUPPLY CURRENT vs. LOAD CURRENT



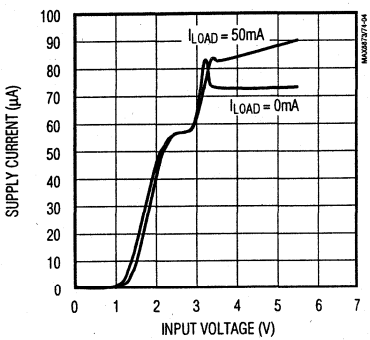
OUTPUT VOLTAGE vs. INPUT VOLTAGE



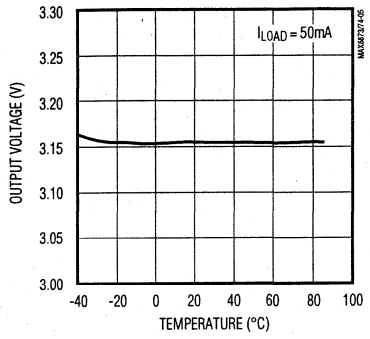
Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, MAX887_T, T_A = +25°C, unless otherwise noted.)

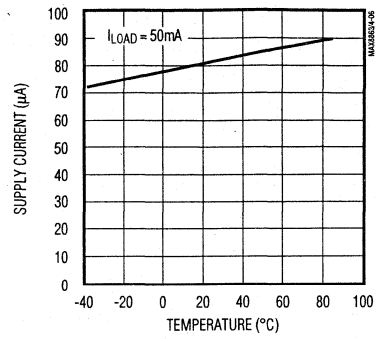
SUPPLY CURRENT vs. INPUT VOLTAGE



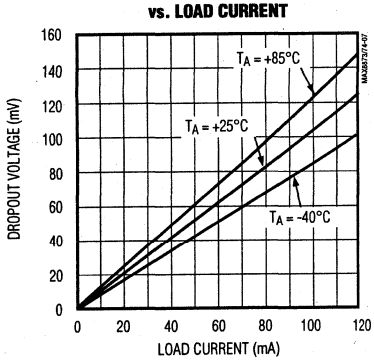
OUTPUT VOLTAGE vs. TEMPERATURE



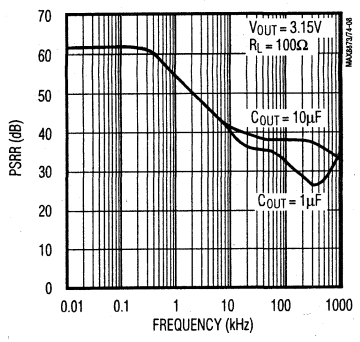
SUPPLY CURRENT vs. TEMPERATURE



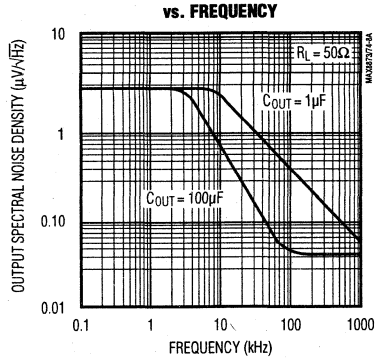
DROPOUT VOLTAGE vs. LOAD CURRENT



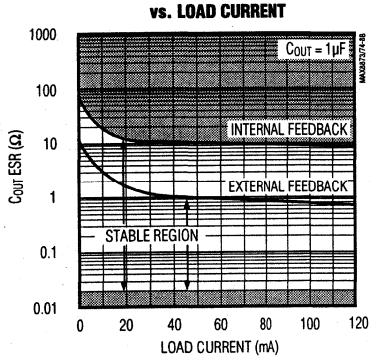
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



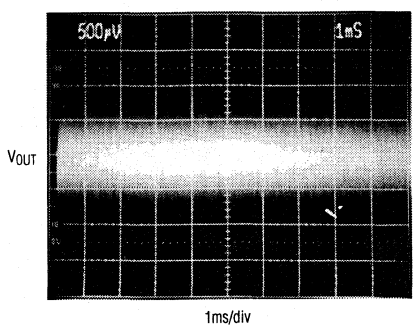
OUTPUT SPECTRAL NOISE DENSITY vs. FREQUENCY



REGION OF STABLE C_{OUT} ESR vs. LOAD CURRENT



OUTPUT NOISE DC TO 1MHz

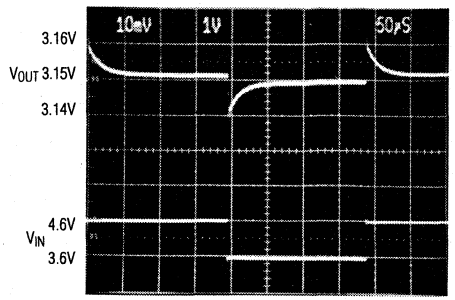


ILOAD = 50mA, VOUT IS AC COUPLED

Typical Operating Characteristics (continued)

(V_{IN} = +3.6V, C_{IN} = 1µF, C_{OUT} = 1µF, MAX887_T, T_A = +25°C, unless otherwise noted.)

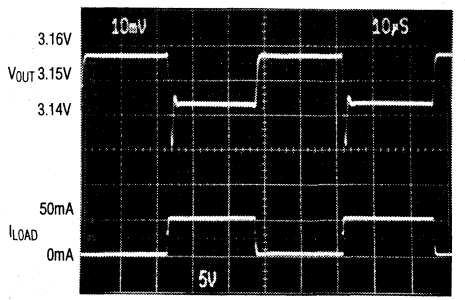
LINE-TRANSIENT RESPONSE



50µs/div

I_{LOAD} = 50mA, V_{OUT} IS AC COUPLED

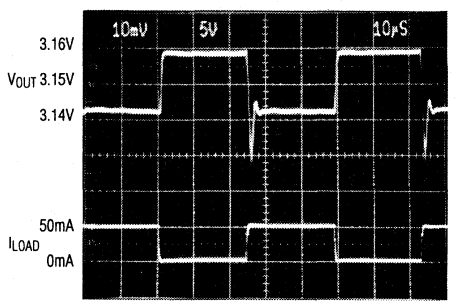
LOAD-TRANSIENT RESPONSE



10µs/div

I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

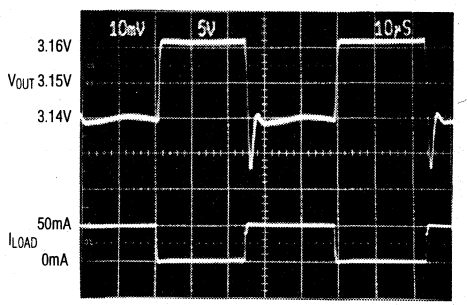
LOAD-TRANSIENT RESPONSE



10µs/div

V_{IN} = V_{OUT} + 0.2V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

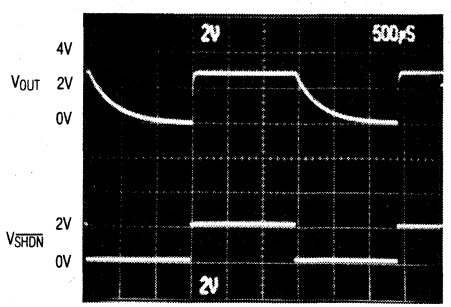
LOAD-TRANSIENT RESPONSE



10µs/div

V_{IN} = V_{OUT} + 0.1V, I_{LOAD} = 0mA to 50mA, C_{IN} = 10µF, V_{OUT} IS AC COUPLED

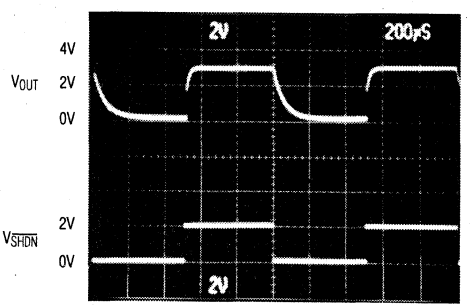
MAX8874 SHUTDOWN (NO LOAD)



500µs/div

NO LOAD

MAX8874 SHUTDOWN



200µs/div

I_{LOAD} = 50mA

Low-Dropout, 120mA Linear Regulators

Pin Description

PIN	NAME	FUNCTION
1	IN	Regulator Input. Supply voltage can range from +2.5V to +5.5V. Bypass with 1µF to GND (see *Capacitor Selection and Regulator Stability*).
2	GND	Ground. This pin also functions as a heatsink. Solder to large pads or the circuit board ground plane to maximize thermal dissipation.
3	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low reduces the supply current to 0.1nA. On the MAX8874, a logic low also causes the output voltage to discharge to GND. Connect to IN for normal operation.
4	SET	Feedback Input for Setting the Output Voltage. Connect to GND to set the output voltage to the preset 2.80V (MAX887_R), 2.84V (MAX887_S), or 3.15V (MAX887_T). Connect to an external resistor divider for adjustable-output operation. **DO NOT LEAVE THIS PIN UNCONNECTED.**
5	OUT	Regulator Output. Fixed or adjustable from 1.25V to 5.5V. Sources up to 120mA. Bypass with a 1µF, <0.2Ω typical ESR capacitor to GND.

Detailed Description

The MAX8873/MAX8874 are low-dropout, low-quiescent-current linear regulators designed primarily for battery-powered applications. They supply an adjustable 1.25V to 5.5V output or a preselected 2.80V (MAX887_R), 2.84V (MAX887_S), or 3.15V (MAX887_T) output for load currents up to 120mA. These devices consist of a 1.25V reference, error amplifier, MOSFET driver, P-channel pass transistor, dual-mode comparator, and internal feedback voltage divider (Figure 1).

The 1.25V bandgap reference is connected to the error amplifier's inverting input. The error amplifier compares this reference with the selected feedback voltage and amplifies the difference. The MOSFET driver reads the error signal and applies the appropriate drive to the P-channel pass transistor. If the feedback voltage is lower than the reference, the pass-transistor gate is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

The output voltage is fed back through either an internal resistor voltage divider connected to the OUT pin, or an external resistor network connected to the SET pin. The dual-mode comparator examines the SET voltage and selects the feedback path. If SET is below 60mV, internal feedback is used and the output voltage is regulated to the preset output voltage. Additional blocks include a current limiter, reverse battery protection, thermal sensor, and shutdown logic.

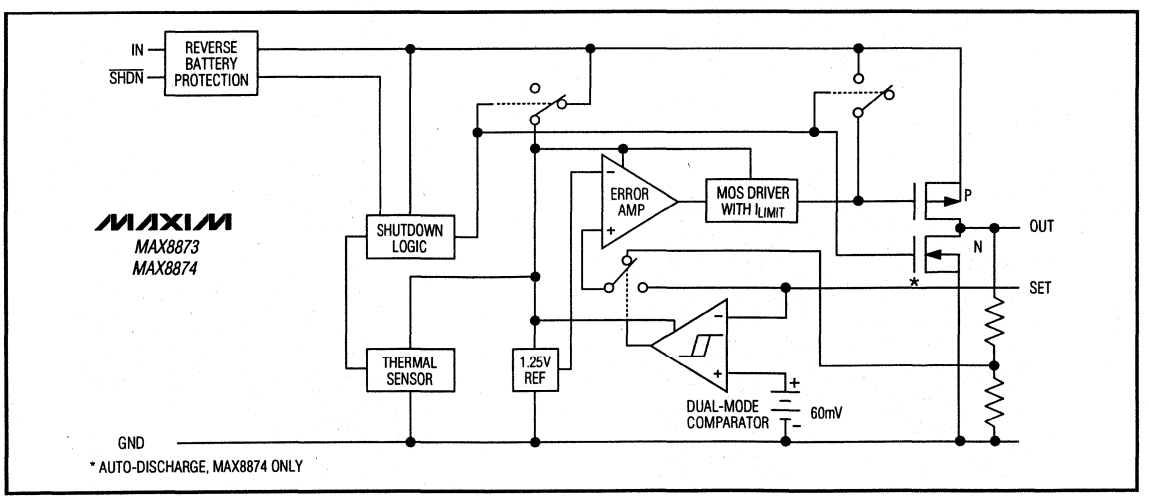


Figure 1. Functional Diagram

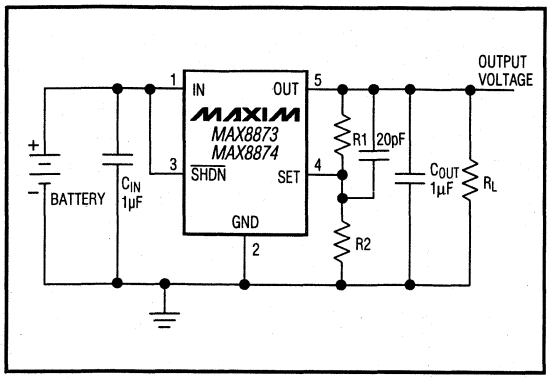


Figure 2. Adjustable Output Using External Feedback Resistors

Internal P-Channel Pass Transistor

The MAX8873/MAX8874 feature a 1.1Ω typical P-channel MOSFET pass transistor. This provides several advantages over similar designs using PNP pass transistors, including longer battery life.

The P-channel MOSFET requires no base drive current, which reduces quiescent current considerably. PNP-based regulators waste considerable amounts of current in dropout when the pass transistor saturates. They also use high base-drive currents under large loads. The MAX8873/MAX8874 do not suffer from these problems, and consume only 82µA of quiescent current, whether in dropout, light load, or heavy load applications (see *Typical Operating Characteristics*).

Output Voltage Selection

The MAX8873/MAX8874 feature Dual Mode operation: they operate in either a preset voltage mode or an adjustable mode.

In preset voltage mode, internal, trimmed feedback resistors set the MAX887_R output to 2.80V, the MAX887_S output to 2.84V, and the MAX887_T output to 3.15V. Select this mode by connecting SET to ground.

In adjustable mode, select an output between 1.25V and 5.5V using two external resistors connected as a voltage divider to SET (Figure 2). The output voltage is set by the following equation:

$$V_{OUT} = V_{SET} (1 + R1 / R2)$$

where V_{SET} = 1.25V. To simplify resistor selection:

$$R1 = R2 \left(\frac{V_{OUT}}{V_{SET}} - 1 \right)$$

Choose R2 = 100kΩ to optimize power consumption, accuracy, and high-frequency power-supply rejection. The total current through the external resistive feedback and load resistors should not be less than 10µA. Since the V_{SET} tolerance is typically less than ±25mV, the output can be set using fixed resistors instead of trim pots. Connect a 10pF to 25pF capacitor across R1 to compensate for layout-induced parasitic capacitances.

In preset voltage mode, impedances between SET and ground should be less than 100kΩ. Otherwise, spurious conditions could cause the voltage at SET to exceed the 60mV dual-mode threshold.

Shutdown

A low input on the $\overline{SHDN}$ pin shuts down the MAX8873/MAX8874. In shutdown mode, the pass transistor, control circuit, reference, and all biases are turned off, reducing the supply current to typically 0.1nA. Connect $\overline{SHDN}$ to IN for normal operation. The MAX8874 output voltage is actively discharged to ground when the part is placed in shutdown (see *Typical Operating Characteristics*).

Current Limit

The MAX8873/MAX8874 include a current limiter that monitors and controls the pass transistor's gate voltage, estimating the output current and limiting it to about 280mA. For design purposes, the current limit should be considered 120mA to 420mA. The output can be shorted to ground for an indefinite time period without damaging the part.

Thermal Overload Protection

Thermal overload protection limits total power dissipation in the MAX8873/MAX8874. When the junction temperature exceeds T_J = +170°C, the thermal sensor sends a signal to the shutdown logic, turning off the pass transistor and allowing the IC to cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature typically cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions.

Thermal overload protection is designed to protect the MAX8873/MAX8874 in the event of fault conditions. Stressing the device with high load currents and high input-output differential voltages (which result in die temperatures above +125°C) may cause a momentary overshoot (2% to 8% for 200ms) when the load is completely removed. This can be remedied by raising the minimum load current from 0µA (+125°C) to 100µA (+150°C). For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

Low-Dropout, 120mA Linear Regulators

Operating Region and Power Dissipation

Maximum power dissipation of the MAX8873/MAX8874 depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and ambient air, and the rate of air flow. The power dissipation across the device is $P = I_{OUT} (V_{IN} - V_{OUT})$. The resulting maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / \theta_{JA}$$

where $(T_J - T_A)$ is the temperature difference between the MAX8873/MAX8874 die junction and the surrounding air, and θ_{JA} is the thermal resistance of the chosen package to the surrounding air.

The GND pin of the MAX8873/MAX8874 performs the dual function of providing an electrical connection to ground and channeling heat away. Connect the GND pin to ground using a large pad or ground plane.

Reverse Battery Protection

The MAX8873/MAX8874 have a unique protection scheme that limits the reverse supply current to less than 1mA when either V_{IN} or $V_{\overline{SHDN}}$ falls below ground. The circuitry monitors the polarity of these two pins, disconnecting the internal circuitry and parasitic diodes when the battery is reversed. This feature prevents the device from overheating and damaging the battery.

Applications Information

Capacitor Selection and Regulator Stability

Normally, use a 1µF capacitor on the input and a 1µF capacitor on the output of the MAX8873/MAX8874. Larger input capacitor values and lower ESR provide better supply-noise rejection and transient response. A higher-value input capacitor (10µF) may be necessary if large, fast transients are anticipated and the device is located several inches from the power source. Improve load-transient response, stability, and power-supply rejection by using large output capacitors. For stable operation over the full temperature range, with load currents up to 120mA, a minimum of 1µF is recommended.

Noise

The MAX8873/MAX8874 exhibit $350\mu V_{RMS}$ noise during normal operation. When using the MAX8873/MAX8874 in applications that include analog-to-digital converters (ADCs) of greater than 12 bits, consider the ADC's power-supply rejection specifications (see the Output Noise DC to 1MHz photo in the *Typical Operating Characteristics*). For devices with lower output noise, refer to the MAX8877/MAX8878.

Power-Supply Rejection and Operation from Sources Other than Batteries

The MAX8873/MAX8874 are designed to deliver low dropout voltages and low quiescent currents in battery-powered systems. Power-supply rejection is 62dB at low frequencies and rolls off above 300Hz. As the frequency increases above 20kHz, the output capacitor is the major contributor to the rejection of power-supply noise (see the Power-Supply Rejection Ratio vs. Frequency graph in the *Typical Operating Characteristics*).

When operating from sources other than batteries, improve supply-noise rejection and transient response by increasing the values of the input and output capacitors, and by using passive filtering techniques (see the supply and load-transient responses in the *Typical Operating Characteristics*).

Load-Transient Considerations

The MAX8873/MAX8874 load-transient response graphs (see *Typical Operating Characteristics*) show two components of the output response: a DC shift of the output voltage due to the different load currents and the transient response. Typical overshoot for step changes in the load current from 0mA to 50mA is 14mV. Increasing the output capacitor's value and decreasing its ESR attenuates transient spikes.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this will determine the useful end-of-life battery voltage. Because the MAX8873/MAX8874 use a P-channel MOSFET pass transistor, their dropout voltage is a function of $R_{DS(ON)}$ multiplied by the load current (see *Electrical Characteristics*).

Chip Information

TRANSISTOR COUNT: 148

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Noise, Low-Dropout, 150mA Linear Regulators with '2982 Pinout

General Description

The MAX8877/MAX8878 low-noise, low-dropout linear regulators operate from a 2.5V to 5.5V input and deliver up to 150mA. These devices are pin compatible with the industry-standard '2982 and have better dropout voltage. Typical output noise is 30µV$_{RMS}$. The output voltage is preset to common voltages from 2.5V to 5.0V in 100mV increments. Typical dropout is 110mV at 100mA. These devices are pin compatible with the MAX8873/MAX8874.

The MAX8877/MAX8878 use an internal P-channel MOSFET pass transistor, which keeps the supply current at a low 90µA, independent of the load current and dropout voltage.

Other features include a 1µA logic-controlled shutdown, short-circuit and thermal-shutdown protection, and reverse battery protection. The MAX8878 also includes an auto-discharge function, which actively discharges output voltage to ground when the device is placed in shutdown. Both devices come in a miniature 5-pin SOT-23 package.

Features

- ♦ **Pin Compatible with the MAX8873/MAX8874 and '2982**
- ♦ **Low 30µV$_{RMS}$ Output Noise**
- ♦ **Low 110mV Dropout at 100mA Output (165mV at 150mA Output)**
- ♦ **Low 90µA Operating Supply Current, Independent of Output Current and Dropout**
- ♦ **Thermal-Overload and Short-Circuit Protection**
- ♦ **Reverse Battery Protection**
- ♦ **Output Current Limit**
- ♦ **Preset Output Voltages (±3.5%)**
- ♦ **1µA Logic-Controlled Shutdown**

Applications

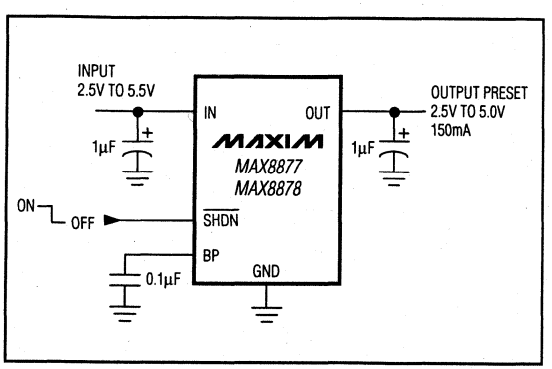
Cellular Telephones
Cordless Telephones
PCS Telephones
PCMCIA Cards
Modems
Hand-Held Instruments
Palmtop Computers
Electronic Planners

Ordering Information

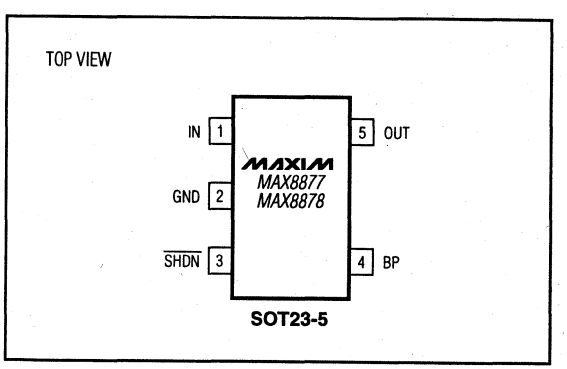
PART	TEMP. RANGE	PIN-PACKAGE
MAX8877C/DXX	0°C to +70°C	Dice*
MAX8877EUKXX-T	-40°C to +85°C	5 SOT23-5
MAX8878C/DXX	0°C to +70°C	Dice*
MAX8878EUKXX-T	-40°C to +85°C	5 SOT23-5

NOTE: XX is the output voltage specification.
**Contact factory for dice specifications.*

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

µP Supervisory Circuits

µP Supervisory Circuits, Product Tables and Trees 5-2

MAX6316 5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$, and Push/Pull $\overline{\text{RESET}}$ Output or Bidirectional $\overline{\text{RESET}}$ Output 5-7*

MAX6317 5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$, and Push/Pull RESET Output 5-7*

MAX6318 5-Pin µP Supervisory Circuit with Watchdog, Push/Pull RESET and Push/Pull $\overline{\text{RESET}}$ Output or Bidirectional $\overline{\text{RESET}}$ Output 5-7*

MAX6319 5-Pin µP Supervisory Circuit with Manual $\overline{\text{RESET}}$, Push/Pull RESET or Bidirectional $\overline{\text{RESET}}$ Output 5-7*

MAX6320 5-Pin µP Supervisory Circuit with Watchdog, Manual $\overline{\text{RESET}}$, and Open-Drain $\overline{\text{RESET}}$ Output 5-7*

MAX6321 5-Pin µP Supervisory Circuit with Watchdog, Open-Drain, and Push/Pull RESET Output 5-7*

MAX6322 5-Pin µP Supervisory Circuit with Manual $\overline{\text{RESET}}$, Open-Drain $\overline{\text{RESET}}$, and Push/Pull RESET Output 5-7*

MAX6326 3-Pin, Ultra-Low-Power µP Reset Circuit with Push/Pull $\overline{\text{RESET}}$ Output 5-9*

MAX6327 3-Pin, Ultra-Low-Power µP Reset Circuit with Push/Pull RESET Output 5-9*

MAX6328 3-Pin, Ultra-Low-Power µP Reset Circuit with Open-Drain $\overline{\text{RESET}}$ Output 5-9*

MAX6330L/S/T µP Reset Circuit with Shunt Regulator in 3-Pin SOT23 with $\overline{\text{RESET}}$ Output 5-11*

MAX6331L/S/T µP Reset Circuit with Shunt Regulator in 3-Pin SOT23 with RESET Output 5-11*

MAX6501 Low-Cost, +2.7V to +5.5V, Micropower, SOT Temperature-Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Hot Temperature Trip Threshold 5-13*

MAX6502 Low-Cost, +2.7V to +5.5V, Micropower, SOT Temperature-Reset IC with Push/Pull RESET Output and Hot Temperature Trip Threshold 5-13*

MAX6503 Low-Cost, +2.7V to +5.5V, Micropower, SOT Temperature-Reset IC with Open-Drain $\overline{\text{RESET}}$ Output and Cold Temperature Trip Threshold 5-13*

MAX6504 Low-Cost, +2.7V to +5.5V, Micropower, SOT Temperature-Reset IC with Push/Pull RESET Output and Cold Temperature Trip Threshold 5-13*

*Advance Information–first page of a data sheet in preparation.

µP Supervisory Circuits

±1% Reset-Threshold Accuracy (Over Temp.)

MAX814K/L/N/T
MAX816
(adj. reset threshold)

With Watchdog

MAX815K/L/N/T

~±1.5% Reset-Threshold Accuracy (Over Temp.)

With Backup-Battery Switchover

MAX801L/N/M

With Chip-Enable Gating

MAX808L/N/M

With Watchdog

MAX807L/N/M
(with low-line)

≥ ±2.5% Reset-Threshold Accuracy (Over Temp.)

MAX707
MAX708
MAX708R/S/T
MAX809L/M/R/S/T
MAX810L/M/R/S/T
MAX811L/M/R/S/T
MAX812L/M/R/S/T
MAX821L/M/R/S/T
MAX822L/M/R/S/T
MAX825L/M/R/S/T
MAX6305-6313
MAX6314
MAX6315
† MAX6316-22
† MAX6326/27/28
† MAX6330/6331L/T/S

With Backup-Battery Switchover

MAX703
MAX704
MAX704R/S/T
MAX806R/S/T
(±2% power fail)
MAX819L/M

With Watchdog

Reset Active High

MAX804R/S/T
(±2% power fail)
MAX805L/R/S/T

Reset Active Low

MAX690A
MAX690R/S/T
MAX692A
MAX802L/M/R/S/T (±2% power fail)
MAX817L/M

With Chip-Enable Gating

MAX691A
MAX693A
MAX793R/S/T
MAX794 (adj. reset threshold)
MAX818L/M
MAX1691
(module: MAX691A + lithium)

With Chip-Enable Gating

MAX795R/S/T

With Integrated RS-232 Interface

★ MAX3320A/B/L/T
(2TX, 2RX)

With Watchdog

Reset Active High

MAX706P
MAX813L
MAX824L/M/R/S/T
MAX1232
MAX6301-4

Reset Active Low

MAX705
MAX706
MAX706R/S/T
MAX823L/M/R/S/T
MAX824L/M/R/S/T
MAX1232

With Chip-Enable Gating

MAX792L/M/R/S/T
MAX820L/M/R/S/T
(±2% power fail)

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	Nominal Watchdog Timeout Period (sec), if available	Separate Watchdog Output	Backup-Battery Switch	$\overline{CE}$ Write Protection	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	Supply Current Operating Mode (µA) max (typ)	Pins	Price† 1000-up ($)
HIGH ACCURACY (1.0%, 1.5%)															
MAX801L/N/M	4.68/4.58/4.43	140	✔/±1.5%	✔/±1.5%	1.6		✔				✔		110(68)	8	3.17
MAX807L/N/M	4.68/4.58/4.43	140	✔/±1.5%	✔/±1.5%	1.6	✔	✔	✔/8ns	✔	✔	✔	✔	110(70)	16	3.29
MAX808L/N/M	4.68/4.58/4.43	140	✔/±1.5%				✔	✔/8ns			✔		90(48)	8	3.17
MAX814K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%	✔/±1%					✔/±2%	✔	✔		75	8	4.39
MAX815K/L/N/T	4.80/4.70/4.55/3.03	140	✔/±1%		1.6	✔			✔/±2%	✔			75	8	4.74
MAX816	Adj.	140	✔/±1%	✔/±1%					✔/±2%	✔			75	8	4.39
BATTERY-BACKUP SWITCHOVER															
MAX690A/692A	4.65/4.40	140	✔		1.6		✔		✔				350(200)	8	3.26
MAX690R/S/T	2.63/2.93/3.08	140	✔		1.6		✔		✔				500(400)	8	3.23
MAX691A/693A	4.65/4.40	140/adj.	✔	✔	1.6/adj.	✔	✔	✔/10ns	✔			✔	100(35)	16	3.61
MAX696	Adj.	35/adj.	✔	✔	1.6/adj.	✔	✔		✔			✔	300(160)	16	3.55
MAX703/704	4.65/4.40	140	✔				✔		✔	✔			350(200)	8	2.65
MAX704R/S/T	2.63/2.93/3.08	140	✔				✔		✔	✔			500(400)	8	2.93
MAX793R/S/T	2.63/2.93/3.08	140	✔	✔	1.6	✔	✔	✔	✔	✔	✔		60(46)	16	3.48
MAX794	Adj.	140	✔	✔	1.6	✔	✔	✔	✔	✔	✔		60(46)	16	3.48
MAX795R/S/T	2.63/2.93/3.08	140	✔				✔	✔			✔		60(46)	8	3.41
MAX804R/S/T	2.63/2.93/3.08	140		✔	1.6		✔		✔/±2%				500(400)	8	3.66
MAX805L/R/S/T	4.65/2.63/2.93/3.08	140		✔	1.6		✔		✔				350(200)	8	3.26
MAX806R/S/T	2.63/2.93/3.08	140	✔	✔			✔		✔/±2%	✔			500(400)	8	3.90
MAX817L/M	4.65/4.40	140	✔		1		✔		✔				45(11)	8	2.44
MAX818L/M	4.65/4.40	140	✔		1		✔	✔/8ns					45(11)	8	2.74
MAX819L	4.65	140	✔				✔		✔	✔			45(11)	8	2.07
MXD1210	4.37/4.62						✔	✔					500(230)	8	2.44
RESET WITHOUT BATTERY BACKUP															
MAX697	Adj.	35/adj.	✔	✔	1.6/adj.	✔		✔	✔				300(160)	16	3.58
MAX700	4.65/adj.	200	✔	✔						✔			200(100)	8	2.17
MAX705/706	4.65/4.40	140	✔		1.6	✔			✔	✔			350(200)	8	1.02*
MAX706R/S/T	2.63/2.93/3.08	140	✔		1.6	✔			✔	✔			350(200)	8	1.71
MAX707/708	4.65/4.40	140	✔	✔					✔	✔			350(200)	8	0.88*
MAX708R/S/T	2.63/2.93/3.08	140	✔	✔					✔	✔			350(200)	8	1.63
MAX792L/M/R/S/T	4.65/4.40/2.63/2.93/3.08	140	✔	✔	1	✔		✔/10ns	✔	✔	✔		150(70)	16	3.42
MAX813L	4.65	140		✔	1.6	✔			✔	✔			350(200)	8	1.02*
MAX1232	4.37/4.62	250	✔	✔	0.15/0.6/ 1.2					✔			200(50)	8	1.71
MAX6301–6304	Adj.	Adj.	✔	✔	Adj.								7(4)	8	1.51

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). Please contact your local sales office for volume pricing. International prices will differ due to local duties, taxes, and exchange rates.

* 25,000 pc. price, factory direct.

** 2,500 pc. price, factory direct. Only factory-direct orders in multiples of 2,500 or 10,000 pieces accepted (smaller quantities are available from distributors).

µP Supervisory Circuits (continued)

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Active-Low Reset	Active-High Reset	Nominal Watchdog Timeout Period (sec), if available	Separate Watchdog Output	Backup-Battery Switch	$\overline{CE}$ Write Protection	Power-Fail Comparator	Manual-Reset Input	Low-Line Output	Battery-On Output	Supply Current Operating Mode (µA) max (typ)	Pins	Price† 1000-up ($)
SOT RESET ICs															
MAX809L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔										60(24)	3	0.98**
MAX810L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔									60(24)	3	0.98**
MAX811L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔							✔			15(6) 10(3)	4	0.99**
MAX812L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140		✔						✔			15(6) 10(3)	4	0.99**
MAX821L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	0.5 to 100	✔										7(2.5) 5.5(1.8)	4	0.90**
MAX822L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	0.5 to 100		✔									7(2.5) 5.5(1.8)	4	0.90**
MAX823L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔		1.1					✔			24(10) 12(5)	5	1.20**
MAX824L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔	1.1								24(10) 2(5)	5	1.20**
MAX825L/M/R/S/T	4.65/4.40/ 2.63/2.93/3.08	140	✔	✔						✔			4(10) 12(5)	5	1.15**
MAX6305–6313	Dual reset with both adj. and customized trip thresholds	1 to 1000 customized								✔			16(8)	5	1.20**
MAX6314/6315	2.5 to 5.0 customized	1 to 1000 customized	✔							✔			12(5)	4	0.99**
MAX6316-22	2.5 to 5.0 customized	1 to 1000 customized	✔	✔	0.063 to 25.6 customized					✔			20(10)	5	††
MAX6326/27/28	2.20 to 3.08 customized	100	✔	✔									1(0.5)	3	††
MAX6330/6331	5.0, 3.3, 3.0	100	✔	✔									100(60)	3	††
SOT RESET ICs PLUS INTEGRATED RS-232 INTERFACE															
MAX3320A/B/L/T	4.25/2.85/4.63/3.08	100	✔										10(4)	20	—

† Prices provided are for design guidance and are FOB USA (unless otherwise noted). Please contact your local sales office for volume pricing. International prices will differ due to local duties, taxes, and exchange rates.

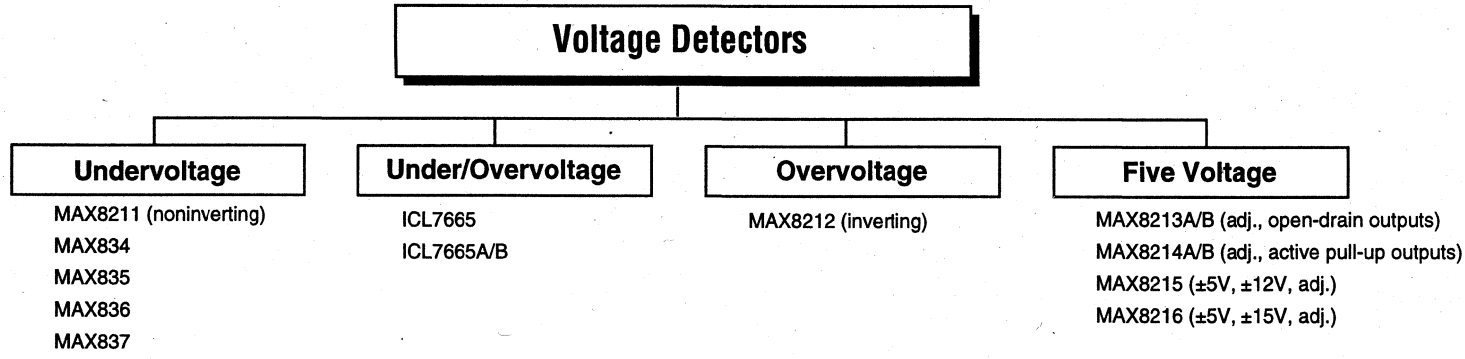
* 25,000 pc. price, factory direct

Reset Trip Threshold and Timeout Information

RESET TRIP THRESHOLDS						
SUFFIX‡	ACCURACY					
	±1%		~±1.5%		>±2.5%	
	MIN	MAX	MIN	MAX	MIN	MAX
K	4.75	4.85	—	—	—	—
L	4.65	4.75	4.60	4.75	4.50	4.75
N	4.50	4.60	4.50	4.65	—	—
M	4.35	4.50	4.35	4.50	4.25	4.50
T	3.00	3.06	—	—	3.00	3.15
S	—	—	—	—	2.85	3.00
R	—	—	—	—	2.55	2.70

CUSTOMIZED THRESHOLDS AND TIMEOUTS						
RESET TRIP THRESHOLD	RESET			WATCHDOG		
	CODE	TIMEOUT DELAY (sec)		CODE	TIMEOUT DELAY (sec)	
		MIN	MAX		MIN	MAX
2.5V to 5.0V in 0.1V increments	D1	1m	2m	W1	4.3m	9.3m
	D2	20m	40m	W2	7.1m	15.3m
	D3	140m	280m	W3	1.12	2.4
	D4	1.12	2.24	W4	17.9	38.4

‡ Not all parts have suffix indicator for trip thresholds. See *µP Supervisory Circuits* table for specific information.



Voltage Detectors

Part Number	Supply Voltage (V)	Supply Current (µA), max(typ)	Threshold Accuracy (%)	Package Options*	Temp. Ranges**	Description	Price† 1000-up ($)
MAX8211	+2 to +16.5	15(5)	±3.5	DIP, SO, TO8	C,E,M	Single channel: noninverting	1.33
MAX8212	+2 to +16.5	15(5)	±3.5	DIP, SO, TO8	C,E,M	Single channel: inverting	1.33
MAX8213A	+2.7 to +11	33(16)	±1	DIP, SO	C,E,M	5 voltage monitors, open-drain outputs	2.88
MAX8213B	+2.7 to +11	33(16)	±2	DIP, SO	C,E,M	5 voltage monitors, open-drain outputs	1.98
MAX8214A	+2.7 to +11	33(16)	±1	DIP, SO	C,E,M	5 voltage monitors, active pull-up outputs	2.88
MAX8214B	+2.7 to +11	33(16)	±2	DIP, SO	C,E,M	5 voltage monitors, active pull-up outputs	1.98
MAX8215	+2.7 to +11	250(137)	±1.25	DIP, SO	C,E,M	5 voltage monitors: ±5V, ±12V, adjustable	1.98
MAX8216	+2.7 to +11	250(137)	±1.25	DIP, SO	C,E,M	5 voltage monitors: ±5V, ±15V, adjustable	1.98
MAX834	+2.5 to +11	10(2.4)	±1.25	SOT23-5	E	Latching voltage monitor, open-drain output	1.20
MAX835	+2.5 to +11	10(2.4)	±1.25	SOT23-5	E	Latching voltage monitor, push/pull output	1.20
MAX836	+2.5 to +11	10(3.5)	±1.25	SOT143	E	Noninverting open-drain output	0.90
MAX837	+2.5 to +11	10(3.5)	±1.25	SOT143	E	Noninverting push/pull output	0.90
ICL7665A	+2 to +16	10(2.5)	±1.9	DIP, SO, TO8	C,E	Dual channel: one inverting, one noninverting	2.03

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO8 = Can
** Temp Ranges: C = 0°C to +70°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

5-Pin µP Supervisory Circuits with Watchdog and Manual Reset

General Description

The MAX6316–MAX6322 family of microprocessor (µP) supervisory circuits offers several combinations of push/pull, bidirectional, and open-drain outputs, along with watchdog and manual-reset features. All of these devices can be factory trimmed to any of 26 reset thresholds (from 2.5V to 5V in 0.1V increments), any of four reset timeout periods (from 1ms to 1.12sec minimum), and any of four watchdog timeout periods (from 6.3ms to 25sec). The MAX6316–MAX6322 are offered in a 5-pin SOT23 package.

Applications

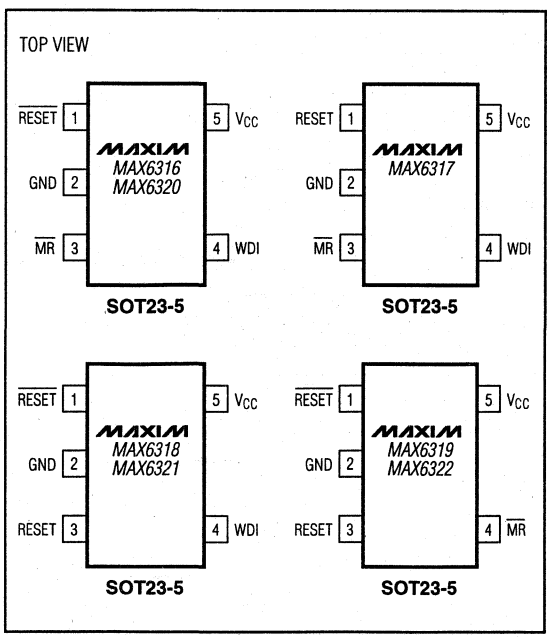
Portable Computers
Computers
Controllers
Intelligent Instruments
Portable/Battery-Powered Equipment
Embedded Control Systems

Features

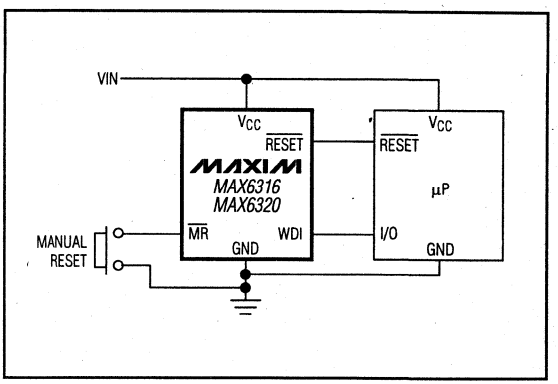
- **26 Factory-Trimmed Reset Voltages from 2.5V to 5V**
- **4 Factory-Trimmed Reset Timeouts from 1ms to 1.12sec (min)**
- **4 Factory-Trimmed Watchdog Timeouts from 6.3ms to 25sec**
- **No External Components**
- **Low Cost**
- **Highly Accurate Reset Threshold**
- **Immunity to Negative-Going V_{CC} Transients**
- **4 Reset Output Stages:**
  Active-Low Push/Pull
  Active-High Push/Pull
  Active-Low Open-Drain
  Bidirectional*
- **5-Pin SOT23 Package**

**A bidirectional reset output stage is designed to interface to µPs that have bidirectional reset pins, such as the Motorola 68HC11. These µPs can often determine if a reset was asserted by an external device (i.e., the supervisor IC) or by the µP itself (due to a watchdog fault, clock error, or other source).*

Pin Configurations



Typical Operating Circuit



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

5-Pin µP Supervisory Circuits with Watchdog and Manual Reset

Table 1. Factory-Trimmed Reset Thresholds*

SUFFIX	T_A = +25°C			T_A = 0°C to +70°C	
	MIN	TYP	MAX	MIN	MAX
MAX63_ _UK50D_W_-T	4.925	5.000	5.075	4.875	5.125
MAX63_ _UK49D_W_-T	4.827	4.900	4.974	4.778	5.023
MAX63_ _UK48D_W_-T	4.728	4.800	4.872	4.680	4.920
MAX63_ _UK47D_W_-T	4.630	4.700	4.771	4.583	4.818
MAX63_ _UK46D_W_-T	4.561	4.630	4.699	4.514	4.746
MAX63_ _UK45D_W_-T	4.433	4.500	4.568	4.388	4.613
MAX63_ _UK44D_W_-T	4.314	4.380	4.446	4.270	4.490
MAX63_ _UK43D_W_-T	4.236	4.300	4.365	4.193	4.408
MAX63_ _UK42D_W_-T	4.137	4.200	4.263	4.095	4.305
MAX63_ _UK41D_W_-T	4.039	4.100	4.162	3.998	4.203
MAX63_ _UK40D_W_-T	3.940	4.000	4.060	3.900	4.100
MAX63_ _UK39D_W_-T	3.842	3.900	3.959	3.803	3.998
MAX63_ _UK38D_W_-T	3.743	3.800	3.857	3.705	3.895
MAX63_ _UK37D_W_-T	3.645	3.700	3.756	3.608	3.793
MAX63_ _UK36D_W_-T	3.546	3.600	3.654	3.510	3.690
MAX63_ _UK35D_W_-T	3.448	3.500	3.553	3.413	3.588
MAX63_ _UK34D_W_-T	3.349	3.400	3.451	3.315	3.485
MAX63_ _UK33D_W_-T	3.251	3.300	3.350	3.218	3.383
MAX63_ _UK32D_W_-T	3.152	3.200	3.248	3.128	3.280
MAX63_ _UK31D_W_-T	3.034	3.080	3.126	3.003	3.157
MAX63_ _UK30D_W_-T	2.955	3.000	3.045	2.925	3.075
MAX63_ _UK29D_W_-T	2.886	2.930	2.974	2.857	3.000
MAX63_ _UK28D_W_-T	2.758	2.800	2.842	2.730	2.870
MAX63_ _UK27D_W_-T	2.660	2.700	2.741	2.633	2.768
MAX63_ _UK26D_W_-T	2.591	2.630	2.669	2.564	2.696
MAX63_ _UK25D_W_-T	2.463	2.500	2.538	2.438	2.563

**Factory-trimmed reset thresholds are available in approximately 100mV increments with a ±1.5% room-temperature variance.*

Selector Guide

PART	WATCHDOG	MANUAL $\overline{\text{RESET}}$	RESET OUTPUT		
			PUSH/PULL	BIDIRECTIONAL	OPEN-DRAIN
MAX6316L	✔	✔	Active low	—	—
MAX6316M	✔	✔	—	Active low	—
MAX6317H	✔	✔	Active high	—	—
MAX6318L/H	✔	—	Active high/low	—	—
MAX6318M/H	✔	—	Active high	Active low	—
MAX6319L/H	—	✔	Active high/low	—	—
MAX6319M/H	—	✔	Active high	Active low	—
MAX6320P	✔	✔	—	—	Active low
MAX6321H/P	✔	—	Active high	—	Active low
MAX6322H/P	—	✔	Active high	—	Active low

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

3-Pin, Ultra-Low-Power µP Reset Circuits

General Description

The MAX6326/MAX6327/MAX6328 microprocessor (µP) supervisory circuits are used to monitor the power supplies in µP and digital systems. These devices provide excellent circuit reliability and low cost by eliminating external components and adjustments when used with 3V-powered circuits.

These circuits perform a single function: they assert a reset signal whenever the V_{CC} supply voltage declines below a preset threshold, keeping it asserted for at least 100ms after V_{CC} has risen above the reset threshold. The only difference between the three devices is in their output. The MAX6326 (push/pull) and MAX6328 (open-drain) have an active-low $\overline{RESET}$ output. The MAX6327 has an active-high push-pull RESET. All three parts are guaranteed to be in the correct state for V_{CC} down to 1V. The reset comparator is designed to ignore fast transients on V_{CC}. Reset thresholds between 2.2V and 3.08V are available.

Ultra-low supply currents (1µA max) make the MAX6326/MAX6327/MAX6328 ideal for use in portable equipment. These devices come in 3-pin SOT23 packages.

Applications

Computers

Controllers

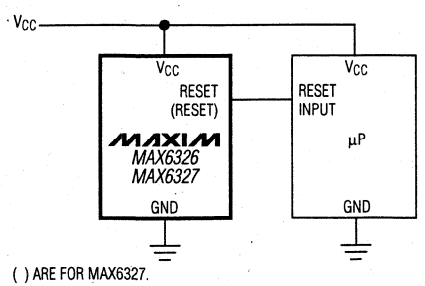
Intelligent Instruments

Critical µP and µC Power Monitoring

Portable/Battery-Powered Equipment

Automotive

Typical Operating Circuits



( ) ARE FOR MAX6327.

Typical Operating Circuits continued on next page.

Features

- **Ultra-Low, 1µA (max) Supply Current at V_{CC} = 3.3V**
- **Precision Monitoring of 2.5V, 3V, and 3.3V Power-Supply Voltages**
- **2.2V to 3.08V Reset Thresholds Available**
- **Fully Specified over Temperature**
- **100ms (min) Power-On-Reset Pulse Width**
- **Low Cost**
- **3 Reset Output Stages: Active-High Push/Pull**
  Active-Low Push/Pull
  Open-Drain
- **Guaranteed Reset Valid to V_{CC} = 1V**
- **Power-Supply Transient Immunity**
- **No External Components**
- **3-Pin SOT23 Package**
- **Pin Compatible with MAX809/MAX810**

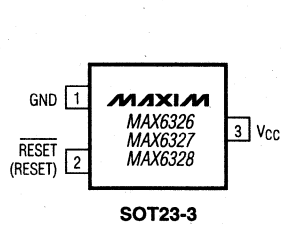
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6326UR31-T	-40°C to +85°C	3 SOT23-3	FDAA
MAX6326UR30-T	-40°C to +85°C	3 SOT23-3	FEAA
MAX6326UR29-T	-40°C to +85°C	3 SOT23-3	FCAA
MAX6326UR28-T	-40°C to +85°C	3 SOT23-3	FBAA

Ordering Information continued on next page.

**These devices are available in factory-set V_{CC} reset thresholds from 2.2V to 3.1V, in approximately 0.1V increments (Table 1). Contact the factory for availability and minimum order sizes.*

Pin Configuration



SOT23-3

( ) ARE FOR MAX6327.

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For small orders, phone 408-737-7600 ext. 3468.

3-Pin, Ultra-Low-Power µP Reset Circuits

Table 1. Factory-Trimmed Reset Thresholds†

SUFFIX	T_A = +25°C			T_A = -40°C to +85°C	
	MIN	TYP	MAX	MIN	MAX
MAX632_UR31	3.034	3.080	3.126	3.003	3.15
MAX632_UR30	2.955	3.000	3.045	2.925	3.075
MAX632_UR29	2.886	2.930	2.974	2.857	3.000
MAX632_UR28	2.758	2.800	2.842	2.730	2.870
MAX632_UR27	2.660	2.700	2.741	2.633	2.768
MAX632_UR26	2.591	2.630	2.669	2.564	2.696
MAX632_UR25	2.463	2.500	2.538	2.438	2.563
MAX632_UR24	2.364	2.400	2.436	2.340	2.460
MAX632_UR23	2.285	2.320	2.355	2.259	2.375
MAX632_UR22	2.162	2.200	2.228	2.140	2.250

†*Factory-trimmed reset thresholds are available in approximately 100mV increments with a ±1.5% room-temperature variance.*

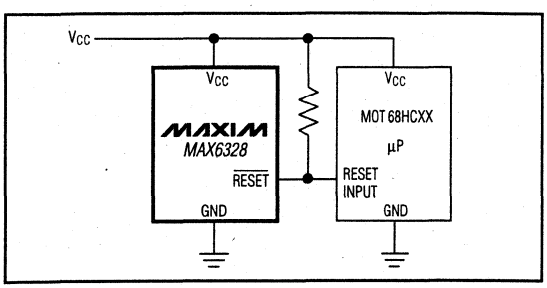
Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6326UR27-T	-40°C to +85°C	3 SOT23-3	FAAA
MAX6326UR26-T	-40°C to +85°C	3 SOT23-3	EZAA
MAX6326UR25-T	-40°C to +85°C	3 SOT23-3	EYAA
MAX6326UR24-T	-40°C to +85°C	3 SOT23-3	EXAA
MAX6326UR23-T	-40°C to +85°C	3 SOT23-3	EWAA
MAX6326UR22-T	-40°C to +85°C	3 SOT23-3	EHAA
MAX6327UR31-T	-40°C to +85°C	3 SOT23-3	FMAA
MAX6327UR30-T	-40°C to +85°C	3 SOT23-3	FNAA
MAX6327UR29-T	-40°C to +85°C	3 SOT23-3	FLAA
MAX6327UR28-T	-40°C to +85°C	3 SOT23-3	FKAA
MAX6327UR27-T	-40°C to +85°C	3 SOT23-3	FJAA
MAX6327UR26-T	-40°C to +85°C	3 SOT23-3	FIAA
MAX6327UR25-T	-40°C to +85°C	3 SOT23-3	FHAA

PART*	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6327UR24-T	-40°C to +85°C	3 SOT23-3	FGAA
MAX6327UR23-T	-40°C to +85°C	3 SOT23-3	FFAA
MAX6327UR22-T	-40°C to +85°C	3 SOT23-3	EIAA
MAX6328UR31-T	-40°C to +85°C	3 SOT23-3	FVAA
MAX6328UR30-T	-40°C to +85°C	3 SOT23-3	FWAA
MAX6328UR29-T	-40°C to +85°C	3 SOT23-3	FUAA
MAX6328UR28-T	-40°C to +85°C	3 SOT23-3	FTAA
MAX6328UR27-T	-40°C to +85°C	3 SOT23-3	FSAA
MAX6328UR26-T	-40°C to +85°C	3 SOT23-3	FRAA
MAX6328UR25-T	-40°C to +85°C	3 SOT23-3	FQAA
MAX6328UR24-T	-40°C to +85°C	3 SOT23-3	FPAA
MAX6328UR23-T	-40°C to +85°C	3 SOT23-3	FOAA
MAX6328UR22-T	-40°C to +85°C	3 SOT23-3	EJAA

**These devices are available in factory-set V_{CC} reset thresholds from 2.2V to 3.1V, in approximately 0.1V increments (Table 1). Contact the factory for availability and minimum order sizes.*

Typical Operating Circuits



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

µP Reset Circuits with Shunt Regulator in 3-Pin SOT23

General Description

The MAX6330L/S/T/MAX6331L/S/T combine a shunt regulator with a power-on reset output in a single SOT23-3 package. These devices come with supply-regulation options that include 5V, 3.3V, and 3V versions and either an active-low or active-high reset.

Reset is asserted when V_{CC} drops 7.5% below the regulation voltage, and it stays asserted for at least 100ms after V_{CC} has risen above the reset threshold. The output voltage has a ±2% tolerance over temperature and over a 100µA to 50mA current range. These two functions combined in a 3-pin SOT23-3 package make these parts space-saving and simple to use.

Features

- **+5V, +3.3V, and +3V Versions**
- **100µA to 50mA Wide Shunt Current Range**
- **±2% Tolerance on Output Voltage**
- **Low Cost**
- **Precision Power-Down Reset Threshold**
- **100ms (min) Timeout Period**
- **Immune to False Resets from Load-Current Transients**
- **3-Pin SOT23 Package**

Applications

Computers

Controllers

Intelligent Instruments

Critical Microprocessor and Microcontroller

Power Monitoring

Portable/Battery-Powered Equipment

Automotive

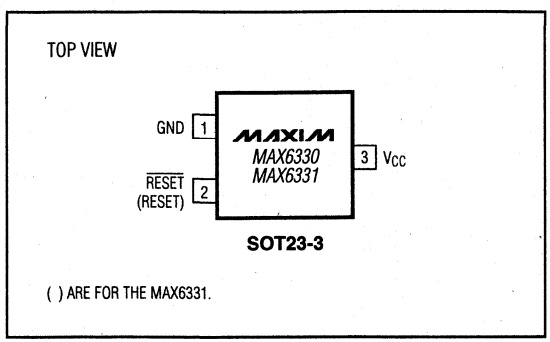
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE
MAX6330_UR-T	-40°C to +85°C	3 SOT23-3
MAX6331_UR-T	-40°C to +85°C	3 SOT23-3

**Insert the desired part-number suffix (from the table below) into the blank to complete the part number.*

SUFFIX	TYPICAL RESET THRESHOLD (V)	TYPICAL V_{CC} REGULATED VOLTAGE (V)	SOT TOP MARK	
			MAX6330	MAX6331
L	4.63	5.0	EKAA	ELAA
T	3.05	3.3	EMAA	ENAA
S	2.78	3.0	EOAA	EPAA

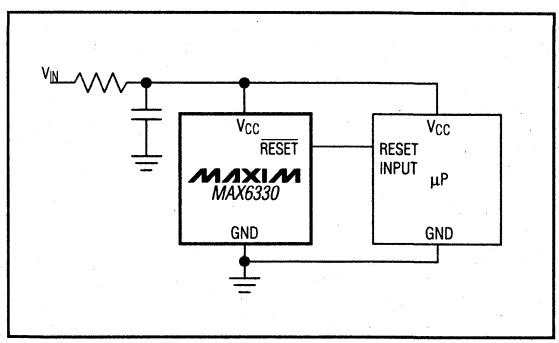
Pin Configuration



SOT23-3

( ) ARE FOR THE MAX6331.

Typical Operating Circuit



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ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Cost, +2.7V to +5.5V Micropower SOT Temperature Resets

General Description

The MAX6501–MAX6504 low-cost, fully integrated temperature resets assert a logic signal when their die temperature crosses a factory-programmed threshold. Operating from a +2.7V to +5.5V supply, these devices feature two on-chip, temperature-dependent voltage references and a comparator. They are available with factory-trimmed temperature trip thresholds from -45°C to +115°C in 10°C increments, and are accurate to ±0.5°C (typ) or ±4°C (max). These devices require no external components, and typically consume 30µA supply current. Hysteresis is pin-selectable at 2°C or 10°C.

The MAX6501/MAX6503 have an active-low, open-drain output intended to interface with a microprocessor (µP) reset input. The MAX6502/MAX6504 have an active-high, push/pull output intended to directly drive fan-control logic. The MAX6501/MAX6502 are offered with hot-temperature thresholds (+35°C to +115°C), asserting when the temperature is above the threshold. The MAX6503/MAX6504 are offered with cold-temperature thresholds (-45°C to +15°C), asserting when the temperature is below the threshold.

The MAX6501–MAX6504 are offered in eight standard-temperature versions; contact the factory for pricing and availability of non-standard temperature versions. They are available in 5-pin SOT23-5 and 7-pin TO-220** packages.

Applications

µP Temperature Monitoring in High-Speed Computers

Temperature Control

Temperature Alarms

Fan Control

Features

- ♦ **±0.5°C (typical) Threshold Accuracy Over Full Temperature Range**
- ♦ **No External Components Required**
- ♦ **Low Cost**
- ♦ **30µA Supply Current**
- ♦ **Factory-Programmed Thresholds from -45°C to +115°C in 10°C Increments**
- ♦ **Open-Drain Output (MAX6501/MAX6503) Push/Pull Output (MAX6502/MAX6504)**
- ♦ **Pin-Selectable +2°C or 10°C Hysteresis**
- ♦ **SOT23-5 Package**

Ordering Information

PART*	OPERATING TEMP. RANGE	PIN-PACKAGE
MAX6501UK____-T	-55°C to +125°C	5 SOT23-5
MAX6502UK____-T	-55°C to +125°C	5 SOT23-5
MAX6503UK____-T	-55°C to +125°C	5 SOT23-5
MAX6504UK____-T	-55°C to +125°C	5 SOT23-5

**These parts are offered in eight standard temperature versions with a minimum order of 2,500 pieces. To complete the suffix information, add P or N for positive or negative trip temperature, and select an available trip point in degrees centigrade. For example, the MAX6501UKP065-T describes a MAX6501 in a SOT23-5 package with a +65°C threshold. Contact the factory for pricing and availability of nonstandard temperature versions (minimum order 10,000 pieces).*

***Future package. Contact factory for availability.*

Selector Guide

PART NUMBER	OUTPUT STAGE	TRIP TEMPERATURE THRESHOLD	STANDARD TEMPERATURE THRESHOLDS (°C)							
			-15	5	45	55	65	75	85	95
MAX6501	Open-Drain	Hot			√	√	√	√	√	√
MAX6502	Push/Pull	Hot			√	√	√	√	√	√
MAX6503	Open-Drain	Cold	√	√						
MAX6504	Push/Pull	Cold	√	√						

†Patent Pending

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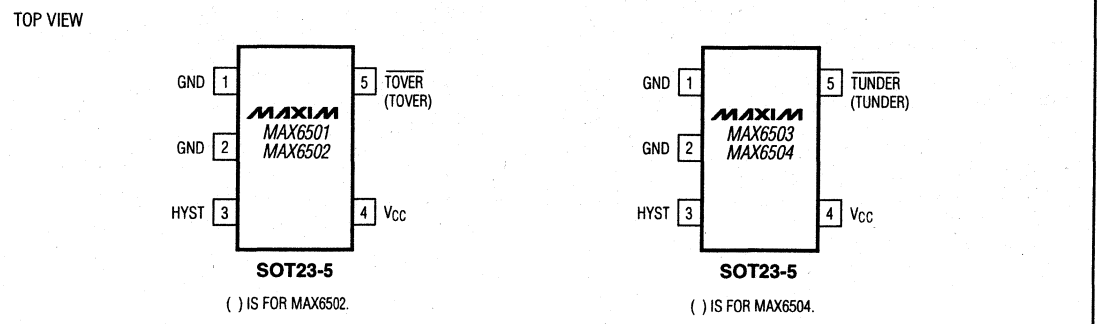
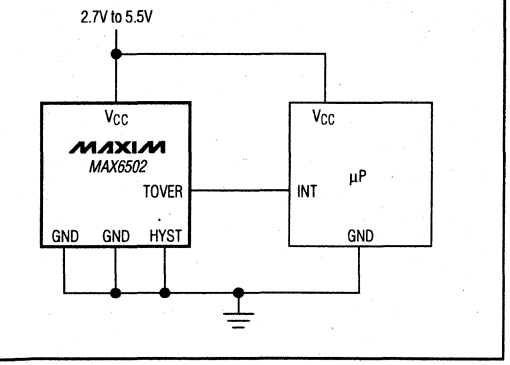
For small orders, phone 408-737-7600 ext. 3468.

Low-Cost, +2.7V to +5.5V Micropower SOT Temperature Resets

Pin Configurations



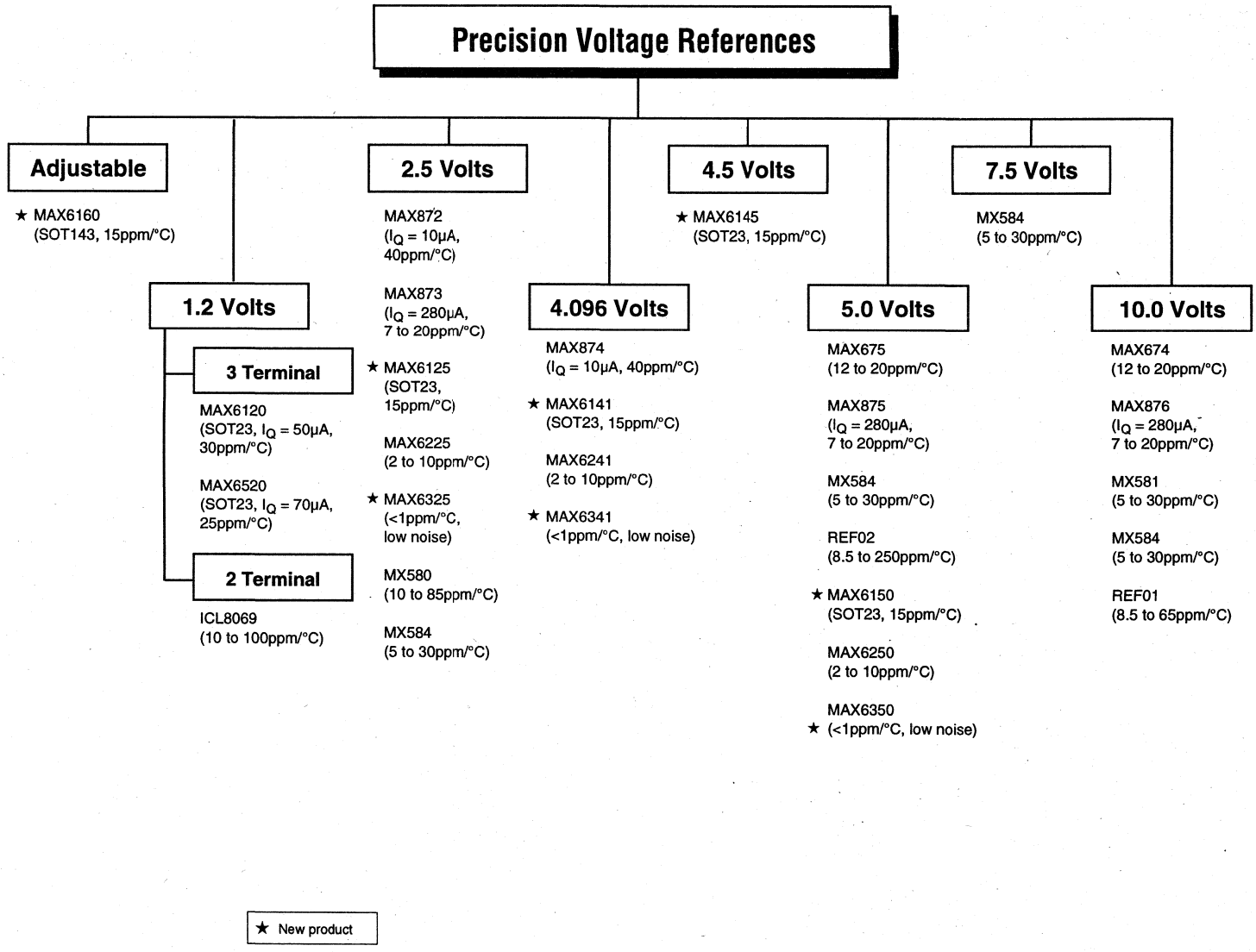
Typical Operating Circuit



Voltage References, Product Tables and Trees 6-2

MAX6125 2.5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23 6-5
MAX6141 4.096V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23 6-5
MAX6145 4.5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23 6-5
MAX6150 5V-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23 6-5
MAX6160 Adjustable-Output, Low-Cost, Low-Dropout, 3-Terminal Voltage Reference in SOT23 6-5
MAX6325 1ppm 1°C, Low-Noise, +2.5V Voltage Reference 6-13
MAX6341 1ppm 1°C, Low-Noise, +4.096V Voltage Reference 6-13
MAX6350 1ppm 1°C, Low-Noise, +5V Voltage Reference 6-13

Precision Voltage References



★ New product

Part Number	Voltage (V)	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (µVp-p), max(typ)	Package Options[1]	Temp. Ranges[2]	Features	Price† 1000-up ($)
MAX6160	Adj.	100 (15 typ)	1	100µA	(15)	SOT143, SO	E	Low-cost, low-dropout 3-terminal adjustable voltage reference	1.50
MAX6120	1.2	100 (30 typ)	1	70µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference	0.80
MAX6520	1.2	50 (25 typ)	1	70µA	(10)	SOT23, SO	E	Low-cost, micropower 3-terminal reference	1.25
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz to 10kHz)	TO-52, TO-92, SO*	C,E,M	Micropower 2-terminal reference	0.65
MAX872	2.5	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. V_{CC} = V_{OUT} + 200mV	2.12
MAX873	2.5	7 to 20	0.06 to 0.1	0.28	(16)	DIP, SO	C,E,M	Low power/drift, REF43 upgrade	2.25
MAX6125	2.5	50 (15 typ)	1	100µA	(15)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6225	2.5	2 to 5	0.04 to 0.1	2.7	(1.5)	DIP, SO, CERDIP	C,E,M	Low drift, less than 1.5µVp-p output noise	2.25
MAX6325	2.5	1 to 2.5	0.04	2.7	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 1.5µVp-p output noise	6.70
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52, SO**	C,M	Low-drift bandgap reference	2.03
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX874	4.096	40	0.2	10µA	(60)	DIP, SO	C,E	Lowest power, lowest dropout precision reference. V_{CC} = V_{OUT} + 200mV	2.12
MAX6141	4.096	50 (15 typ)	1	105µA	(25)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6241	4.096	2 to 5	0.02 to 0.1	2.9	(2.4)	DIP, SO, CERDIP	C,E,M	Low drift, less than 2.4µVp-p output noise	2.25
MAX6341	4.096	1 to 2.5	0.02	2.9	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 2.4µVp-p output noise	6.70
MAX6145	4.5	50	1	105µA	(30)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX675	5.0	12 to 20	0.15	1.4	15	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX875	5.0	7 to 20	0.06 to 0.1	0.28	(32)	DIP, SO	C,E,M	Low power/drift, REF02 upgrade	2.10
MAX6150	5.0	50 (15 typ)	1	110µA	(35)	SOT23, SO	E	Low-cost, low-dropout 3-terminal reference	1.25
MAX6250	5.0	2 to 5	0.02 to 0.1	3	(3)	DIP, SO, CERDIP	C,E,M	Low drift, less than 3.0µVp-p output noise	2.25
MAX6350	5.0	1 to 2.5	0.02	3	(1.5)	DIP, SO, CERDIP	C,E,M	Ultra-low drift, 3.0µVp-p output noise	6.70
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	1.28
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
MAX674	10.0	12 to 20	0.15	1.4	30	TO-99, DIP, SO, CERDIP	C,E,M	Low-drift, low-noise bandgap reference	3.08
MAX876	10.0	7 to 20	0.06 to 0.1	0.28	(64)	DIP, SO	C,E,M	Low power/drift, REF01 upgrade	2.10
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39, SO***	C,M	Low-drift bandgap reference	2.30
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C,M	Low-drift programmable reference	3.09
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	TO-99, DIP, SO, CERDIP	C,M	Low-drift bandgap reference	1.28

* The ICL8069 is available in 2-pin TO-52, 2-pin TO-92, and 8-pin SO packages.
** The MX580 is available in 3-pin TO-52 and 8-pin SO packages.
*** The MX581 is available in 3-pin TO-39 and 8-pin SO packages.
1 Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leadless Chip Carrier (quad pack), FP = Flat Pack
2 Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Lowest grade pricing.

19-1177; Rev. 0; 12/96

MAXIM

SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

General Description

The MAX6125/MAX6141/MAX6145/MAX6150/MAX6160 low-dropout, micropower, three-terminal voltage references offer 2.5V, 4.096V, 4.5V, 5.0V, and adjustable (1.23V to 12.4V) output voltages, respectively. Low, 200mV dropout makes these devices ideal for 3V and 5V systems. Unlike two-terminal references that waste battery current and require an external resistor, the MAX61xx family's supply current is virtually independent of input voltage variations, which translates to longer battery life.

Initial accuracy for these devices is ±1%. The output temperature coefficient is typically 15ppm/°C, and guaranteed to be less than 50ppm/°C (except for the MAX6160). The MAX6125/MAX6141/MAX6145/MAX6150 are available in 3-pin SOT23 and 8-pin SO packages. The MAX6160 is available in 4-pin SOT143 and 8-pin SO packages.

Selector Guide

PART	PRESET OUTPUT VOLTAGE (V)	PACKAGE
MAX6125	2.5	3 SOT23/8 SO
MAX6141	4.096	3 SOT23/8 SO
MAX6145	4.5	3 SOT23/8 SO
MAX6150	5	3 SOT23/8 SO
MAX6160	Adjustable (1.23 to 12.40)	4 SOT143/8 SO

Typical Operating Circuit appears on last page.

Features

- **3-Pin SOT23 Package (MAX6125/41/45/50) 4-Pin SOT143 Package (MAX6160)**
- **Low, 200mV Dropout Voltage**
- **75µA Supply Current, Independent of Input Voltage**
- **15ppm/°C Typical Tempco (50ppm/°C max)**
- **Stable for All Capacitive Loads up to 10nF**
- **Adjustable Output Voltage from 1.23V to (V_{IN} - 0.2V) (MAX6160)**
- **Optimized for 3V/5V Operation**

Applications

3V/5V Systems
Battery-Powered Systems
Portable and Hand-Held Equipment
Data-Acquisition Systems
Instrumentation and Process Control

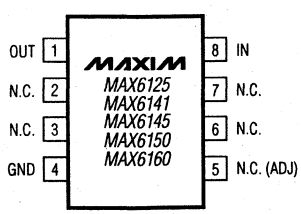
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6125ESA	-40°C to +85°C	8 SO	—
MAX6125EUR	-40°C to +85°C	3 SOT23-3	EBAA
MAX6141ESA	-40°C to +85°C	8 SO	—
MAX6141EUR	-40°C to +85°C	3 SOT23-3	ECAA

Ordering Information continued on last page.

Pin Configurations

TOP VIEW



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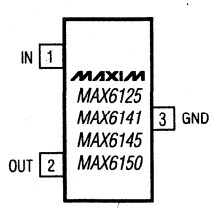
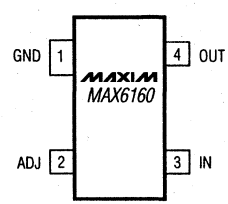


SOT23-3



SOT143

( ) ARE FOR MAX6160 ONLY

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SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
IN .....-0.3V to +13.5V
OUT, ADJ .....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration (to IN or GND).....Continuous
Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
3-Pin SOT23 (derate 4mW/°C above +70°C).....320mW
4-Pin SOT143 (derate 4mW/°C above +70°C).....320mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX6125

(V_{IN} = 2.7V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}	$T_A = T_{MIN}$ to T_{MAX}	2.7		12.6	V
Output Voltage	V_{OUT}	T_A = +25°C	2.475	2.500	2.525	V
		$T_A = T_{MIN}$ to T_{MAX}	2.450		2.550	
Output Voltage Temperature Coefficient	TCV_{OUT}	$T_A = T_{MIN}$ to T_{MAX}		15	50	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz		15		µVp-p
		10Hz to 10kHz		500		
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 2.7V to 12.6V, $T_A = T_{MIN}$ to T_{MAX}		1	50	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{SOURCE} = 0mA to 1mA		0.4	1	mV/mA
		I_{SINK} = 0mA to 1mA		1.15	10	
Quiescent Supply Current	I_Q	T_A = +25°C		75	100	µA
		$T_A = T_{MIN}$ to T_{MAX}			130	
Change in Supply Current vs. Change in Input Voltage	$\Delta I_Q/\Delta V_{IN}$	V_{IN} = 2.7V to 12.6V		1.7	6	µA/V

ELECTRICAL CHARACTERISTICS—MAX6141

(V_{IN} = 4.3V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}	$T_A = T_{MIN}$ to T_{MAX}	4.3		12.6	V
Output Voltage	V_{OUT}	T_A = +25°C	4.055	4.096	4.140	V
		$T_A = T_{MIN}$ to T_{MAX}	4.015		4.180	
Output Voltage Temperature Coefficient	TCV_{OUT}	$T_A = T_{MIN}$ to T_{MAX}		15	50	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz		25		µVp-p
		10Hz to 10kHz		700		
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.3V to 12.6V, $T_A = T_{MIN}$ to T_{MAX}		2	50	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{SOURCE} = 0mA to 1mA		0.55	1.6	mV/mA
		I_{SINK} = 0mA to 1mA		1.65	16	
Quiescent Supply Current	I_Q	T_A = +25°C		78	105	µA
		$T_A = T_{MIN}$ to T_{MAX}			130	
Change in Supply Current vs. Change in Input Voltage	$\Delta I_Q/\Delta V_{IN}$	V_{IN} = 4.3V to 12.6V		1.7	6	µA/V

ELECTRICAL CHARACTERISTICS—MAX6145

(V_{IN} = 4.7V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}	T_A = T_{MIN} to T_{MAX}	4.7		12.6	V
Output Voltage	V_{OUT}	T_A = +25°C	4.455	4.500	4.545	V
		T_A = T_{MIN} to T_{MAX}	4.410		4.590	
Output Voltage Temperature Coefficient	TCV_{OUT}	T_A = T_{MIN} to T_{MAX}		15	50	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz		30		µVp-p
		10Hz to 10kHz		800		
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.7V to 12.6V, T_A = T_{MIN} to T_{MAX}		2	50	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{SOURCE} = 0mA to 1mA		0.6	1.8	mV/mA
		I_{SINK} = 0mA to 1mA		1.75	18	
Quiescent Supply Current	I_Q	T_A = +25°C		79	105	µA
		T_A = T_{MIN} to T_{MAX}			130	
Change in Supply Current vs. Change in Input Voltage	$\Delta I_Q/\Delta V_{IN}$	V_{IN} = 4.7V to 12.6V		1.7	6	µA/V

ELECTRICAL CHARACTERISTICS—MAX6150

(V_{IN} = 5.2V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}	T_A = T_{MIN} to T_{MAX}	5.2		12.6	V
Output Voltage	V_{OUT}	T_A = +25°C	4.950	5.000	5.050	V
		T_A = T_{MIN} to T_{MAX}	4.900		5.100	
Output Voltage Temperature Coefficient	TCV_{OUT}	T_A = T_{MIN} to T_{MAX}		15	50	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz		35		µVp-p
		10Hz to 10kHz		900		
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 5.2V to 12.6V, T_A = T_{MIN} to T_{MAX}		1	50	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{SOURCE} = 0mA to 1mA		0.65	2	mV/mA
		I_{SINK} = 0mA to 1mA		1.9	20	
Quiescent Supply Current	I_Q	T_A = +25°C		80	110	µA
		T_A = T_{MIN} to T_{MAX}			145	
Change in Supply Current vs. Change in Input Voltage	$\Delta I_Q/\Delta V_{IN}$	V_{IN} = 5.2V to 12.6V		1.7	6	µA/V

SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

ELECTRICAL CHARACTERISTICS—MAX6160

(V_{IN} = 2.7V; I_{OUT} = 0mA; R1 = 215kΩ ±0.1%, R2 = 208kΩ ±0.1% (circuit of Figure 1); T_A = +25°C; unless otherwise noted.) (Notes 1, 2)

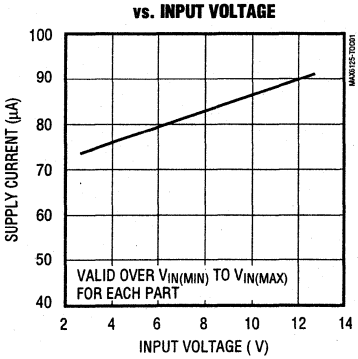
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{IN}	T_A = T_{MIN} to T_{MAX}	2.7		12.6	V
Output Voltage Range		T_A = T_{MIN} to T_{MAX}	1.23		V_{IN} - 0.2	V
Output Voltage	V_{OUT}	T_A = +25°C	2.475	2.500	2.525	V
		T_A = T_{MIN} to T_{MAX}	2.450		2.550	
ADJ Feedback Voltage Threshold	V_{ADJ}			1.23		V
ADJ Input Current	I_{ADJ}	V_{ADJ} = 1.23V		70		nA
Output Voltage Temperature Coefficient	TCV_{OUT}	T_A = T_{MIN} to T_{MAX}		15	100	ppm/°C
Output Voltage Noise	e_n	0.1Hz to 10Hz		15		µVp-p
		10Hz to 10kHz		500		
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 2.7V to 12.6V, T_A = T_{MIN} to T_{MAX}		1	50	µV/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{SOURCE} = 0mA to 1mA		0.35	1	mV/mA
		I_{SINK} = 0mA to 1mA		1.15	10	
Quiescent Supply Current	I_Q	T_A = +25°C		75	100	µA
		T_A = T_{MIN} to T_{MAX}			130	
Change in Supply Current vs. Change in Input Voltage	$\Delta I_Q/\Delta V_{IN}$	V_{IN} = 2.7V to 12.6V		1.7	6	µA/V

Note 1: All devices are 100% production tested at T_A = +25°C, and are guaranteed by design for T_A = T_{MIN} to T_{MAX} as specified.
Note 2: R1 and R2 program the output voltage in the 1.23V to (V_{IN} - 0.2V) range (see the section *Setting the MAX6160 Output Voltage*).

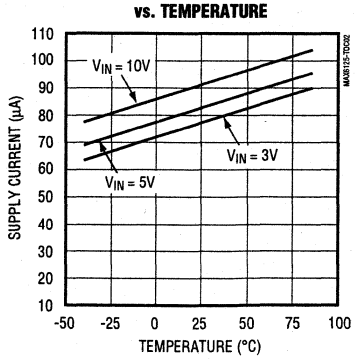
Typical Operating Characteristics

(V_{IN} = $V_{IN(MIN)}$, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

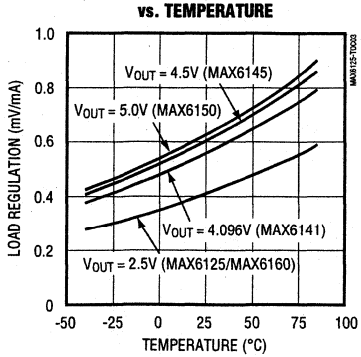
SUPPLY CURRENT vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



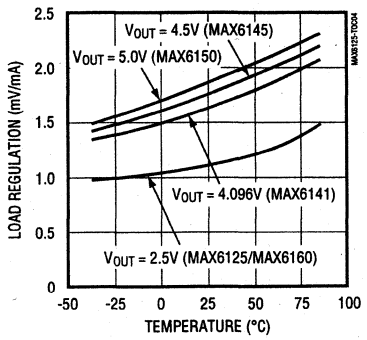
LOAD REGULATION (SOURCING) vs. TEMPERATURE



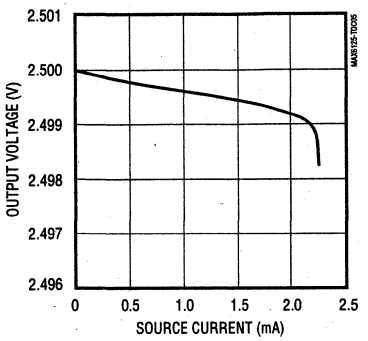
Typical Operating Characteristics (continued)

(V_{IN} = $V_{IN(MIN)}$, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

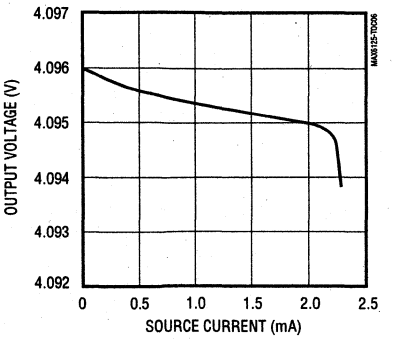
LOAD REGULATION (SINKING) vs. TEMPERATURE



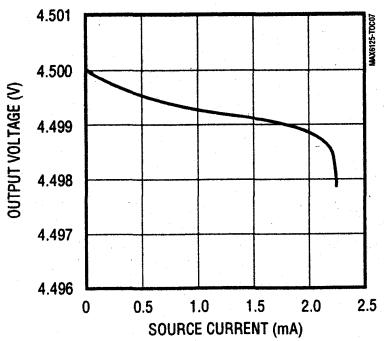
MAX6125/MAX6160 OUTPUT VOLTAGE vs. SOURCE CURRENT



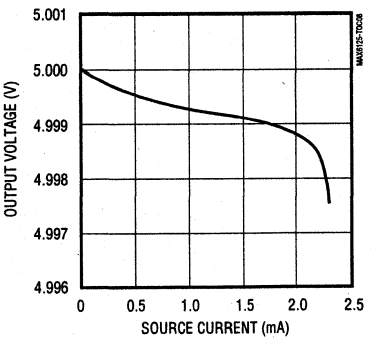
MAX6141 OUTPUT VOLTAGE vs. SOURCE CURRENT



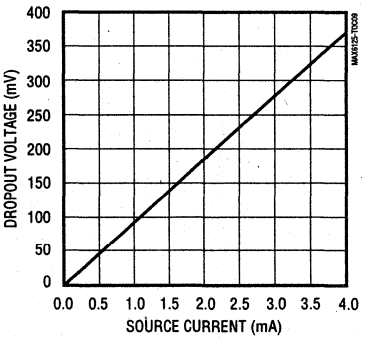
MAX6145 OUTPUT VOLTAGE vs. SOURCE CURRENT



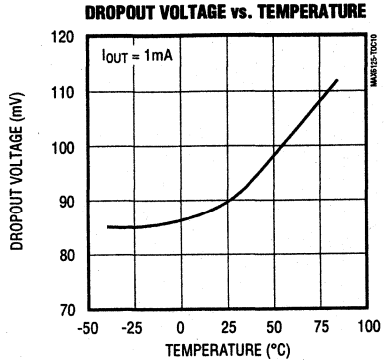
MAX6150 OUTPUT VOLTAGE vs. SOURCE CURRENT



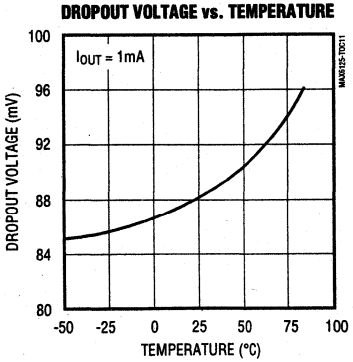
DROPOUT VOLTAGE vs. SOURCE CURRENT



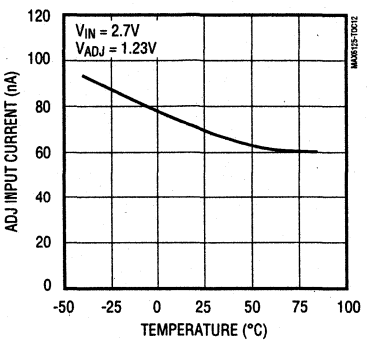
MAX6125/MAX6160 DROPOUT VOLTAGE vs. TEMPERATURE



MAX6141/MAX6145/MAX6150 DROPOUT VOLTAGE vs. TEMPERATURE



MAX6160 ADJ INPUT CURRENT vs. TEMPERATURE

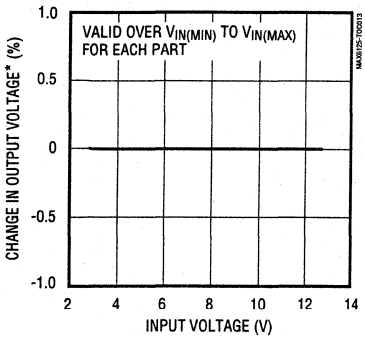


SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

Typical Operating Characteristics (continued)

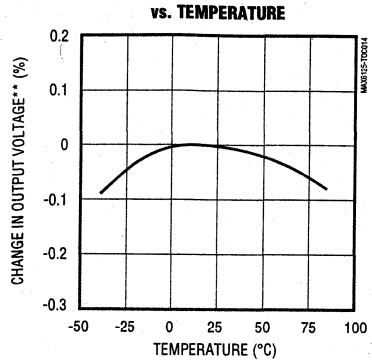
(V_{IN} = $V_{IN(MIN)}$, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE



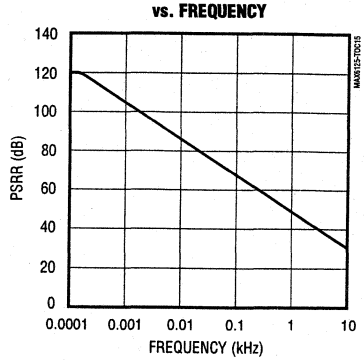
*With respect to output voltage at V_{IN} = $V_{IN(MIN)}$.

CHANGE IN OUTPUT VOLTAGE vs. TEMPERATURE

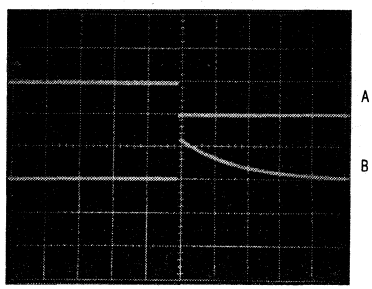


**With respect to output voltage at T_A = +25°C.

POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



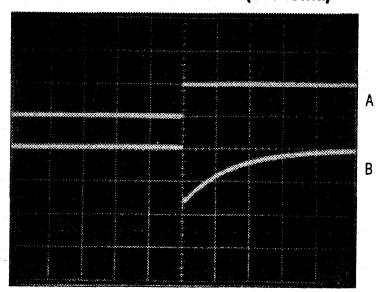
MAX6125 LOAD-TRANSIENT RESPONSE (SINKING)



10µs/div

A = OUTPUT CURRENT, 1mA/div, I_{OUT} = 0mA to -1mA
B = OUTPUT VOLTAGE, 200mV/div

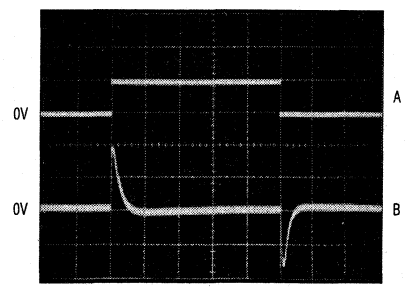
MAX6125 LOAD-TRANSIENT RESPONSE (SOURCING)



10µs/div

A = OUTPUT CURRENT, 1mA/div, I_{OUT} = 0mA to 1mA
B = OUTPUT VOLTAGE, 50mV/div

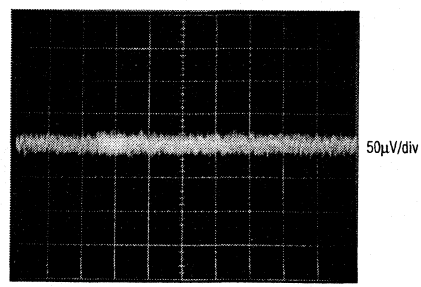
MAX6125 LINE-TRANSIENT RESPONSE



5µs/div

A = INPUT VOLTAGE, 100mV/div, V_{IN} = 3V ±50mV
B = OUTPUT VOLTAGE, 20mV/div

MAX6125 0.1Hz TO 100Hz NOISE



1sec/div

SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

Pin Description

PIN			NAME	FUNCTION
SO	SOT23-3	SOT143		
1	2	4	OUT	Reference Output
2, 3, 5*, 6, 7	—	—	N.C.	No Connection. Not internally connected.
4	3	1	GND	Ground
5**	—	2	ADJ	Adjustable output voltage feedback input. Connect a resistor divider between OUT, ADJ, and GND (Figure 1).
8	1	3	IN	Input Voltage

*Except MAX6160.
**MAX6160 only.

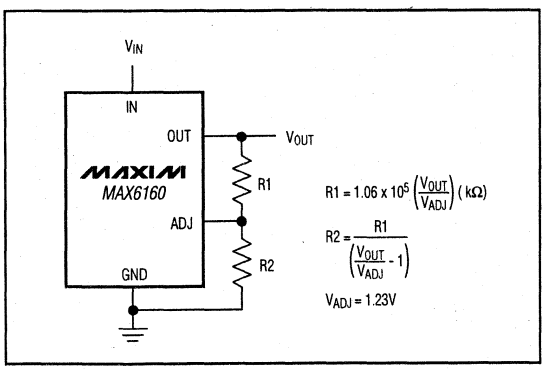


Figure 1. MAX6160 Adjustable Output Circuit

Applications Information

Setting the MAX6160 Output Voltage

Set the output voltage on the MAX6160 by connecting a resistor divider between OUT, ADJ, and GND (Figure 1). Choose R1 according to the following equation:

$$R1 = (1.06 \times 10^5)(V_{OUT} / V_{ADJ})(k\Omega)$$

where V_{TH} = 1.23V. The scaling factor (1.06×10^5) compensates for the MAX6160's change in ADJ input current over temperature. When R1 is chosen correctly, the change in voltage across R1 caused by the ADJ input current is properly cancelled. Choose R1 to within ±5% of this calculated value (nearest standard value plus specified resistor tolerance) to optimize the output voltage temperature coefficient. Using R1 = 215kΩ:

$$R2 = 215k\Omega \left(\frac{2.5V}{1.23V} - 1 \right) \approx 208k\Omega,$$

which is also the nearest 0.1% resistor value.

Choose R2 according to the following equation:

$$R2 = R1 / (V_{OUT} / V_{ADJ} - 1)$$

For example, a 2.5V output requires R1 = (1.06×10^5) (2.5V / 1.23V) ≈ 215Ω, which is the nearest standard-value 0.1% resistor.

Input Bypassing

For the best line-transient performance, decouple the input with a 0.1µF ceramic capacitor, as shown in the *Typical Operating Circuit*. Locate the capacitor as close to the device pin as possible. Where transient performance is less important, no capacitor is necessary.

Output Bypassing

The MAX6125/MAX6141/MAX6145/MAX6150/MAX6160 do not require an output capacitor. They are stable for capacitive loads from 0nF to 10nF. If your application requires an output charge reservoir (e.g., to decouple the reference from a DAC's input), then make sure that the total output capacitive load does not exceed 10nF for optimum settling-time performance.

SOT23, Low-Cost, Low-Dropout, 3-Terminal Voltage References

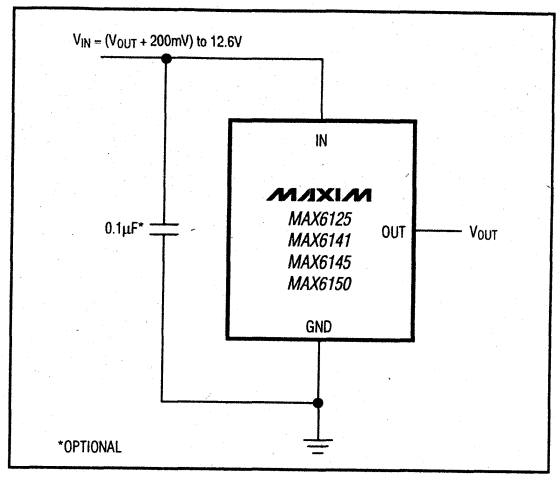
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX6145ESA	-40°C to +85°C	8 SO	—
MAX6145EUR	-40°C to +85°C	3 SOT23-3	EDAA
MAX6150ESA	-40°C to +85°C	8 SO	—
MAX6150EUR	-40°C to +85°C	3 SOT23-3	EEAA
MAX6160ESA	-40°C to +85°C	8 SO	—
MAX6160EUS	-40°C to +85°C	4 SOT143	JXAA

Chip Information

TRANSISTOR COUNT: 42

Typical Operating Circuit



19-1203; Rev 0; 4/97

MAXIM

1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

General Description

The MAX6325/MAX6341/MAX6350 are low-noise, precision voltage references with extremely low, 0.5ppm/°C typical temperature coefficients and excellent, ±0.02% initial accuracy. These devices feature buried-zener technology for lowest noise performance. Load-regulation specifications are guaranteed for source and sink currents up to 15mA. Excellent line and load regulation and low output impedance at high frequencies make them ideal for high-resolution data-conversion systems up to 16 bits.

The MAX6325 is set for a 2.500V output, the MAX6341 is set for a 4.096V output, and the MAX6350 is set for a 5.000V output. All three provide for the option of external trimming and noise reduction.

Features

- ♦ **Ultra-Low, 1ppm/°C Max Tempco**
- ♦ **Very Low, 1.5µVp-p Noise (0.1Hz to 10Hz) (MAX6325)**
- ♦ **±0.02% Initial Accuracy (MAX6350)**
- ♦ **±15mA Output Source and Sink Current**
- ♦ **Low, 18mW Power Consumption (MAX6325)**
- ♦ **Industry-Standard Pinout**
- ♦ **Optional Noise Reduction and Voltage Trim**
- ♦ **Excellent Transient Response**
- ♦ **8-Pin SO Package Available**
- ♦ **Low, 30ppm/1000h Long-Term Stability**
- ♦ **Stable for All Capacitive Loads**

Applications

High-Resolution Analog-to-Digital and Digital-to-Analog Converters

High-Accuracy Reference Standard

High-Accuracy Industrial and Process Control

Digital Voltmeters

ATE Equipment

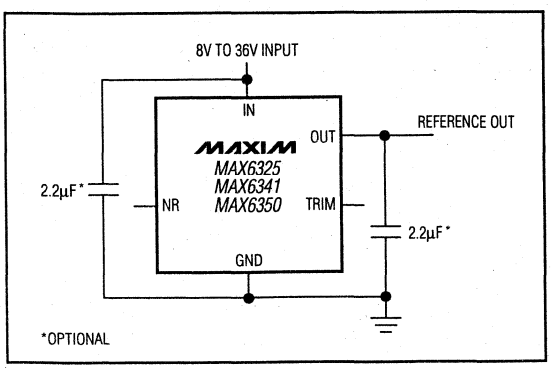
Precision Current Sources

Ordering Information

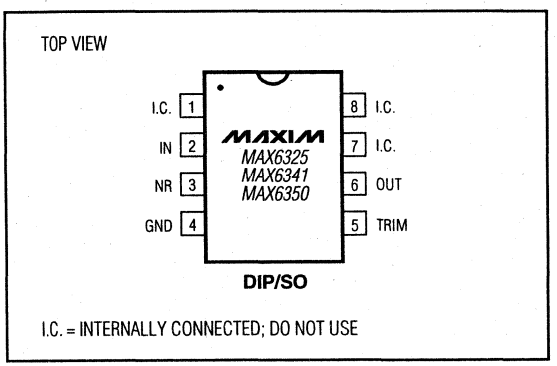
PART	TEMP. RANGE	PIN-PACKAGE	MAX TEMPCO (ppm/°C)
MAX6325CPA	0°C to +70°C	8 Plastic DIP	1.0
MAX6325CSA	0°C to +70°C	8 SO	1.0
MAX6325EPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX6325ESA	-40°C to +85°C	8 SO	1.5
MAX6325MJA	-55°C to +125°C	8 CERDIP	2.5

Ordering Information continued at end of data sheet.

Typical Operating Circuit



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

ABSOLUTE MAXIMUM RATINGS

(Voltages Referenced to GND)
IN ..... -0.3V to 40V
OUT, TRIM ..... -0.3V to 12V
NR ..... -0.3V to 6V
OUT Short Circuit to GND Duration ($V_{IN} \le 12V$) ..... Continuous
OUT Short Circuit to GND Duration ($V_{IN} \le 40V$) 5sec
OUT Short Circuit to IN Duration ($V_{IN} \le 12V$) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
MAX63_ _ C_ A ..... 0°C to +70°C
MAX63_ _ E_ A ..... -40°C to +85°C
MAX63_ _ MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX6325

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		C, E, M	8		36	V
Output Voltage	V_{OUT}	MAX6325	+25°C	2.499	2.500	2.501	V
Output Voltage Temperature Coefficient (Note 1)	TCV_{OUT}	MAX6325C_A	C		0.5	1.0	ppm/°C
		MAX6325E_A	E		0.75	1.5	
		MAX6325MJA	M		1.0	2.5	
Line Regulation (Note 2)	$\Delta V_{OUT} / \Delta V_{IN}$	8V ≤ V_{IN} ≤ 10V	+25°C		10	18	ppm/V
			C			30	
			E			35	
			M			45	
		10V ≤ V_{IN} ≤ 36V	+25°C		2	5	
			C			7	
			E			8	
			M			10	
Load Regulation (Note 2)	$\Delta V_{OUT} / \Delta I_{OUT}$	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA	C		1	6	ppm/mA
			E		1	7	
			M		3	15	
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA	C		1	6	
			E		1	7	
			M		10	30	
Supply Current	I_{IN}		+25°C		1.8	2.7	mA
			C, E, M			3.0	
Trim-Adjustment Range	ΔV_{OUT}	Figure 1	C, E, M	±15	±25		mV
Turn-On Settling Time	t_{ON}	To ±0.01% of final value	+25°C		5		µs
Output Noise Voltage (Note 3)	e_n	0.1Hz ≤ f ≤ 10Hz	+25°C		1.5		µVp-p
		10Hz ≤ f ≤ 1kHz	+25°C		1.3	2.8	μV_{RMS}
Temperature Hysteresis		(Note 4)	+25°C		20		ppm
Long-Term Stability	$\Delta V_{OUT} / t$		+25°C		30		ppm/1000h

ELECTRICAL CHARACTERISTICS—MAX6341

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		C, E, M	8		36	V
Output Voltage	V_{OUT}	MAX6341	+25°C	4.095	4.096	4.097	V
Output Voltage Temperature Coefficient (Note 1)	TCV_{OUT}	MAX6341C_A	C		0.5	1.0	ppm/°C
		MAX6341E_A	E		0.75	1.5	
		MAX6341MJA	M		1.0	2.5	
Line Regulation (Note 2)	ΔV_{OUT} / ΔV_{IN}	8V ≤ V_{IN} ≤ 10V	+25°C		10	18	ppm/V
			C			30	
			E			35	
			M			45	
		10V ≤ V_{IN} ≤ 36V	+25°C		2	5	
			C			7	
			E			8	
			M			10	
Load Regulation (Note 2)	ΔV_{OUT} / ΔI_{OUT}	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA	C		1	6	ppm/mA
			E		1	7	
			M		3	9	
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA	C		1	6	
			E		1	7	
			M		7	18	
Supply Current	I_{IN}		+25°C		1.9	2.9	mA
			C, E, M			3.2	
Trim-Adjustment Range	ΔV_{OUT}	Figure 1	C, E, M	±24	±40		mV
Turn-On Settling Time	t_{ON}	To ±0.01% of final value	+25°C		8		µs
Output Noise Voltage (Note 3)	e_n	0.1Hz ≤ f ≤ 10Hz	+25°C		2.4		µVp-p
		10Hz ≤ f ≤ 1kHz	+25°C		2.0	4.0	μV_{RMS}
Temperature Hysteresis		(Note 4)	+25°C		20		ppm
Long-Term Stability	ΔV_{OUT} / t		+25°C		30		ppm/ 1000h

1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

ELECTRICAL CHARACTERISTICS—MAX6350

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	T_A	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		C, E, M	8		36	V
Output Voltage	V_{OUT}	MAX6350	+25°C	4.999	5.000	5.001	V
Output Voltage Temperature Coefficient (Note 1)	TCV_{OUT}	MAX6350C_A	C		0.5	1.0	ppm/°C
		MAX6350E_A	E		0.75	1.5	
		MAX6350MJA	M		1.0	2.5	
Line Regulation (Note 2)	ΔV_{OUT} / ΔV_{IN}	8V ≤ V_{IN} ≤ 10V	+25°C		10	18	ppm/V
			C			30	
			E			35	
			M			45	
		10V ≤ V_{IN} ≤ 36V	+25°C		2	5	
			C			7	
			E			8	
			M			10	
Load Regulation (Note 2)	ΔV_{OUT} / ΔI_{OUT}	Sourcing: 0mA ≤ I_{OUT} ≤ 15mA	C		1	6	ppm/mA
			E		1	7	
			M		2	9	
		Sinking: -15mA ≤ I_{OUT} ≤ 0mA	C		1	6	
			E		1	7	
			M		6	15	
Supply Current	I_{IN}		+25°C		2.0	3.0	mA
			C, E, M			3.3	
Trim-Adjustment Range	ΔV_{OUT}	Figure 1	C, E, M	±30	±50		mV
Turn-On Settling Time	t_{on}	To ±0.01% of final value	+25°C		10		µs
Output Noise Voltage (Note 3)	e_n	0.1Hz ≤ f ≤ 10Hz	+25°C		3.0		µVp-p
		10Hz ≤ f ≤ 1kHz	+25°C		2.5	5.0	μV_{RMS}
Temperature Hysteresis		(Note 4)	+25°C		20		ppm
Long-Term Stability	ΔV_{OUT} / t		+25°C		30		ppm/ 1000h

Note 1: Temperature coefficient is measured by the box method; i.e., the maximum ΔV_{OUT} is divided by $\Delta T \times V_{OUT}$.

Note 2: Line regulation (ΔV_{OUT} / ($V_{OUT} \times \Delta V_{IN}$)) and load regulation ($\Delta V_{OUT}$ / ($V_{OUT} \times \Delta I_{OUT}$)) are measured with pulses and do not include output voltage changes due to die-temperature changes.

Note 3: Noise specifications are 100% tested for the 10Hz to 1kHz bandwidth. Production testing in the 0.1Hz to 10Hz bandwidth is available upon request.

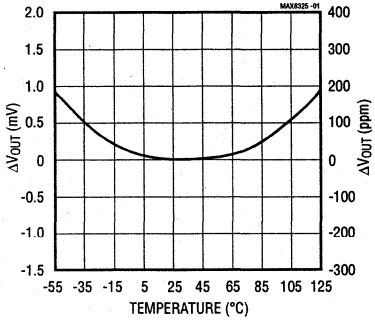
Note 4: Temperature hysteresis is specified at T_A = +25°C by measuring V_{OUT} before and after changing temperature by +25°C using the plastic DIP package.

1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

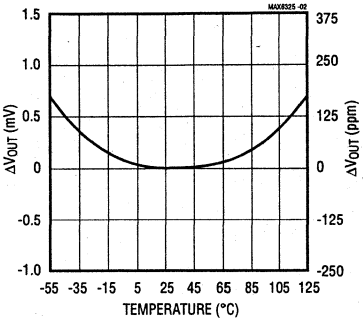
Typical Operating Characteristics

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

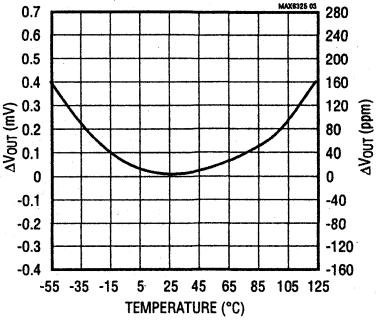
MAX6350
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



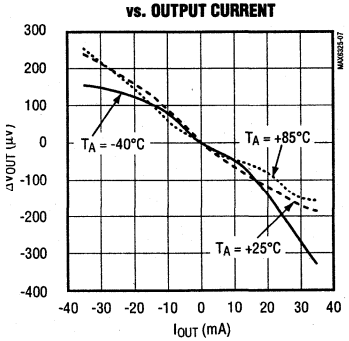
MAX6341
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



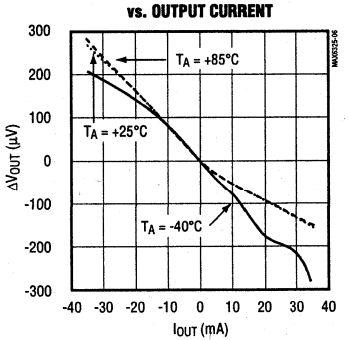
MAX6325
NORMALIZED OUTPUT VOLTAGE vs. TEMPERATURE



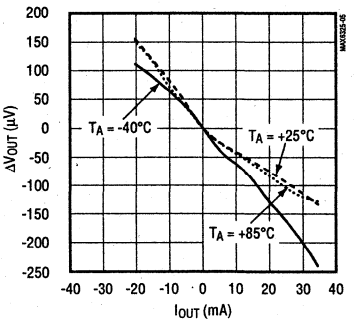
MAX6350
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



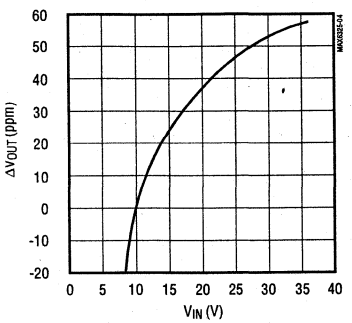
MAX6341
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



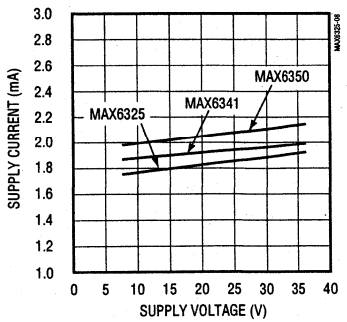
MAX6325
CHANGE IN OUTPUT VOLTAGE vs. OUTPUT CURRENT



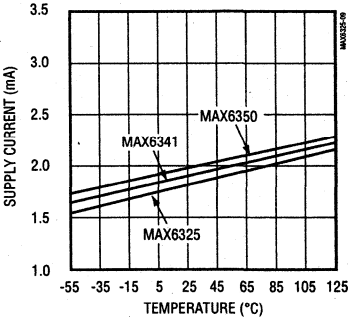
CHANGE IN OUTPUT VOLTAGE vs. INPUT VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE

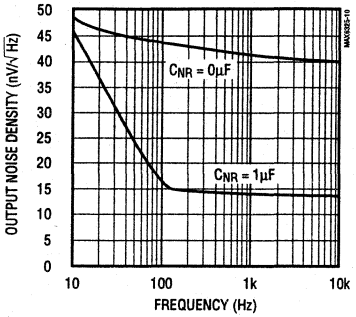


1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

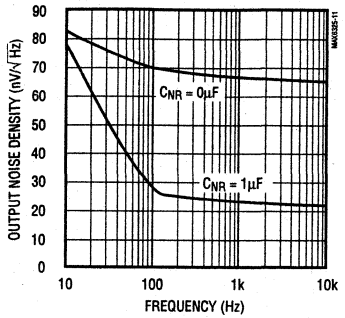
Typical Operating Characteristics (continued)

(V_{IN} = 10V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

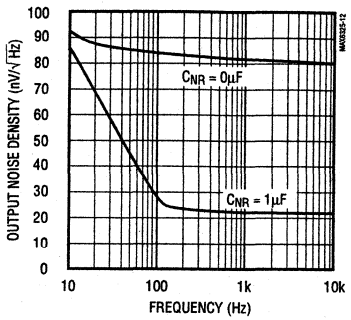
MAX6325 OUTPUT NOISE-VOLTAGE DENSITY vs. FREQUENCY



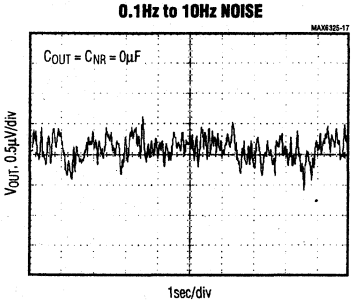
MAX6341 OUTPUT NOISE-VOLTAGE DENSITY vs. FREQUENCY



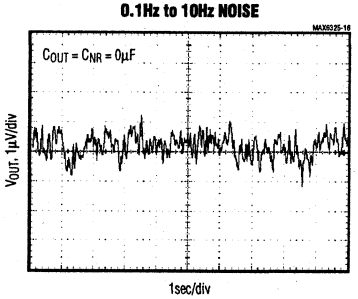
MAX6350 OUTPUT NOISE-VOLTAGE DENSITY vs. FREQUENCY



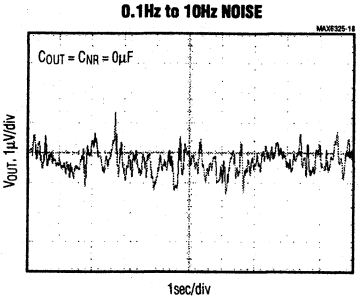
MAX6325 0.1Hz to 10Hz NOISE



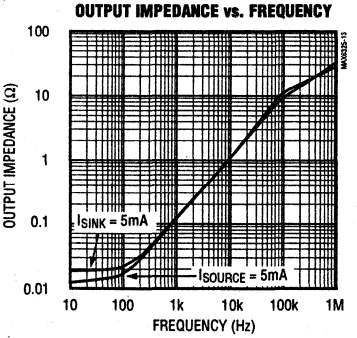
MAX6341 0.1Hz to 10Hz NOISE



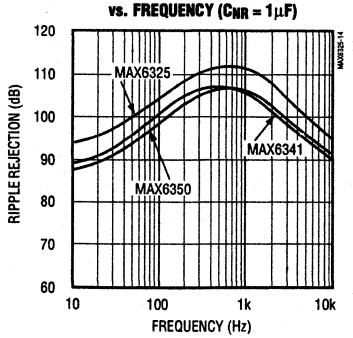
MAX6350 0.1Hz to 10Hz NOISE



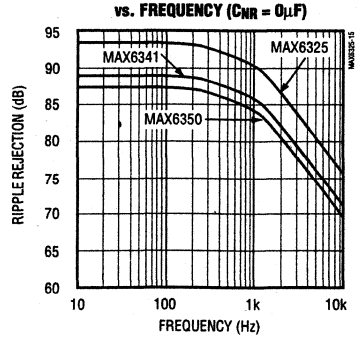
OUTPUT IMPEDANCE vs. FREQUENCY



RIPPLE REJECTION vs. FREQUENCY (C_{NR} = 1µF)



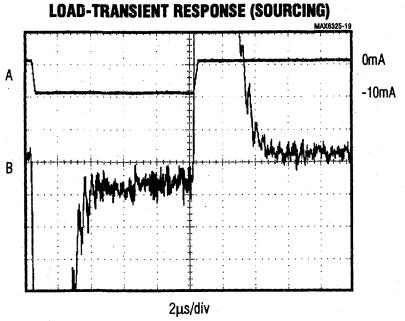
RIPPLE REJECTION vs. FREQUENCY (C_{NR} = 0µF)



Typical Operating Characteristics (continued)

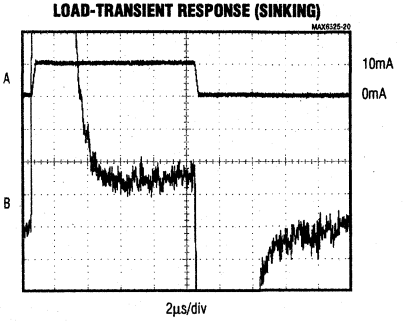
(V_{IN} = 10V, I_{OUT} = 0mA, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (SOURCING)



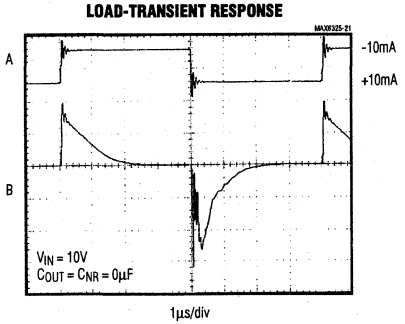
A: I_{OUT}, 10mA/div (SOURCING)
B: V_{OUT}, 500µV/div

LOAD-TRANSIENT RESPONSE (SINKING)



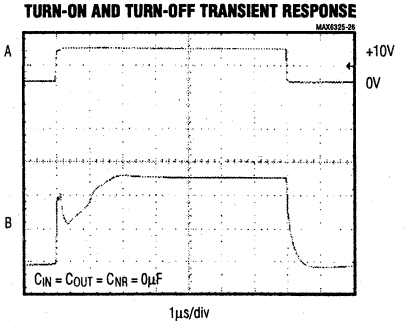
A: I_{OUT}, 10mA/div (SINKING)
B: V_{OUT}, 500µV/div

LOAD-TRANSIENT RESPONSE



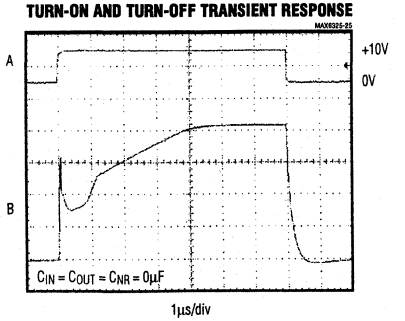
A: I_{OUT} (±10mA SOURCE AND SINK), 20mA/div, AC COUPLED
B: V_{OUT}, 20mV/div, AC COUPLED

MAX6325
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



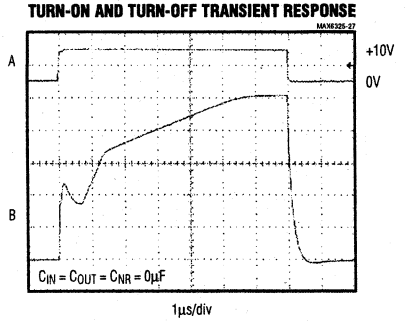
A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

MAX6341
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

MAX6350
TURN-ON AND TURN-OFF TRANSIENT RESPONSE



A: V_{IN}, 10V/div
B: V_{OUT}, 1V/div

1ppm/°C, Low-Noise, +2.5V/+4.096V/+5V Voltage References

Pin Description

PIN	NAME	FUNCTION
1, 7, 8	I.C.	Internally Connected. **Do not use.**
2	IN	Positive Power-Supply Input
3	NR	Noise Reduction. Optional capacitor connection for wideband noise reduction. Leave open if not used (Figure 2).
4	GND	Ground
5	TRIM	External Trim Input. Allows ±1% output adjustment (Figure 1). Leave open if not used.
6	OUT	Voltage Reference Output

Detailed Description

Temperature Stability

The MAX6325/MAX6341/MAX6350 are highly stable, low-noise voltage references that use a low-power temperature-compensation scheme to achieve laboratory-standard temperature stability. This produces a nearly flat temperature curve, yet does not require the power associated with heated references.

The output voltage can be trimmed a minimum of 0.6% by connecting a 10kΩ potentiometer between OUT and GND, and connecting its tap to the TRIM pin, as shown in Figure 1. The external trimming does not affect temperature stability.

Noise Reduction

To augment wideband noise reduction, add a 1µF capacitor to the NR pin (Figure 2). Larger values do not improve noise appreciably (see *Typical Operating Characteristics*).

Noise in the power-supply input can affect output noise, but can be reduced by adding an optional bypass capacitor to the IN pin and GND.

Bypassing

The MAX6325/MAX6341/MAX6350 are stable with capacitive load values from 0µF to 100µF, for all values of load current. Adding an output bypass capacitor can help reduce noise and output glitching caused by load transients.

Applications Information

Negative Regulator

Figure 3 shows how both a +5V and -5V precision reference can be obtained from a single, unregulated +5V supply. A MAX681 generates approximately ±9V to operate the MAX6350 reference and MAX400 inverting amplifier. The +5V is inverted by the ultra-low offset MAX400 op amp. Resistor R1 is optional, and may be used to trim the ±5V references. R2 and R4 should be matched, both in absolute resistance and temperature coefficient. R3 is optional, and is adjusted to set the -5V reference.

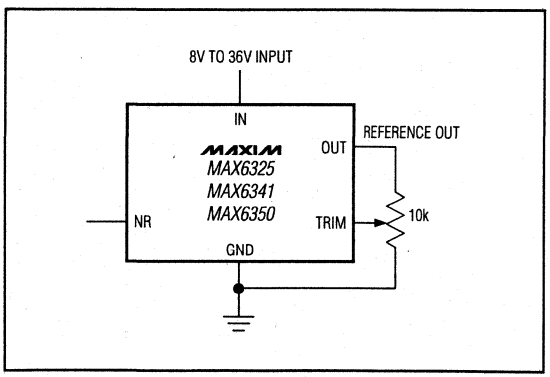


Figure 1. Output Voltage Adjustment

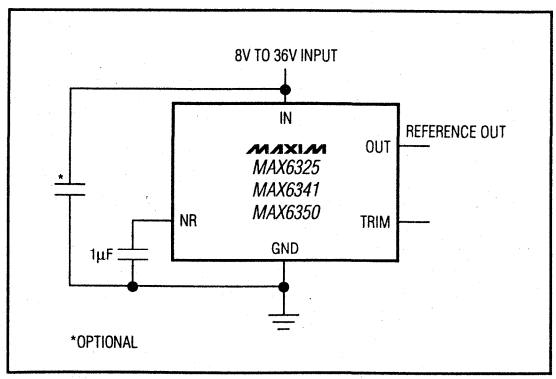


Figure 2. Noise-Reduction Capacitor

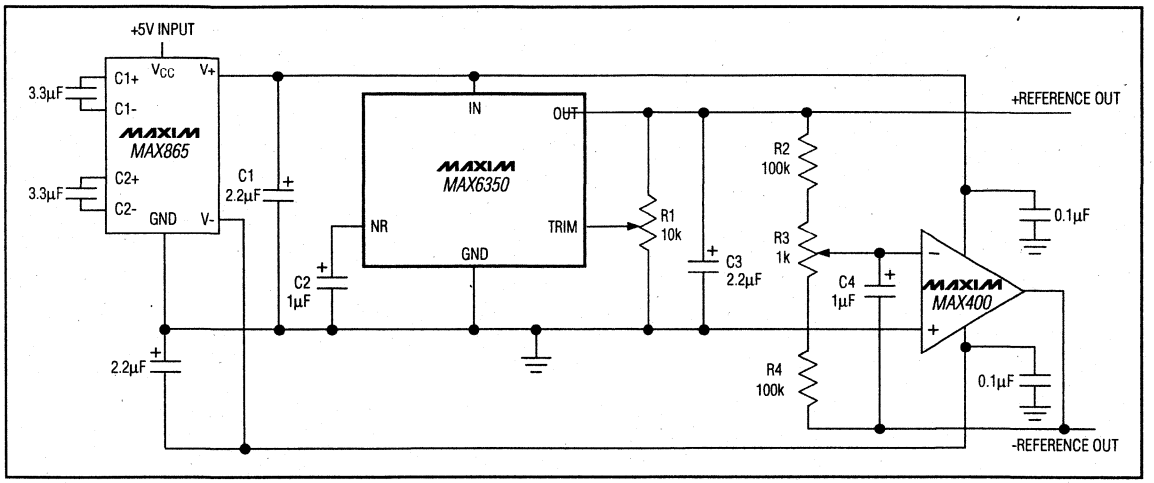


Figure 3. +5V and -5V References from a Single +5V Supply

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	MAX. TEMPCO (ppm/°C)
MAX6341CPA	0°C to +70°C	8 Plastic DIP	1.0
MAX6341CSA	0°C to +70°C	8 SO	1.0
MAX6341EPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX6341ESA	-40°C to +85°C	8 SO	1.5
MAX6341MJA	-55°C to +125°C	8 CERDIP	2.5
MAX6350CPA	0°C to +70°C	8 Plastic DIP	1.0
MAX6350CSA	0°C to +70°C	8 SO	1.0
MAX6350EPA	-40°C to +85°C	8 Plastic DIP	1.5
MAX6350ESA	-40°C to +85°C	8 SO	1.5
MAX6350MJA	-55°C to +125°C	8 CERDIP	2.5

_Chip Information

TRANSISTOR COUNT: 435

A/D Converters

A/D Converters, Product Tables and Trees 7-2

MAX104	1Gsps, 8-Bit ADC with Track/Hold	7-9*
MAX115	±5V Input, 2x4-Channel, Simultaneous-Sampling 12-Bit DAS	7-11*
MAX116	±2.5V Input, 2x4-Channel, Simultaneous-Sampling 12-Bit DAS	7-11*
MAX125	±5V Input, 2x4-Channel, Simultaneous-Sampling 14-Bit DAS	7-13*
MAX126	±2.5V Input, 2x4-Channel, Simultaneous-Sampling 14-Bit DAS	7-13*
MAX146	+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC with Internal Reference	7-15
MAX147	+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADC	7-15
MAX148	+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADC	7-39
MAX149	+2.7V, Low Power, 8-Channel, Serial 10-Bit ADC with Internal Reference	7-39
MAX1002	Low Power, 60Msps, Dual, 6-Bit ADC	7-61
MAX1003	Low-Power, 90Msps, Dual 6-Bit ADC	7-73
MAX1005	Intermediate Frequency Undersampler (CODEC)	7-85*
MAX1007	Mobile-Radio Analog Controller	7-87*
MAX1101	Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA	7-89
MAX1110	+2.7V, Low-Power, 8-Channel, Serial 8-Bit ADC	7-101
MAX1111	+2.7V, Low-Power, 4-Channel, Single-Ended or 2-Channel Differential, Serial 8-Bit ADC	7-101
MAX1112	+5V, Low-Power, 8-Channel Single-Ended/4-Channel Differential, Serial 8-Bit ADC	7-121
MAX1113	+5V, Low-Power, 4-Channel Single-Ended/2-Channel Differential, Serial 8-Bit ADC	7-121
MAX1160	10-Bit, 20Msps, TTL-Output ADC	7-141
MAX1161	10-Bit, 40Msps, TTL-Output ADC	7-149
MAX1202	+5V, 8-Channel, Serial, 12-Bit ADC with 3V Digital Interface and Internal Reference	7-157
MAX1203	+5V, 8-Channel, Serial, 12-Bit ADC with 3V Digital Interface	7-157
MAX1204	+5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface and Internal Reference	7-181
MAX1240	+2.7V to +3.6V, Low-Power, 12-Bit Serial ADC with Internal Reference	7-203
MAX1241	+2.7V to +5.25V, Low-Power, 12-Bit Serial ADC with Internal Reference	7-203
MAX1242	+2.7V to +3.6V, Low-Power, 10-Bit Serial ADC with Internal Reference	7-217
MAX1243	+2.7V to +3.6V, Low-Power, 10-Bit Serial ADC	7-217
MAX1246	+2.7V to +3.6V, Low-Power, 4-Channel, Serial 12-Bit ADC with Internal Reference	7-229
MAX1247	+2.7V to +5.25V, Low-Power, 4-Channel, Serial 12-Bit ADC in QSOP-16 Package	7-229
MAX1248	+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC with Internal Reference	7-251
MAX1249	+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADC in QSOP-16 Package	7-251

*Advance Information–first page of a data sheet in preparation.

A/D Converters

Ultra-High-Speed Conversion (<0.5µs)

6 Bits

Multichannel

★ ☆ MAX1002 (60Msps)
★ ☆ MAX1003 (90Msps)

8 Bits

Internal T/H

☆ MAX100 (250Msps)
☆ MAX101A (500Msps)
† ☆ MAX104 (1Gsps)
☆ MAX1114* (150Msps)

External T/H

☆ MAX1125* (300Msps)
★ ☆ MAX1150* (500Msps)
★ ☆ MAX1151* (750Msps)

10 Bits

Internal T/H

★☆ MAX1160* (20Msps)
★☆ MAX1161* (40Msps)

12 Bits

Internal T/H

☆ MAX1170* (10Msps)
☆ MAX1171* (20Msps)
☆ MAX1172* (30Msps)

Fast Conversion (<100µs) (SAR/Flash ADCs)

8 Bits

Single Channel

Internal T/H

MAX150 (1.34µs/ref)
☆ MAX152 (3V)
☆ MAX153 (0.66µs)
MAX165 (5µs/ref)
MAX166 (5µs/ref/diff in)
ADC0820 (1.38µs)
MX7575 (5µs)
MX7820 (1.34µs)
MX7821 (0.66µs)

External T/H

MAX160 (4µs)
MAX1101 (1.5µs CCD digitizer)
MX7574 (15µs)
MX7576 (10µs)

Multichannel

Internal T/H

MAX113 (3V/1.8µs/4-ch)
MAX114 (1Msps)
☆ MAX117 (3V/1.8µs/8-ch)
☆ MAX118 (1Msps)
MAX154 (2µs/4-ch/ref)
☆ MAX155 (3µs/8-ch/ref/ simultaneous T/Hs)
MAX156 (3µs/4-ch/ref/ simultaneous T/Hs)
MAX158 (2µs/8-ch/ref)
★☆ MAX1110 (2.7V/16µs/8-ch/ref)
★ MAX1111 (2.7V/16µs/4-ch/ref)
★☆ MAX1112 (5V/16µs/8-ch/ref)
★ MAX1113 (5V/16µs/4-ch/ref)
MX7824 (2µs/4-ch)
MX7828 (2µs/8-ch)

External T/H

MAX161 (20µs/8-ch)
MX7581 (67µs/8-ch)

10 Bits

Single Channel

Internal T/H

MAX151 (2.5µs/ref)
MAX177 (8.33µs/ref)
★ MAX1242 (2.7V/7.5µs/ref/serial)
MAX1243 (2.7V/7.5µs/serial)

External T/H

MAX173 (5µs/ref)

Multichannel

Internal T/H

MAX148 (2.7V/7.5µs/serial/8-ch)
★ MAX149 (2.7V/7.5µs/ref/serial/8-ch)
MAX192 (7.5µs/ref/serial/8-ch)
★ MAX1204 (5V/7.5µs/8-ch/ref/3V logic)
★ MAX1248 (2.7V/7.5µs/ref/serial/4-ch)
MAX1249 (2.7V/7.5µs/4-ch)

★ New product
† Future product
☆ Evaluation kit available
* Not available in Japan

12 Bits

Single Channel

Internal T/H

☆ MAX120 (1.6µs/ref)
☆ MAX122 (2.6µs/ref)
MAX163 (8µs/ref)
MAX164 (8µs/ref)
MAX167 (8µs/ref)
☆ MAX176 (3.5µs/ref/serial)
MAX178 (60µs/ref)
☆ MAX187 (8.5µs/ref/serial)
☆ MAX189 (8.5µs/serial)
☆ MAX190 (7.8µs/ref/serial & parallel)
☆ MAX191 (7.5µs/ref/serial & parallel)
★☆ MAX1241 (2.7V/7.5µs/serial)
★☆ MAX1240 (2.7V/7.5µs/ref/serial)

External T/H

MAX162 (3.25µs/ref)
MAX170 (5µs/ref/serial)
MAX172 (10µs/ref)
MAX174 (8µs/ref)
MAX183 (3.25µs)
MAX184 (5µs)
MAX185 (10µs)
MX574A (25µs/ref)
MX674A (15µs/ref)
MX7572-05 (5µs/ref)
MX7572-12 (12µs/ref)
MX7578 (100µs)
MX7672-03 (3µs)
MX7672-05 (5µs)
MX7672-10 (10µs)

Multichannel

Internal T/H

† MAX127 (bus/ref/8-ch/serial)
† MAX128 (bus/ref/8-ch/serial)
★☆ MAX146 (2.7V/7.5µs/ref/serial/8-ch)
☆ MAX147 (2.7V/7.5µs/serial/8-ch)
☆ MAX180 (8.33µs/ref/8-ch)
☆ MAX181 (8.33µs/ref/6-ch)
MAX182 (60µs/ref/4-ch)
☆ MAX186 (7.5µs/ref/serial/8-ch)
☆ MAX188 (7.5µs/serial/8-ch)
☆ MAX196 (6µs/ref/6-ch)
☆ MAX197 (6µs/ref/8-ch)
☆ MAX198 (6µs/ref/6-ch)
☆ MAX199 (6µs/ref/8-ch)
★☆ MAX1202 (5V/7.5µs/8-ch/ref/3V logic)
★☆ MAX1203 (5V/7.5µs/8-ch/3V logic)
MAX1245 (2.375V/serial/8-ch)
★☆ MAX1246 (2.7V/7.5µs/ref/serial/4-ch)
☆ MAX1247 (2.7V/7.5µs/4-ch)

External T/H

MX7582 (100µs/4-ch)

14 Bits

Internal T/H

☆ MAX121 (2.9µs/ref/serial)
☆ MAX194 (10µs/serial)

External T/H

MAX162 (3.25µs/ref)
MAX170 (5µs/ref/serial)
MAX172 (10µs/ref)
MAX174 (8µs/ref)
MAX183 (3.25µs)
MAX184 (5µs)
MAX185 (10µs)
MX574A (25µs/ref)
MX674A (15µs/ref)
MX7572-05 (5µs/ref)
MX7572-12 (12µs/ref)
MX7578 (100µs)
MX7672-03 (3µs)
MX7672-05 (5µs)
MX7672-10 (10µs)

16 Bits

Internal T/H

☆ MAX195 (10µs/serial)

Multichannel

†☆ MAX125 (3µs/ref/ 2x4-ch/simult. T/Hs)
†☆ MAX126 (3µs/ref/ 2x4-ch/simult. T/Hs)

see next page for Slow Conversion (>10ms)

A/D Converters

see previous page for Fast Conversion (<100µs) and Ultra-High-Speed Conversion (<0.5µs)

Slow Conversion (>10ms) (Integrating & Σ - Δ ADCs)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
MAX131 (3 1/2 D, B/G, L)
MAX136 (3 1/2 D, B/G, HOLD, L)
MAX138 (3 1/2 D, B/G, S/S)
ICL7106 (3 1/2 D, Z)
ICL7116 (3 1/2 D, Z, HOLD)
ICL7126 (3 1/2 D, Z, L)
ICL7129A (4 1/2 D)
ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
MAX140 (3 1/2 D, B/G, S/S)
ICL7107 (3 1/2 D, Z)
ICL7117 (3 1/2 D, Z, HOLD)
ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

☆ MAX132 (±18 bit, serial, L)
MAX133 (±40,000 count, L)
☆ MAX134 (±40,000 count, L)
MAX135 (±15 bit, L)
ICL7109 (12 bit, Z)
ICL7135 (±20,000 count)

Σ - Δ ADCs

☆ MAX110 (±14 bit, serial, no ext. components, L)

☆ MAX111 (±14 bit, serial, no ext. components, L)

Integrated Converter Systems (CODECs)

Fast Conversion (<100µs)

† MAX1005 (5-bit ADC, 7-bit DAC)
† MAX1007 (8-bit ADC, four 7-bit DACs)

† Future product
☆ Evaluation kit available

NOTES: HOLD – Includes display-hold input
S/S – Includes +5V single supply
B/G – Includes bandgap reference
Z – Includes zener reference
L – Low power

Ultra-High-Speed A/D Converters

Part Number	Resolution (Bits)	Sample Rate (Msps max)	Input Channels	Voltage Reference* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX1002	6	60	2	I	Parallel	+5	±250mV, ±500mV	Yes	Dual ADC with internal oscillator & PGA	3.40
MAX1003	6	90	2	I	Parallel	+5 & +3.3	±250mV, ±500mV	Yes	Dual ADC with internal oscillator & PGA	3.96
MAX1114(1)	8	150	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, high SNR	‡
MAX100	8	250	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P, highest bandwidth	‡
MAX1125(1)	8	300	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth	‡
MAX101A	8	500	1	E	Parallel	+5 & -5.2	±0.27	Yes	50Ω I/P, highest bandwidth, demuxed outputs	‡
MAX1150(1)	8	500	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, demuxed output	‡
MAX1151(1)	8	750	1	E	Parallel	-5.2	0 to +2	Yes	Wide bandwidth, demuxed output	‡
MAX104	8	1000	1	E	Parallel	±5	300mV	Yes	7.3 ENOB at 500Msps, demuxed outputs	††
MAX1160(1)	10	20	1	E	Parallel	+5	±2	Yes	5pF input capacitance	‡
MAX1161(1)	10	40	1	E	Parallel	+5	±2	Yes	5pF input capacitance	‡
MAX1170(1)	12	10	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡
MAX1171(1)	12	20	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡
MAX1172(1)	12	30	1	E	Parallel	+5	±2	Yes	Low input capacitance, high SFDR	‡

Integrating A/D Converters

Part Number	Resolution (digits)	(counts)	Output Type	Supply Voltage (V)	Supply Current (mA), max(typ)	References	EV Kit	Features	Price† 1000-up ($)
DUAL-SLOPE ADCs									
MAX130	3 1/2	±2000	LCD	+4.5 to +14	0.25(0.1)	Bandgap		Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to +14	0.1(0.06)	Bandgap		Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15(0.06)	Bandgap		Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to +7	0.8(0.2)	Bandgap		± inputs with single supply	4.40
ICL7106	3 1/2	±2000	LCD	+9	1.8(0.6)	Zener		For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8(0.8)	Zener		ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1(0.06)	Zener		Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		± inputs with single supply	4.40
MAX140	3 1/2	±2000	LED	+5	0.8(0.2)	Bandgap		Low segment current (2mA)	4.40
ICL7107	3 1/2	±2000	LED	+9	1.8(0.6)	Zener		For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8(0.8)	Zener		ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2(0.06)	Zener		Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
MAX134	3 3/4	±40,000	µP	±5	0.2(0.09)	External	Yes	20 conv/sec, ±10µV resolution	9.75
ICL7109	12 bits + sign	±4096	8-/16-bit µP/UART	±5	1.5(0.7)	Zener		Three-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4(1)	External		Lowest noise ±3µV	5.48
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2(1)	External		For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	±5	0.125(0.06)	External		Three-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	±5	0.125(0.06)	External	Yes	Serial high-resolution ADC, <1mW	8.00
SIGMA-DELTA ADCs									
MAX110	14 bits + sign	–	Serial	±5	0.95(0.55)	External	Yes	No external components, low power, dual supplies	4.80
MAX111	14 bits + sign	–	Serial	+5	1.2(0.64)	External	Yes	No external components, low power, single supply	4.80

* E = external reference, I = internal reference

(1) Not available in Japan

† Prices provided are for design guidance and are for the lowest grade, commercial temperature

Low-Power A/D Converters

Part Number	Resolution (Bits)	Input Channels	Data-Bus Interface (Bits)	Supply Voltage (V)	Supply Current (mA)	Power-Down Current (µA)	Conversion Time (µs max)	Voltage Reference* (V)	EV Kit	Features	Price† 1000-up ($)
MAX113	8	4	µP/8	+3 to +3.6	1.5	1	1.8	E		3V, 8-bit, 4-channel ADC with power-down	3.45
MAX117	8	8	µP/8	+3 to +3.6	1.5	1	1.8	E	Yes	3V, 8-bit, 8-channel ADC with power-down	3.55
MAX152	8	1	µP/8	+3 or ±3	1.5	1	1.8	E	Yes	3V ADC with 1µA power-down	3.10
MAX114	8	4	µP/8	+5	8	1	0.66	E		5V, 8-bit, 4-channel ADC with power-down	3.30
MAX118	8	8	µP/8	+5	8	1	0.66	E	Yes	5V, 8-bit, 8-channel ADC with power-down	3:40
MAX153	8	1	µP/8	+5 or ±5	8	1	0.66	E	Yes	High-speed ADC with 1µA power-down	2.95
MAX1110	8	8	Serial	+2.7 to +5.5	0.25	2	16	I/+2.048 or E	Yes	2.7V, 8-channel, 250µA ADC with power-down	2.70
MAX1111	8	4	Serial	+2.7 to +5.5	0.25	2	16	I/+2.048 or E		2.7V, 4-channel, 250µA ADC with power-down	2.45
MAX1112	8	8	Serial	+5	0.25	2	16	I/+4.096 or E	Yes	5V, 8-channel, 250µA ADC with power-down	2.70
MAX1113	8	4	Serial	+5	0.25	2	16	I/+4.096 or E		5V, 4-channel, 250µA ADC with power-down	2.45
MAX148	10	8	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, 8-channel serial ADC	3.10
MAX149	10	8	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5		2.7V, 8-channel serial ADC with reference	3.20
MAX192	10	8	Serial	+5	1.5	2	7.5	I/+4.096 or E		Low power, low cost, small package	2.95**
MAX1204	10	8	Serial	+5 or ±5	1.5	2	7.5	I/+4.096 or E		5V, 10-bit 8-channel ADC with 3V logic interface	4.25
MAX1242	10	1	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5		MAX1243 with internal reference	2.75
MAX1243	10	1	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, 10-bit serial ADC in 8-pin package	2.45
MAX1248	10	4	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5		MAX1249 with internal reference	3.40
MAX1249	10	4	Serial	+2.7 to +5.25	0.9	1	7.5	E		2.7V, low-power, serial, 4-ch ADC, QSOP-16 pkg.	3.25
MAX146	12	8	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5	Yes	2.7V, 8-channel serial ADC with reference	6.25
MAX147	12	8	Serial	+2.7 to +5.25	0.9	1	7.5	E	Yes	2.7V, 8-channel serial ADC	5.95
MAX186	12	8	Serial	+5 or ±5	1.5	2	7.5	I/+4.096	Yes	7mW, 10µA power-down	6.75
MAX187	12	1	Serial	+5	1.5	2	8.5	I/+4.096	Yes	7mW, 8-pin package	6.45
MAX188	12	8	Serial	+5 or ±5	1	2	7.5	E	Yes	MAX186 without reference	6.25
MAX189	12	1	Serial	+5	1	2	8.5	E	Yes	MAX187 without reference	5.95
MAX191	12	1	Serial and µP/8	+5 or ±5	2.5	2	7.5	I/+4.096 or E	Yes	15mW, 20µA power-down	9.60
MAX1202	12	8	Serial	+5 or ±5	1.5	2	7.5	I/+4.096	Yes	5V, 12-bit 8-channel ADC with 3V logic interface	6.50
MAX1203	12	8	Serial	+5 or ±5	0.9	1	7.5	E	Yes	MAX1202 with external reference	5.45
MAX1240	12	1	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5	Yes	MAX1241 with internal reference	3.85
MAX1241	12	1	Serial	+2.7 to +5.25	0.9	1	7.5	E	Yes	2.7V, 12-bit serial ADC in 8-pin package	3.10
MAX1245	12	8	Serial	+2.375 to +3.6	0.8	1	7.5	E		2.375V, 12-bit, 8-channel serial ADC	6.25
MAX1246	12	4	Serial	+2.7 to +3.6	1.5	1	7.5	I/+2.5	Yes	MAX1247 with internal reference	6.15
MAX1247	12	4	Serial	+2.7 to +5.25	0.9	1	7.5	E	Yes	2.7V, low-power, serial, 4-ch ADC, QSOP-16 pkg.	5.80
MAX194	14	1	Serial	±5	5.5	2	9.4	E	Yes	14-bit, high-speed serial ADC	14.00
MAX110	14 + sign	2	Serial	±5	550µA	1	20ms	E	Yes	Low-power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	Serial	+5	640µA	1	20ms	E	Yes	Low-power, shutdown mode, single supply	4.80
MAX135	15 + sign	1	µP/8	±5	60µA	1	10ms	E		High-resolution ADC, <1mW	8.00
MAX195	16	1	Serial	±5	5.5	2	10	E	Yes	High-speed serial 16-pin ADC	22.50
MAX132	18 + sign	1	Serial	±5	60µA	1	10ms	E	Yes	Serial high-resolution ADC, <1mW	8.00

* E = external reference, I = internal reference
** 25,000 pc. price, factory direct.

† Prices provided are for design guidance and are for the lowest grade, commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Other Sampling A/D Converters

Part Number	Resolution (Bits)	Sample Rate (kHz max)	Conversion Time (µs max)	Input Channels	Voltage Reference* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX1101	8	1000	1.5	1	E	Serial	+5	±VREF		CCD digitizer with 6-bit PGA	‡
MAX150	8	500	1.34	1	I/+2.5 or E	µP/8	+5	+5		Complete ADC with T/H and reference	5.85
MAX154	8	400	2	4	I/+2.5 or E	µP/8	+5	+5		4-channel ADC with T/H and reference	6.45
MAX158	8	400	2	8	I/+2.5 or E	µP/8	+5	+5		8-channel ADC with T/H and reference	6.85
MAX155	8	250	3.6	8	I/+2.5 or E	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-channel ADC with simult. T/Hs and reference	9.50
MAX156	8	250	3.6	4	I/+2.5 or E	µP/8	+5 or ±5	+2.5 or ±2.5		4-channel ADC with simult. T/Hs and reference	7.19
MAX165	8	200	5	1	I/+1.23 or E	µP/8	+5	+5		Low-cost sampling ADC with reference	3.95
MAX166	8	200	5	1	I/+1.23 or E	µP/8	+5	+5		Differential-input complete ADC	4.20
MAX151	10	300	2.5	1	I/+4.0 or E	µP/10	±5	+5		Sampling ADC with reference	7.95
MAX177	10 or 12	100	8.33	1	I/-5.25	µP/8 or 12	+5 & -12 to -15	±2.5		MAX167 with 10-bit accuracy	7.96
MAX120	12	500	1.6	1	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC	10.80
MAX122	12	333	2.6	1	I/-5.0	µP/12	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC	8.95
MAX176	12	250	3.5	1	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	Serial ADC, 8-pin miniDIP with T/H	9.85
MAX170	12	125**	5	1	I/-5.25	Serial	+5 & -12 to -15	+5		Serial ADC, 8-pin DIP with external T/H	11.96
MAX196	12	100	6	6	I/+4.096 or E	µP/12	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected, 6-channel	9.90
MAX197	12	100	6	8	I/+4.096 or E	µP/8	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected, 8-channel	9.90
MAX198	12	100	6	6	I/+4.096 or E	µP/12	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected, 6-channel	9.90
MAX199	12	100	6	8	I/+4.096 or E	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected, 8-channel	9.90
MAX163	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	+5		Complete sampling ADC with reference	14.40
MAX164	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	±5		Complete sampling ADC with reference	14.40
MAX167	12	100	8.33	1	I/-5.0	µP/8 or 12	+5 & -12 to -15	±2.5		Complete sampling ADC with reference	14.40
MAX180	12	100	8.33	8	I/-5.0 or E	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX181	12	100	8.33	6	I/-5.0 or E	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX178	12	20	60	1	I/+5.0 or E	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and reference	15.24
MAX182	12	20	60	4	I/+5.0 or E	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and reference	17.55
MAX121	14	308	2.9	1	I/-5.0	Serial	+5 & -12 to -15	±5	Yes	High-speed, complete sampling ADC with DSP interface,16-pin package	12.00
MAX125	14	75	3	4	I/+2.5 or E	µP/14	±5	±5	Yes	2 x 4 channels, 4 simultaneous T/Hs, ±5V input	††
MAX126	14	75	3	4	I/+2.5 or E	µP/14	±5	±2.5	Yes	2 x 4 channels, 4 simultaneous T/Hs, ±5V input	††

Integrated Converter Systems

Part Number	DAC Resolution (Bits)	ADC Resolution (Bits)	ADC Input Channels	ADC Sample Rate (MHz max)	DAC Update Rate (MHz max)	Voltage Reference* (V)	Data-Bus Interface	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX1005	7	5	1	15	15	I	Parallel	+3	IF undersampler for use with MAX2411 and MAX2511	‡
MAX1101	—	8	3	1	—	E	Serial	+5	CCD digitizer with clamp, PGA	2.95†††

Part Number	DAC Resolution (Bits)	ADC Resolution (Bits)	ADC Input Channels	ADC Conversion Time (µs)	DAC Settling Time (µs)	Voltage Reference* (V)	Data-Bus Interface	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX1007	7	8	4	5.2	10	I/1.21	Serial	+2.85 to +5.5	Mobile radio controller with 1 ADC, 4 DACs	††

* E = external reference, I = internal reference
** With external track/hold
‡ Contact factory for pricing
††† 100,000 pc. factory-direct price, FOB USA.

† Prices provided are for design guidance and are for the lowest grade, commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Resolution (Bits)	Input Channels	Conversion Time (µs max)	Sample Rate (kHz max)	Voltage Reference* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	EV Kit	Features	Price† 1000-up ($)
MAX114	8	4	0.66	1000	E	µP/8	+5	+5 or ±2.5		5V, 4-channel ADC with 1µA power-down	3.30
MAX113	8	4	1.8	400	E	µP/8	+3	+3 or ±1.5		3V, 4-channel ADC with 1µA power-down	3.45
MAX154	8	4	2	400	I/+2.5 or E	µP/8	+5	+5		4-channel ADC with T/H and reference	5.65
MX7824	8	4	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7824	5.30
MAX156	8	4	3.6	250	I/+2.5 or E	µP/8	+5 or ±5	+2.5 or ±2.5		4-channel ADC with simult. T/Hs and reference	7.19
MAX1111	8	4	16	50	I/+2.048 or E	Serial	+2.7 to +5	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, 8-channel, 250µA ADC with power-down	2.45
MAX1113	8	4	16	50	I/+4.096 or E	Serial	+5	$+V_{REF}$ or $\pm V_{REF}/2$		5V, 8-channel, 250µA ADC with power-down	2.45
MAX118	8	8	0.66	1000	E	µP/8	+5	+5 or ±2.5	Yes	5V, 8-channel ADC with 1µA power-down	3.40
MAX117	8	8	1.8	400	E	µP/8	+3	+3 or ±1.5	Yes	3V, 8-channel ADC with 1µA power-down	3.55
MAX158	8	8	2	400	I/+2.5 or E	µP/8	+5	+5		8-channel ADC with T/H and reference	6.00
MX7828	8	8	2	400	E	µP/8	+5	+5		Plug-in replacement for AD7828	5.70
MAX155	8	8	3.6	250	I/+2.5 or E	µP/8	+5 or ±5	+2.5 or ±2.5	Yes	8-channel ADC with simult. T/Hs and reference	9.50
MAX1110	8	8	16	50	I/+2.048 or E	Serial	+2.7 to +5	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, 8-channel 250µA ADC with power-down	2.70
MAX1112	8	8	16	50	I/+4.096 or E	Serial	+5	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	5V, 8-channel 250µA ADC with power-down	2.70
MAX161	8	8	20	–	E	µP/8	+5	+10		8-channel ADC with RAM buffer	11.12
MX7581	8	8	66.6	–	E	µP/8	+5	+10		Plug-in replacement for AD7581	11.08
MAX1248	10	4	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25		MAX1249 with internal reference	3.40
MAX1249	10	4	7.5	133	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, 10-bit, low-power serial ADC	3.25
MAX1204	10	8	7.5	133	I/+4.096 or E	Serial	+5 or ±5	$+V_{REF}$ or $\pm V_{REF}$		5V, 10-bit, 8-channel ADC with 3V logic interface	4.25
MAX192	10	8	7.5	133	I/+4.096 or E	Serial	+5	+5 or ±2.5		Low power, low cost, small package	2.95**
MAX148	10	8	7.5	133	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$		2.7V, lowest power 10-bit ADC	3.10
MAX149	10	8	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25		8-channel serial ADC with reference	3.20
MAX1246	12	4	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25	Yes	MAX1247 with internal reference	6.15
MAX1247	12	4	7.5	133	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, 12-bit, low-power serial ADC	5.80
MAX182	12	4	60	20	I/+5.0 or E	µP/8 or 12	±5 & +15	+5		1LSB TUE, has T/H and reference	17.55
MX7582	12	4	100	–	E	µP/8 or 12	±5 & +15	+5		Plug-in replacement for AD7582	19.50
MAX196	12	6	6	100	I/+4.096 or E	µP/12	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX198	12	6	6	100	I/+4.096 or E	µP/12	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX181	12	6	8.33	100	I/-5.0 or E	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX197	12	8	6	100	I/+4.096 or E	µP/8	+5	±10, +10, ±5, +5	Yes	Multi-range, fault protected	9.90
MAX199	12	8	6	100	I/+4.096 or E	µP/8	+5	±4, +4, ±2, +2	Yes	Multi-range, fault protected	9.90
MAX146	12	8	7.5	133	I/+2.5	Serial	+2.7 to +3.6	+2.5 or ±1.25	Yes	MAX147 with internal reference	6.25
MAX147	12	8	7.5	133	E	Serial	+2.7 to +5.25	$+V_{REF}$ or $\pm V_{REF}/2$	Yes	2.7V, low power, serial, 8-channel, 12-bit ADC	5.95
MAX186	12	8	7.5	133	I/+4.096	Serial	+5 or ±5	+5 or ±2.5	Yes	7mW, 10µA power-down	6.75
MAX188	12	8	7.5	133	E	Serial	+5 or ±5	+5 or ±2.5	Yes	MAX186 without reference	6.25
MAX1202	12	8	7.5	133	I/+4.096	Serial	+5 or ±5	$+V_{REF}$ or $\pm V_{REF}$	Yes	5V, 12-bit, 8-channel ADC with 3V logic interface	6.50
MAX1203	12	8	7.5	133	E	Serial	+5 or ±5	$+V_{REF}$ or $\pm V_{REF}$	Yes	5V, 12-bit, 8-channel ADC with 3V logic interface	5.45
MAX1245	12	8	7.5	100	E	Serial	+2.375 to +3.6	$+V_{REF}$ or $\pm V_{REF}/2$		2.375V, 12-bit, 8-channel serial ADC	6.25
MAX180	12	8	8.33	100	I/-5.0 or E	µP/8 or 12	+5 & -12 to -15	+5 or ±2.5	Yes	Data-acquisition system	12.75
MAX125	14	8	3	75	I/+2.5 or E	µP/14	±5	±5	Yes	2x4 channels, 4 simultaneous T/Hs, ±5V input	††
MAX126	14	8	3	75	I/+2.5 or E	µP/14	±5	±2.5	Yes	2x4 channels, 4 simultaneous T/Hs, ±2.5V input	††
MAX110	14 + sign	2	20ms	–	E	Serial	±5	±3	Yes	Low power, shutdown mode, dual supplies	4.80
MAX111	14 + sign	2	20ms	–	E	Serial	+5	±2	Yes	Low power, shutdown mode, single supply	4.80

* E = external reference, I = internal reference

** 25,000 pc. price, factory direct

† Prices provided are for design guidance and are for the lowest grade, commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

MAXIM

1Gsps, 8-Bit ADC with Track/Hold

General Description

The MAX104 PECL-compatible, 1Gsps, 8-bit analog-to-digital converter (ADC) allows accurate digitizing of analog signals from DC to 1.5GHz. Designed on Maxim's proprietary advanced GST-2 bipolar process, the MAX104 integrates a high-performance track/hold (T/H) amplifier and quantizer on a single monolithic die.

The innovative design of the internal T/H, which has an exceptionally wide 1.5GHz input bandwidth, results in high, 7.3 effective bits performance at Nyquist. Special comparator design and decoding circuitry reduce out-of-sequence code errors and provide excellent metastable performance of less than one error per 10^{12} clock cycles. Unlike other ADCs, which can have errors that result in false full-scale or zero-scale outputs, the MAX104 keeps the error magnitude to 1LSB.

The analog input is designed for differential or single-ended use with a ±250mV input range. Dual differential PECL-compatible output data paths provide for easy interfacing and include an 8:16 demultiplexer that reduces output data rates to one-half the clock rate. Control inputs are provided for interleaving additional MAX104 devices to increase the effective system sampling rate.

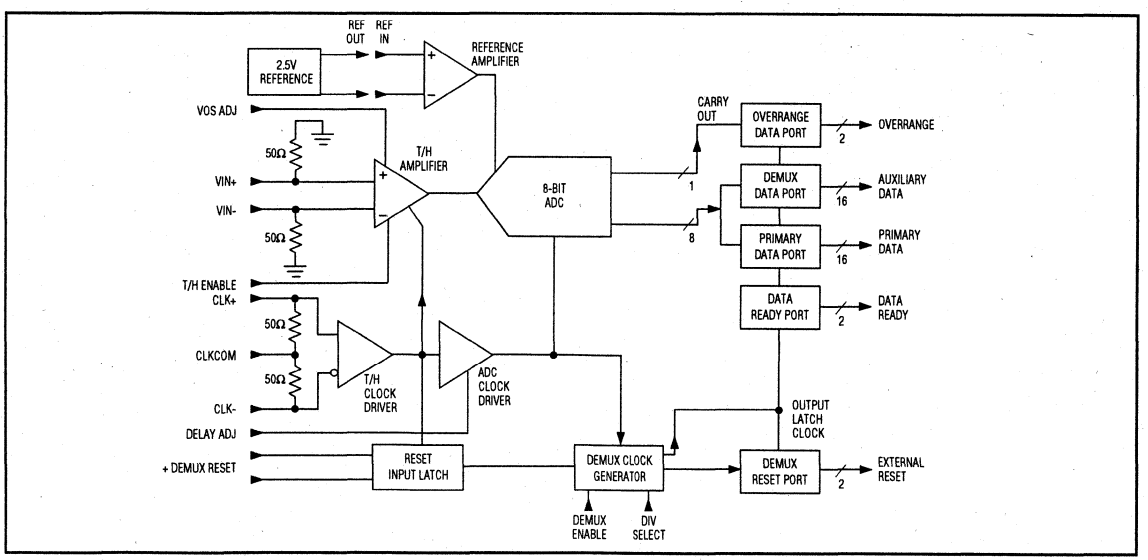
Features

- **1Gsps (min) Conversion Rate**
- **7.3 Effective Bits at 500MHz**
- **Less than ±1/2LSB DNL and INL**
- **50Ω Differential Input**
- **±250mV Input Signal Range**
- **On-Chip Reference**
- **4.5W Power Dissipation**
- **Latched, 3.3V PECL Digital Outputs**
- **Low Error Rate, Less than 10^{-12} Metastable States**
- **Selectable On-Chip 8:16 Demultiplexer**
- **Internal Demux Reset Input**
- **±5V Power Supplies**
- **192-Contact Super Ball Grid Array (SBGA)**

Applications

Digital RF/IF Signal Processing
High-Speed Data Acquisition
High-Energy Physics
Medical Systems
Radar/Sonar/ECM Systems

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

2x4-Channel, Simultaneous-Sampling 12-Bit DAS

General Description

The MAX115/MAX116 are high-speed, multichannel, 12-bit data-acquisition systems (DAS) with simultaneous track/hold (T/H) amplifiers. These devices contain a 12-bit, 3µs, successive-approximation analog-to-digital converter (ADC), a 2.5V reference, a buffered reference input, and a bank of four simultaneous-sampling T/H amplifiers that preserve the relative phase information of the sampled inputs. The MAX115/MAX116 have two multiplexed inputs for each T/H, allowing a total of eight inputs. In addition, the converters are overvoltage tolerant to ±17V; i.e., these input voltages will not harm the ICs. Available input ranges are ±5V (MAX115) and ±2.5V (MAX116).

An on-board sequencer converts from one to four channels with a single $\overline{CONVST}$ pulse. In default mode, one T/H output (CH1A) is converted. An interrupt signal ($\overline{INT}$) is provided after the last conversion is complete. Convert two, three, or four channels by reprogramming the MAX115/MAX116 through the bidirectional parallel interface. Once programmed, the MAX115/MAX116 continue to convert the specified number of channels per $\overline{CONVST}$ pulse until they are reprogrammed. The channels are converted sequentially beginning with CH1. The $\overline{INT}$ signal always follows the end of the last conversion in a conversion sequence. The ADC converts each assigned channel in 3µs and stores the result in an internal 12x4 RAM. Upon completion of the conversions, data can be accessed by applying successive pulses to the $\overline{RD}$ pin. Four successive reads access four data words sequentially.

The parallel interface's data-access and bus-release timing specifications are compatible with most popular digital-signal processors (DSPs) and 16-bit/32-bit microprocessors, so the MAX115/MAX116 conversion results can be accessed without resorting to wait states.

Applications

Multiphase Motor Control
Power-Grid Synchronization
Power-Factor Monitoring
Digital-Signal Processing
Vibration and Waveform Analysis

Features

- **Four Simultaneous-Sampling T/H Amplifiers with Two Multiplexed Inputs (eight single-ended inputs total)**
- **2µs Conversion Time per Channel**
- **Throughput: 400ksps (1 channel)**
  222ksps (2 channels)
  153ksps (3 channels)
  117ksps (4 channels)
- **Input Range: 5V (MAX115)**
  ±2.5V (MAX116)
- **Fault-Protected Input Multiplexer (±17V)**
- **±5V Supplies**
- **+2.5V Buffered Internal or External Reference**
- **Programmable On-Board Sequencer**
- **High-Speed Parallel DSP Interface**

Ordering Information

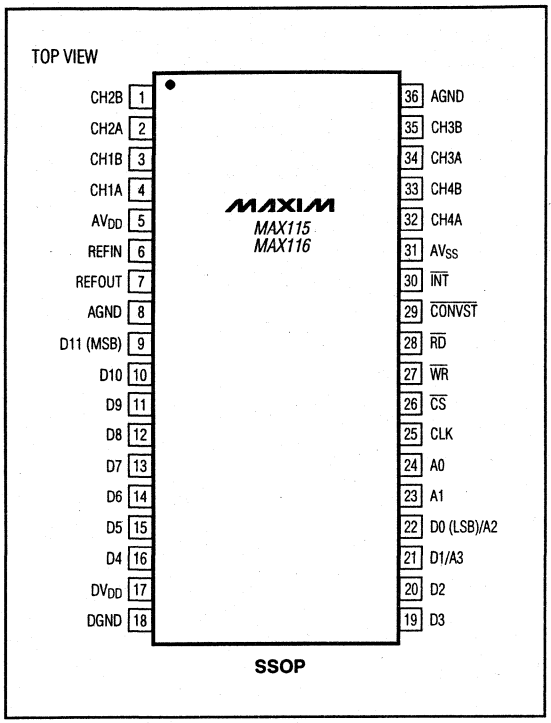
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX115ACAX	0°C to +70°C	36 SSOP	±1
MAX115BCAX	0°C to +70°C	36 SSOP	±2
MAX115BC/D	0°C to +70°C	Dice*	±2
MAX115AEAX	-40°C to +85°C	36 SSOP	±1
MAX115BEAX	-40°C to +85°C	36 SSOP	±2
MAX116ACAX	0°C to +70°C	36 SSOP	±1
MAX116BCAX	0°C to +70°C	36 SSOP	±2
MAX116BC/D	0°C to +70°C	Dice*	±2
MAX116AEAX	-40°C to +85°C	36 SSOP	±1
MAX116BEAX	-40°C to +85°C	36 SSOP	±2

**Dice are tested at T_A = +25°C only.*

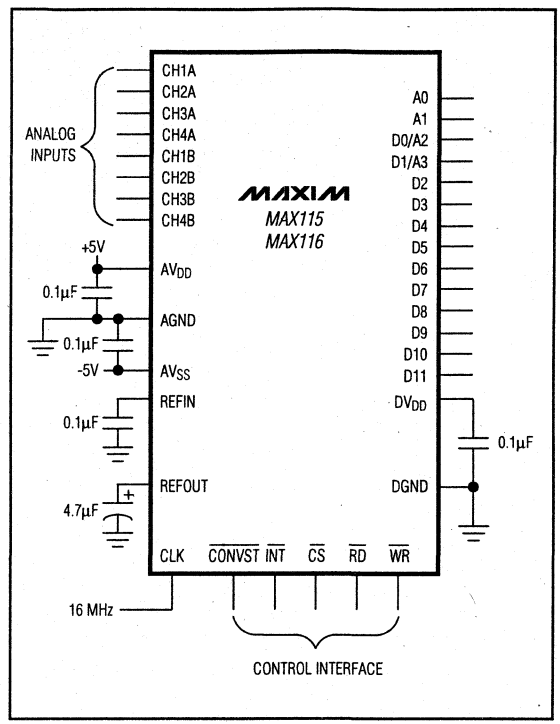
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

2x4-Channel, Simultaneous-Sampling 12-Bit DAS

Pin Configuration



Typical Operating Circuit



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

2x4-Channel, Simultaneous-Sampling 14-Bit DAS

General Description

The MAX125/MAX126 are high-speed, multichannel, 14-bit data-acquisition systems (DAS) with simultaneous track/holds (T/Hs). These devices contain a 14-bit, 3µs successive-approximation analog-to-digital converter (ADC), a +2.5V reference, a buffered reference input, and a bank of four simultaneous-sampling T/H amplifiers that preserve the relative phase information of the sampled inputs. The MAX125/MAX126 have two multiplexed inputs for each T/H, allowing a total of eight inputs. In addition, the converter is overvoltage tolerant to ±17V; when a conversion is in progress, a fault condition on any other channel will not harm the IC. Available input ranges are ±5V (MAX125) and ±2.5V (MAX126).

An on-board sequencer converts from one to four channels with a single $\overline{CONVST}$ pulse. In default mode, one T/H output (CH1A) is converted. An interrupt signal ($\overline{INT}$) is provided after the last conversion is complete. Convert two, three, or four channels by reprogramming the MAX125/MAX126 through the bidirectional parallel interface. Once programmed, the MAX125/MAX126 continue to convert the specified number of channels per $\overline{CONVST}$ pulse until they are reprogrammed. The channels are converted sequentially beginning with CH1. The $\overline{INT}$ signal always follows the end of the last conversion in a conversion sequence. The ADC converts each assigned channel in 3µs and stores the result in an internal 14x4 RAM. Upon completion of the conversions, data can be accessed by applying successive pulses to the $\overline{RD}$ pin. Four successive reads access the four data words sequentially.

The parallel interface's data-access and bus-release timing specifications are compatible with most popular digital-signal processors and 16-bit/32-bit microprocessors, so the MAX125/MAX126 conversion results can be accessed without resorting to wait states.

Applications

Multiphase Motor Control
Power-Grid Synchronization
Power-Factor Monitoring
Digital-Signal Processing
Vibration and Waveform Analysis

Features

- **Four Simultaneous-Sampling T/H Amplifiers with Two Multiplexed Inputs (eight single-ended inputs total)**
- **3µs Conversion Time per Channel**
- **Throughput: 250ksps (1 channel)**
  142ksps (2 channels)
  100ksps (3 channels)
  75ksps (4 channels)
- **Input Range: ±5V (MAX125), ±2.5V (MAX126)**
- **Fault-Protected Input Multiplexer (±17V)**
- **±5V Supplies**
- **+2.5V Buffered Internal or External Reference**
- **Programmable On-Board Sequencer**
- **High-Speed Parallel DSP Interface**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX125ACAX	0°C to +70°C	36 SSOP	±2
MAX125BCAX	0°C to +70°C	36 SSOP	±4
MAX125BC/D	0°C to +70°C	Dice*	±4
MAX125AEAX	-40°C to +85°C	36 SSOP	±2
MAX125BEAX	-40°C to +85°C	36 SSOP	±4
MAX126ACAX	0°C to +70°C	36 SSOP	±2
MAX126BCAX	0°C to +70°C	36 SSOP	±4
MAX126BC/D	0°C to +70°C	Dice*	±4
MAX126AEAX	-40°C to +85°C	36 SSOP	±2
MAX126BEAX	-40°C to +85°C	36 SSOP	±4

*Dice are tested at T_A = +25°C only.

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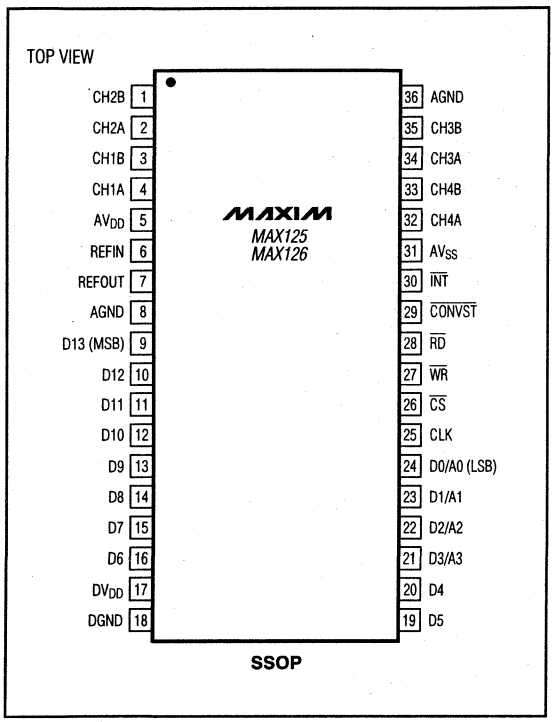
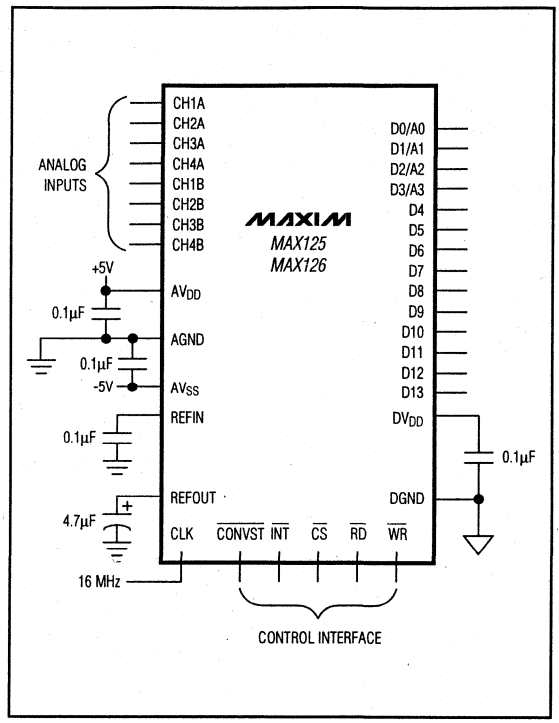
For small orders, phone 408-737-7600 ext. 3468.

2x4-Channel, Simultaneous-Sampling 14-Bit DAS

Pin Configuration



Typical Operating Circuit



19-0465; Rev 1; 6/97

EVALUATION KIT AVAILABLE

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

General Description

The MAX146/MAX147 12-bit data-acquisition systems combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption. The MAX146 operates from a single +2.7V to +3.6V supply; the MAX147 operates from a single +2.7V to +5.25V supply. Both devices' analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX146/MAX147 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX146 has an internal 2.5V reference, while the MAX147 requires an external reference. Both parts have a reference-buffer amplifier with a ±1.5% voltage-adjustment range.

These devices provide a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX146/MAX147, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current to under 60µA at reduced sampling rates.

The MAX146/MAX147 are available in 20-pin DIP and SSOP packages.

For 4-channel versions of these devices, see the MAX1246/MAX1247 data sheet.

Applications

Portable Data Logging	Data Acquisition
Medical Instruments	Battery-Powered Instruments
Pen Digitizers	Process Control

Pin Configuration appears at end of data sheet.

SPI and QSPI are registered trademarks of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single-Supply Operation:**
  +2.7V to +3.6V (MAX146)
  +2.7V to +5.25V (MAX147)
- **Internal 2.5V Reference (MAX146)**
- **Low Power: 1.2mA (133ksps, 3V supply)**
  54µA (1ksps, 3V supply)
  1µA (power-down mode)
- **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **20-Pin DIP/SSOP Packages**

Ordering Information

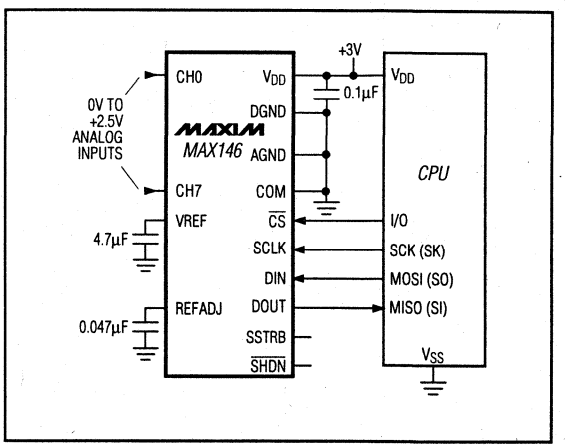
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX146ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX146BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX146ACAP	0°C to +70°C	20 SSOP	±1/2
MAX146BCAP	0°C to +70°C	20 SSOP	±1
MAX146BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

**Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to 6V
AGND to DGND ..... -0.3V to 0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF, REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to 6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX146_C_P/MAX147_C_P ..... 0°C to +70°C
MAX146_E_P/MAX147_E_P ..... -40°C to +85°C
MAX146_MJP/MAX147_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX146); V_{DD} = +2.7V to +5.25V (MAX147); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX146—4.7µF capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX14_A			±0.5	LSB
		MAX14_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX14_A		±0.5	±3	LSB
		MAX14_B		±0.5	±4	
Gain Error (Note 3)				±0.5	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.25		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		70	73		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-88	-80	dB
Spurious-Free Dynamic Range	SFDR		80	90		dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	tCONV	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	tACQ				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX146); V_{DD} = +2.7V to +5.25V (MAX147); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX146—4.7µF capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF / 2			±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX146 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C	2.480	2.500	2.520	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX146_C		±30	±50	ppm/°C
		MAX146_E		±30	±60	
		MAX146_M		±30	±80	
Load Regulation (Note 7)		0mA to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.047			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 8)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
REFADJ Buffer Disable Threshold			V_{DD} - 0.5			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference Buffer Gain		MAX146		2.06		V/V
		MAX147		2.00		
REFADJ Input Current		MAX146			±50	µA
		MAX147			±10	

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX146); V_{DD} = +2.7V to +5.25V (MAX147); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX146—4.7µF capacitor at VREF pin; MAX147—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)							
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$		2.0			V
		V_{DD} > 3.6V, MAX147 only		3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}					0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 9)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid Voltage	V_{SM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Input Low Voltage	V_{SL}					0.4	V
$\overline{SHDN}$ Input Current	I_S	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = FLOAT			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = FLOAT				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 9)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	MAX146		2.70		3.60	V
		MAX147		2.70		5.25	
Positive Supply Current, MAX146	I_{DD}	V_{DD} = 3.6V	Operating mode, full-scale input		1.2	2.0	mA
			Fast power-down		30	70	µA
			Full power-down		1.2	10	
Positive Supply Current, MAX147	I_{DD}	Operating mode, full-scale input	V_{DD} = 5.25V		1.8	2.5	mA
			V_{DD} = 3.6V		0.9	1.5	
Positive Supply Current, MAX147	I_{DD}	Full power-down	V_{DD} = 5.25V		2.1	15	µA
			V_{DD} = 3.6V		1.2	10	
Supply Rejection (Note 10)	PSR	Full-scale input, external reference = 2.500V, V_{DD} = 2.7V to $V_{DD(MAX)}$			±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX146); V_{DD} = +2.7V to +5.25V (MAX147); T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX14_ _C/E	20		200	ns
			MAX14_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 9)		0			ns

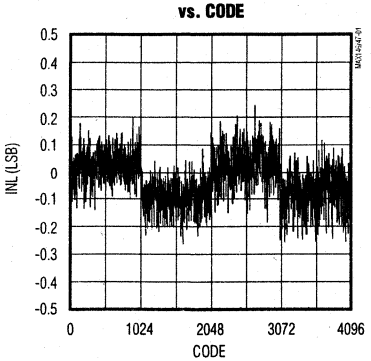
Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX146—internal reference, offset nulled; MAX147—external reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: External load should not change during conversion for specified accuracy.
Note 8: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 9: Guaranteed by design. Not subject to production testing.
Note 10: Measured as $|V_{FS}(2.7V) - V_{FS}(V_{DD, MAX})|$.

7

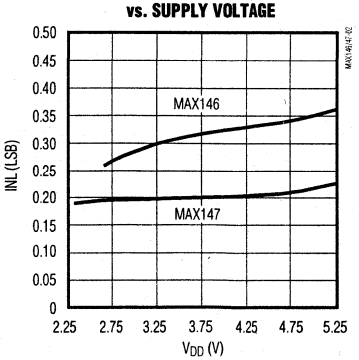
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

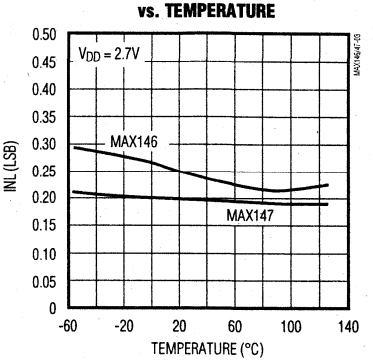
INTEGRAL NONLINEARITY vs. CODE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE

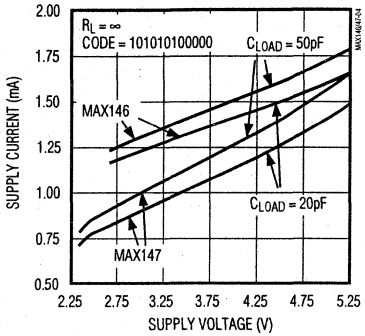


+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

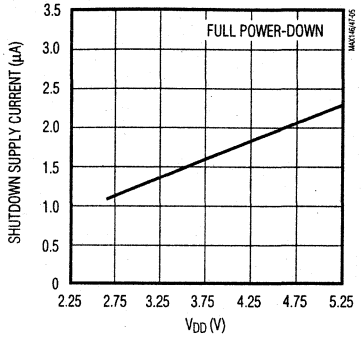
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

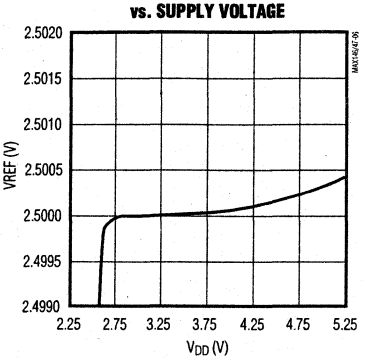
SUPPLY CURRENT vs. SUPPLY VOLTAGE



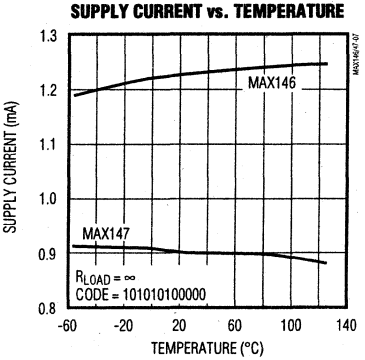
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



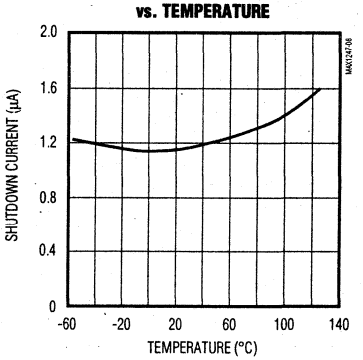
MAX146 INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



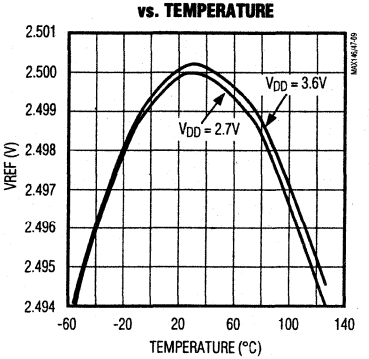
SUPPLY CURRENT vs. TEMPERATURE



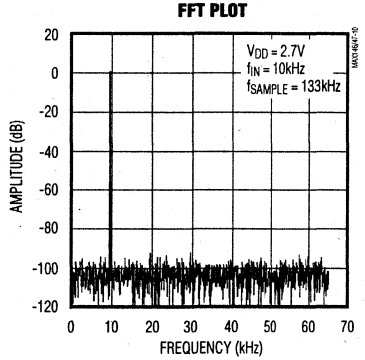
SHUTDOWN CURRENT vs. TEMPERATURE



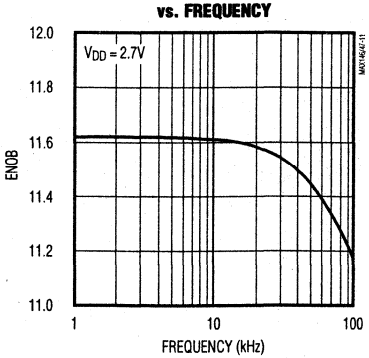
MAX146 INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



FFT PLOT



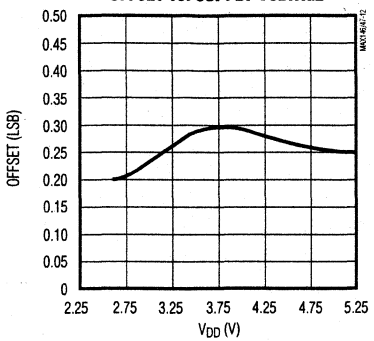
EFFECTIVE NUMBER OF BITS vs. FREQUENCY



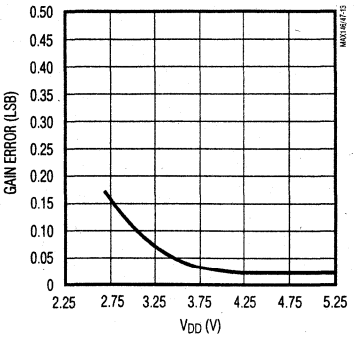
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

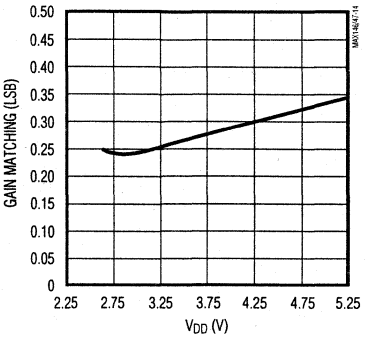
OFFSET vs. SUPPLY VOLTAGE



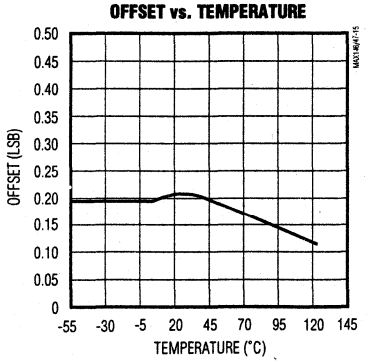
GAIN ERROR vs. SUPPLY VOLTAGE



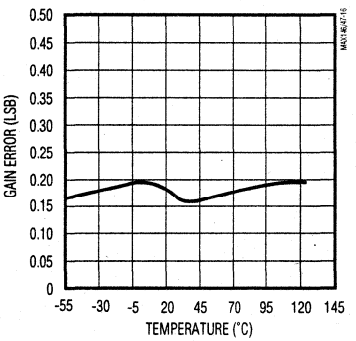
CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



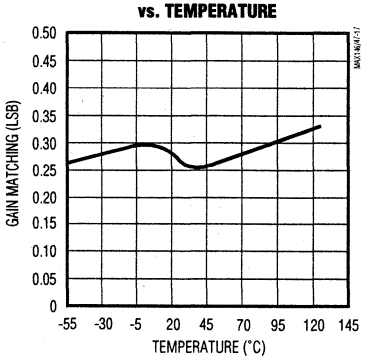
OFFSET vs. TEMPERATURE



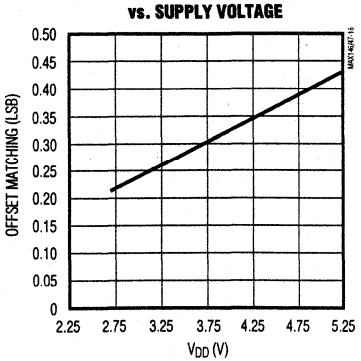
GAIN ERROR vs. TEMPERATURE



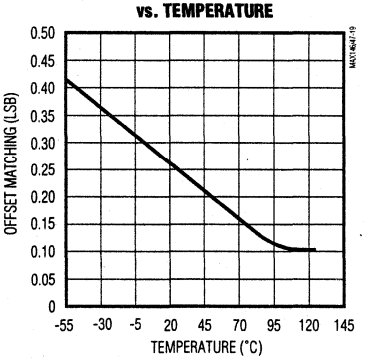
CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. COM sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX146/MAX147 down; otherwise, they are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX146 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX146/MAX147 begin the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)
20	V_{DD}	Positive Supply Voltage

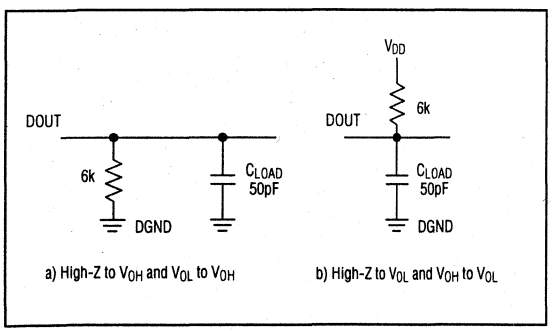


Figure 1. Load Circuits for Enable Time

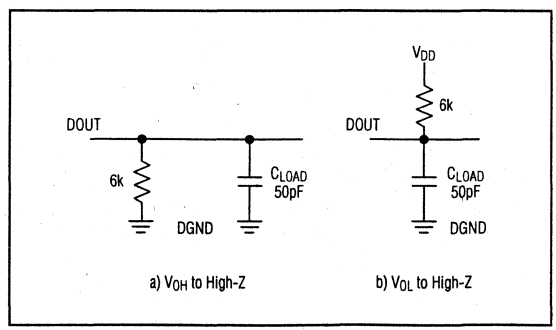


Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX146/MAX147 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX146/MAX147.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a 16pF x [(V_{IN+}) - (V_{IN-})] charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

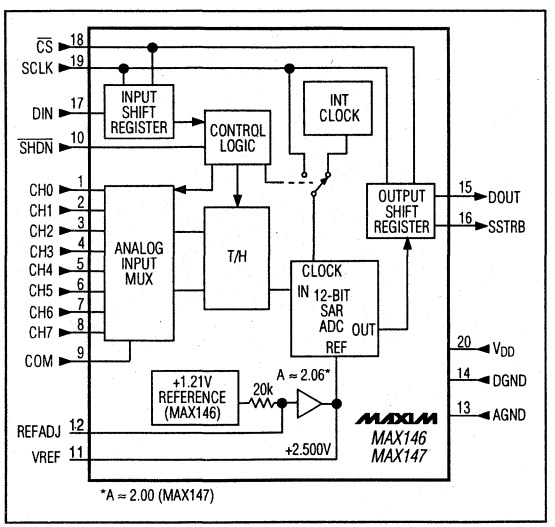


Figure 3. Block Diagram

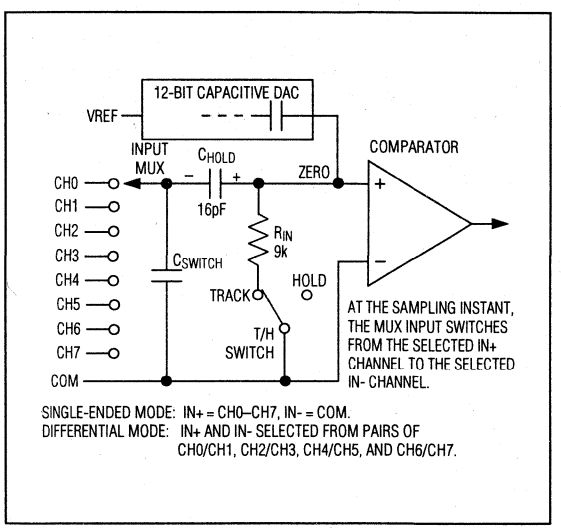


Figure 4. Equivalent Input Circuit

7

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The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 1kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

Quick Look

To quickly evaluate the MAX146/MAX147's analog performance, use the circuit of Figure 5. The MAX146/MAX147 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

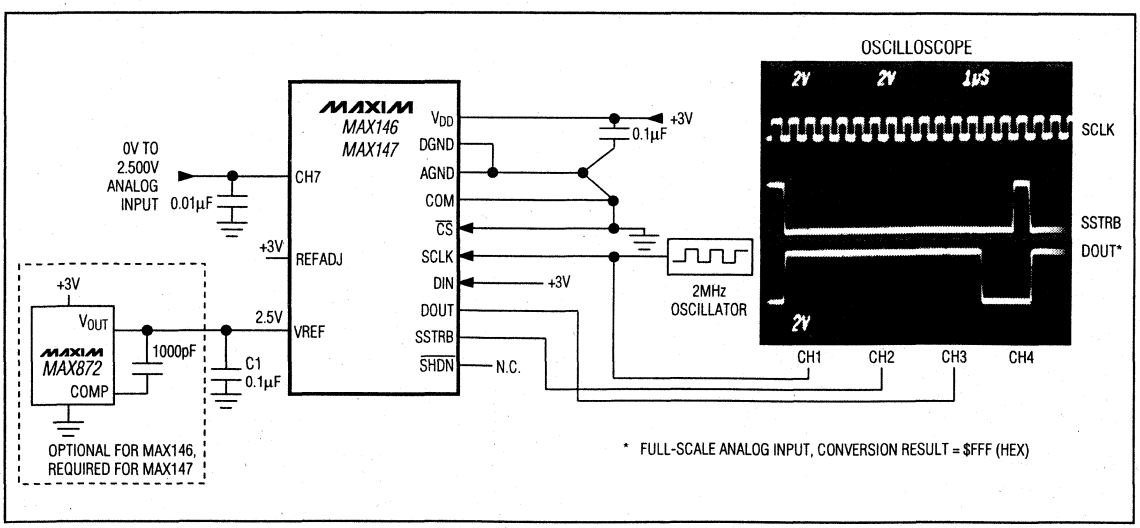

Figure 5. Quick-Look Circuit

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{\text{BIP}}$	SGL/$\overline{\text{DIF}}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{\text{CS}}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{\text{BIP}}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{\text{DIF}}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Full power-down 0 1 Fast power-down (MAX146 only) 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{\text{DIF}}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								−
1	0	0		+							−
0	0	1			+						−
1	0	1				+					−
0	1	0					+				−
1	1	0						+			−
0	1	1							+		−
1	1	1								+	−

Table 3. Channel Selection in Differential Mode (SGL/$\overline{\text{DIF}}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	−						
0	0	1			+	−				
0	1	0					+	−		
0	1	1							+	−
1	0	0	−	+						
1	0	1			−	+				
1	1	0					−	+		
1	1	1							−	+

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How to Start a Conversion

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX146/MAX147's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX146/MAX147 are compatible with SPI™/QSPI™ and Microwire™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 20 for MAX146/MAX147 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 17). For bipolar input mode, the output is two's complement (Figure 18). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX146/MAX147 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX146/MAX147. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

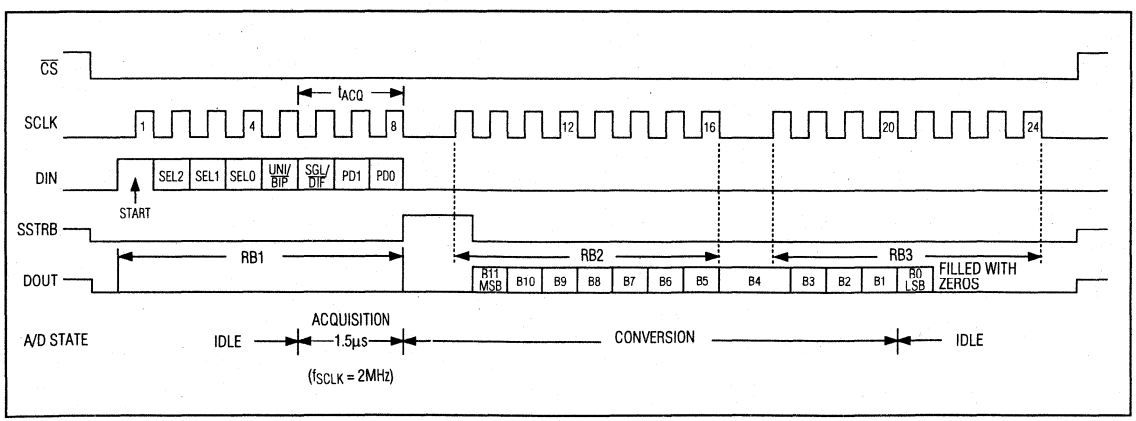

Figure 6. 24-Clock External Clock Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{SCLK} \leq 2MHz$)

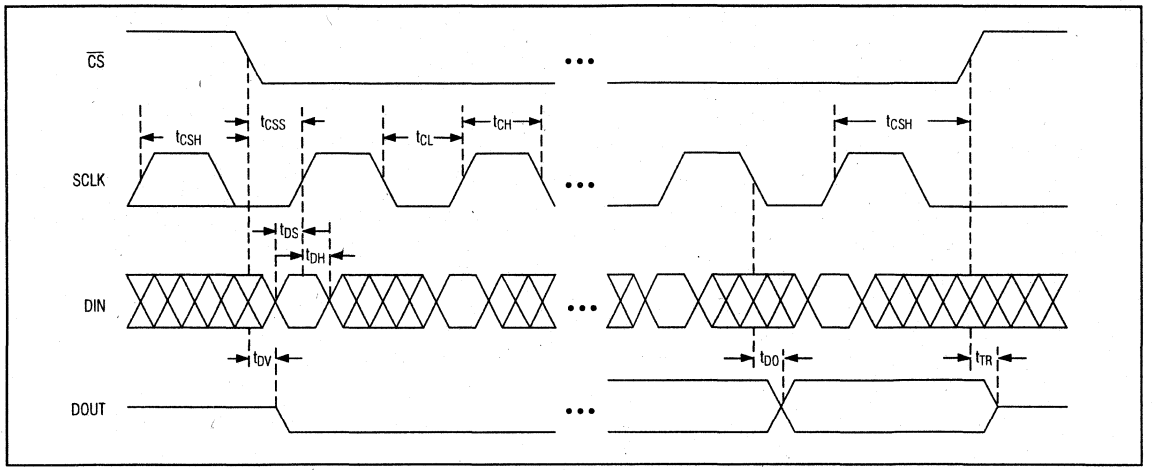

Figure 7. Detailed Serial-Interface Timing

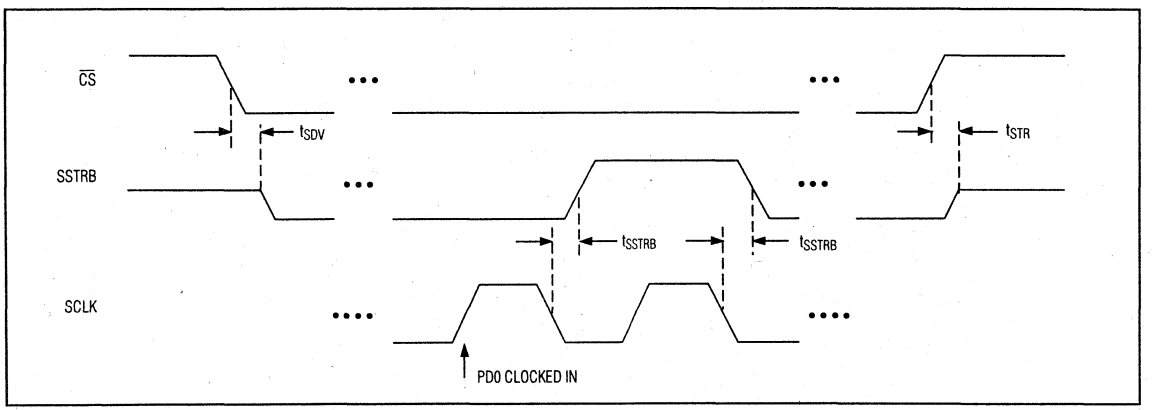

Figure 8. External Clock Mode SSTRB Detailed Timing

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX146/MAX147 generate their own conversion clocks internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the

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processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started.

Pulling $\overline{CS}$ high prevents data from being clocked into the MAX146/MAX147 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX146/MAX147 at clock rates exceeding 2.0MHz if the minimum acquisition time (t_{ACQ}) is kept above 1.5µs.

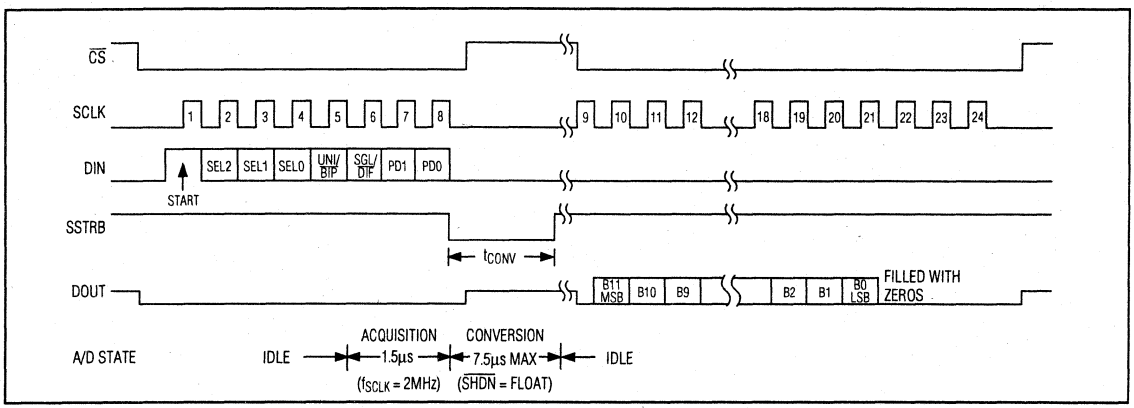

Figure 9. Internal Clock Mode Timing

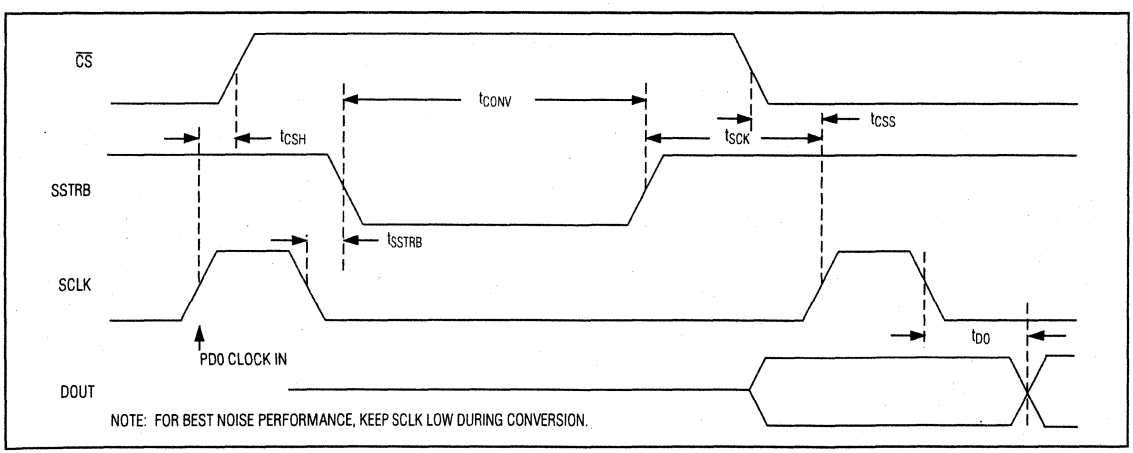

Figure. 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX146/MAX147 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX146/MAX147. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX146/MAX147 in internal clock mode, ready to convert with SSTRB = high. After the power supplies stabilize, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. (Also see Table 4.)

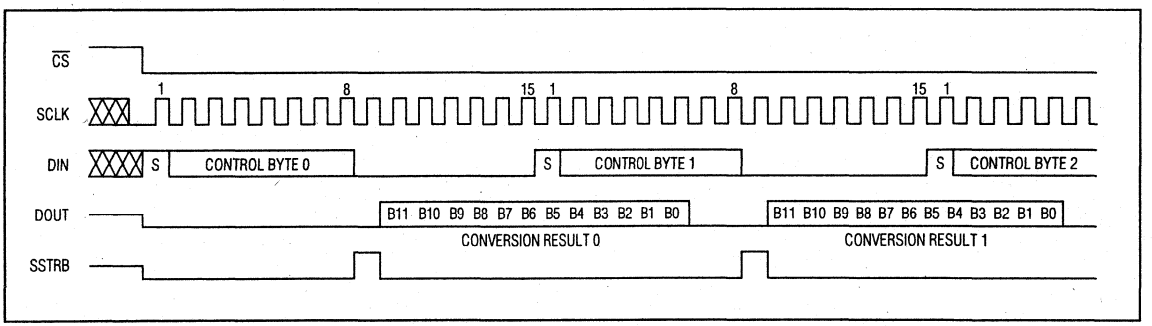

Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

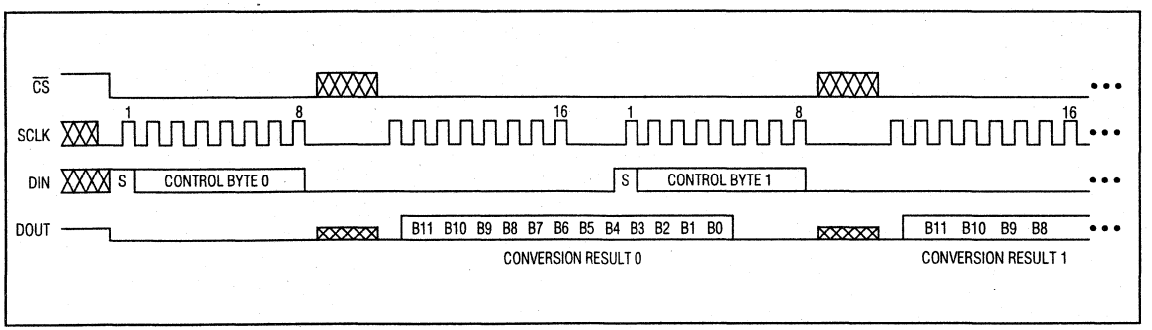

Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

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Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The100kHz minimum clock rate is limited by droop on the sample-and-hold and is independent of the compensation used.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at VREF. A 4.7µF value ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the *Choosing Power-Down Mode* section and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down mode or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current to 2µA (typ). Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX146/MAX147 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX146/MAX147. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

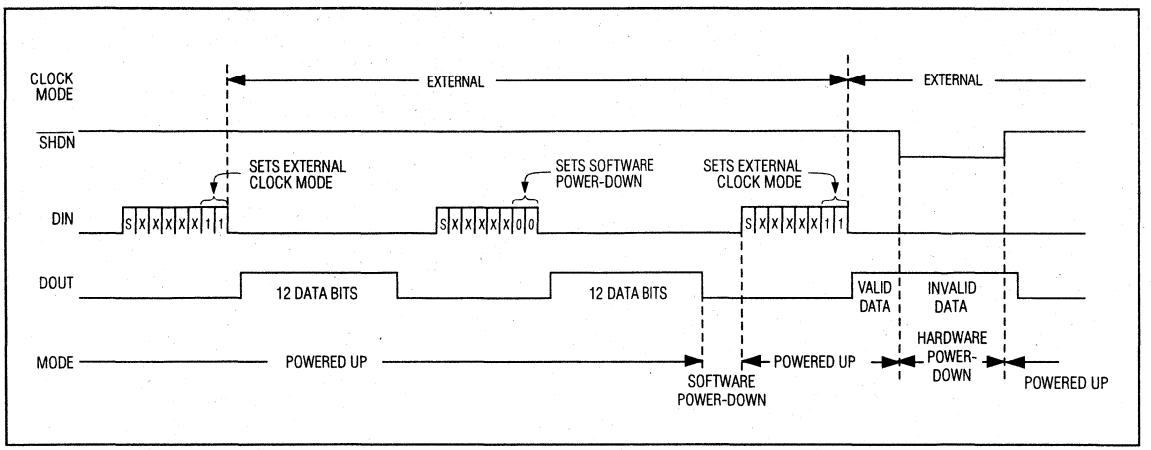

Figure 12a. Timing Diagram Power-Down Modes, External Clock

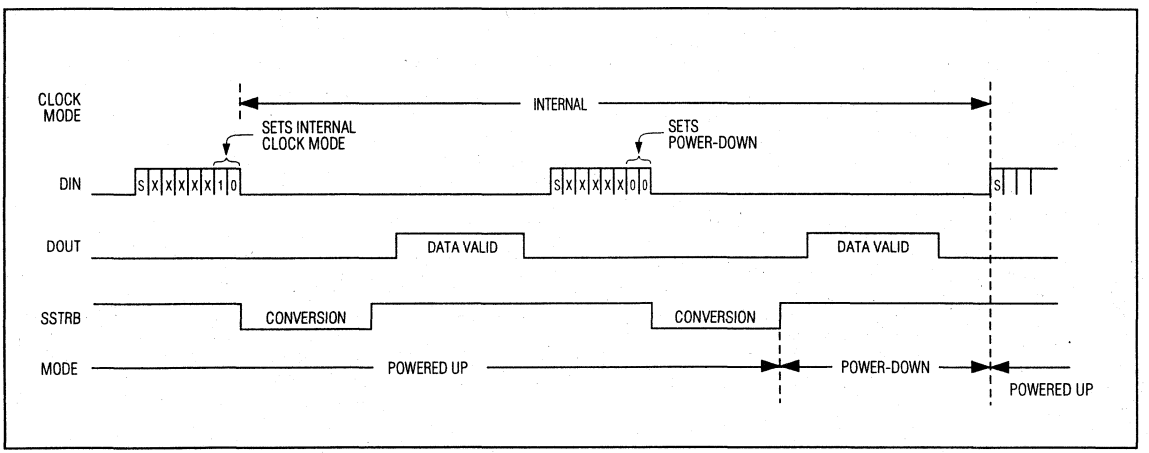

Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately $2M\Omega \times C_L$, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX146/MAX147 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

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Power-Down Sequencing

The MAX146/MAX147 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 13, 14a, and 14b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples show two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX146 power consumption for one or eight channel conversions utilizing full power-down mode and internal-reference compensation. A 0.047µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.9ms time constant. To achieve full 12-bit accuracy, 10 time constants or 9ms are required after power-up. Waiting this 9ms in FASTPD mode instead of in full power-up can reduce power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 15.

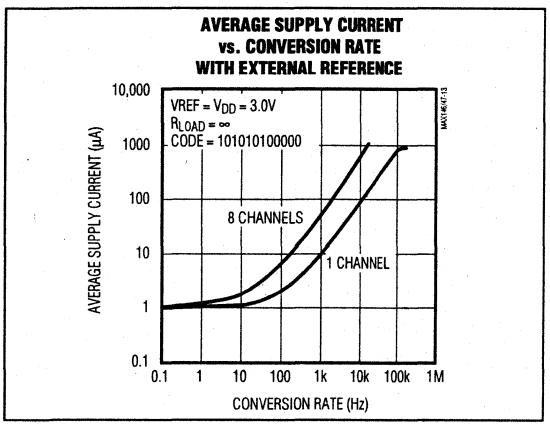

Figure 13. Average Supply Current vs. Conversion Rate with External Reference

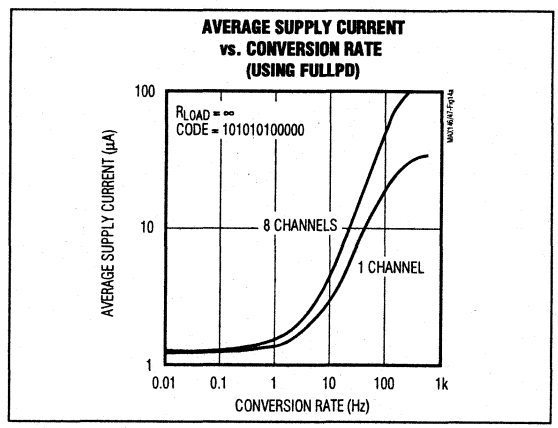

Figure 14a. MAX146 Supply Current vs. Conversion Rate, FULLPD

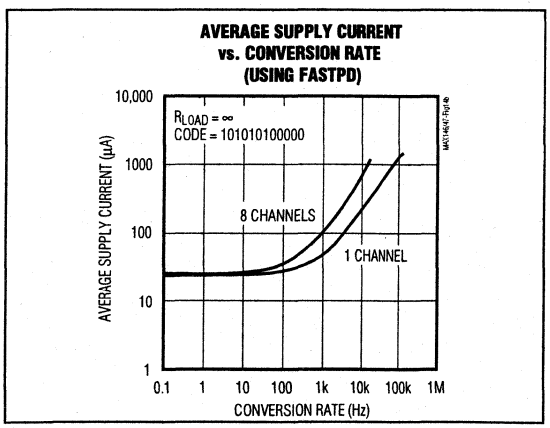

Figure 14b. MAX146 Supply Current vs. Conversion Rate, FASTPD

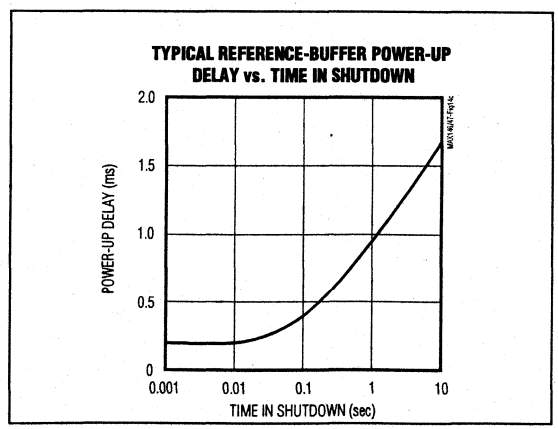

Figure 14c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

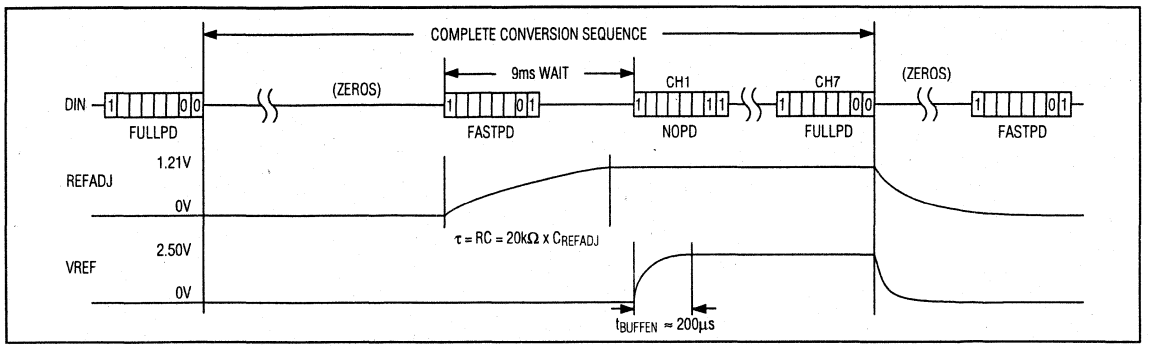

Figure 15. MAX146 FULLPD/FASTPD Power-Up Sequence

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 200µs wait after power-up with one dummy conversion. This graph shows fast multi-channel conversion with the lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX146/MAX147 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX146 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX147. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX146 and the MAX147. The MAX146's internally trimmed 1.21V reference is buffered with a 2.06 gain. The MAX147's REFADJ pin is also buffered with a 2.00 gain to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

Internal Reference (MAX146)

The MAX146's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit in Figure 16.

External Reference

With both the MAX146 and MAX147, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX146, and higher than 100kΩ for the MAX147. At

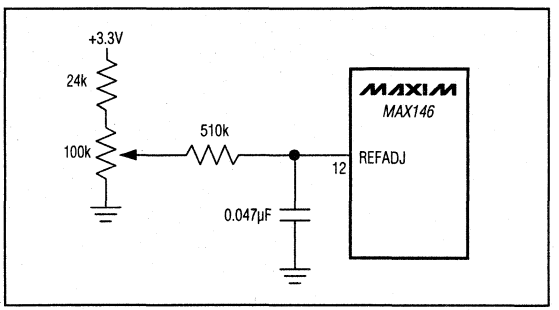

Figure 16. MAX146 Reference-Adjust Circuit

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

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VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ is typically 25µA (MAX146) with REFADJ tied to V_{DD}. Pull REFADJ to AGND to minimize the input bias current in power-down.

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the 0°C to +70°C commercial temperature range.

Figure 17 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 18 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610µV (2.500V / 4096) for unipolar operation, and 1LSB = 610µV [(2.500V / 2 - -2.500V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 19 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

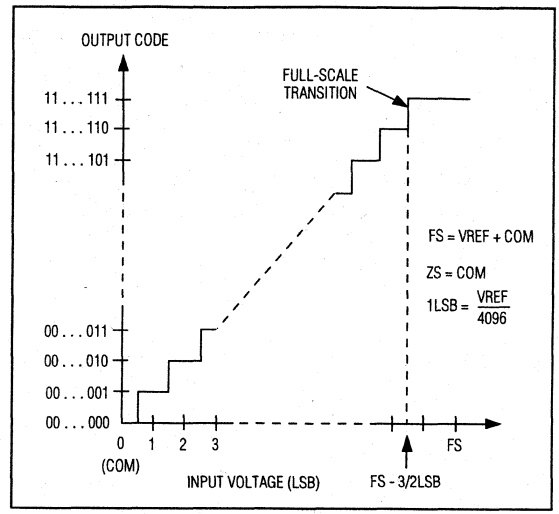


Figure 17. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 20 of the MAX146/MAX147. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 19).

High-Speed Digital Interfacing with QSPI

The MAX146/MAX147 can interface with QSPI using the circuit in Figure 20 (f_{SCLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

The MAX146/MAX147 are QSPI compatible up to the maximum external clock frequency of 2MHz.

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

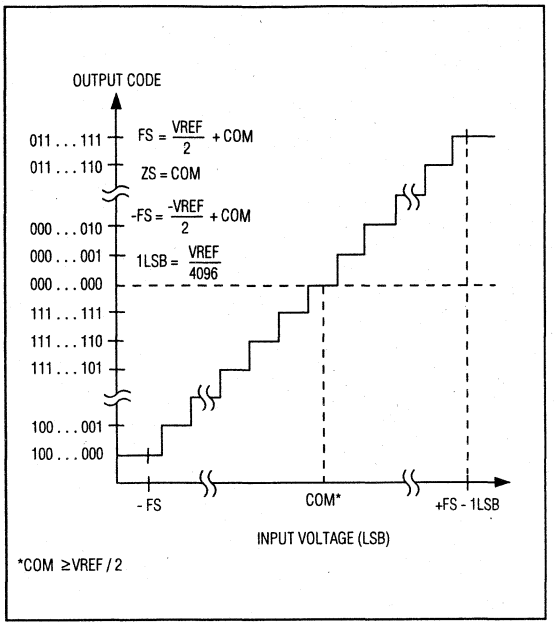


Figure 18. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

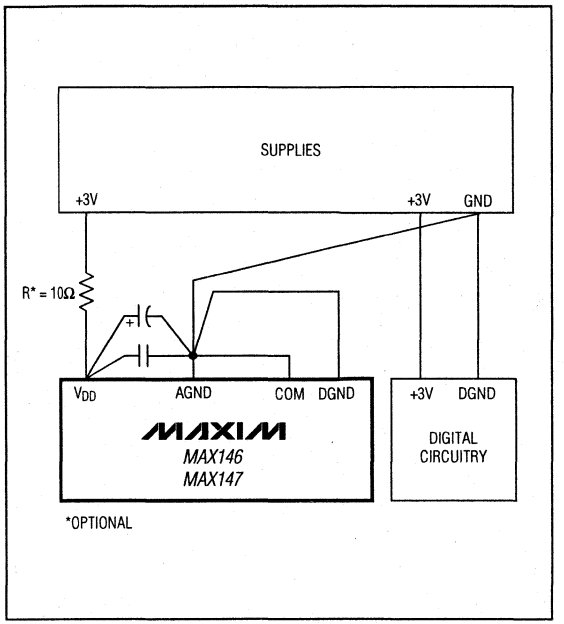


Figure 19. Power-Supply Grounding Connection

TMS320LC3x Interface

Figure 21 shows an application circuit to interface the MAX146/MAX147 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 22.

Use the following steps to initiate a conversion in the MAX146/MAX147 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX146/MAX147's SCLK input.
2) The MAX146/MAX147's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX146/MAX147's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX146/MAX147 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX146/MAX147's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX146/MAX147.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX146/MAX147 until the next conversion is initiated.

+2.7V, Low-Power, 8-Channel, Serial 12-Bit ADCs

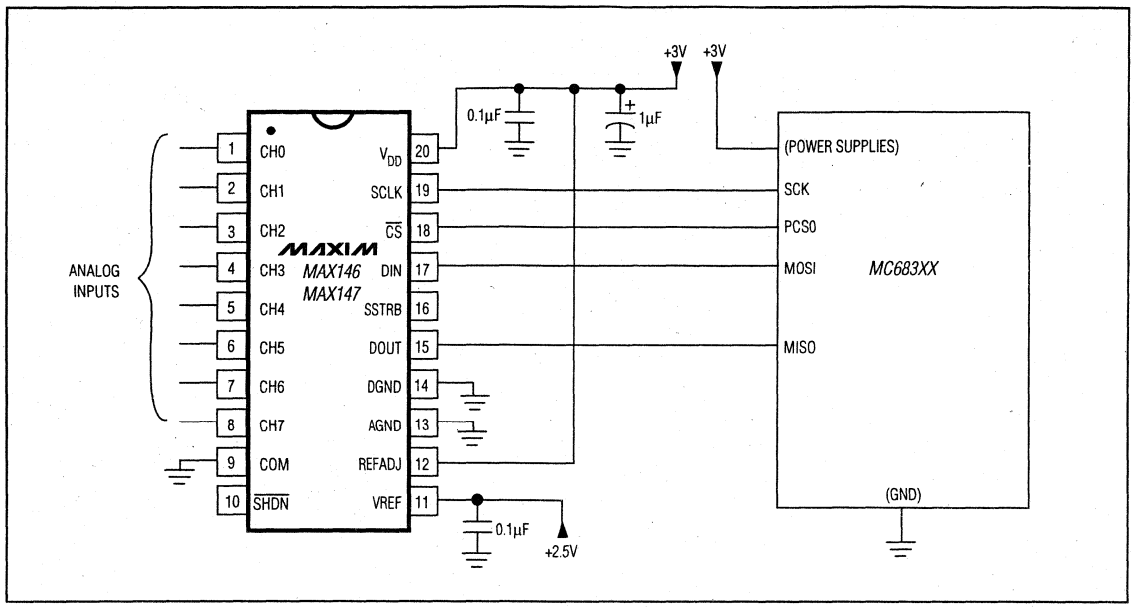


Figure 20. MAX146/MAX147 QSPI Connections, External Reference

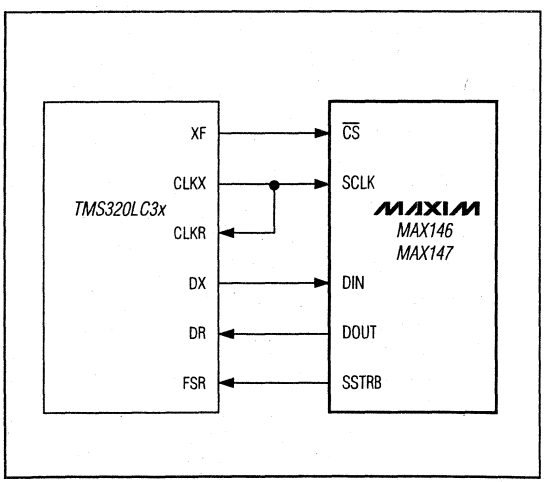


Figure 21. MAX146/MAX147-to-TMS320 Serial Interface

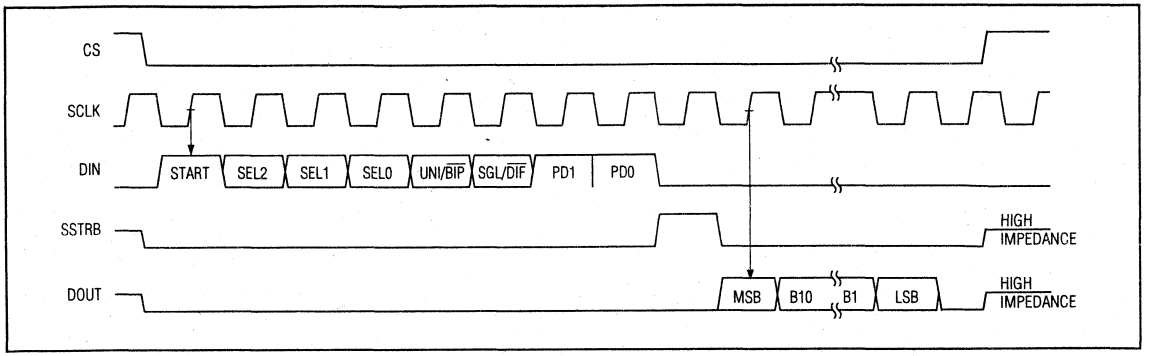


Figure 22. TMS320 Serial-Interface Timing Diagram

_Ordering Information (continued)

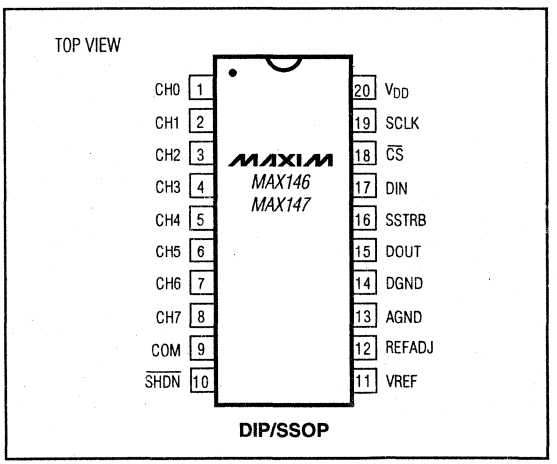
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX146AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX146BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX146AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX146BEAP	-40°C to +85°C	20 SSOP	±1
MAX146AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX146BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX147ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX147BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX147ACAP	0°C to +70°C	20 SSOP	±1/2
MAX147BCAP	0°C to +70°C	20 SSOP	±1
MAX147BC/D	0°C to +70°C	Dice*	±1
MAX147AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX147BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX147AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX147BEAP	-40°C to +85°C	20 SSOP	±1
MAX147AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX147BMJP	-55°C to +125°C	20 CERDIP**	±1

† *Contact factory for availability of alternate surface-mount packages.*

* *Dice are specified at T_A = +25°C, DC parameters only.*

** *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

_Pin Configuration



_Chip Information

TRANSISTOR COUNT: 2554

19-0464; Rev 1; 7/97

EVALUATION KIT AVAILABLE

MAXIM

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

General Description

The MAX148/MAX149 10-bit data-acquisition systems combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption. They operate from a single +2.7V to +5.25V supply, and sample to 133ksps. Both devices' analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™ and Microwire™ devices without external logic. A serial-strobe output allows direct connection to TMS320-family digital signal processors. The MAX148/MAX149 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX149 has an internal 2.5V reference, while the MAX148 requires an external reference. Both parts have a reference-buffer amplifier with a ±1.5% voltage-adjustment range.

These devices provide a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX148/MAX149, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current to under 60µA at reduced sampling rates.

The MAX148/MAX149 are available in a 20-pin DIP and a 20-pin SSOP.

For 4-channel versions of these devices, see the MAX1248/MAX1249 data sheet.

Applications

Portable Data Logging

Data Acquisition

Medical Instruments

Battery-Powered Instruments

Pen Digitizers

Process Control

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Single-Supply Operation: +2.7V to +5.25V (MAX148)**
- **Internal 2.5V Reference (MAX149)**
- **Low Power: 1.2mA (133ksps, 3V supply) 54µA (1ksps, 3V supply) 1µA (power-down mode)**
- **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **20-Pin DIP/SSOP Packages**

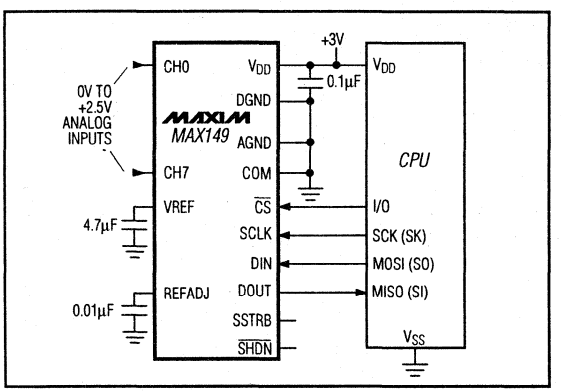
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX148ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX148BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX148ACAP	0°C to +70°C	20 SSOP	±1/2
MAX148BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

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+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to 6V
AGND to DGND ..... -0.3V to 0.3V
CH0–CH7, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF, REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to 6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C)* 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX148_C_P/MAX149_C_P ..... 0°C to +70°C
MAX148_E_P/MAX149_E_P ..... -40°C to +85°C
MAX148_MJP/MAX149_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at VREF pin; MAX148—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX14_A			±0.5	LSB
		MAX14_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX14_A		±0.15	±1	LSB
		MAX14_B		±0.15	±2	
Gain Error (Note 3)		MAX14_A			±1	LSB
		MAX14_B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at VREF pin; MAX148—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE (continued)						
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF / 2			±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX149 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C (Note 7)	2.470	2.500	2.530	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX149		±30		ppm/°C
Load Regulation (Note 8)		0mA to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 9)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
REFADJ Buffer-Disable Threshold			V_{DD} - 0.5			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference Buffer Gain		MAX149		2.06		V/V
		MAX148		2.00		
REFADJ Input Current		MAX149			±50	µA
		MAX148			±10	

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX149—4.7µF capacitor at VREF pin; MAX148—external reference, VREF = 2.500V applied to VREF pin; $T_A = T_{MIN}$ to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)							
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$		2.0			V
		$V_{DD} > 3.6V$		3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}					0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 10)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid Voltage	V_{SM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Input Low Voltage	V_{SL}					0.4	V
$\overline{SHDN}$ Input Current	I_S	$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = FLOAT			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = FLOAT				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 10)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input (Note 11)	V_{DD} = 5.25V		1.6	3.0	mA
			V_{DD} = 3.6V		1.2	2.0	
		Full power-down	V_{DD} = 5.25V		3.5	15	µA
			V_{DD} = 3.6V		1.2	10	
	I_{DD}	Fast power-down (MAX149)			30	70	
Supply Rejection (Note 12)	PSR	Full-scale input, external reference = 2.500V, V_{DD} = 2.7V to 5.25V			±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

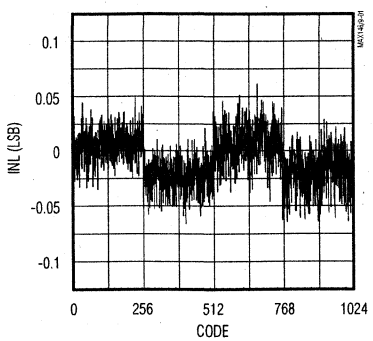
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX14_ _C/E	20		200	ns
			MAX14_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX149—internal reference, offset nulled; MAX148—external reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Sample tested to 0.1% AQL.
Note 8: External load should not change during conversion for specified accuracy.
Note 9: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 10: Guaranteed by design. Not subject to production testing.
Note 11: The MAX148 typically draws 400µA less than the values shown.
Note 12: Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

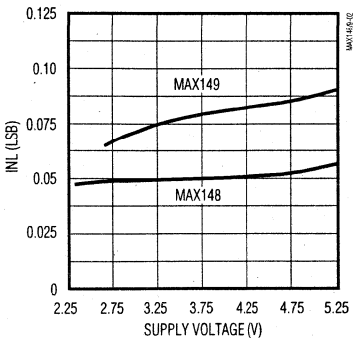
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

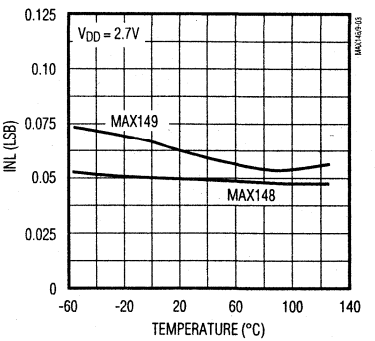
INTEGRAL NONLINEARITY vs. CODE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE

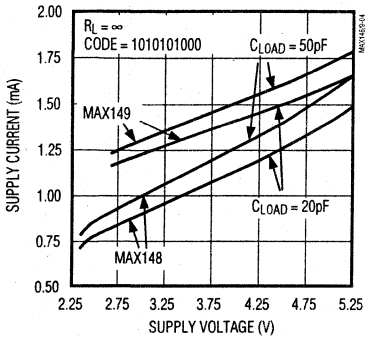


+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

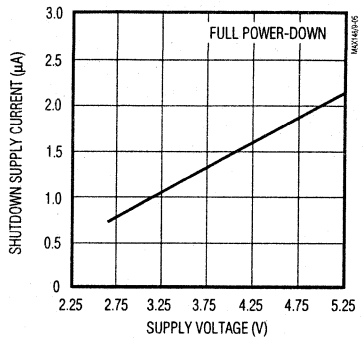
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

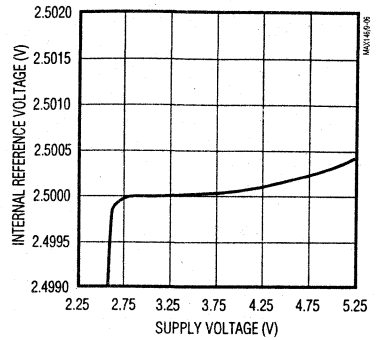
SUPPLY CURRENT vs. SUPPLY VOLTAGE



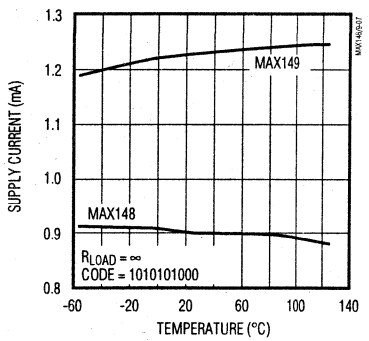
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



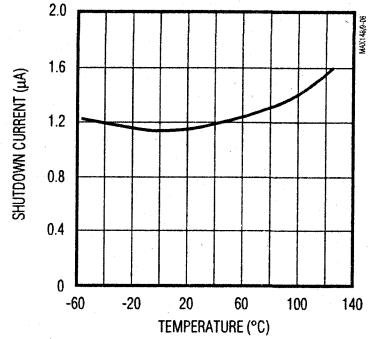
MAX149 INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



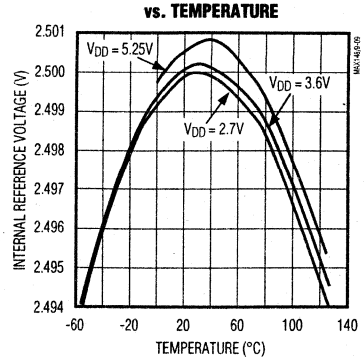
SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN CURRENT vs. TEMPERATURE



MAX149 INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	COM	Ground reference for analog inputs. COM sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX148/MAX149 down; otherwise, they are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX149 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
13	AGND	Analog Ground
14	DGND	Digital Ground
15	DOUT	Serial-Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX148/MAX149 begin the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)
20	V_{DD}	Positive Supply Voltage

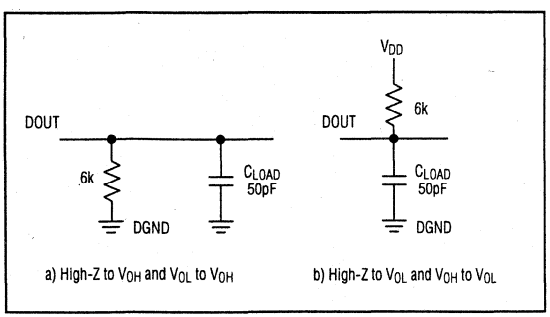


Figure 1. Load Circuits for Enable Time

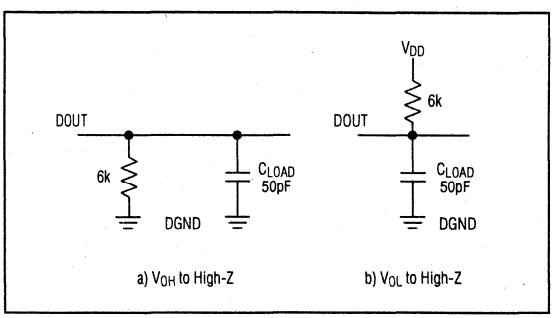


Figure 2. Load Circuits for Disable Time

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

Detailed Description

The MAX148/MAX149 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX148/MAX149.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH7, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels with Tables 2 and 3.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a 16pF x $[(V_{IN+}) - (V_{IN-})]$ charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be

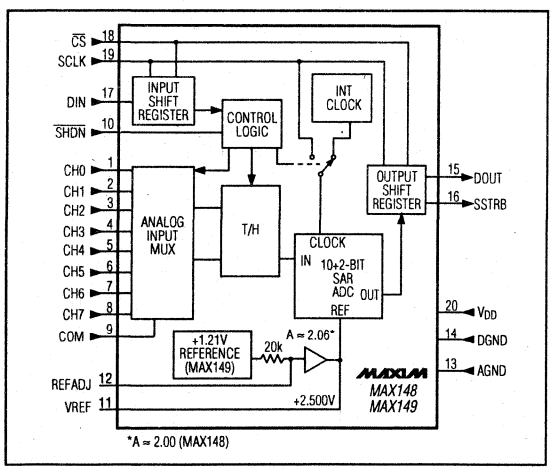


Figure 3. Block Diagram

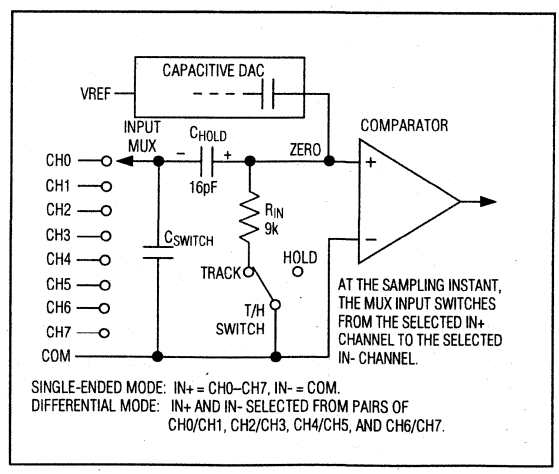


Figure 4. Equivalent Input Circuit

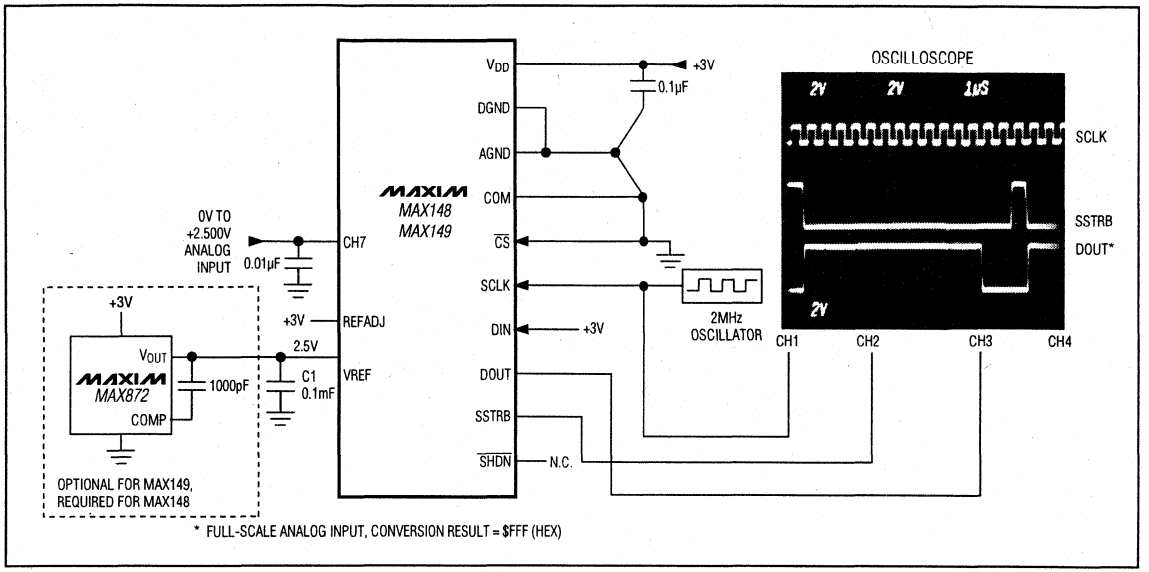


Figure 5. Quick-Look Circuit

allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

Quick Look

To quickly evaluate the MAX148/MAX149's analog performance, use the circuit of Figure 5. The MAX148/MAX149 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control bytes of $FF (HEX), which trigger single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result is shifted out of DOUT. Varying the analog input to CH7 will alter the sequence of bits from DOUT. A total of 15 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on the falling edge of SCLK.

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF/2 to +VREF/2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Full power-down 0 1 Fast power-down (MAX149 only) 1 0 Internal clock mode 1 1 External clock mode

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

How to Start a Conversion

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX148/MAX149's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX148/MAX149 are compatible with SPI/QSPI and Microwire devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the conversion result). See Figure 20 for MAX148/MAX149 QSPI connections.

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	−						
0	0	1			+	−				
0	1	0					+	−		
0	1	1							+	−
1	0	0	−	+						
1	0	1			−	+				
1	1	0					−	+		
1	1	1							−	+

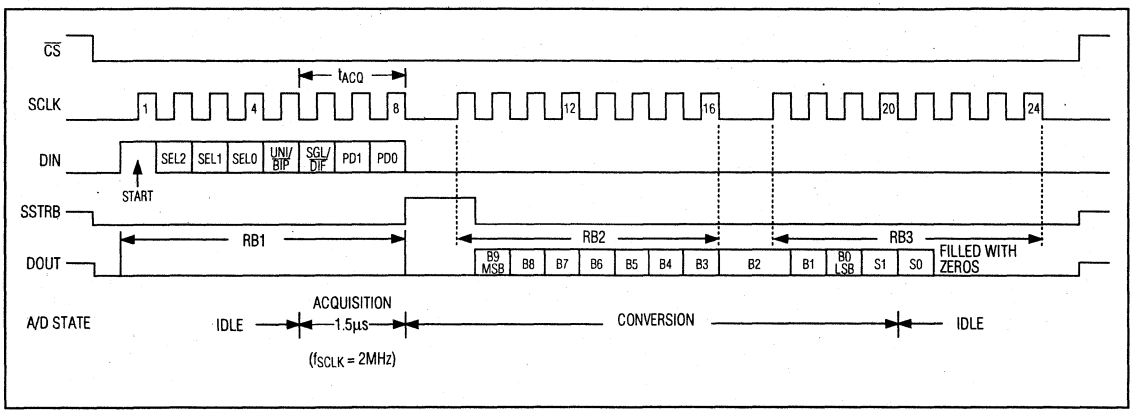


Figure 6. 24-Clock External Clock Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{SCLK} \leq$ 2MHz)

7

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with one leading zero, two sub-LSB bits, and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 17). For bipolar input mode, the output is twos complement (Figure 18). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX148/MAX149 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the

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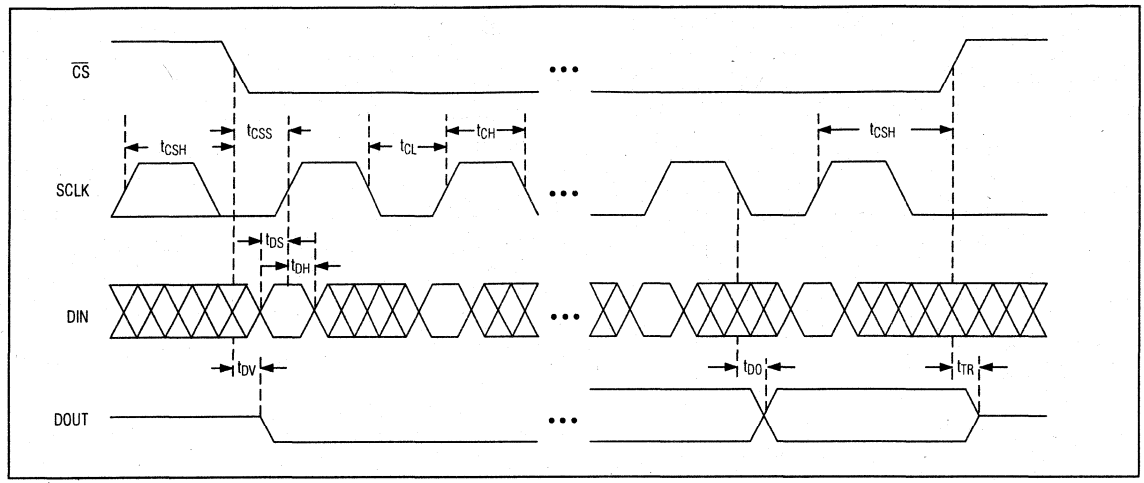

Figure 7. Detailed Serial-Interface Timing

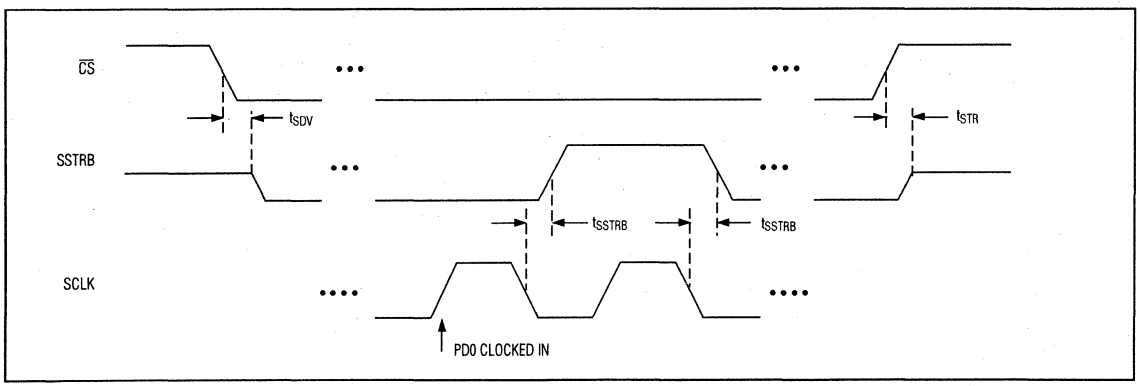

Figure 8. External Clock Mode SSTRB Detailed Timing

MAX148/MAX149. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX148/MAX149 generate their own conversion clocks internally. This frees the µP

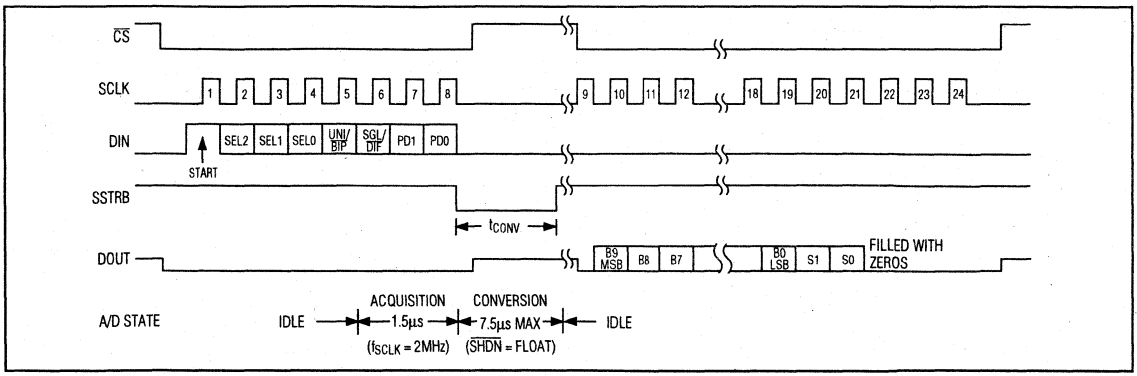

Figure 9. Internal Clock Mode Timing

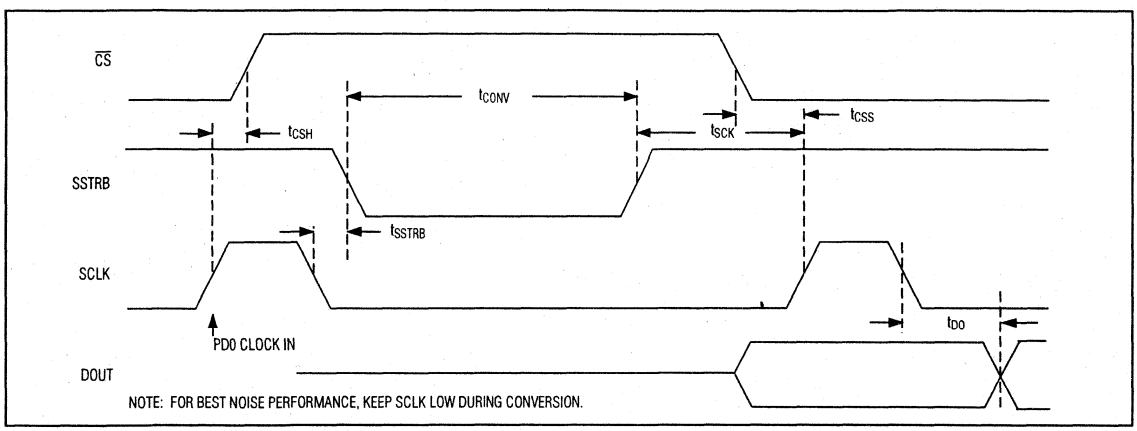

Figure 10. Internal Clock Mode SSTRB Detailed Timing

from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started.

Pulling $\overline{CS}$ high prevents data from being clocked into the MAX148/MAX149 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX148/MAX149 at clock rates exceeding 2.0MHz if the minimum acquisition time (t_{ACQ}) is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge, after the eighth

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Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast	See Figure 14c	133
Enabled	External	4.7	Full	See Figure 14c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle, e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX148/MAX149 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX148/MAX149. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX148/MAX149 in internal clock mode, ready to convert with SSTRB = high. After the power supplies stabilize, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. (Also see Table 4.)

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The100kHz minimum clock rate is limited by droop on the sample-and-hold and is independent of the compensation used.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at VREF. A 4.7µF value ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the *Choosing Power-Down Mode* section and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down mode or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current to 2µA (typ). Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up

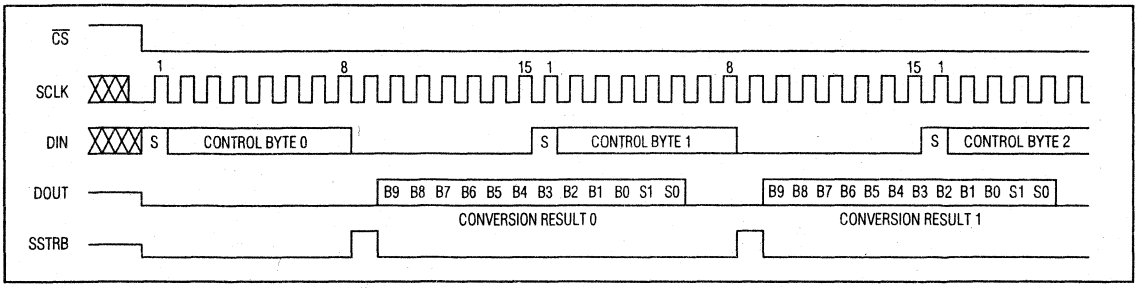

Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

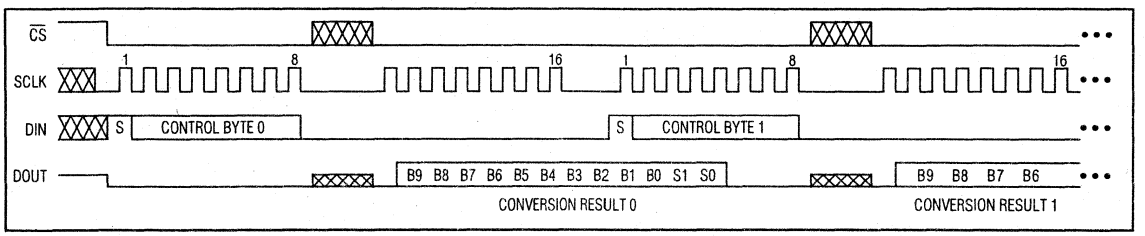

Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

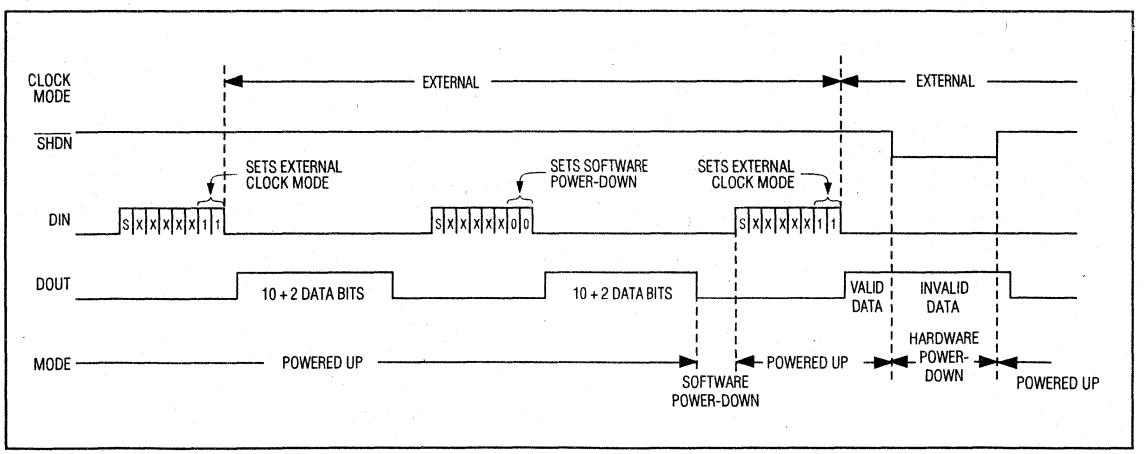

Figure 12a. Timing Diagram Power-Down Modes, External Clock

delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

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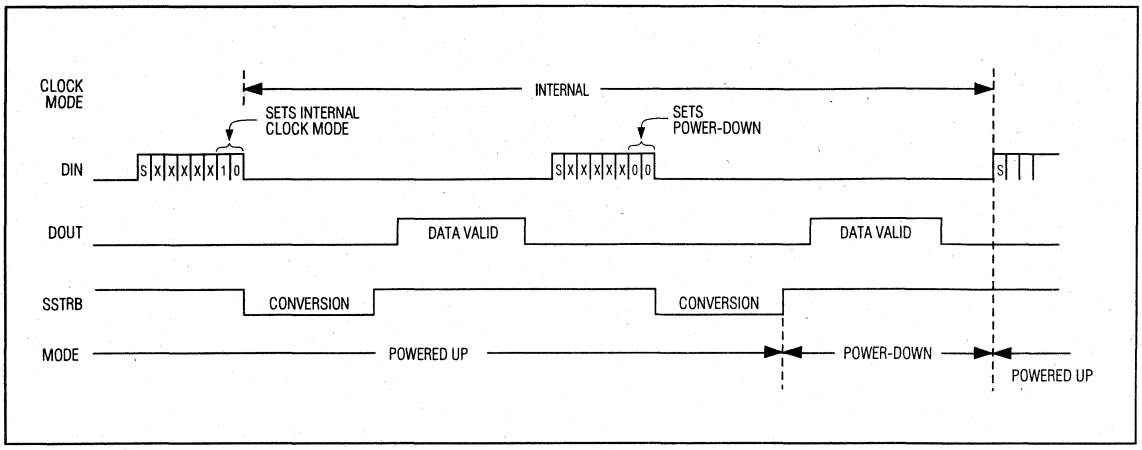


Figure 12b. Timing Diagram Power-Down Modes, Internal Clock

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

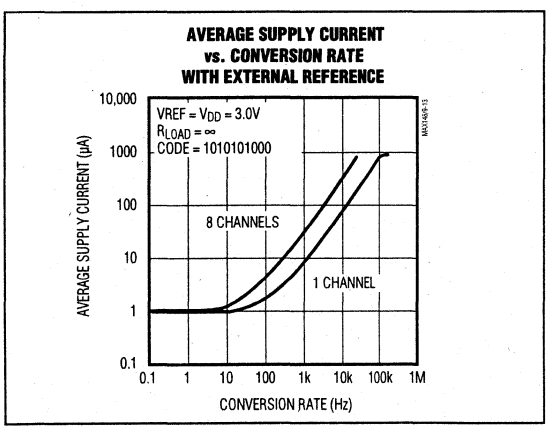


Figure 13. Average Supply Current vs. Conversion Rate with External Reference

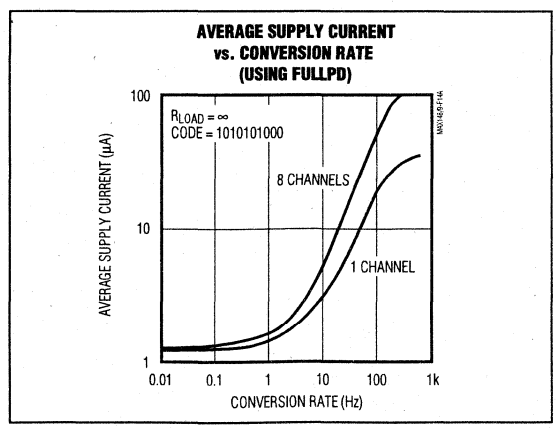


Figure 14a. MAX149 Supply Current vs. Conversion Rate, FULLPD

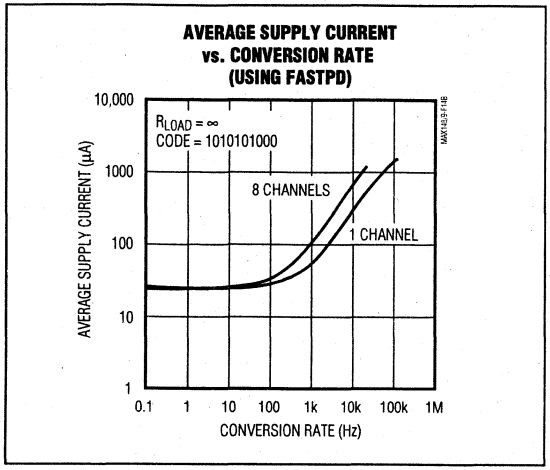


Figure 14b. MAX149 Supply Current vs. Conversion Rate, FASTPD

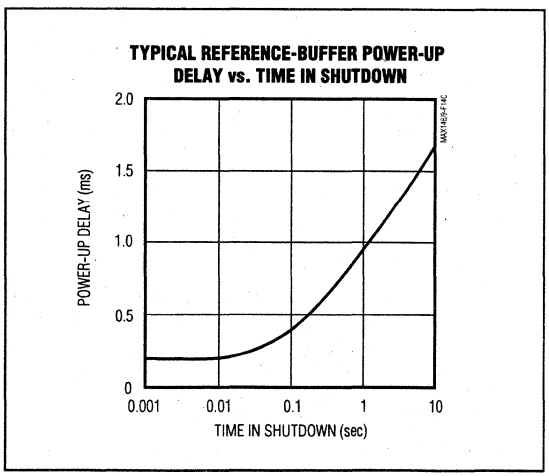


Figure 14c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX148/MAX149 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX148/MAX149. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX148/MAX149 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

Power-Down Sequencing

The MAX148/MAX149 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 13, 14a, and 14b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples show two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 14a depicts the MAX149 power consumption for one or eight channel conversions utilizing full power-down mode and internal-reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 8 time constants or 1.6ms are required after power-up. Waiting this 1.6ms in FASTPD mode instead of in full power-up can reduce power consumption by a factor

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

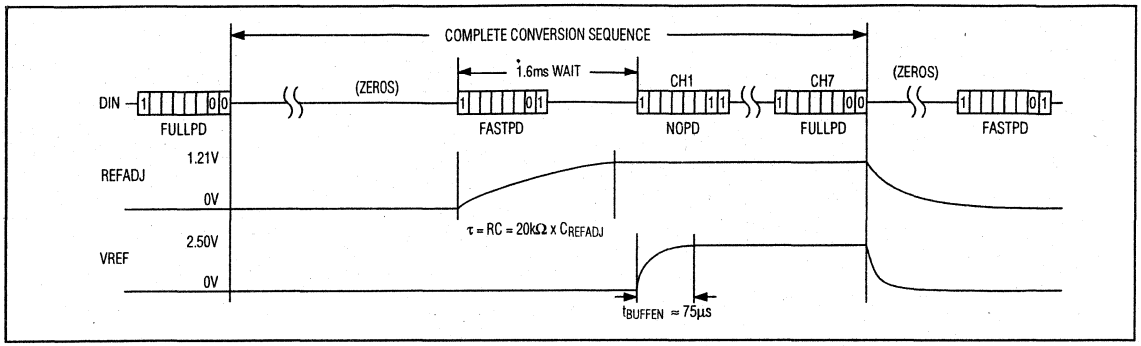


Figure 15. MAX149 FULLPD/FASTPD Power-Up Sequence

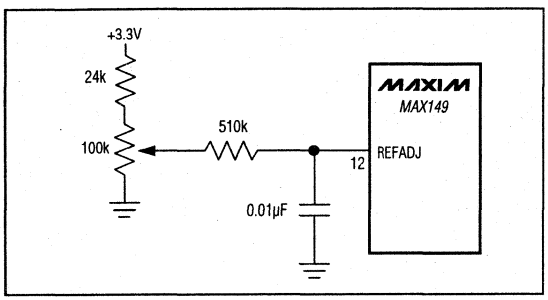


Figure 16. MAX149 Reference-Adjust Circuit

of 10 or more. This is achieved by using the sequence shown in Figure 15.

Lowest Power at Higher Throughputs

Figure 14b shows the power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 75µs wait after power-up with one dummy conversion. This graph shows fast multi-channel conversion with the lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX148/MAX149 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX149 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX148. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX149 and the MAX148. The MAX149's internally trimmed 1.21V reference is buffered with a 2.06 gain. The MAX148's REFADJ pin is also buffered with a 2.00 gain to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

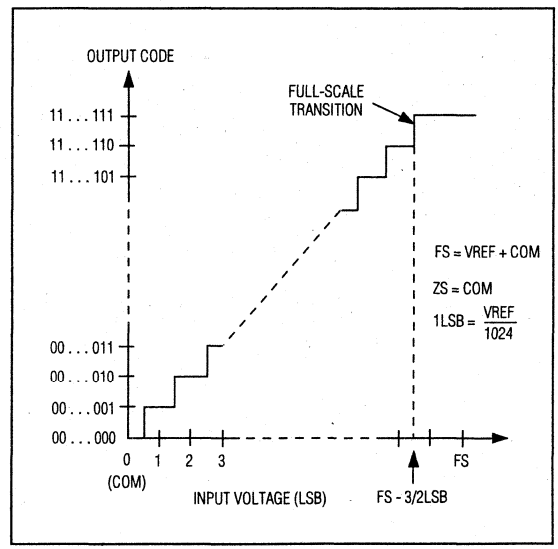


Figure 17. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

Internal Reference (MAX149)

The MAX149's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit in Figure 16.

External Reference

With both the MAX149 and MAX148, an external reference can be placed at either the input (REFADJ) or the

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

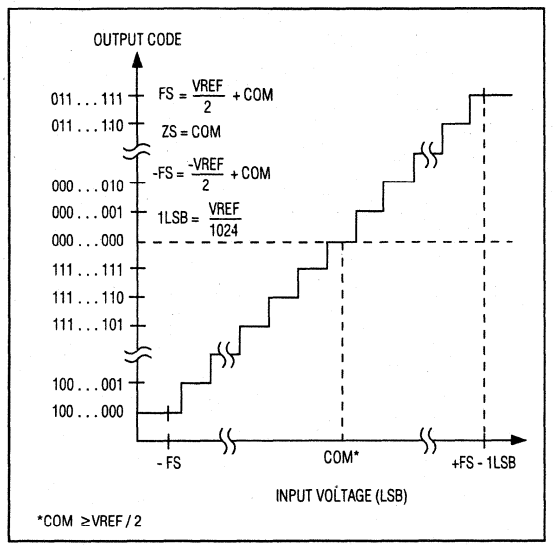


Figure 18. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

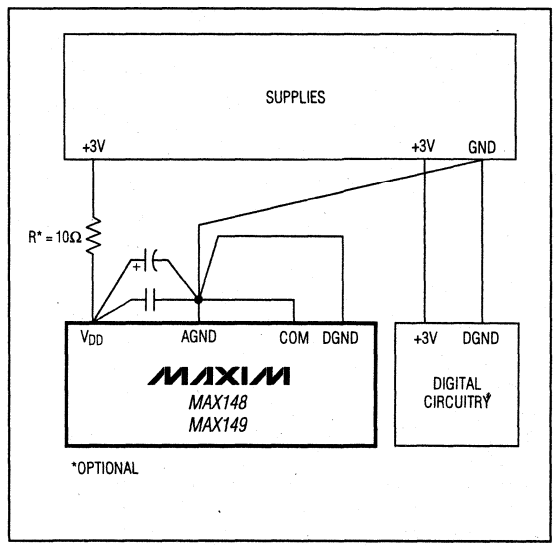


Figure 19. Power-Supply Grounding Connection

output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX149, and higher than 100kΩ for the MAX148. At VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ is typically 25µA (MAX149) with REFADJ tied to V_{DD}. Pull REFADJ to AGND to minimize the input bias current in power-down.

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1LSB over the 0°C to +70°C commercial temperature range.

Figure 17 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 18 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 2.44mV (2.500V / 1024) for unipolar operation, and 1LSB = 2.44mV [(2.500V / 2 - -2.500V / 2) / 1024] for bipolar operation.

+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

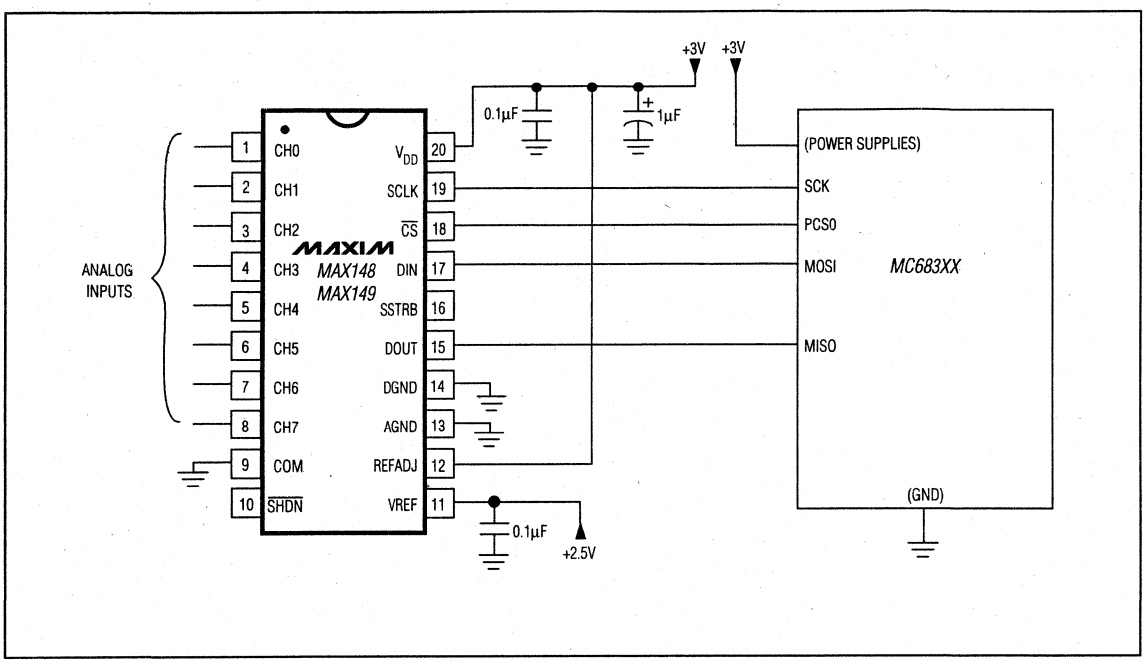


Figure 20. MAX148/MAX149 QSPI Connections, External Reference

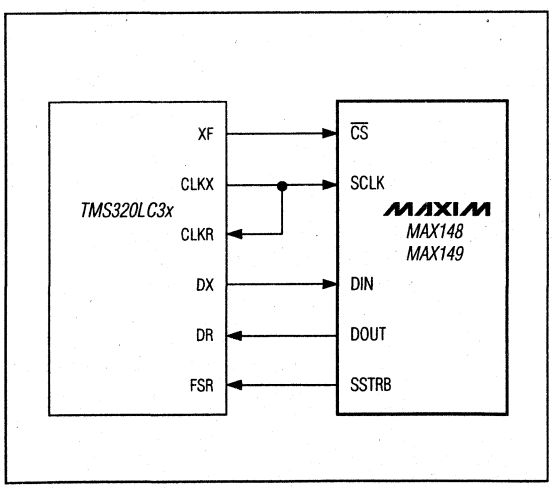


Figure 21. MAX148/MAX149-to-TMS320 Serial Interface

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 19 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 20 of the MAX148/MAX149. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 19).

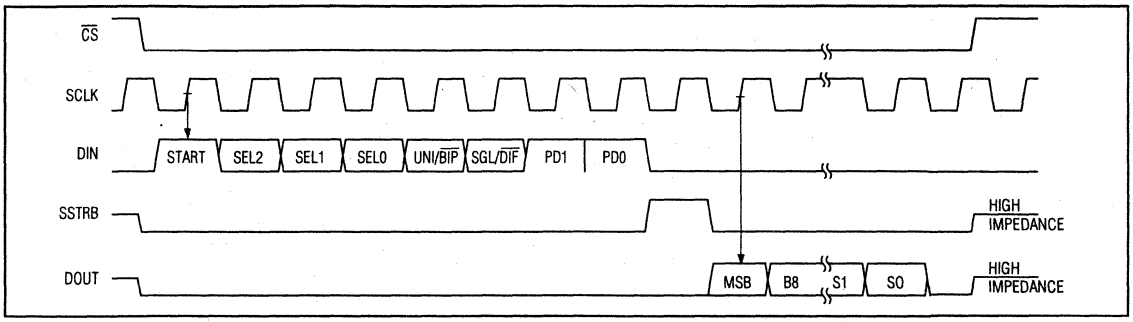


Figure 22. TMS320 Serial-Interface Timing Diagram

High-Speed Digital Interfacing with QSPI

The MAX148/MAX149 can interface with QSPI using the circuit in Figure 20 (f_{SCLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the eight channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

The MAX148/MAX149 are QSPI compatible up to the maximum external clock frequency of 2MHz.

TMS320LC3x Interface

Figure 21 shows an application circuit to interface the MAX148/MAX149 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 22.

Use the following steps to initiate a conversion in the MAX148/MAX149 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX148/MAX149's SCLK input.
2) The MAX148/MAX149's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX148/MAX149's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX148/MAX149 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX148/MAX149's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX148/MAX149.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10 + 2-bit conversion result followed by 4 trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX148/MAX149 until the next conversion is initiated.

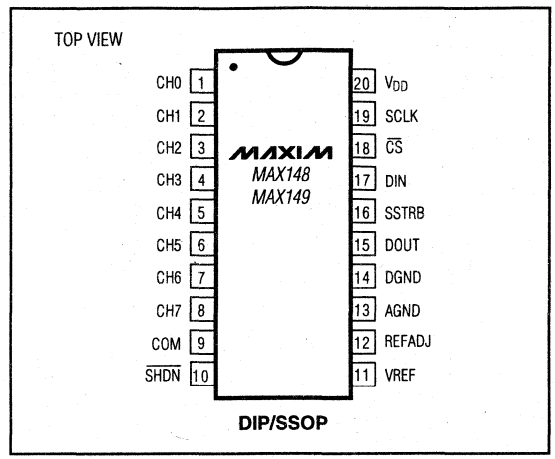
+2.7V, Low-Power, 8-Channel, Serial 10-Bit ADCs

_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX148AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX148BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX148AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX148BEAP	-40°C to +85°C	20 SSOP	±1
MAX148AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX148BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX149ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX149BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX149ACAP	0°C to +70°C	20 SSOP	±1/2
MAX149BCAP	0°C to +70°C	20 SSOP	±1
MAX149AEPP	-40°C to +85°C	20 Plastic DIP*	±1/2
MAX149BEPP	-40°C to +85°C	20 Plastic DIP*	±1
MAX149AEAP	-40°C to +85°C	20 SSOP*	±1/2
MAX149BEAP	-40°C to +85°C	20 SSOP*	±1
MAX149AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX149BMJP	-55°C to +125°C	20 CERDIP**	±1

† *Contact factory for availability of alternate surface-mount packages.*
* *Contact factory for availability.*
** *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

Pin Configuration



Chip Information

TRANSISTOR COUNT: 2554

19-1270; Rev 0; 7/97

EVALUATION KIT AVAILABLE

MAXIM

Low-Power, 60Msps, Dual, 6-Bit ADC

General Description

The MAX1002 is a dual, 6-bit analog-to-digital converter (ADC) that combines high-speed, low-power operation with a user-selectable input range, an internal reference, and a clock oscillator. The dual, parallel ADCs are designed to convert in-phase (I) and quadrature (Q) analog signals into two 6-bit offset-binary-coded digital outputs at sampling rates up to 60Msps while achieving typical integral nonlinearity (INL) and differential nonlinearity (DNL) of ±1/4LSB. The ability to interface directly with baseband I and Q signals makes the MAX1002 ideal for use in direct-broadcast satellite, VSAT, and QAM16 demodulation applications.

The MAX1002 input amplifiers feature true differential inputs, a 55MHz -0.5dB analog bandwidth, and user-programmable input full-scale ranges of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled input signal, matching performance between input channels is typically 0.1dB gain, 1/4LSB offset, and 0.5° phase. Dynamic performance is 5.85 effective number of bits (ENOB) with a 20MHz analog input signal, or 5.78 ENOB with a 50MHz input signal.

The MAX1002 operates with a single +5V power supply and provides TTL-compatible digital outputs. The device is available in the commercial temperature range (0°C to +70°C) and comes in a 36-pin SSOP package.

Applications

Direct Broadcast Satellite (DBS) Receivers
VSAT Receivers
Wide Local Area Networks (WLAN)
Cable Television Set-Top Boxes

Features

- ±1/4LSB INL and DNL, Typical
- 1/4LSB (typ) Channel-to-Channel Offset Matching
- 0.1dB Gain and 0.5° Phase Matching, Typical
- Internal Bandgap Voltage Reference
- Two Matched 6-Bit, 60Msps ADCs
- Excellent Dynamic Performance:
  5.85 ENOB with 20MHz Analog Input
  5.7 ENOB with 50MHz Analog Input
- Internal Oscillator with Overdrive Capability
- 55MHz (-0.5dB) Bandwidth Input Amplifiers with True Differential Inputs
- User-Selectable Input Full-Scale Range (125mVp-p, 250mVp-p, or 500mVp-p)
- Single-Ended or Differential Input Drive
- +5V Single Supply
- TTL Outputs
- 90Msps Upgrade with +3.3V CMOS-Compatible Output Available (MAX1003)

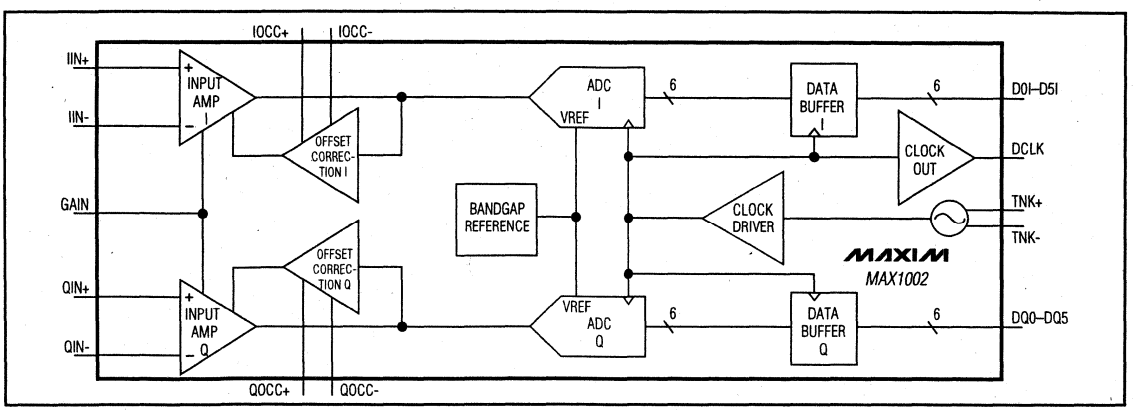
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1002CAX	0°C to +70°C	36 SSOP

Pin Configuration appears at end of data sheet.

7

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Power, 60Msps, Dual, 6-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6.5V
V_{CCO} to OGND.....-0.3V, +6.5V
GND to OGND .....-0.3V, +0.3V
Digital and Clock Output Pins to OGND .....-0.3V, V_{CCO} (<10sec)
All Other Pins to GND.....-0.3V, V_{CC}

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 45mW/°C above +70°C) 941mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, <10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC}, V_{CCO} = +5V ±5%; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	RES		6			Bits
Integral Nonlinearity	INL		-0.5	±0.25	0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-0.5	±0.25	0.5	LSB
Full-Scale Input Range	V_{FSH}	GAIN = V_{CC} (high gain)	118.75	125	131.25	mVp-p
	V_{FSM}	GAIN = open (mid gain)	237.5	250	262.5	
	V_{FSL}	GAIN = GND (low gain)	475	500	525	
INVERTING AND NONINVERTING ANALOG INPUTS						
Input Open-Circuit Voltage	V_{AOC}		2.25	2.35	2.45	V
Input Resistance	R_{IN}		13	20	29	kΩ
Input Capacitance	C_{IN}	Guaranteed by design		3	5	pF
Common-Mode Voltage Range	V_{CM}	Other analog input driven with external source (Note 2)	1.75		2.75	V
OSCILLATOR INPUTS						
Oscillator Input Resistance	R_{OSC}	Other oscillator input tied to V_{CC} + 0.3V	4.8	8	12.1	kΩ
DIGITAL OUTPUTS (DI0–DI5, DQ0–DQ5)						
Digital Outputs Logic-High Voltage	V_{OH}	I_{SOURCE} = 50µA	2.4			V
Digital Outputs Logic-Low Voltage	V_{OL}	I_{SINK} = 400µA			0.5	V
POWER SUPPLY						
Supply Current	I_{CC}			63	104	mA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.75V to 5.25V (Note 3)		-75	-40	dB
Digital Outputs Supply Current	I_{CCO}	20MHz, FS I & Q analog inputs, C_{LOAD} = 15pF (Note 4)			24	mA
Power Dissipation	PD			380		mW

AC ELECTRICAL CHARACTERISTICS

(V_{CC}, V_{CCO} = +5V ±5%; T_A = +25°C; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (GAIN = open; external 60MHz clock (Figure 7); V_{INI}, V_{INIQ} = 20MHz sine; amplitude -1dB below FS; unless otherwise noted.)						
Maximum Sample Rate	f_{MAX}		60			Msps
Analog Input -0.5dB Bandwidth	BW	Gain = GND, open, V_{CC}		55		MHz
Effective Number of Bits	$ENOB_M$	GAIN = open (mid gain)	5.6	5.85		Bits
		GAIN = open (mid gain), V_{IN} = 50MHz, -1dB below FS		5.7		
	$ENOB_H$	Gain = V_{CC} (high gain)		5.8		
	$ENOB_L$	Gain = V_{CC} (low gain)		5.85		
Signal-to-Noise and Distortion Ratio	SINAD	Gain = open (mid gain)	35.4	37		dB
Input Offset (Note 5)	OFF	I channel	-0.5		0.5	LSB
		Q channel	-0.5		0.5	
Crosstalk Between ADCs	XTLK			-55		dB
Offset Mismatch Between ADCs	OMM2	(Note 5)	-0.5	±0.25	0.5	LSB
Amplitude Match Between ADCs	AM		-0.2	±0.1	0.2	dB
Phase Match Between ADCs	PM		-2	±0.5	2	degrees
TIMING CHARACTERISTICS (data outputs: R_L = 1MΩ, C_L = 15pF, Figure 8)						
DCLK to Data-Propagation Delay	t_{PD}	(Note 6)		7.1		ns
Data Valid Skew	t_{SKEW}	(Note 6)		3.6		ns
Input to DCLK Delay	t_{DCLK}	TNK+ to DCLK (Note 6)		5.3		ns
Aperture Delay	t_{AP}			5.5		ns
Pipeline Delay	PD			1		clock cycle

Note 1: Best straight-line linearity method.

Note 2: A typical application will AC couple the analog input to the DC bias level present at the analog inputs (typically 2.35V). However, it is also possible to DC couple the analog input (using differential or single-ended drive) within this common-mode input range (Figures 4, 5).

Note 3: PSSR is defined as the change in the mid-gain, full-scale range as a function of the variation in V_{CC} supply voltage (expressed in decibels).

Note 4: The current in the V_{CCO} supply is a strong function of the capacitive loading on the digital outputs. To minimize supply transients and achieve the best dynamic performance, reduce the capacitive loading effects by keeping line lengths on the digital outputs to a minimum.

Note 5: Offset-correction compensation enabled, 0.22µF at Q and I compensation inputs (Figures 2, 3).

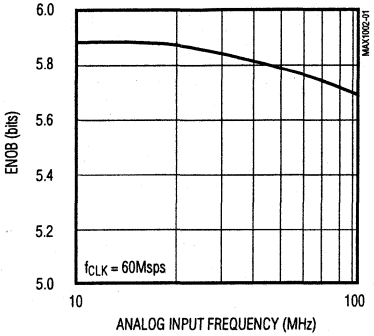
Note 6: t_{PD} and t_{SKEW} are measured from the 1.4V level of the output clock, to the 1.4V level of either the rising or falling edge of a data bit. t_{DCLK} is measured from the 50% level of the clock overdrive signal on TNK+ to the 1.4V level of D_{CLK}. The capacitive load on the outputs is 15pF.

Low-Power, 60Msps, Dual, 6-Bit ADC

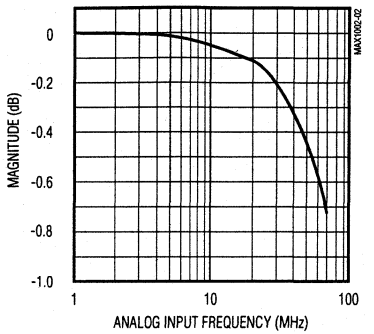
Typical Operating Characteristics

(V_{CC}, V_{CCO} = +5V ±5%; MAX1002/MAX1003 evaluation kit; T_A = +25°C; unless otherwise noted.)

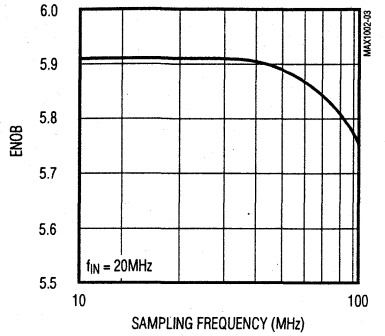
EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY



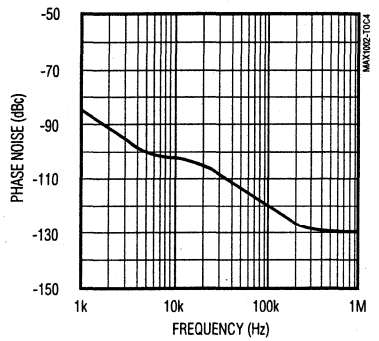
ANALOG INPUT BANDWIDTH



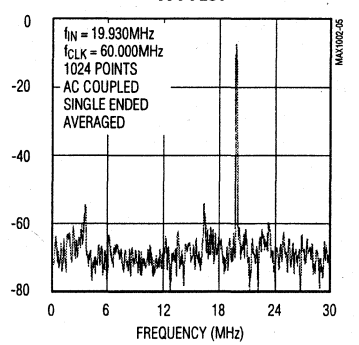
EFFECTIVE NUMBER OF BITS vs. SAMPLING FREQUENCY



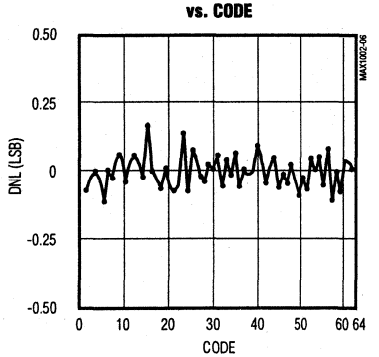
OPEN-LOOP PHASE NOISE vs. FREQUENCY



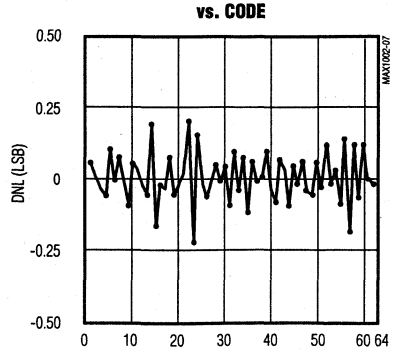
FFT PLOT



DIFFERENTIAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



Pin Description

PIN	NAME	FUNCTION
1	GAIN	Gain-Select Input. Sets input full-scale range: 125/250/500mVp-p (Table 1).
2	IOCC+	Positive I-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
3	IOCC-	Negative I-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
4	IIN+	I-Channel Noninverting Analog Input
5	IIN-	I-Channel Inverting Analog Input
6	VCC	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 7).
7, 11, 12, 18, 19	GND	Analog Ground
8	VCC	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 11).
9	TNK+	Positive Oscillator/Clock Input
10	TNK-	Negative Oscillator/Clock Input
13	VCC	+5V ±5% Supply. Bypass with 0.01µF capacitor to GND (Pin 12).
14	QIN-	Q-Channel Inverting Analog Input
15	QIN+	Q-Channel Noninverting Analog Input
16	QOCC-	Negative Q-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
17	QOCC+	Positive Q-Channel Offset-Correction Compensation. Connect 0.22µF capacitor for AC-coupled inputs (Figures 2, 3). Ground for DC-coupled inputs (Figures 4, 5).
20–25	DQ5–DQ0	Q-Channel Digital Outputs 0–5. DQ5 is the most significant bit (MSB).
26, 28	VCCO	+5V ±5% Digital Supply. Bypass each with 47pF to OGND (Pin 27).
27	OGND	Digital Output Ground
29	DCLK	Digital Clock Output. Frames the output data.
30–35	DI0–DI5	I-Channel Digital Outputs 0–5. DI5 is the most significant bit (MSB).
36	VCC	+5V ±5% Supply. Bypass with 0.01µF to GND (Pin 19).

Detailed Description

Converter Operation

The MAX1002 contains two 6-bit analog-to-digital converters (ADCs), a buffered voltage reference, and oscillator circuitry. The ADCs use a flash-conversion technique to convert an analog input signal into a 6-bit parallel digital output code. The MAX1002's unique design includes 63 fully differential comparators and a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. The control logic interfaces easily to most digital signal processors (DSPs) and microprocessors (µPs) with +5V CMOS-compatible logic interfaces. Figure 1 shows the MAX1002 in a typical application.

Programmable Input Amplifiers

The MAX1002 has in-phase (I) and quadrature (Q) programmable-gain input amplifiers with a 55MHz -0.5dB bandwidth and true differential inputs. To maximize performance in high-speed systems, each amplifier has less than 5pF of input capacitance. The input amplifier gain is programmed via the GAIN pin to provide three possible input full-scale ranges (FSR) (Table 1).

Table 1. Input Amplifier Programming

GAIN	INPUT FULL-SCALE RANGE (mVp-p)
GND	500
Open	250
VCC	125

Low-Power, 60Msps, Dual, 6-Bit ADC

Figures 2 and 3 show single-ended and differential AC-coupled input circuits. Each of the amplifier inputs is internally biased to a 2.35V reference through a 20kΩ resistor, eliminating external DC bias circuits. A series 0.1µF capacitor is required at each amplifier input for AC-coupled signals.

When operating with AC-coupled inputs, the input amplifiers' DC offset voltage is nulled to within ±1/2LSB by an on-chip offset-correction amplifier. An external compensation capacitor is required to set the dominant pole of the offset-correction amplifier's frequency response (Figures 2 and 3). The compensation capacitor determines the low-frequency corner of the analog input response according to the following formula:

$$f_C = 1 / (0.1 \times C)$$

where C is the value of the compensation capacitor in µF, and fc is the corner frequency in Hz.

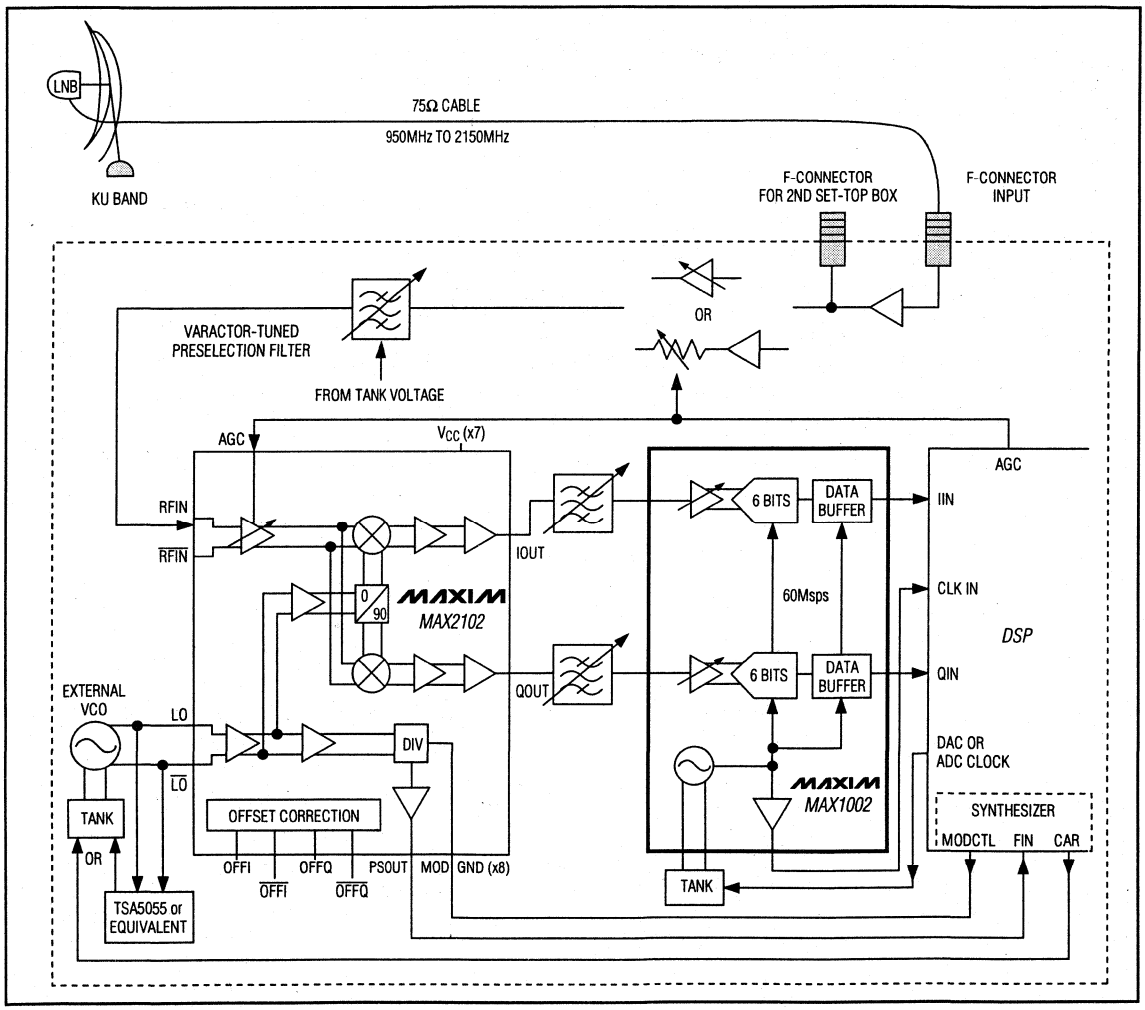


Figure 1. Commercial Satellite Receiver System

Figures 4 and 5 show single-ended and differential DC-coupled input circuits for applications where a DC component of the input signal is present. The amplifiers' input common-mode voltage range extends from 1.75V to 2.75V. To prevent attenuation of the input signal's DC component when operating in this mode, disable the offset-correction amplifier by grounding the _OCC+ and _OCC- pins for the I and Q blocks (Figures 4 and 5).

ADCs

The I and Q ADC blocks receive the analog signals from the respective I and Q input amplifiers. The ADCs use flash conversion with 63 fully differential comparators to digitize the analog input signal into a 6-bit output in offset binary format.

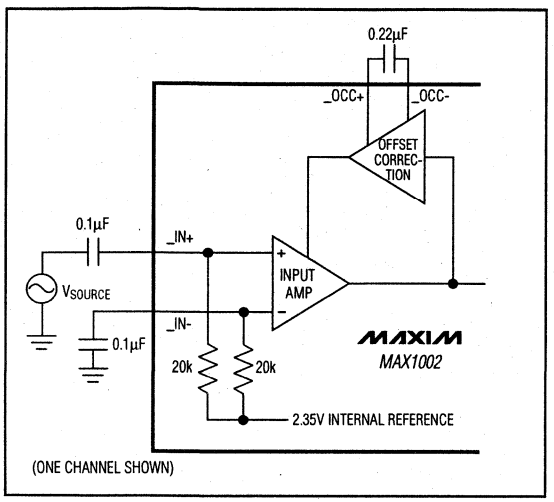


Figure 2. Single-Ended AC-Coupled Input

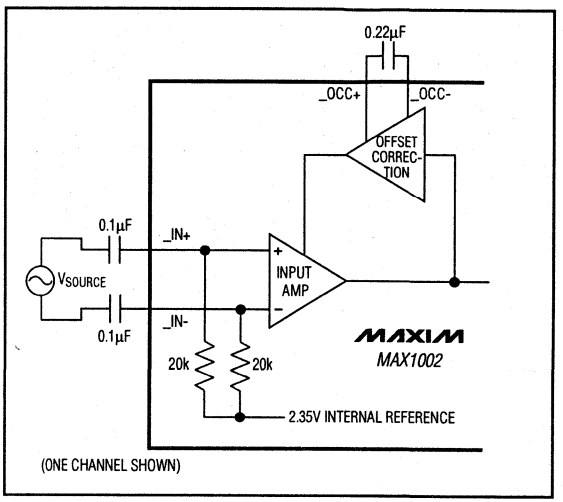


Figure 3. Differential AC-Coupled Input

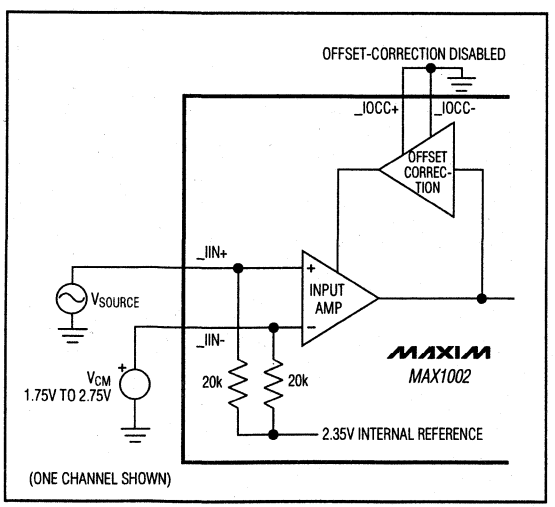


Figure 4. Single-Ended DC-Coupled Input

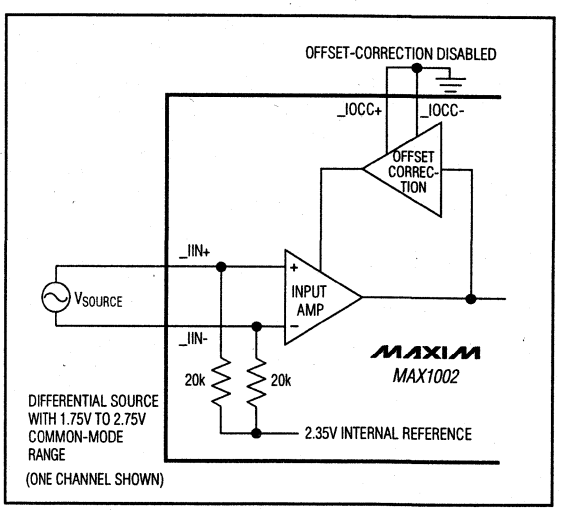


Figure 5. Differential DC-Coupled Input

Low-Power, 60Msps, Dual, 6-Bit ADC

The MAX1002 features a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. Dynamic encoding errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for typical converters can be incorrect, including false full- or zero-scale outputs. The MAX1002's unique design reduces the magnitude of this type of error to 1LSB.

Internal Voltage Reference

An internal buffered bandgap reference is included on the MAX1002 to drive the ADC's reference ladders. The on-chip reference and buffer eliminate any external (high-impedance) connections to the reference ladder, minimizing the potential for noise coupling from external circuitry while ensuring that the voltage reference, input amplifier, and reference ladder track well with variations in temperature and power supplies.

Oscillator Circuit

The MAX1002 includes a differential oscillator, which is controlled by an external parallel resonant (tank) network (Figure 6). As an alternative, the oscillator may be overdriven with an external clock source (Figure 7).

Internal-Clock Operation (Tank)

If the tank circuit is used, the resonant inductor should have a sufficiently high Q and a self-resonant frequency (SRF) of at least twice the intended oscillator frequency. Coilcraft's 1008HS-221, with a 700MHz SRF and a Q of 45, works well for this application. Generate different clock-frequency ranges by adjusting varactor and tank elements.

An internal-clock-driver buffer is included to provide sharp clock edges to the internal flash comparators. The buffer ensures that the comparators are simultaneously clocked, maximizing the ADC's effective number of bits of performance.

External-Clock Operation

To accommodate designs that use an external clock, the MAX1002's internal oscillator can be overdriven by an external clock source (Figure 7). The external clock source should be a sinusoid to minimize clock-phase noise and jitter, which can degrade the ADC's effective bits performance. AC couple the clock source (recommended voltage level is approximately 1Vp-p) to the oscillator inputs (Figure 7).

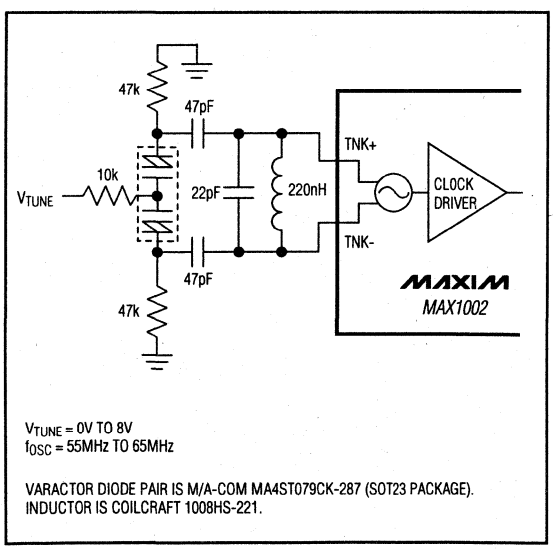


Figure 6. Tank-Resonator Oscillator

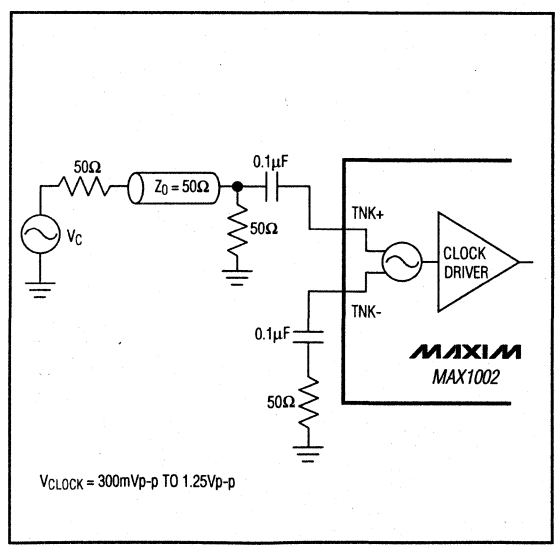


Figure 7. External-Clock-Drive Circuit

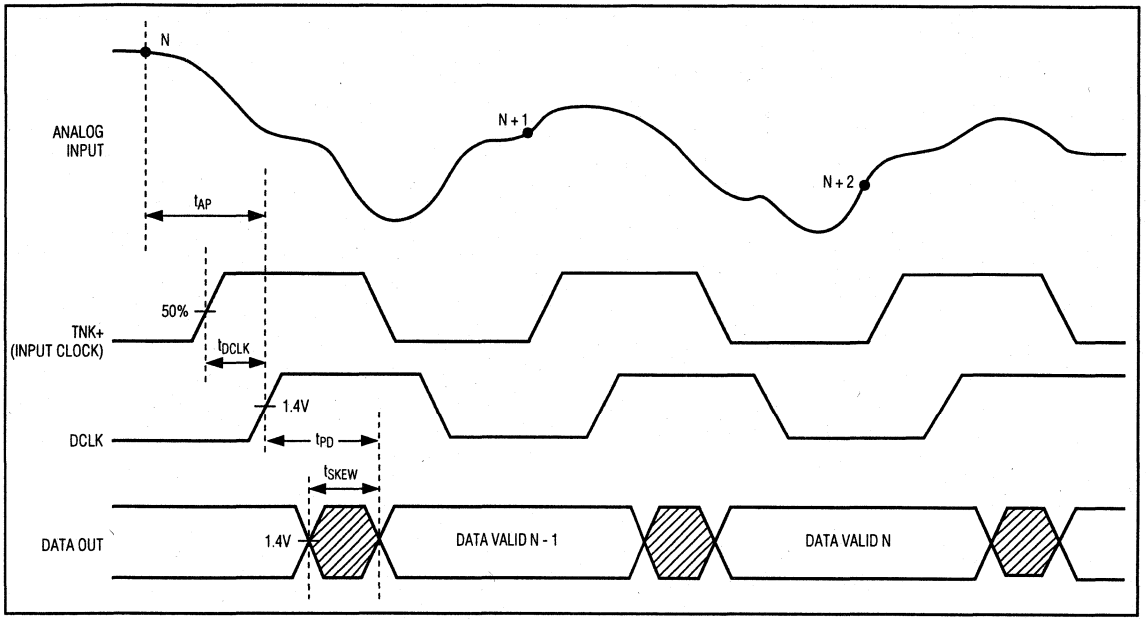


Figure 8. MAX1002 Timing Diagram

Output Data Format

The conversion results are output on a dual 6-bit-wide data bus. Data is latched into the ADC output latch following a pipeline delay of one clock cycle (Figure 8). Output data is clocked out of the respective ADC's data-output pins (D_0 through D_5) on the rising edge of the clock output (DCLK), with a DCLK-to-data propagation delay (t_{PD}) of 7.1ns. The MAX1002 outputs are TTL compatible.

Transfer Function

Figure 9 shows the MAX1002's nominal transfer function. Output coding is offset binary with 1LSB = FSR / 63.

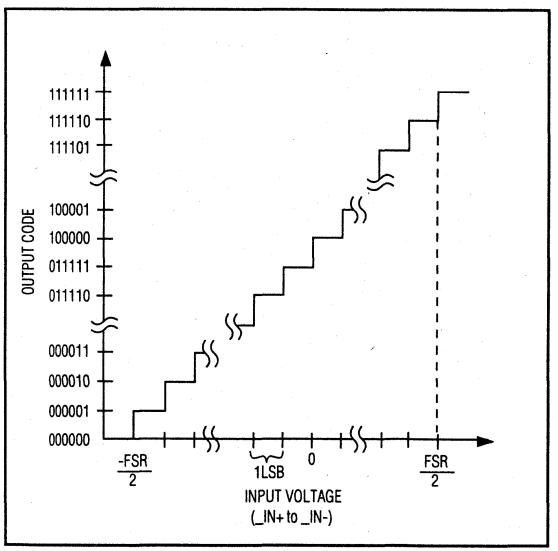


Figure 9. Ideal Transfer Function

Low-Power, 60Msps, Dual, 6-Bit ADC

Applications Information

Layout, Grounding, and Bypassing

The MAX1002 is designed with separate analog and digital power-supply and ground connections to isolate high-current digital noise spikes from the more sensitive analog circuitry. The high-current digital output ground (OGND) and analog ground (GND) should be at the same DC level, connected at only one location on the board. This provides best noise immunity and improved conversion accuracy. Use of separate ground planes is strongly recommended.

The entire board requires good DC bypassing for both analog and digital supplies. Place the bypass capacitors close to where the power is routed onto the board, i.e., close to the connector. 10µF electrolytic capacitors with low ESR-ratings are recommended. For best effective bits performance, minimize capacitive loading at the digital outputs. Keep the digital output traces as short as possible.

The MAX1002 can operate with one +5V supply. For optimum performance, separate +5V ±5% supplies and bypassing are recommended. Bypass each of the V_{CC} supply pins to its respective GND with high-quality ceramic capacitors located as close to the package as possible (Table 2). Consult the evaluation kit for a suggested layout and bypassing scheme.

Table 2. Bypassing

SUPPLY FUNCTION	V_{CC} / V_{CCO}	BYPASS TO GND/OGND	CAPACITOR VALUE
Analog Inputs	6	7	0.01µF
Oscillator/Clock	8	11	0.01µF
Converter	13	12	0.01µF
Digital Q Output	26	27	47pF
Digital I Output	28	27	47pF
Buffer	36	19	0.01µF

Dynamic Performance

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

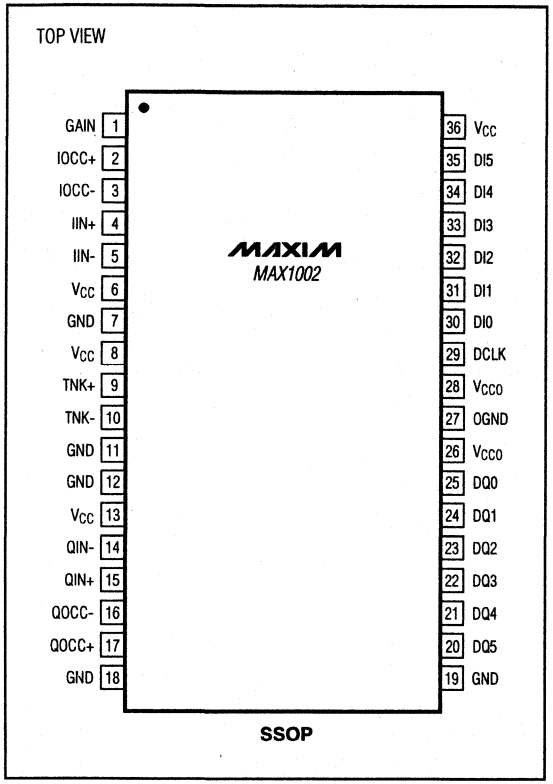
The theoretical minimum A/D noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 6-bit ADC can do no better than 38dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 20MHz sinusoid at a 60MHz clock rate. This FFT plot of the output shows the output level in various spectral bands. The plot has been averaged to reduce the quantization noise floor and reveal the low-amplitude spurs. This emphasizes the excellent spurious-free dynamic range of the MAX1002.

The effective resolution (or ENOB) the ADC provides can be measured by transposing the equation that converts resolution to SNR: N = (SINAD - 1.76) / 6.02 (see *Typical Operating Characteristics).*

Low-Power, 60Msps, Dual, 6-Bit ADC

Pin Configuration



Chip Information

TRANSISTOR COUNT: 6097

7

19-1236; Rev 0; 6/97

EVALUATION KIT AVAILABLE

MAXIM

Low-Power, 90Msps, Dual 6-Bit ADC

General Description

The MAX1003 is a dual, 6-bit analog-to-digital converter (ADC) that combines high-speed, low-power operation with a user-selectable input range, an internal reference, and a clock oscillator. The dual parallel ADCs are designed to convert in-phase (I) and quadrature (Q) analog signals into two 6-bit, offset-binary-coded digital outputs at sampling rates up to 90Msps. The ability to directly interface with baseband I and Q signals makes the MAX1003 ideal for use in direct-broadcast satellite, VSAT, and QAM16 demodulation applications.

The MAX1003 input amplifiers feature true differential inputs, a -0.5dB analog bandwidth of 55MHz, and user-programmable input full-scale ranges of 125mVp-p, 250mVp-p, or 500mVp-p. With an AC-coupled input signal, matching performance between input channels is typically better than 0.1dB gain, 1/4LSB offset, and 0.5° phase. Dynamic performance is 5.85 effective number of bits (ENOB) with a 20MHz analog input signal, or 5.7 ENOB with a 50MHz signal.

The MAX1003 operates with +5V analog and +3.3V digital supplies for easy interfacing to +3.3V-logic-compatible digital signal processors and microprocessors. It comes in a 36-pin SSOP package.

Applications

Direct Broadcast Satellite (DBS) Receivers

VSAT Receivers

Wide Local Area Networks (WLANs)

Cable Television Set-Top Boxes

Features

- ♦ **Two Matched 6-Bit ADCs**
- ♦ **High Sampling Rate: 90Msps per ADC**
- ♦ **Low Power Dissipation: 350mW**
- ♦ **Excellent Dynamic Performance:**
  5.85 ENOB with 20MHz Analog Input
  5.7 ENOB with 50MHz Analog Input
- ♦ **±1/4LSB INL and DNL (typ)**
- ♦ **Internal Bandgap Voltage Reference**
- ♦ **Internal Oscillator with Overdrive Capability**
- ♦ **55MHz (-0.5dB) Bandwidth Input Amplifiers with True Differential Inputs**
- ♦ **User-Selectable Input Full-Scale Range (125mVp-p, 250mVp-p, or 500mVp-p)**
- ♦ **1/4LSB Channel-to-Channel Offset Matching (typ)**
- ♦ **0.1dB Gain and 0.5° Phase Matching (typ)**
- ♦ **Single-Ended or Differential Input Drive**
- ♦ **Flexible, 3.3V, CMOS-Compatible Digital Outputs**

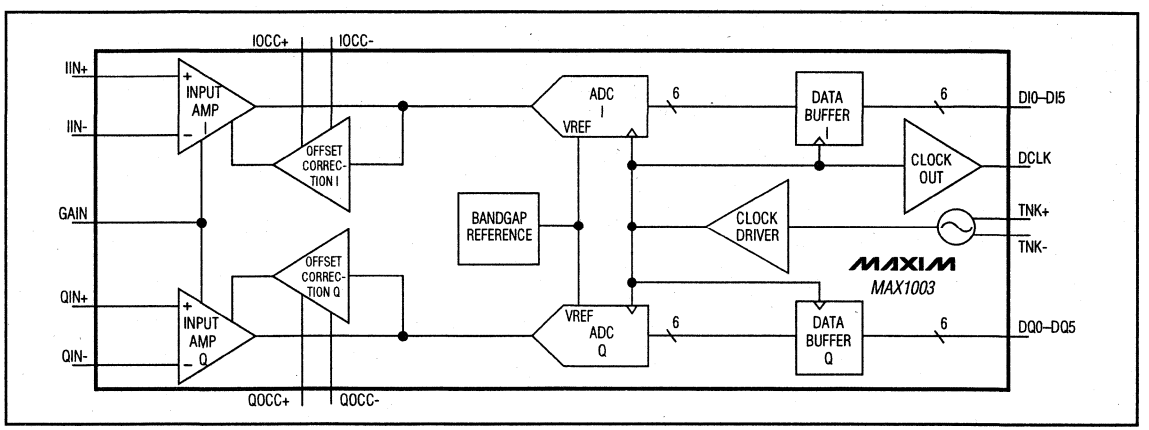
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1003CAX	0°C to +70°C	36 SSOP

Pin Configuration appears at end of data sheet.

7

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Power, 90Msps, Dual 6-Bit ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to 6.5V
V_{CCO} to OGND .....-0.3V to 6.5V
GND to OGND .....-0.3V to 0.3V
Digital and Clock Output Pins to OGND...-0.3V to V_{CCO} (10sec)
All Other Pins to GND.....-0.3V to V_{CC}

Continuous Power Dissipation (T_A = +70°C)
SSOP (derate 11.8mW/°C above +70°C) 941mW
Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, <10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	RES		6			Bits
Integral Nonlinearity	INL		-0.5	±0.25	0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature	-0.5	±0.25	0.5	LSB
Full-Scale Input Range	V_{FSH}	GAIN = V_{CC} (high gain)	118.75	125	131.25	mVp-p
	V_{FSM}	GAIN = open (mid gain)	237.5	250	262.5	
	V_{FSL}	GAIN = GND (low gain)	475	500	525	
INVERTING AND NONINVERTING ANALOG INPUTS						
Input Open-Circuit Voltage	V_{AOC}		2.25	2.35	2.45	V
Input Resistance	R_{IN}		13	20	29	kΩ
Input Capacitance	C_{IN}	Guaranteed by design		3	5	pF
Common-Mode Voltage Range	V_{CM}	Other analog input driven with external source (Note 2)	1.75		2.75	V
OSCILLATOR INPUTS						
Oscillator Input Resistance	R_{OSC}	Other oscillator input tied to V_{CC} + 0.3V	4.8	8	12.1	kΩ
DIGITAL OUTPUTS (DI0–DI5, DQ0–DQ5)						
Digital Outputs Logic-High Voltage	V_{OH}	I_{SOURCE} = 50µA	0.7V_{CCO}			V
Digital Outputs Logic-Low Voltage	V_{OL}	I_{SINK} = 400µA			0.5	V
POWER SUPPLY						
Supply Current	I_{CC}			63	104	mA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.75V to 5.25V (Note 3)		-75	-40	dB
Digital Outputs Supply Current	I_{CCO}	20MHz, full-scale I and Q analog inputs, C_L = 15pF (Note 4)			21	mA
Power Dissipation	PD			350		mW

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (Gain = open, external 90MHz clock (Figure 7), V_{INI} = V_{INQ} = 20MHz sine, amplitude -1dB below full scale, unless otherwise noted.)						
Maximum Sample Rate	f_{MAX}		90			Msps
Analog Input -0.5dB Bandwidth	BW	GAIN = GND, open, V_{CC}		55		MHz
Effective Number of Bits	$ENOB_M$	GAIN = open (mid gain)	5.6	5.85		Bits
		GAIN = open (mid gain), f_{IN} = 50MHz, -1dB below full scale		5.7		
	$ENOB_H$	GAIN = V_{CC} (high gain)		5.8		
	$ENOB_L$	GAIN = GND (low gain)		5.85		
Signal-to-Noise plus Distortion Ratio	SINAD	GAIN = open (mid gain)	35.5	37		dB
Input Offset (Note 5)	OFF	I channel	-0.5		0.5	LSB
		Q channel	-0.5		0.5	
Crosstalk Between ADCs	XTLK			-55		dB
Offset Mismatch Between ADCs	OMM	(Note 5)	-0.5	±0.25	0.5	LSB
Amplitude Match Between ADCs	AM		-0.2	±0.1	0.2	dB
Phase Match Between ADCs	PM		-2	±0.5	2	degrees
TIMING CHARACTERISTICS (Data outputs: R_L = 1MΩ, C_L = 15pF)						
Clock to Data Propagation Delay	t_{PD}	(Note 6)		3.6		ns
Data Valid Skew	t_{SKEW}	(Note 6)		1.5		ns
Input to DCLK Delay	t_{DCLK}	TNK+ to DCLK (Note 6)		5.3		ns
Aperture Delay	t_{AD}	Figure 8		7.5		ns
Pipeline Delay	PD	Figure 8		1		clock cycle

Note 1: Best-fit straight-line linearity method.

Note 2: A typical application will AC couple the analog input to the DC bias level present at the analog inputs (typically 2.35V). However, it is also possible to DC couple the analog input (using differential or single-ended drive) within this common-mode input range (Figures 4 and 5).

Note 3: PSRR is defined as the change in the mid-gain full-scale range as a function of the variation in V_{CC} supply voltage, expressed in decibels.

Note 4: The current in the V_{CCO} supply is a strong function of the capacitive loading on the digital outputs. To minimize supply transients and achieve optimal dynamic performance, reduce the capacitive-loading effects by keeping line lengths on the digital outputs to a minimum.

Note 5: Offset-correction compensation enabled, 0.22µF at Q and I compensation inputs (Figures 2 and 3).

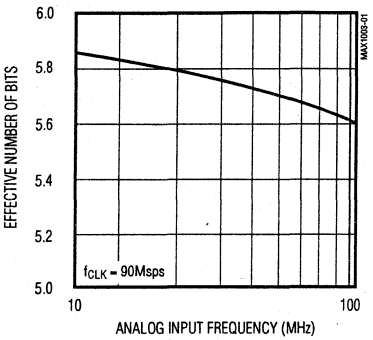
Note 6: t_{PD} and t_{SKEW} are measured from the 1.4V level of the output clock, to the 1.4V level of either the rising or falling edge of a data bit. t_{DCLK} is measured from the 50% level of the clock-overdrive signal on TNK+ to the 1.4V level of DCLK. The capacitive load on the outputs is 15pF.

Low-Power, 90Msps, Dual 6-Bit ADC

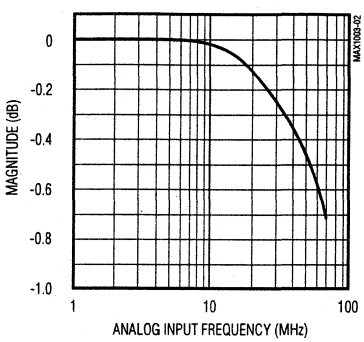
Typical Operating Characteristics

(V_{CC} = +5V ±5%, V_{CCO} = 3.3V ±300mV, f_{CLK} = 90Msps, GAIN = open (midgain) MAX1003 evaluation kit, T_A = +25°C, unless otherwise noted.)

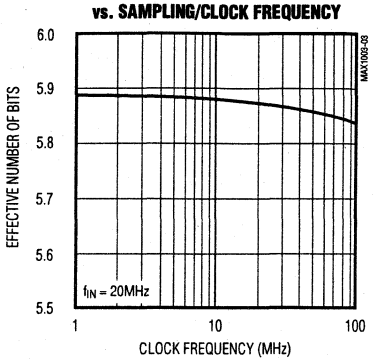
EFFECTIVE NUMBER OF BITS vs. ANALOG INPUT FREQUENCY



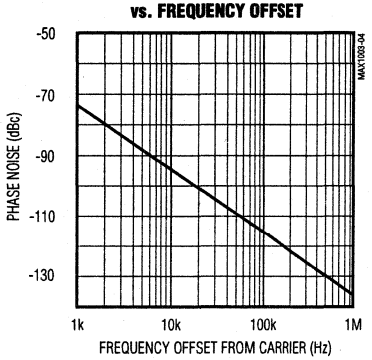
ANALOG INPUT BANDWIDTH



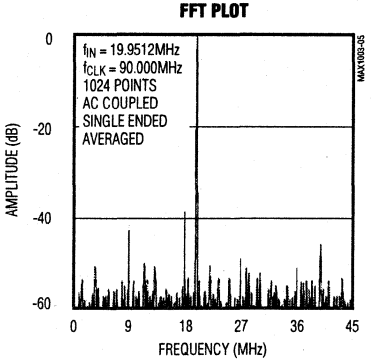
EFFECTIVE NUMBER OF BITS vs. SAMPLING/CLOCK FREQUENCY



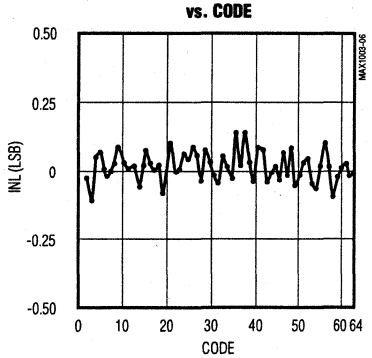
OSCILLATOR OPEN-LOOP PHASE NOISE vs. FREQUENCY OFFSET



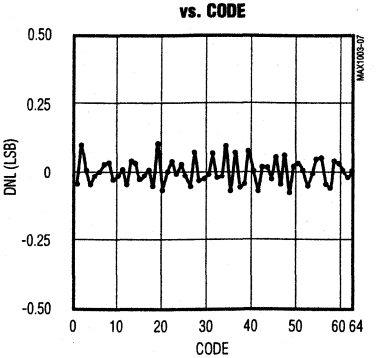
FFT PLOT



INTEGRAL NONLINEARITY vs. CODE



DIFFERENTIAL NONLINEARITY vs. CODE



Pin Description

PIN	NAME	FUNCTION
1	GAIN	Gain-Select Input. Sets input full-scale range: 125/250/500mVp-p (Table 1).
2	IOCC+	Positive I-Channel Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground for DC-coupled inputs.
3	IOCC-	Negative I-Channel Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground for DC-coupled inputs.
4	IIN+	I-Channel Noninverting Analog Input
5	IIN-	I-Channel Inverting Analog Input
6	VCC	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 7).
7, 11, 12, 18, 19	GND	Analog Ground
8	VCC	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 11).
9	TNK+	Positive Oscillator/Clock Input
10	TNK-	Negative Oscillator/Clock Input
13	VCC	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 12).
14	QIN-	Q-Channel Inverting Analog Input
15	QIN+	Q-Channel Noninverting Analog Input
16	QOCC-	Negative Q-Channel Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground for DC-coupled inputs.
17	QOCC+	Positive Q-Channel Offset-Correction Compensation. Connect a 0.22µF capacitor for AC-coupled inputs. Ground for DC-coupled inputs.
20–25	DQ5–DQ0	Q-Channel Digital Outputs 0–5. DQ5 is the most significant bit (MSB).
26, 28	VCCO	Digital Output Supply, +3.3V ±300mV. Bypass each with a 47pF capacitor to OGND (pin 27).
27	OGND	Digital Output Ground
29	DCLK	Digital Clock Output. Frames the output data.
30–35	DI0–DI5	I-Channel Digital Outputs 0–5. DI5 is the most significant bit (MSB).
36	VCC	+5V ±5% Supply. Bypass with a 0.01µF capacitor to GND (pin 19).

Detailed Description

Converter Operation

The MAX1003 contains two 6-bit analog-to-digital converters (ADCs), a buffered voltage reference, and oscillator circuitry. The ADCs use a flash conversion technique to convert an analog input signal into a 6-bit parallel digital output code. The MAX1003's unique design includes 63 fully differential comparators and a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. The control logic interfaces easily to most digital signal processors (DSPs) and microprocessors (µPs) with +3.3V CMOS-compatible logic interfaces. Figure 1 shows the MAX1003 in a typical application.

Programmable Input Amplifiers

The MAX1003 has two (I and Q) programmable-gain input amplifiers with a -0.5dB bandwidth of 55MHz and true differential inputs. To maximize performance in high-speed systems, each amplifier has less than 5pF of input capacitance. The input amplifier gain is programmed, via the GAIN pin, to provide three possible input full-scale ranges (FSRs) as shown in Table 1.

Table 1. Input Amplifier Programming

GAIN	INPUT FULL-SCALE RANGE (mVp-p)
GND	500
Open	250
VCC	125

Low-Power, 90Msps, Dual 6-Bit ADC

Single-ended and differential AC-coupled input circuits are shown in Figures 2 and 3. Each of the amplifier inputs is internally biased to a 2.35V reference through a 20kΩ resistor, eliminating external DC bias circuits. A series 0.1µF capacitor is required at each amplifier input for AC-coupled signals.

When operating with AC-coupled inputs, the input amplifiers' DC offset voltage is nulled to within ±1/2LSB by an on-chip offset-correction amplifier. An external compensation capacitor is required to set the dominant pole of the offset-correction amplifier's frequency response (Figures 2 and 3). The compensation capacitor will determine the low-frequency corner of the analog input response according to the following formula:

$$f_C = 1 / (0.1 \times C)$$

where C is the value of the compensation capacitor in µF, and f_C is the corner frequency in Hz.

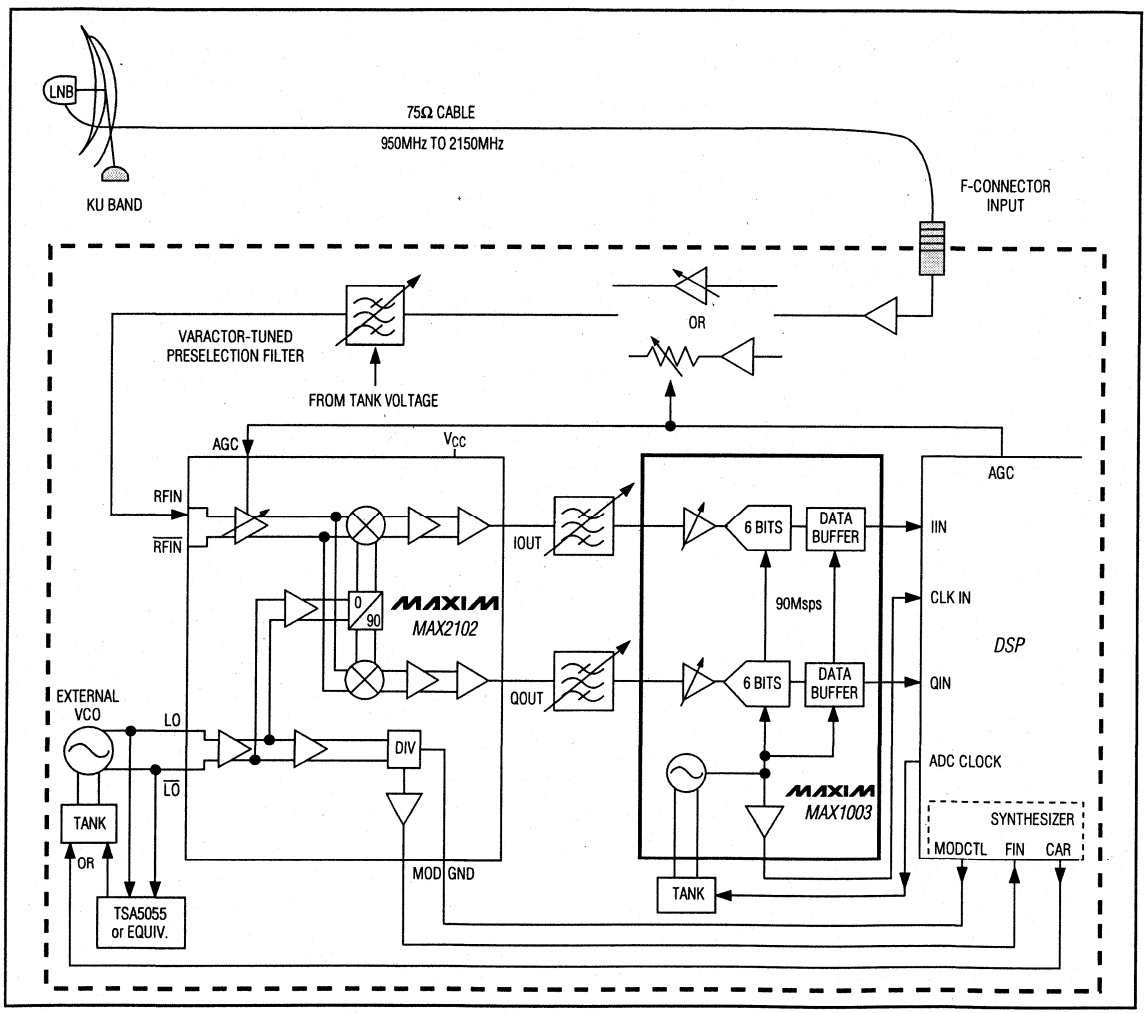


Figure 1. Commercial Satellite Receiver System

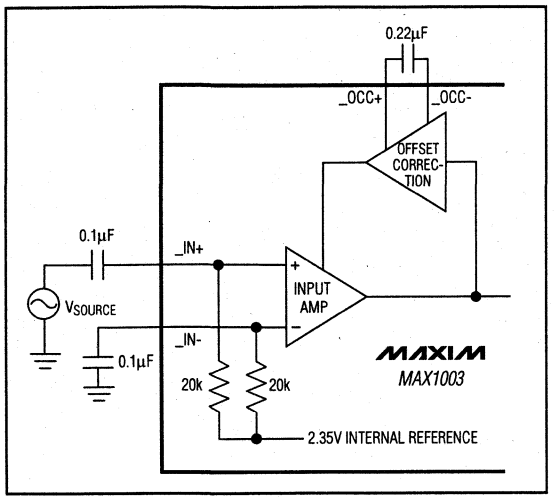


Figure 2. Single-Ended AC-Coupled Input

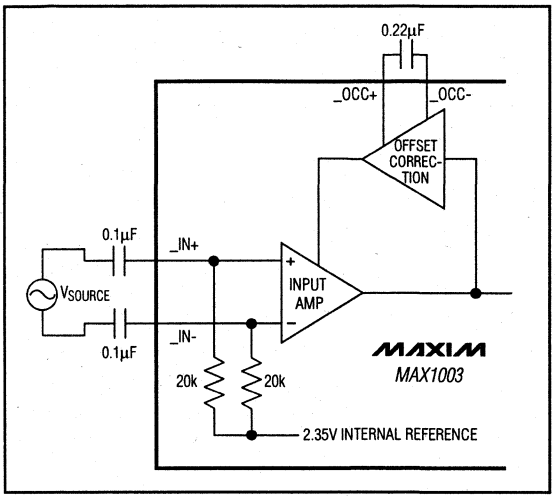


Figure 3. Differential AC-Coupled Input

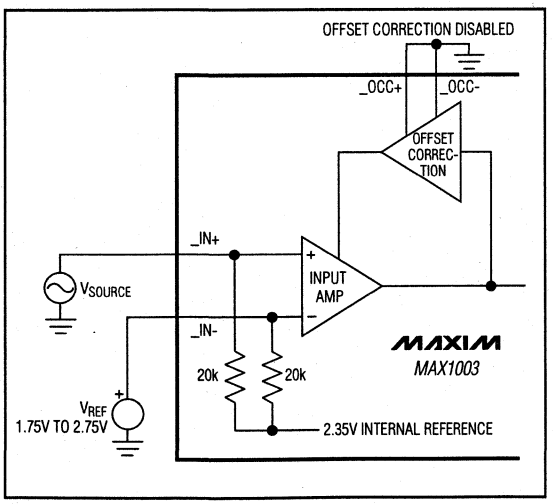


Figure 4. Single-Ended DC-Coupled Input

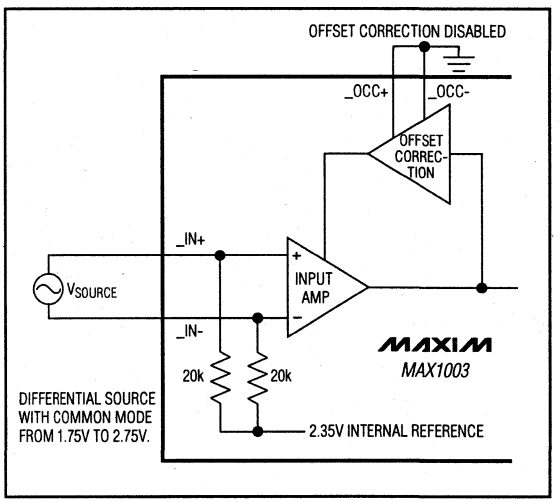


Figure 5. Differential DC-Coupled Input

For applications where a DC component of the input signal is present, Figures 4 and 5 show single-ended and differential DC-coupled input circuits. The amplifiers' input common-mode voltage range extends from 1.75V to 2.75V. To prevent attenuation of the input signal's DC component in this mode, disable the offset-correction amplifier by grounding the _OCC+ and _OCC- pins for the I and Q blocks (Figures 4 and 5).

ADCs

The I and Q ADC blocks receive the analog signals from the respective I and Q input amplifiers. The ADCs use flash conversion with 63 fully differential comparators to digitize the analog input signal into a 6-bit output in offset binary format.

The MAX1003 features a proprietary encoding scheme that ensures no more than 1LSB dynamic encoding error. Dynamic encoding errors resulting from metastable states may occur when the analog input voltage, at the time the sample is taken, falls close to the decision point for any one of the input comparators. The resulting output code for typical converters can be incorrect, including false full- or zero-scale outputs. The MAX1003's unique design reduces the magnitude of this type of error to 1LSB.

Internal Voltage Reference

An internal buffered bandgap reference is included on the MAX1003 to drive the ADCs' reference ladders. The on-chip reference and buffer eliminate any external (high-impedance) connections to the reference ladder, minimizing the potential for noise coupling from external circuitry while ensuring that the voltage reference, input amplifier, and reference ladder track well with variations of temperature and power supplies.

Oscillator Circuit

The MAX1003 includes a differential oscillator, which is controlled by an external parallel resonant (tank) network as shown in Figure 6. Alternatively, the oscillator may be overdriven with an external clock source as shown in Figure 7.

Internal Clock Operation (Tank)

If the tank circuit is used, the resonant inductor should have a sufficiently high Q and a self-resonant frequency (SRF) of at least twice the intended oscillator frequency. Coilcraft's 1008HS-221, with an SRF of 700MHz and a Q of 45, works well for this application. Generate different clock frequency ranges by adjusting varactor and tank elements.

An internal clock-driver buffer is included to provide sharp clock edges to the internal flash comparators. The buffer ensures that the comparators are simultaneously clocked, maximizing the ADCs' effective number of bits (ENOB) performance.

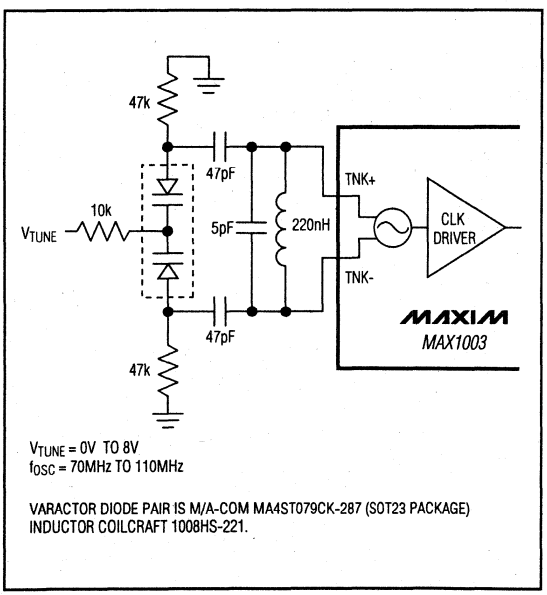


Figure 6. Tank Resonator Oscillator

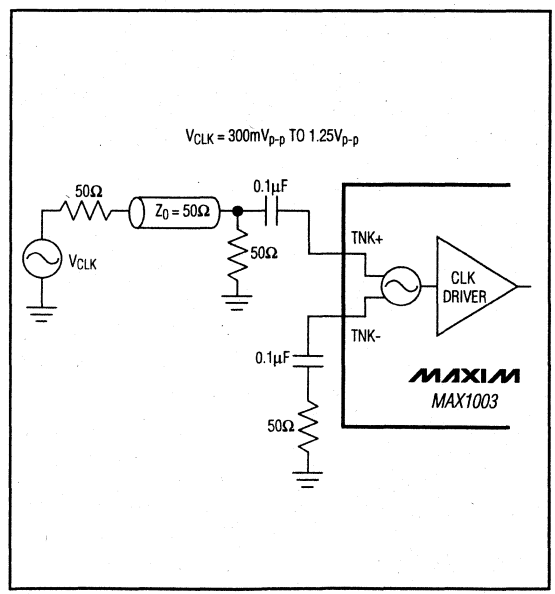


Figure 7. External Clock Drive Circuit

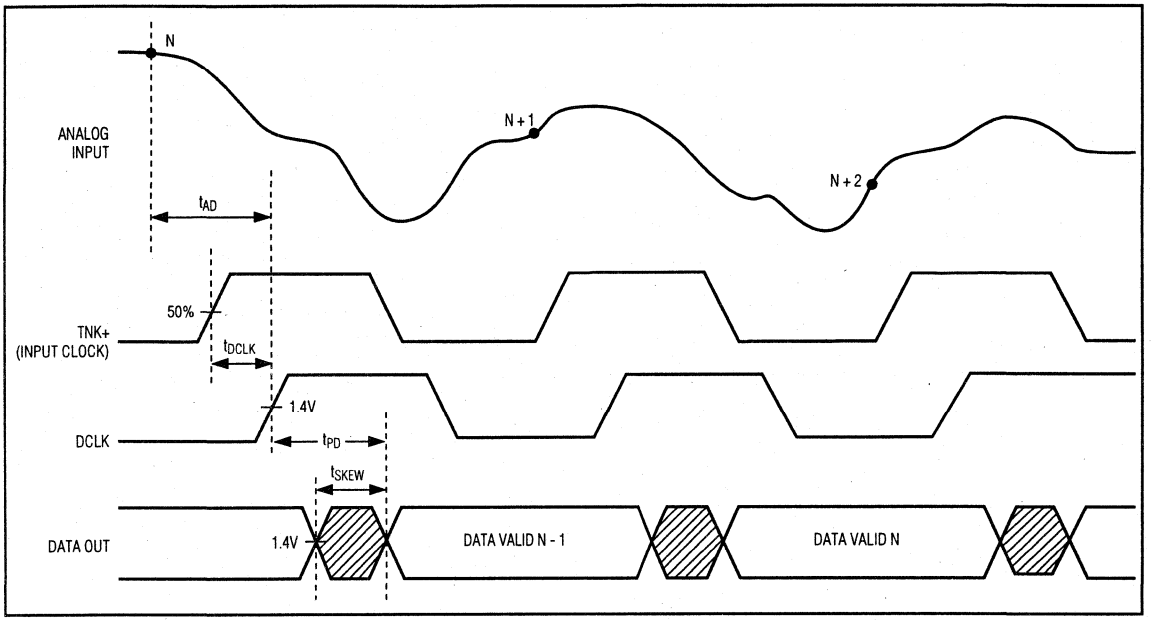


Figure 8. MAX1003 Timing Diagram

External Clock Operation

To accommodate designs that use an external clock, the MAX1003's internal oscillator can be overdriven by an external clock source as shown in Figure 7. The external clock source should be a sinusoid to minimize clock phase noise and jitter, which can degrade the ADCs' ENOB performance. AC couple the clock source (recommended voltage level is approximately 1Vp-p) to the oscillator inputs as shown in Figure 7.

Output Data Format

The conversion results are output on a dual, 6-bit-wide data bus. Data is latched into the ADC output latch following a pipeline delay of one clock cycle, as shown in Figure 8. Output data is clocked out of the respective ADC's data output pins (D_0 through D_5) on the rising edge of the clock output (DCLK), with a DCLK-to-data propagation delay (t_{PD}) of 3.6ns. The MAX1003 outputs are +3.3V CMOS-logic compatible.

Transfer Function

Figure 9 shows the MAX1003's nominal transfer function. Output coding is offset binary with 1LSB = FSR / 63.

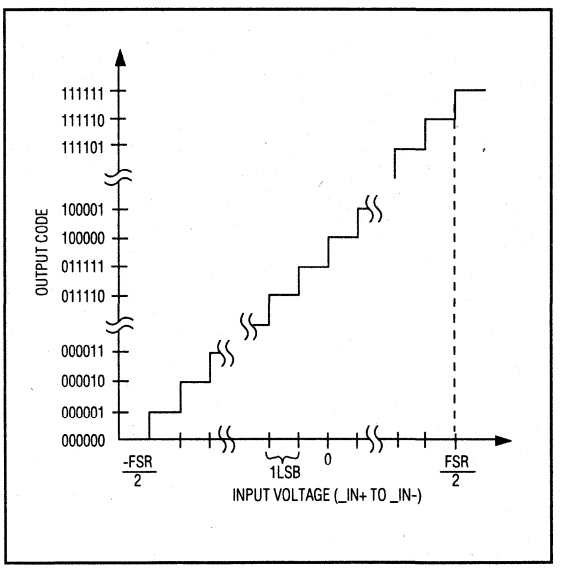


Figure 9. Ideal Transfer Function

Low-Power, 90Msps, Dual 6-Bit ADC

Applications Information

The MAX1003 is designed with separate analog and digital power-supply and ground connections to isolate high-current digital noise spikes from the more sensitive analog circuitry. The high-current digital output ground (OGND) and analog ground (GND) should be at the same DC level, connected at only one location on the board. This will provide best noise immunity and improved conversion accuracy. Use of separate ground planes is strongly recommended.

The entire board needs good DC bypassing for both analog and digital supplies. Place the power-supply bypass capacitors close to where the power is routed onto the board, i.e., close to the connector. 10µF electrolytic capacitors with low-ESR ratings are recommended. For best effective bits performance, minimize capacitive loading at the digital outputs. Keep the digital output traces as short as possible.

The MAX1003 requires a +5V ±5% power supply for the analog supply (V_{CC}) and a +3.3V ±300mV power supply connected to V_{CCO} for the logic outputs. Bypass each of the $V_{CC_}$ supply pins to its respective GND with high-quality ceramic capacitors located as close to the package as possible (Table 2). Consult the evaluation kit manual for a suggested layout and bypassing scheme.

Table 2. Bypassing

SUPPLY FUNCTION	V_{CC}/ V_{CCO}	BYPASS TO GND/ OGND	CAPACITOR VALUE
Analog Inputs	6	7	0.01µF
Oscillator/Clock	8	11	0.01µF
Converter	13	12	0.01µF
Digital Q-Output	26	27	47pF
Digital I-Output	28	27	47pF
Buffer	36	19	0.01µF

Dynamic Performance

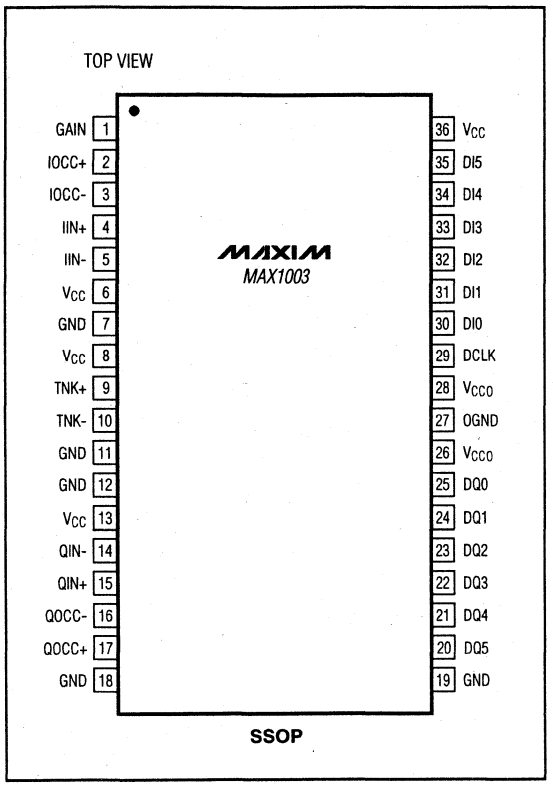
Signal-to-noise and distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to all other ADC output signals. The output spectrum is limited to frequencies above DC and below one-half the ADC sample rate.

The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. Therefore, a perfect 6-bit ADC can do no better than 38dB.

The FFT Plot (see *Typical Operating Characteristics*) shows the result of sampling a pure 20MHz sinusoid at a 90MHz clock rate. This FFT plot of the output shows the output level in various spectral bands. The plot has been averaged to reduce the quantization noise floor and reveal the low-amplitude spurs. This emphasizes the excellent spurious-free dynamic range of the MAX1003.

The effective resolution (or effective number of bits) the ADC provides can be measured by transposing the equation that converts resolution to SINAD: N = (SINAD - 1.76) / 6.02 (see *Typical Operating Characteristics*).

Pin Configuration



Chip Information

TRANSISTOR COUNT: 6097

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

IF Undersampler

MAX1005

General Description

The MAX1005 is a combination, low-power digitizer and reconstruction IC designed to work in systems that modulate and demodulate communications signals. The analog-to-digital converter (ADC) directly samples or undersamples a downconverted RF signal. The digital-to-analog converter (DAC) recreates the IF subcarrier and transmission data. The MAX1005's ADC is ideal for undersampling applications due to the analog input amplifier's wide (15MHz) bandwidth. The DAC has very low glitch energy, which minimizes the transmission of unwanted spurious signals. An on-chip reference provides for low-noise ADC and DAC conversions.

The MAX1005 provides a high level of signal integrity on a small power budget. This device can be operated from a single +2.7V to +5.5V power supply or from separate analog and digital supplies with independent voltages ranging from +2.7V to +5.5V. The MAX1005 can operate with an unregulated +5.5V analog supply and a regulated digital supply down to +2.7V. This flexible power-supply operation can save additional power in complex digital systems.

The MAX1005 has three operating modes: transmit (ADC inactive), receive (DAC inactive), and shutdown (ADC and DAC inactive). In shutdown mode, the total supply current drops below 5µA. Only 2.4µs is required for the MAX1005 to wake up from shutdown mode. This device is ideal for hand-held as well as base-station applications. The MAX1005 is available in a tiny, 16-pin QSOP package and is specified for operation over the -40°C to +85°C extended temperature range.

Applications

PWT1900

PHS/P

Wireless Loops

PCS/N

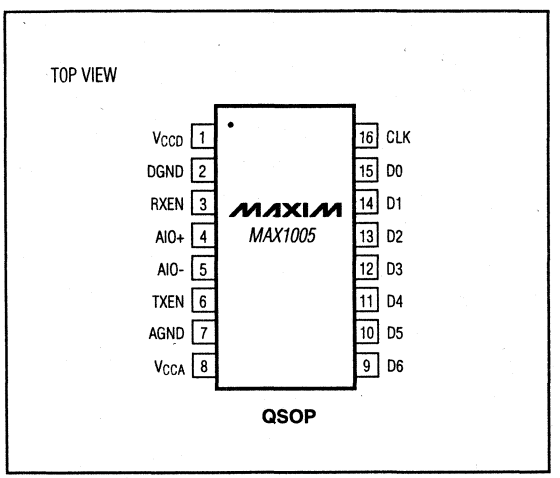
Features

- **Differential-Input, 5-Bit ADC**
- **Differential-Output, 7-Bit DAC**
- **15Msps Conversion Rate**
- **25MHz -1dB Full-Power Bandwidth**
- **44dB of SFDR for ADC**
- **39dB of SFDR for DAC at 10.7MHz (imaged)**
- **Internal Voltage Reference**
- **Parallel Logic Interface**
- **Single-Supply Operation (+2.7V to +5.5V)**
- **0.1µA Low-Power Shutdown Mode**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1005CEE	0°C to +70°C	16 QSOP
MAX1005EEE	-40°C to +85°C	16 QSOP

Pin Configuration



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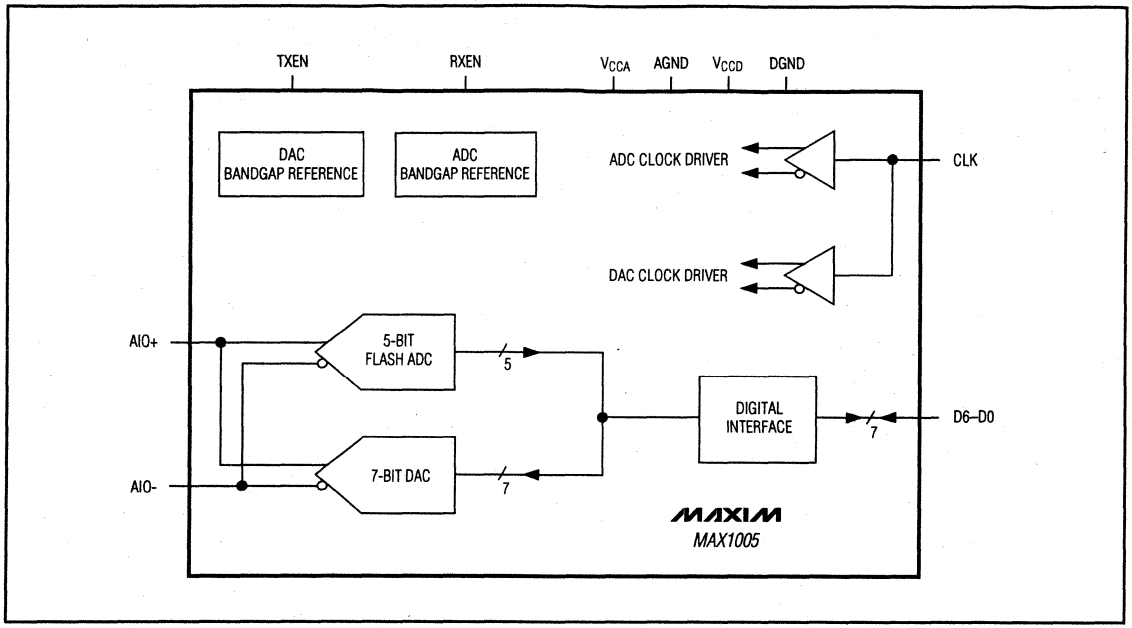
IF Undersampler

Functional Diagram



MAXIM

Mobile-Radio Analog Controller

General Description

The MAX1007 is a multifunctional integrated circuit designed for high-performance mobile radios. It includes one 8-bit analog-to-digital converter (ADC), two 7-bit and two 6-bit digital-to-analog converters (DACs) for functions including radio-frequency (RF) power sensing, and antenna-diversity selection.

The ADC provides for power sense, receive-signal strength intensity (RSSI) measurements, and system supervision. In the power-sense mode, the ADC converts the power-sensing circuitry signal (representing either the transmitted (Tx) or received (Rx) RF power) into a digital code, ensuring optimum Tx power setting and Rx signal analysis. An additional direct input to the ADC provides for system-supervision measurements, such as power-supply voltages, battery voltage, and temperature.

Four DAC blocks control DC levels in the radio. As part of the Maxim PWT1900 chip set, the two 7-bit DACs control the gain settings, and the two 6-bit DACs control the varactor diodes to tune a TCXO and bias a GaAs amplifier. Each DAC register and output can be updated independently, providing maximum flexibility.

For antenna diversity, a magnitude-comparison circuit captures and compares two peak signals. A latched logic-comparator output reveals which signal has the largest magnitude. The MAX1007 also includes an on-board voltage reference for the ADC and DACs.

The MAX1007 offers a high level of signal integrity with minimal power dissipation. Single-supply operation ranges from +2.85V to +5.5V. To further save power, there are two shutdown modes: standby and total shutdown. Standby is a partial shutdown that keeps the bandgap reference and the 2.4V reference generator active. Total shutdown disables all circuit blocks except the serial interface, reducing supply current to less than 1µA.

The MAX1007 is available in a 24-pin SSOP and is specified for the commercial and extended temperature ranges.

Applications

PWT1900 Wireless Communications:

Cellular Radios PMR/SMR

PCS Radios WLL

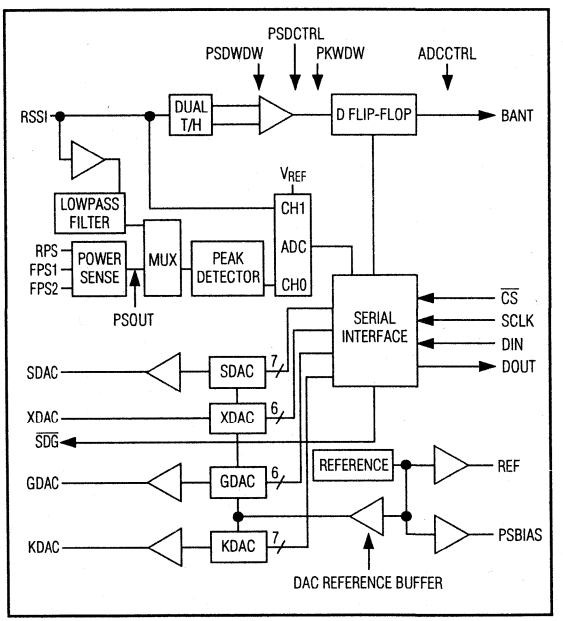
Features

- ♦ **+2.85V to +5.5V Single-Supply Operation**
- ♦ **Multi-Input 8-Bit ADC**
- ♦ **Two 7-Bit DACs with Buffered Outputs**
- ♦ **Two 6-Bit DACs: Buffered/Unbuffered**
- ♦ **Power-Sense Conditioning Circuitry**
- ♦ **RSSI Measurement**
- ♦ **Antenna-Diversity Circuitry**
- ♦ **Internal Reference**
- ♦ **Serial Interface**
- ♦ **Two Shutdown Modes**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1007CAG	0°C to +70°C	24 SSOP
MAX1007EAG	-40°C to +85°C	24 SSOP

Functional Diagram



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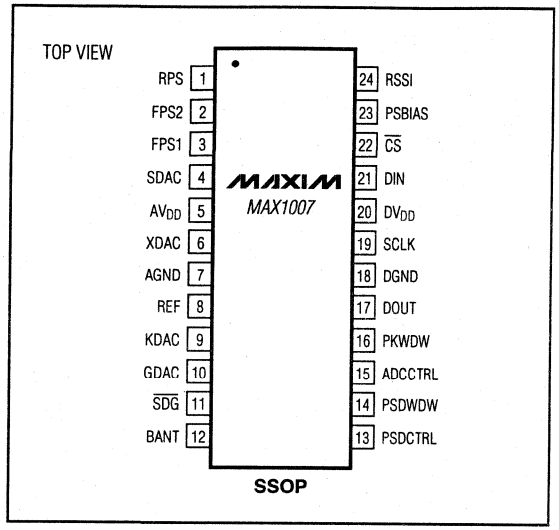
Mobile-Radio Analog Controller

Pin Configuration



19-1166; Rev 0; 12/96

MAXIM

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

General Description

The MAX1101 is a highly integrated IC designed primarily for digitizing the output of a linear CCD array. It provides the components required for all necessary analog functions, including clamp circuitry for black-level correction or correlated double sampling (CDS), a three-input multiplexer (mux), and an 8-bit analog-to-digital converter (ADC).

The MAX1101 operates with a sample rate up to 1MHz and with a wide range of linear CCDs. The logic interface is serial, and a single input sets the bidirectional data line as either data in or data out, thus minimizing the I/O pins required for communication.

Packaged in a 24-pin SO, the MAX1101 is available in the commercial (0°C to +70°C) temperature range.

Features

- ♦ **1.0 Million Pixels/sec Conversion Rate**
- ♦ **Built-In Clamp Circuitry for Black-Level Correction or Correlated Double Sampling**
- ♦ **64-Step PGA, Programmable from Gain = -2 to -10**
- ♦ **Auxiliary Mux Inputs for Added Versatility**
- ♦ **Compatible with a Large Range of CCDs**
- ♦ **8-Bit ADC Included**
- ♦ **Space-Saving, 24-Pin SO Package**

Applications

Scanners

Fax Machines

Digital Copiers

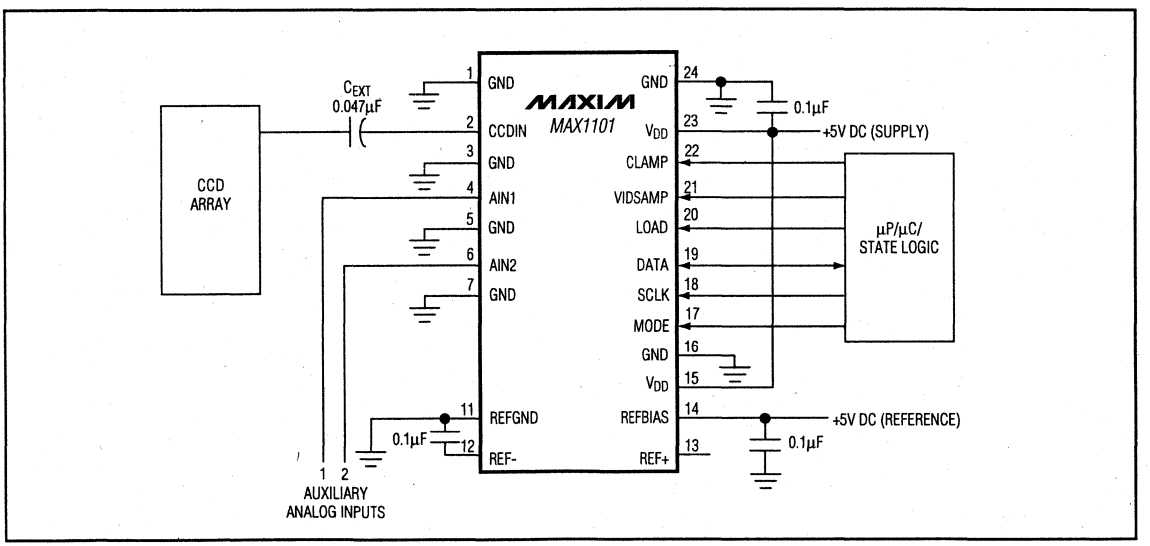
CCD Imaging

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1101CWG	0°C to +70°C	24 Wide SO

Pin Configuration appears on last page.

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +12V
All Pins to GND.....-0.3V to (V_{DD} + 0.3V)
Current into Every Pin (except V_{DD}).....±20mA
Current into V_{DD} .....±50mA
Continuous Power Dissipation (T_A = +70°C)
SO (derate 11.76mW/°C above +70°C).....941mW

Operating Temperature Range.....0°C to +70°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = $V_{REFBIAS}$ = +4.75V to +5.25V, REFGND = 0V, REF- bypassed to REFGND with 0.1µF, C_{EXT} = 47nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG-TO-DIGITAL CONVERTER							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	No-missing-codes guaranteed			±0.5	±1	LSB
Integral Nonlinearity	INL	Best straight-line fit			±1	±1.5	LSB
Total Unadjusted Error	TUE					±2.5	LSB
Zero-Scale Drift	TCVOS				125		%µV/°C
Full-Scale Drift	TCFS				0.016		%FS/°C
Maximum Sample Rate	f_S			0.67	1.2		MHz
Minimum Sample Rate		(Note 1)		1			kHz
Input Full-Power Bandwidth		V_{IN} = 2.5Vp-p			1		MHz
Aperture Delay	t_{AP}				10		ns
ANALOG INPUT—CCD INTERFACE							
Maximum Peak CCD Differential Signal Range	V_{WHITE}	V_{WHITE} = (V_{REF+} - V_{REF-}) / G_{PGA}	G_{PGA} = -2		1.25		V
			G_{PGA} = -10		0.25		
Minimum PGA Gain Setting				-1.9	-2	-2.1	V/V
Maximum PGA Gain Setting				-9.375	-9.875	-10.375	V/V
Gain Adjust Resolution					64		Steps
Gain Adjust Step Size					0.125		V/V
PGA Gain Error					±5		% Gain
Black Sample Switch On-Resistance	$R_{ON(BSS)}$				60	150	Ω
Input Leakage (Note 2)	$I_{L(CCDIN)}$	Including black sample switch off-leakage			1	50	nA
CCD Interface Offset Voltage	$V_{OS(CCD)}$	V_{VIDEO} = V_{RESET} (Figure 4)		0	4	8	LSB
ANALOG INPUT—AUXILIARY INPUTS							
Input Voltage Range	V_{IN}			V_{REF-}		V_{REF+}	V
Input Capacitance (Note 1)	$C_{IN(ON)}$	Channel on				45	pF
	$C_{IN(OFF)}$	Channel off				10	
On-Resistance	R_{ON}				120		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{REFBIAS}$ = +4.75V to +5.25V, REFGND = 0V, REF- bypassed to REFGND with 0.1µF, C_{EXT} = 47nF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE INPUT						
Positive Reference Voltage	V_{REF+}	Internally generated, $V_{REFBIAS}$ = 5V	2.94	3.00	3.06	V
Negative Reference Voltage	V_{REF-}	Internally generated, $V_{REFBIAS}$ = 5V	0.49	0.50	0.51	V
POWER SUPPLIES						
Positive Supply-Voltage Range	V_{DD}		4.75	5	5.25	V
PSRR, PGA and ADC	PSRR	4.75V ≤ V_{DD} ≤ 5.25V	48	60		dB
Supply Current	I_{DD}			20	40	mA
DIGITAL INPUTS/OUTPUTS						
Digital Input Voltage High	V_{IH}		3.5			V
Digital Input Voltage Low	V_{IL}				1.5	V
Digital Input Leakage Current	I_{IL}		-10		10	µA
Digital Output Voltage High	V_{OH}	I_{SOURCE} = 4mA	V_{DD} - 0.5			V
Digital Output Voltage Low	V_{OL}	I_{SINK} = 4mA			0.5	V
Digital Output Leakage Current	I_{OL}	Output in high-impedance mode	-10		10	µA
DIGITAL TIMING SPECIFICATIONS (t_r, t_f ≤ 10ns, C_L ≤ 50pF, unless otherwise noted)						
SCLK Frequency	f_{SCLK}				10	MHz
SCLK Pulse Width	t_{SPW}		50			ns
VIDSAMP Pulse Width	t_{VS}		500			ns
VIDSAMP to CLAMP Separation	t_{VB}		50			ns
LOAD Pulse Width	t_{LD}		50			ns
VIDSAMP Fall to SCLK Rise Time	t_{VLS}	MODE = 1	50			ns
VIDSAMP Fall to DATA	t_{VLD}	MODE = 1			60	ns
VIDSAMP to Reset Separation	t_{VR}	(Note 2)	50			ns
Reset to CLAMP Separation	t_{RB}	(Note 2)	50			ns
SCLK Rise to DATA	t_{SD}				60	ns
DATA Set-Up Time	t_{DSU}		20			ns
DATA Hold Time	t_{DH}		20			ns
LOAD Fall to SCLK Rise Time	t_{LS}	MODE = 0	50			ns
SCLK Rise to LOAD Rise Time	t_{SL}	MODE = 0	50			ns
MODE Setup Time	t_{MSU}	Same as bus-relinquish time	50			ns
CLAMP Pulse Width	t_{BS}		300			ns
CLAMP Fall to Video Update	t_{BC}	(Note 1)	20			ns
Digital Quiet Time (Note 3)	t_Q	± around VIDSAMP falling edge	20			ns

Note 1: Due to leakage in the PGA and ADC, operation at sample rates below 1ksps is not recommended, as performance may degrade, particularly at high temperatures.

Note 2: Production test equipment settling time prohibits leakage measurements below 1nA. Lab equipment has shown the MAX1101 switch input leakage below 1pA at T_A = +25°C, and below 50pA at T_A = +70°C.

Note 3: Not a test parameter. Recommended for optimal performance.

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 10, 16, 24	GND	Ground
2	CCDIN	CCD Input. Connect CCD through a series 0.047µF capacitor (C_{EXT}).
4	AIN1	Auxiliary Analog Input Channel 1
6	AIN2	Auxiliary Analog Input Channel 2
8, 9, 10	I.C.	Internally Connected. Do not connect to this pin.
11	REFGND	Reference Ground. Ground reference for all analog signals.
12	REF-	Lower Limit of Reference Span. Sets the zero-code voltage. Range is GND ≤ REF- ≤ REF+. Nominally 0.5V.
13	REF+	Upper Limit of Reference Span. Sets the full-scale input. Voltage range is REF- ≤ REF+ ≤ V_{DD}. Nominally 3.0V.
14	REFBIAS	Reference Power Supply. Connect to external +5.0V to set V_{REF+} to +3.0V and V_{REF-} to +0.5V.
15, 23	V_{DD}	Power Supply, +5V. Bypass to ground very close to the device and connect the two pins together, close to the MAX1101.
17	MODE	Control Input. Set high, DATA is an output of the ADC. Set low, DATA enables programming of the PGA and mux.
18	SCLK	Serial Clock Input
19	DATA	Data Input or Output, as controlled by MODE
20	LOAD	Control Input. Loads serial shift-register data to PGA and multiplexer registers when MODE = 0.
21	VIDSAMP	Control Input. Samples the video level and initiates the ADC conversion.
22	CLAMP	Control Input. Samples black level. Can be used for correlated double sampling.

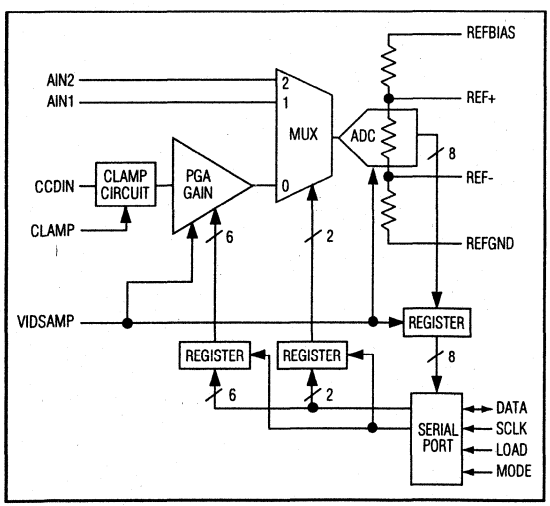


Figure 1. MAX1101 Functional Diagram

Detailed Description

Overview

The MAX1101 directly processes the pixel stream from a monochrome CCD, and removes black level, offset, and noise errors through an internal clamp circuit, which can be used as a correlated double sampler (CDS). It uses a 6-bit, programmable-gain amplifier (PGA) to adjust gain. A three-input multiplexer (mux) selects either the PGA output or two unassigned inputs (AIN1, AIN2). The processed analog signal is digitized by an 8-bit, half-flash analog-to-digital converter (ADC), and output serially through the DATA pin.

Digital data is input and output through the bidirectional serial pin (DATA) synchronously with the external serial clock (SCLK). When MODE = 0, the mux channels and the PGA gain can be programmed via DATA. With MODE = 1 (high), ADC serial data is output through this pin.

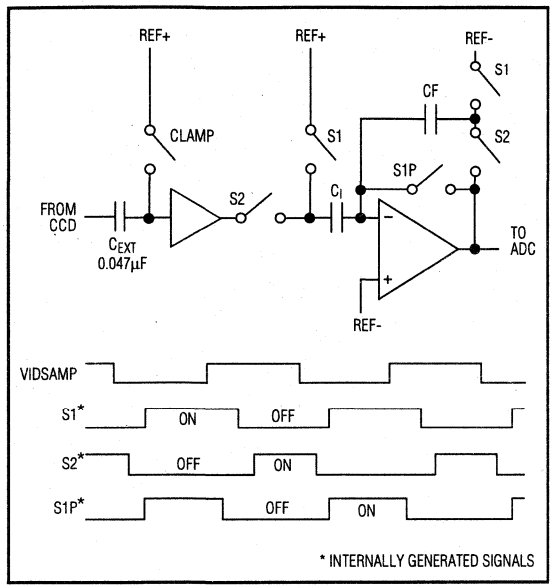


Figure 2. PGA Functional Diagram

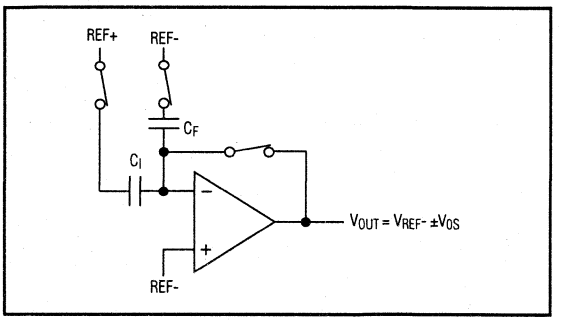


Figure 3a. PGA Connection with VIDSAMP = Low

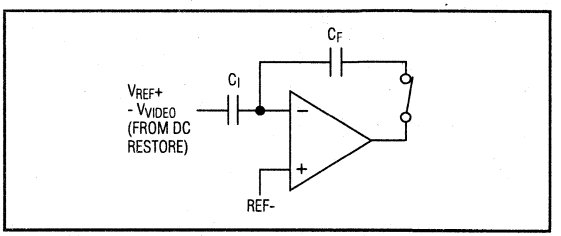


Figure 3b. PGA Connection with VIDSAMP = High

Programmable-Gain Amplifier

The PGA amplifies the differential video signal from the CCD (at CCDIN). Gain is settable with the 6-bit control word from -2 to -10 in 64 steps, in increments of -0.125. The PGA also provides for periodic DC restoration of the capacitively coupled input.

As shown in Figure 2, the switched-capacitor amplifier's gain is set by the ratio C_I/C_F. The input is sampled on the C_I capacitors, which is a set of equal capacitors. The 6-bit gain control word determines the number of capacitors used. Thus the PGA gain is set from -2 to -10.

A voltage equal to V_{REF-} is applied to the PGA's noninverting input. This offsets the PGA output to be within the range of the ADC (V_{REF-} to V_{REF+}).

Clamp Circuit

As shown in Figure 2, the CCD output is connected to the MAX1101 input (CCDIN) through an external capacitor, which removes the potentially large DC common-mode voltages from the input signal. Whenever CLAMP is high, the CLAMP switch is closed and C_{EXT} is charged to V_{REF+}. It can be actuated either once per pixel (sampling reset level) or less frequently (such as for restoring optical black level once per line), as required by the application.

VIDSAMP controls the sampling of the video signal and offset nulling of the PGA. To null out the offset, VIDSAMP causes switches S1 and S1P to close, placing the amplifier in a unity-gain configuration, as shown in Figure 3a. This configuration causes the amplifier's offset voltage to be stored on CF. In the next portion of the cycle, when VIDSAMP returns low, the S1 switches are opened and S2 is closed (Figure 3b). This is the standard inverting op-amp configuration. The only difference is that capacitors are used to set the gain, and the amplifier's offset voltage has been stored on these capacitors and is thus canceled. The amplifier's output is $[C_F/C_I] \times V_{VIDEO} + V_{REF-}$. The CDS function is shown in Figure 4.

ADC

The ADC uses a recycling half-flash conversion technique in which a 4-bit flash ADC section achieves an 8-bit result in two steps (Figure 5). Using 15 comparators, the flash ADC compares the unknown input voltage to the reference ladder (using REF+ and REF-) and provides the upper four data bits.

An internal digital-to-analog converter (DAC) uses the four most significant bits (MSBs) to generate the analog result from the first flash conversion and a residue voltage that is the difference between the unknown voltage

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

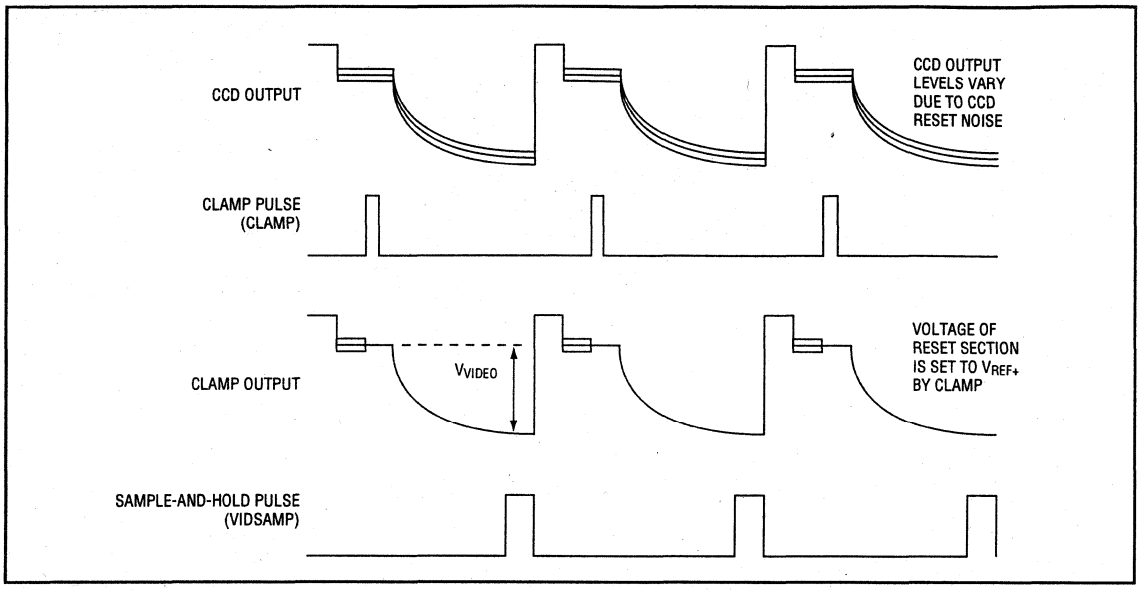


Figure 4. Correlated Double Sampler (CDS)

and the DAC output. The residue is then compared again with the flash comparators to obtain the lower four data bits.

Single-shot timers control the timing of the two conversion steps. Once both MSBs and LSBs have been determined, the comparators return to input-acquisition/auto-zero mode.

REF+ and REF-

The REF+ and REF- pins set the ADC's full-scale range. The optimum input range is +0.5V to +3.0V. Figure 6 shows a matched resistive ladder that generates the reference voltages. Four pins are available: REF+, REF-, REFBIAS, and REFGND. If 5.00V is applied to REFBIAS while REFGND is grounded, then 3.00V and 0.50V are generated at REF+ and REF-, respectively.

For increased accuracy or power-supply immunity, REF+ can be connected to an external +3.00V reference. If this is done, the accuracy must be better than ±5%. REFBIAS should be left open in this case.

Multiplexer

The mux selects either the output of the PGA or one of two other inputs to the ADC. The mux switching is break-before-make to prevent transient shorts between channels. The first two bits of the input control byte select the mux input channel (Table 1).

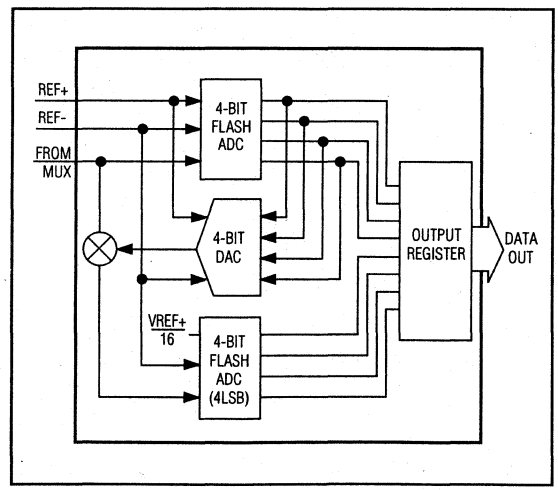


Figure 5. ADC Functional Diagram

Serial-Interface Logic

The serial interface inputs and outputs data in 8-bit words. The interface is controlled by four signals: MODE, LOAD, DATA, and SCLK.

MODE

MODE controls the direction of data transfer. When MODE = 0, data is being shifted into the MAX1101 at the DATA pin either for the mux or the PGA. When MODE = 1, the ADC output is shifted out from the MAX1101 at the DATA pin. Data is shifted in and out of the MAX1101 at the rising edge of SCLK.

LOAD

LOAD is normally low and used only when MODE = 0. Once all eight bits have been clocked in, bring LOAD high to update the MAX1101 registers.

DATA

DATA is a bidirectional I/O pin. MODE controls the direction of data transfer. When MODE = 1, DATA is configured as an output from the shift register. Data is clocked out of the shift register by SCLK's rising edge. When MODE = 0, DATA is configured as an input to the shift register, shifted in by the rising edge of SCLK. In this mode, the DATA output driver is disabled, putting DATA into a high-impedance state and allowing it to be driven externally.

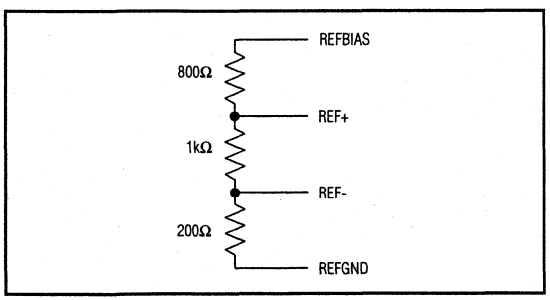


Figure 6. Reference Resistor String

Data Output

Data is clocked in and out of the device with the rising edge of SCLK. The first bit (the MSB, D7) immediately follows the falling edge of VIDSAMP (Figures 7 and 8). The first rising edge of SCLK clocks out the next bit, D6. Data is loaded into the shift register at the falling edge of VIDSAMP. Following the output of D0, DATA output is unspecified for additional SCLK pulses.

Eight-bit-wide storage and output registers hold data from the ADC and delay the data output. The timing diagram in Figure 9 shows the data latency of two VIDSAMP cycles. New data is available after the second falling edge of VIDSAMP.

Data Input

During data input, the first two bits (A0, A1) are the address, selecting either the mux or PGA. The next six bits set the input channel or PGA gain (Table 1).

CLAMP and VIDSAMP

The last two digital inputs are VIDSAMP and CLAMP. VIDSAMP controls the overall cycle timing, with one VIDSAMP cycle corresponding to one CCD pixel. The input is sampled into the ADC by the falling edge of VIDSAMP. CLAMP controls the black sample switch, which sets a reference DC voltage level (V_{REF+}) at the capacitively coupled CCDIN input. The sample switch is on when CLAMP is high.

Control and Interface Logic

The control and interface logic consists of a serial I/O port, which shifts data into and out of the MAX1101, and two registers for storing the mux channel and the PGA gain data.

Table 1. Control-Byte Format

FUNCTION	A0	A1	D5 MSB	D4	D3	D2	D1	D0 LSB
Address Analog Input Mux	0	0	—	—	—	—	—	—
Address CCD PGA	0	1	—	—	—	—	—	—
No Operation	1	X	X	X	X	X	X	X
Select CCD input	0	0	0	0	0	X	X	X
Select AIN1	0	0	0	1	0	X	X	X
Select AIN2	0	0	1	0	0	X	X	X
Set PGA Gain to -2	0	1	0	0	0	0	0	0
Set PGA Gain to -2.125	0	1	0	0	0	0	0	1
Set PGA Gain to -9.750	0	1	1	1	1	1	1	0
Set PGA Gain to -9.875	0	1	1	1	1	1	1	1

X = Don't Care

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

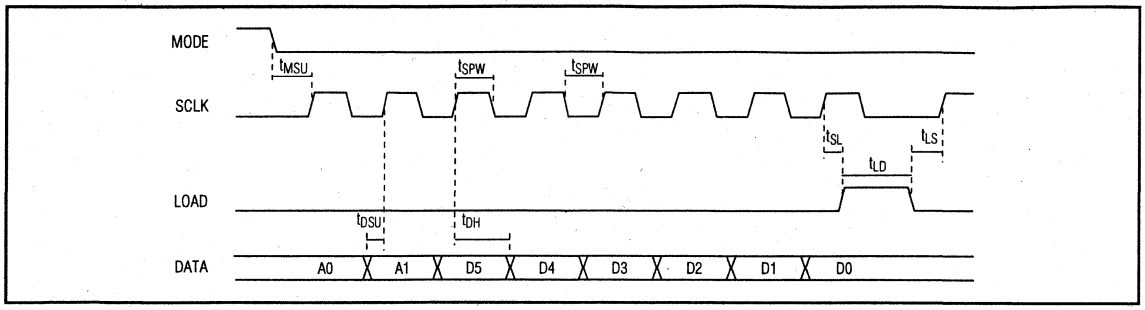


Figure 7. MODE = 0 Timing

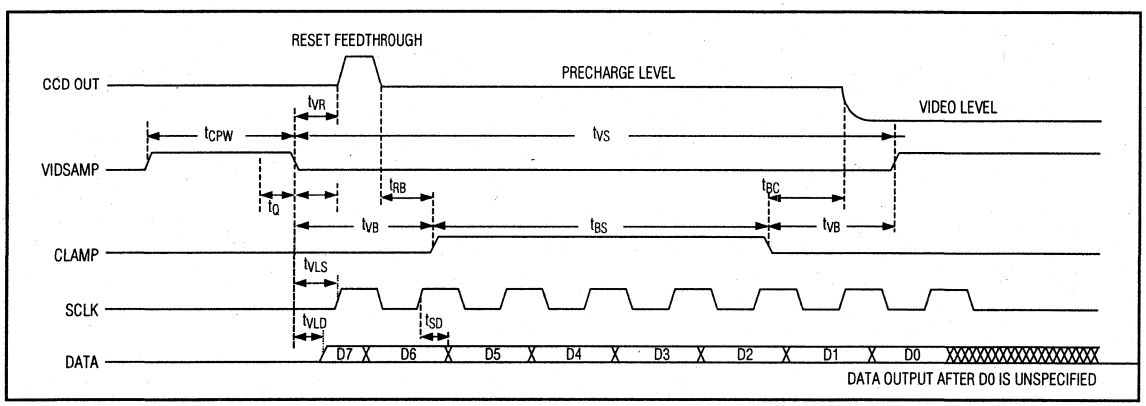


Figure 8. MODE = 1 Timing

LOAD controls the loading of data into the internal storage registers during data input. Once all eight input bits have been clocked into the shift register, a rising edge on LOAD clocks the data into the appropriate storage register (mux or PGA), decoded from the first two input bits.

The logic is divided into four blocks: the two storage registers, the serial I/O port, and a power-on reset generator. The registers are reset by the power-on reset to place them in a predictable state (input channel = CCD, PGA gain = -2) on power-up. The power-on reset typically has a 2.1µs pulse width.

The serial I/O port consists of a shift register, an 8-bit storage register, decode logic to clock input data into the appropriate storage register, and an output driver. The 8-bit storage register takes input data from the ADC.

Input Buffers and Output Drivers

The DATA driver is capable of driving 50pF load capacitance while meeting the output delay specifications given in the *Electrical Characteristics*. The gates of the P-channel and N-channel drivers are driven separately. If MODE is low, both drivers are off and the output is high impedance.

The VIDSAMP, CLAMP, SCLK, and LOAD inputs are buffered and have hysteresis to reject noise with slow-slewing signal edges.

Applications Information

MAX1101 Timing

Figure 7 shows the timing configuration when MODE = 0 and data is loaded into the MAX1101. Figure 8 shows timing when MODE = 1 and the CCD signal is digitized. Figure 9 is an expansion of Figure 8, illustrating the two-VIDSAMP-cycle data latency. Figure 10 shows the relationship of CLAMP to VIDSAMP when MODE = 1.

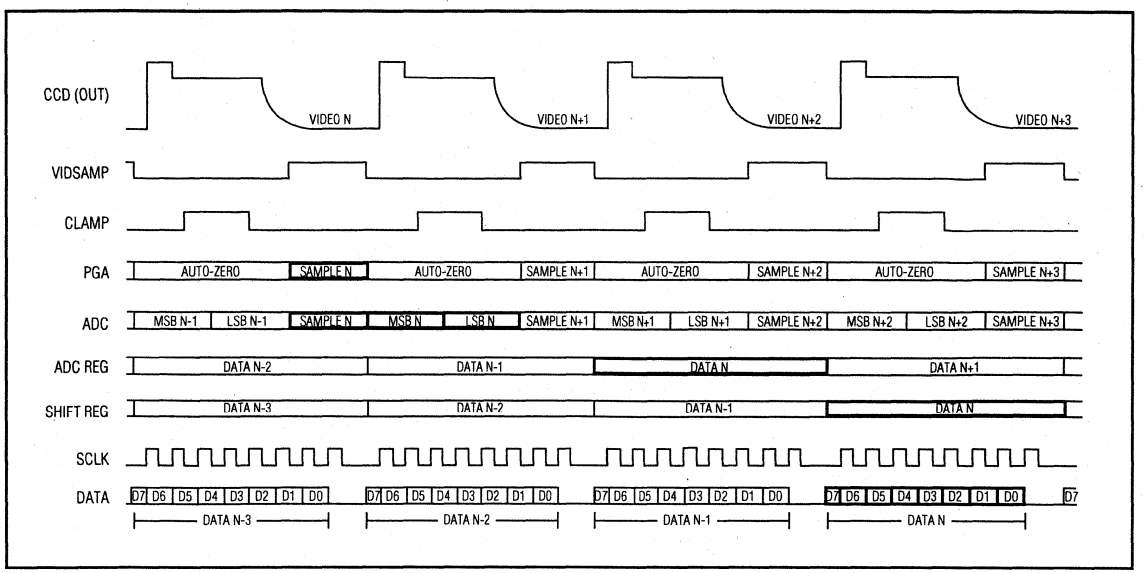


Figure 9. MODE = 1 Timing Showing Data Latency

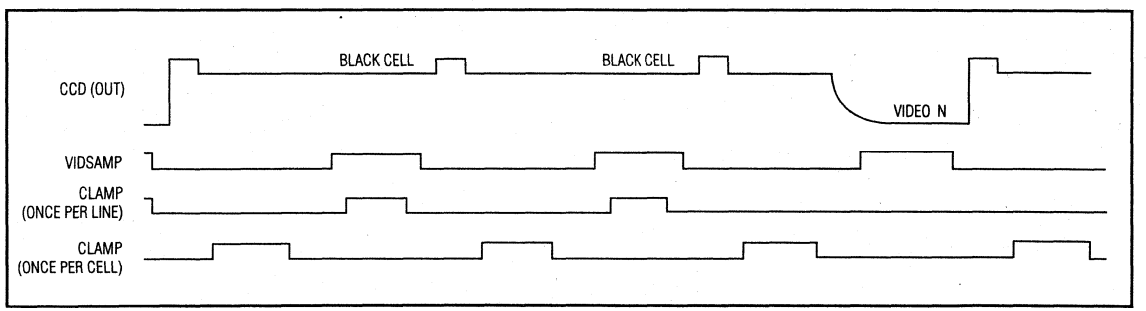


Figure 10. MODE = 1 Timing Showing Relationship of CLAMP to VIDSAMP

Input/Output Transfer Function

CCD Input

Figure 11 shows the MAX1101 transfer function for CCDIN. Coding is binary, with a -4LSB offset added to ensure that offsets within the MAX1101, which can be positive or negative, do not cause the ADC to be out of range. Full-scale input range at CCDIN is:

$$(V_{REF+} - V_{REF-}) / G_{PGA}$$

where G_{PGA} is the gain of the programmable gain amplifier.

Analog Inputs (AIN_)

The transfer function for auxiliary inputs is shown in Figure 11. Again, coding is binary and full-scale range is V_{REF-} to V_{REF+}. An offset has not been added to these channels; however, code transitions occur at the 1/2LSB point, as shown in Figure 12.

Implementing Correlated Double Sampling (CDS) or Black-Level Compensation

The CLAMP circuit in the MAX1101 can be used to either accomplish CDS or to compensate for the CCD black level. To accomplish CDS, CLAMP is activated once per

Single-Chip, 8-Bit CCD Digitizer with Clamp and 6-Bit PGA

pixel during the CCD output waveform's reset phase. To compensate for the CCD black level, CLAMP is activated during the black-pixel portion of the linear array, as shown in Figure 10. Each of these modes requires a different value of C_{EXT}, as described in the following section.

Choosing C_{EXT} for CDS

In CDS applications, C_{EXT} = 4nF. This value is the best compromise to minimize errors due to the CLAMP switch resistance/C_{EXT} time constant and switch charge injection. The following equation represents the error due to incomplete charging of C_{EXT} during integration time:

$$\varepsilon = \Delta V_{RESET} \times e^{-t/RC}$$

where ΔV_{RESET} = the maximum change in reset level from one pixel to the next, t = CLAMP pulse width, and R = CLAMP switch resistance (150Ωmax). At a sample rate of 670kHz, with t = 750nsec, a 4nF capacitor removes at least 70% of the change in reset voltage level. Typically, R = 60Ω, which corresponds to a 96% cancellation of the change in reset level.

The offset due to switch charge injection is represented by 13pC / 4nF = 3mV. Note that this error will behave like any DC offset; that is, it will be constant from pixel to pixel.

Choosing C_{EXT} in Black-Level Compensation

In activating CLAMP once per line to compensate for the CCD black level, the recommended value of C_{EXT} is governed by the following equations:

$$C_{EXT} \geq 12nF$$

and

$$C_{EXT} \leq N \times t \times 760pF/\mu sec$$

where N is the number of light-shielded cells, and t is the width of the CLAMP pulse in µsec.

The second equation ensures that the time constant formed by R x C_{EXT} is small enough that the black level is captured to within 0.5mV during the dark pixel phase. For example, in an array with 27 dark pixels at a 670kHz sample rate, with t = 750nsec, the second equation becomes $C_{EXT} \leq 15nF$. Capacitors smaller than 12nF can be used; however, offset increases due to switch charge injection, as explained in the section *Choosing C_{EXT} for CDS*.

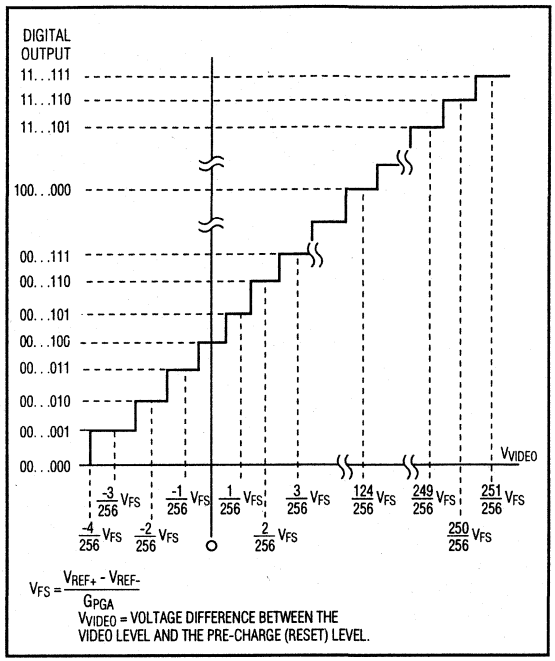


Figure 11. Transfer Function for CCDIN

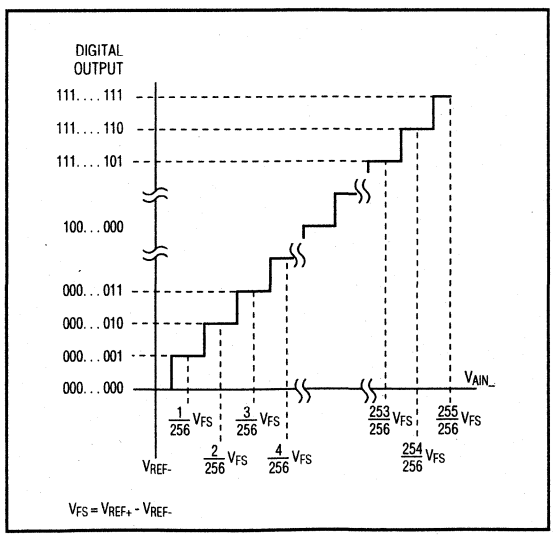


Figure 12. Transfer Function for AIN

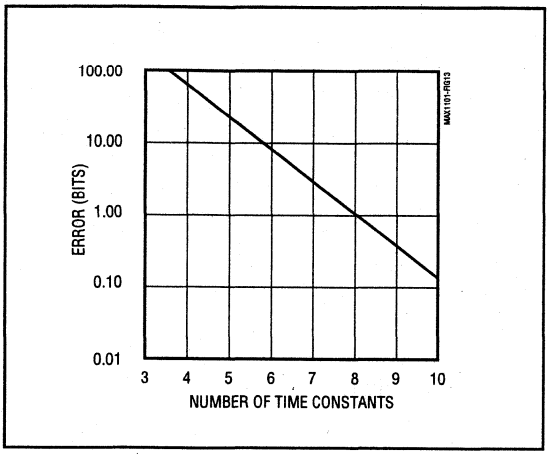


Figure 13. Black Level Error vs. C_{EXT} Time Constant at Maximum PGA Gain (1mV/bit)

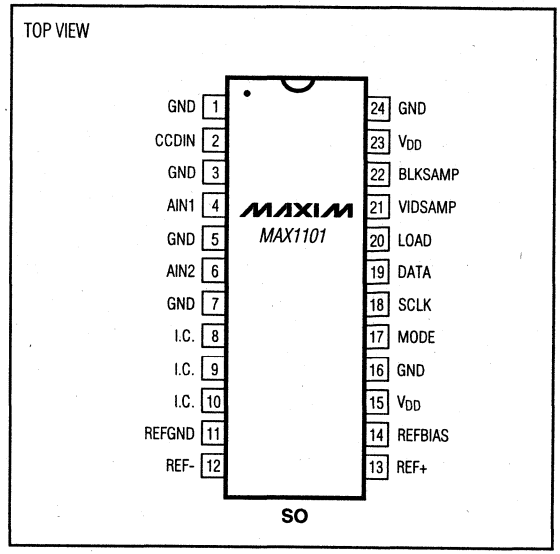
Bypassing and Layout Considerations

Solder the MAX1101 to a multilayer board (two or more layers) where the layer immediately beneath the device is a ground plane.

Connect the V_{DD} pins together at the MAX1101. Connect all ground pins together at the device.

Bypass V_{DD} to ground with at least a 0.1µF ceramic capacitor. If larger capacitors are used, tantalum is satisfactory.

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3430

19-1194; Rev 1; 5/97

EVALUATION KIT AVAILABLE

MAXIM

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

General Description

The MAX1110/MAX1111 are low-power, 8-bit, 8-channel analog-to-digital converters (ADCs) that feature an internal track/hold, voltage reference, clock, and serial interface. They operate from a single +2.7V to +5.5V supply and consume only 85µA while sampling at rates up to 50ksps. The MAX1110's 8 analog inputs and the MAX1111's 4 analog inputs are software-configurable, allowing unipolar/bipolar and single-ended/differential operation.

Successive-approximation conversions are performed using either the internal clock or an external serial-interface clock. The full-scale analog input range is determined by the 2.048V internal reference, or by an externally applied reference ranging from 1V to V_{DD}. The 4-wire serial interface is compatible with the SPI™, QSPI™, and Microwire™ serial-interface standards. A serial-strobe output provides the end-of-conversion signal for interrupt-driven processors.

The MAX1110/MAX1111 have a software-programmable, 2µA automatic power-down mode to minimize power consumption. Using power-down, the supply current is reduced to 6µA at 1ksps, and only 52µA at 10ksps. Power-down can also be controlled using the $\overline{SHDN}$ input pin. Accessing the serial interface automatically powers up the device.

The MAX1110 is available in 20-pin SSOP and DIP packages. The MAX1111 is available in small 16-pin QSOP and DIP packages.

Applications

Portable Data Logging

Hand-Held Measurement Devices

Medical Instruments

System Diagnostics

Solar-Powered Remote Systems

4–20mA-Powered Remote Data-Acquisition Systems

Pin Configurations appear at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Features

- **+2.7V to +5.5V Single Supply**
- **Low Power: 85µA at 50ksps**
  6µA at 1ksps
- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1110)**
- **4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1111)**
- **Internal Track/Hold; 50kHz Sampling Rate**
- **Internal 2.048V Reference**
- **SPI/QSPI/Microwire-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Small Packages:**
  20-Pin SSOP (MAX1110)
  16-Pin QSOP (MAX1111)

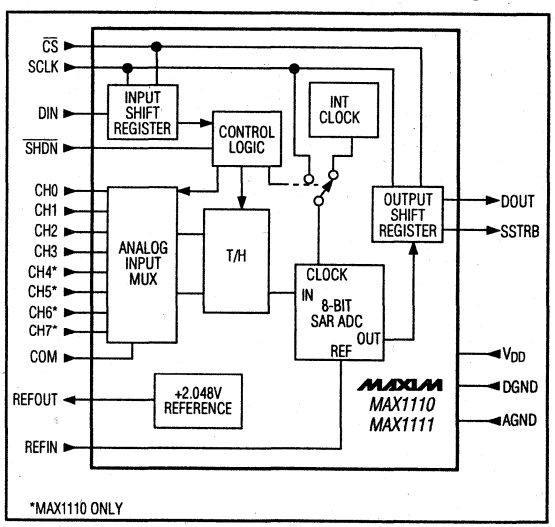
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1110CPP	0°C to +70°C	20 Plastic DIP
MAX1110CAP	0°C to +70°C	20 SSOP
MAX1110C/D	0°C to +70°C	Dice*

**Dice are specified at T_A = +25°C, DC parameters only.*

Ordering Information continued at end of data sheet.

Functional Diagram



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+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to 6V
AGND to DGND .....-0.3V to 0.3V
CH0–CH7, COM, REFIN,
REFOUT to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to 6V
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16 Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16 QSOP (derate 8.30mW/°C above +70°C) 667mW
16 CERDIP (derate 10.00mW/°C above +70°C) 800mW
20 Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20 SSOP (derate 8.00mW/°C above +70°C) 640mW
20 CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX1110C_P/MAX1111C_E.....0°C to +70°C
MAX1110E_P/MAX1111E_E .....-40°C to +85°C
MAX1110MJP/MAX1111MJE.....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL	V_{DD} = 2.7V to 3.6V		±0.15	±0.5	LSB
		V_{DD} = 5.5V (Note 2)		±0.2		
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		V_{DD} = 2.7V to 3.6V		±0.35	±1	LSB
		V_{DD} = 5.5V (Note 2)		±0.5		
Gain Error (Note 3)		Internal or external reference			±1	LSB
Gain Temperature Coefficient		External reference, 2.048V		±0.8		ppm/°C
Total Unadjusted Error	TUE			±1		LSB
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10.034kHz sine-wave input, 2.048Vp-p, 50ksps, 500kHz external clock)						
Signal-to-Noise and Distortion Ratio	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			68		dB
Channel-to-Channel Crosstalk		$V_{CH_}$ = 2.048Vp-p, 25kHz (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		1.5		MHz
Full-Power Bandwidth				800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CONVERSION RATE							
Conversion Time (Note 5)	t_{CONV}	Internal clock			25	55	µs
		External clock, 500kHz, 10 clocks/conversion		20			
Track/Hold Acquisition Time	t_{ACQ}	External clock, 2MHz		1			µs
Aperture Delay					10		ns
Aperture Jitter					<50		ps
Internal Clock Frequency					400		kHz
External Clock-Frequency Range		(Note 6)		50		500	kHz
		Used for data transfer only				2	MHz
ANALOG INPUT							
Input Voltage Range, Single-Ended and Differential (Note 7)		Unipolar input, COM = 0V		0		V_{REFIN}	V
		Bipolar input, COM = V_{REFIN} / 2				COM ± V_{REFIN} / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}			±0.01	±1	µA
Input Capacitance					18		pF
INTERNAL REFERENCE							
REFOUT Voltage				1.968	2.048	2.128	V
REFOUT Short-Circuit Current					3.5		mA
REFOUT Temperature Coefficient					±50		ppm/°C
Load Regulation (Note 8)		0mA to 0.5mA output load			2.5		mV
Capacitive Bypass at REFOUT				1			µF
EXTERNAL REFERENCE AT REFIN							
Input Voltage Range				1		V_{DD} + 50mV	V
Input Current		(Note 9)			1	20	µA
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			2.7		5.5	V
Supply Current (Note 2)	I_{DD}	V_{DD} = 2.7V to 3.6V Full-scale input C_{LOAD} = 10pF	Operating mode		85	250	µA
			Reference disabled		45		
		V_{DD} = 5.5V Full-scale input C_{LOAD} = 10pF	Operating mode		120	250	
			Reference disabled		80		
		Power-down	Software		2		
			$\overline{SHDN}$ at DGND		3.2	10	
Power-Supply Rejection (Note 10)	PSR	V_{DD} = 2.7V to 3.6V; external reference, 2.048V; full-scale input			±0.4	±4	mV

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+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$	2			V
		$V_{DD} > 3.6V$	3			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	Digital inputs = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ INPUT						
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD} / 2		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}			±4	µA
$\overline{SHDN}$ Maximum Allowed Leakage for Mid-Input		$\overline{SHDN}$ = open			±100	nA
DIGITAL OUTPUTS: DOUT, SSTRB						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 6)			15	pF

TIMING CHARACTERISTICS (Figures 8 and 9)

(V_{DD} = +2.7V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}			1			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 100pF	MAX111_C/E	20		200	ns
			MAX111_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	Figure 1, external clock mode only, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	Figure 2, external clock mode only, C_{LOAD} = 100pF				240	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Figure 11, internal clock mode only		0			ns
Wakeup Time	t_{WAKE}	External reference			20		µs
		Internal reference (Note 11)			12		ms

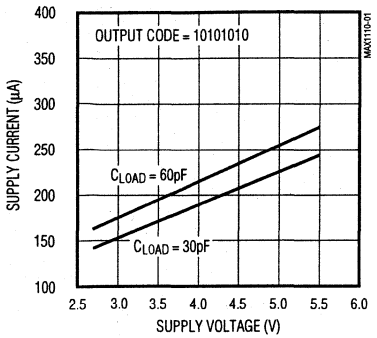
Note 1: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
Note 2: See *Typical Operating Characteristics.*
Note 3: V_{REFIN} = 2.048V, offset nulled.
Note 4: On-channel grounded; sine wave applied to all off-channels.
Note 5: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: Common-mode range for the analog inputs is from AGND to V_{DD}.
Note 8: External load should not change during the conversion for specified accuracy.
Note 9: External reference at 2.048V, full-scale input, 500kHz external clock.
Note 10: Measured as | V_{FS} (2.7V) - V_{FS} (3.6V) |.
Note 11: 1µF at REFOUT; internal reference settling to 0.5LSB.

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

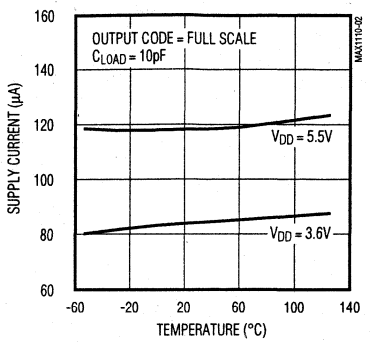
Typical Operating Characteristics

(V_{DD} = +2.7V; f_{SCLK} = 500kHz; external clock (50% duty cycle); R_L = ∞; T_A = +25°C, unless otherwise noted.)

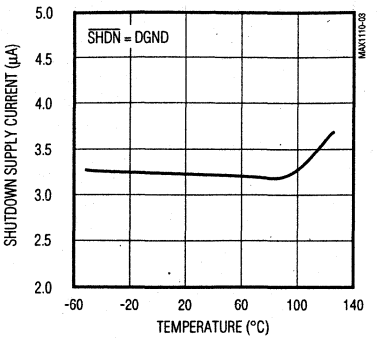
SUPPLY CURRENT vs. SUPPLY VOLTAGE



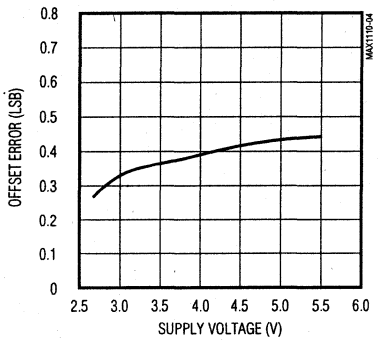
SUPPLY CURRENT vs. TEMPERATURE



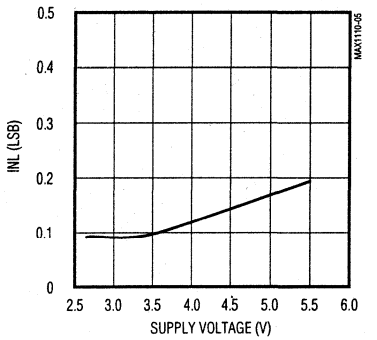
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



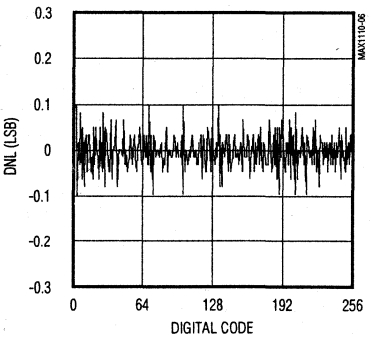
OFFSET ERROR vs. SUPPLY VOLTAGE



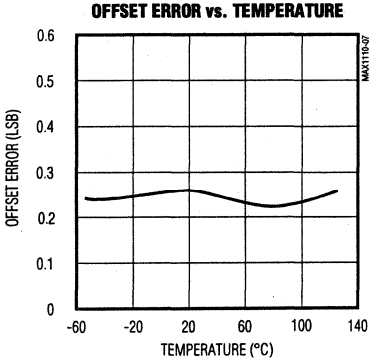
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



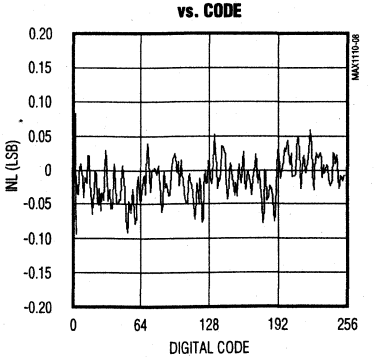
DIFFERENTIAL NONLINEARITY vs. CODE



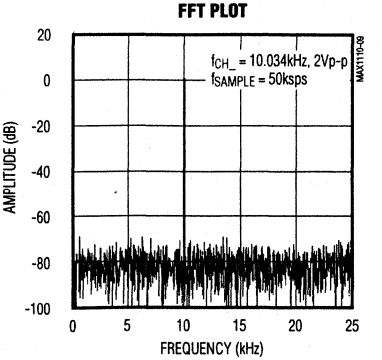
OFFSET ERROR vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



FFT PLOT



Pin Description

PIN		NAME	FUNCTION
MAX1110	MAX1111		
1–4	1–4	CH0–CH3	Sampling Analog Inputs
5–8	—	CH4–CH7	Sampling Analog Inputs
9	5	COM	Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	6	$\overline{SHDN}$	Three-Level Shutdown Input. Normally floats. Pulling $\overline{SHDN}$ low shuts the MAX1110/MAX1111 down to 10µA (max) supply current; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high shuts down the internal reference.
11	7	REFIN	Reference Voltage Input for Analog-to-Digital Conversion. Connect to REFOUT to use the internal reference.
12	8	REFOUT	Internal Reference Generator Output. Bypass with a 1µF capacitor to AGND.
13	9	AGND	Analog Ground
14	10	DGND	Digital Ground
15	11	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	12	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1110/MAX1111 begin the A/D conversion and goes high when the conversion is done. In external clock mode, SSTRB pulses high for two clock periods before the MSB is shifted out. High impedance when $\overline{CS}$ is high (external clock mode only).
17	13	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge. The voltage at DIN may exceed V_{DD} (up to 5.5V).
18	14	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. The voltage at $\overline{CS}$ may exceed V_{DD} (up to 5.5V).
19	15	SCLK	Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 45% to 55%). The voltage at SCLK may exceed V_{DD} (up to 5.5V).
20	16	V_{DD}	Positive Supply Voltage, +2.7V to +5.5V

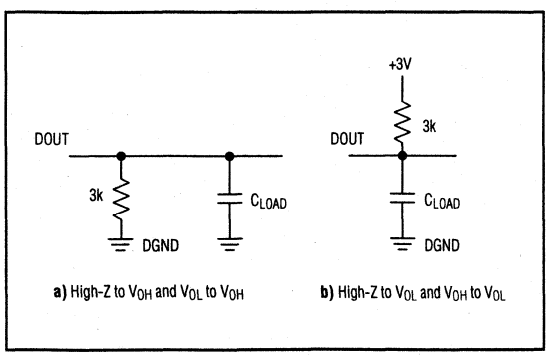


Figure 1. Load Circuits for Enable Time

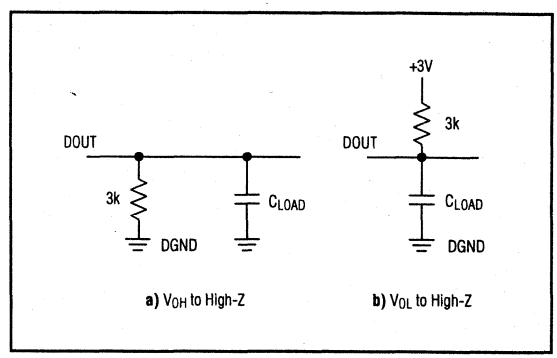


Figure 2. Load Circuits for Disable Time

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Detailed Description

The MAX1110/MAX1111 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows the Typical Operating Circuit.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in Figure 4, the equivalent input circuit. In single-ended mode, IN+ is internally switched to the selected input channel, CH_, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the MAX1110 channels with Table 1 and the MAX1111 channels with Table 2.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor CHOLD. The acquisition interval spans two SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on CHOLD as a sample of the signal at IN+. The conversion interval begins with the input multiplexer switching CHOLD from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF x (V_{IN+} - V_{IN-}) from CHOLD to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the sixth bit of the 8-bit control byte has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control byte has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input; if it is set up for differential inputs, IN- connects to the "-" input, and the difference (IN+ - IN-) is sampled. At the end of the conversion, the positive input connects back to IN+, and CHOLD charges to the input signal.

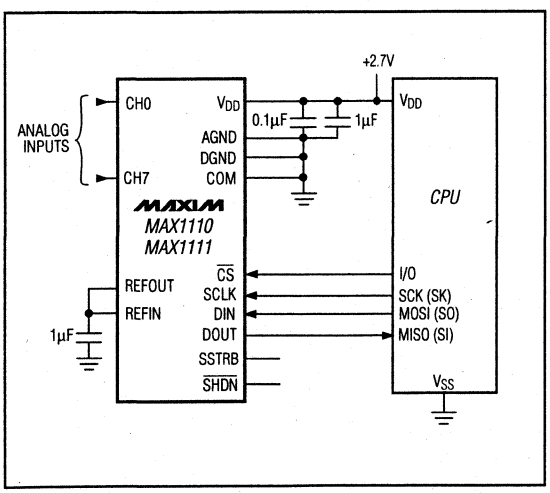


Figure 3. Typical Operating Circuit

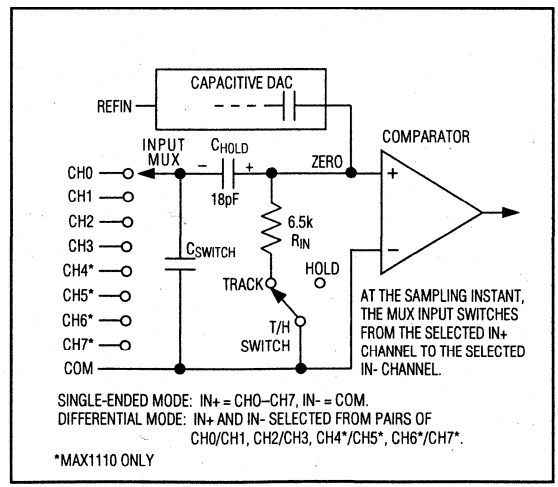


Figure 4. Equivalent Input Circuit

Table 1a. MAX1110 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 1b. MAX1110 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

Table 2a. MAX1111 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	X	+				–
1	0	X		+			–
0	1	X			+		–
1	1	X				+	–

Table 2b. MAX1111 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	X	+	–		
0	1	X			+	–
1	0	X	–	+		
1	1	X			–	+

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 6 \times (R_S + R_{IN}) \times 18pF$$

where R_{IN} = 6.5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1µs. Note that source impedances below 2.4kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Inputs

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from (AGND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

The MAX1110/MAX1111 can be configured for differential or single-ended inputs with bits 2 and 3 of the control byte (Table 3). In single-ended mode, the analog inputs are internally referenced to COM with a full-scale input range from COM to V_{REFIN} + COM. For bipolar operation, set COM to V_{REFIN} / 2.

In differential mode, choosing unipolar mode sets the differential input range at 0V to V_{REFIN}. In unipolar mode, the output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to ±V_{REFIN} / 2. Note that in this mode, the common-mode input range includes both supply rails. Refer to Table 4 for input voltage ranges.

Quick Look

To quickly evaluate the MAX1110/MAX1111's analog performance, use the circuit of Figure 5. The MAX1110/MAX1111 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds

Table 3. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	Select which of the input channels are to be used for the conversion (Tables 1 and 2).
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. Select differential operation if bipolar mode is used. See Table 4.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured. See Tables 1 and 2.
1	PD1	**1** = fully operational, **0** = power-down. Selects fully operational or power-down mode.
0 (LSB)	PD0	**1** = external clock mode, **0** = internal clock mode. Selects external or internal clock mode.

Table 4. Full-Scale and Zero-Scale Voltages

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
V_{REFIN} + COM	COM	+V_{REFIN} / 2 + COM	COM	-V_{REFIN} / 2 + COM

in control bytes of $FF (hex), which trigger single-ended, unipolar conversions on CH7 (MAX1110) or CH3 (MAX1111) in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the most significant bit of the 8-bit conversion result is shifted out of DOUT. Varying the analog input alters the output code. A total of 10 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on SCLK's falling edge.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1110/MAX1111's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit at DIN defines the MSB of the control byte. Until this first start bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 3 shows the control-byte format.

The MAX1110/MAX1111 are compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the Typical Operating Circuit (Figure 3), the simplest software interface requires three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 8-bit conversion result). Figure 6 shows the MAX1110/MAX1111 common serial-interface connections.

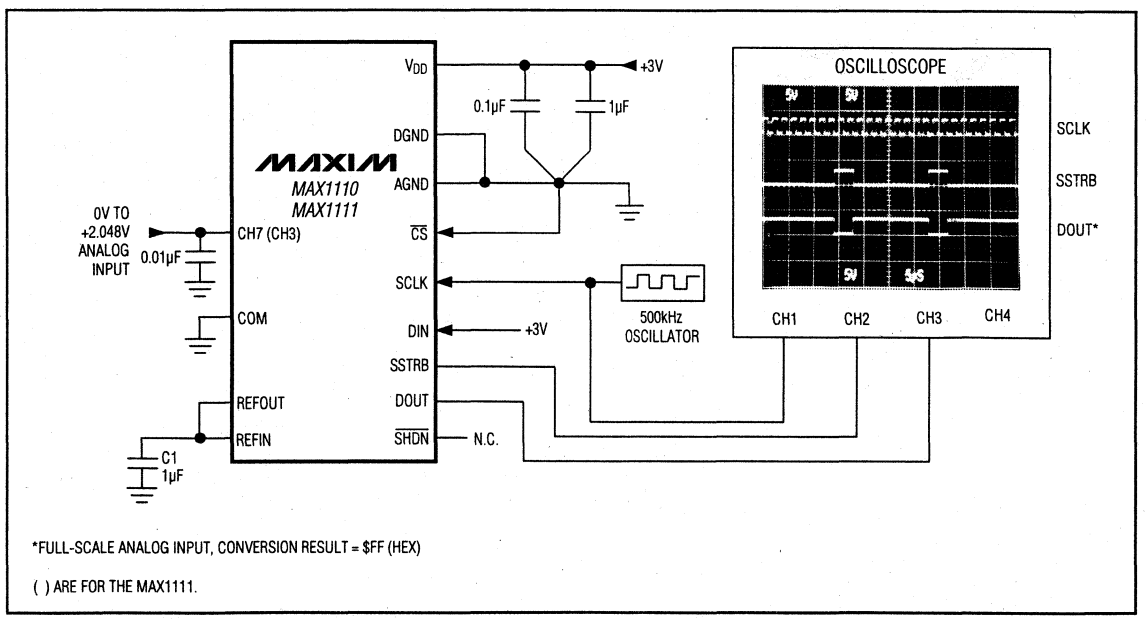


Figure 5. Quick-Look Circuit

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

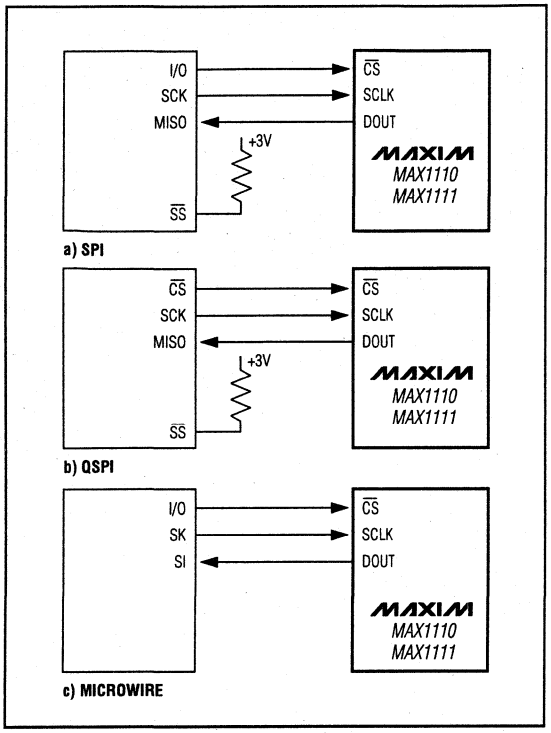


Figure 6. Common Serial-Interface Connections to the MAX1110/MAX1111

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 50kHz to 500kHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 7 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with two leading zeros and six trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 1ms, to avoid excessive T/H droop.

Digital Inputs

$\overline{CS}$, SCLK, and DIN can accept input signals up to 5.5V, regardless of the supply voltages. This allows the MAX1110/MAX1111 to accept digital inputs from both 3V and 5V systems.

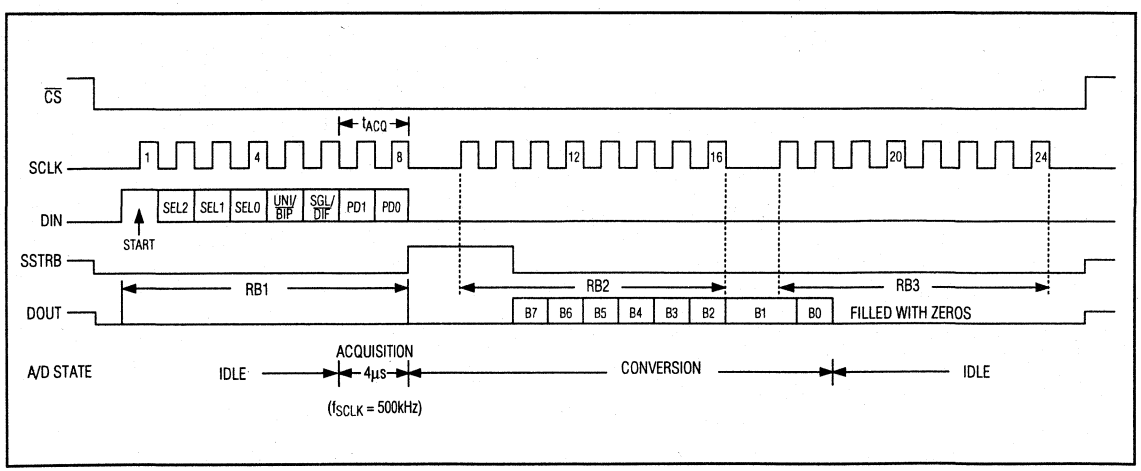


Figure 7. Single-Conversion Timing, External Clock Mode, 24 Clocks

Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format.

Clock Modes

The MAX1110/MAX1111 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit PD0 of the control byte programs the clock mode. Figures 8–11 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next eight SCLK falling edges (Figure 7). After the eight data bits are clocked out, subsequent clock pulses clock out zeros from the DOUT pin.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 9 shows the SSTRB timing in external clock mode.

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.

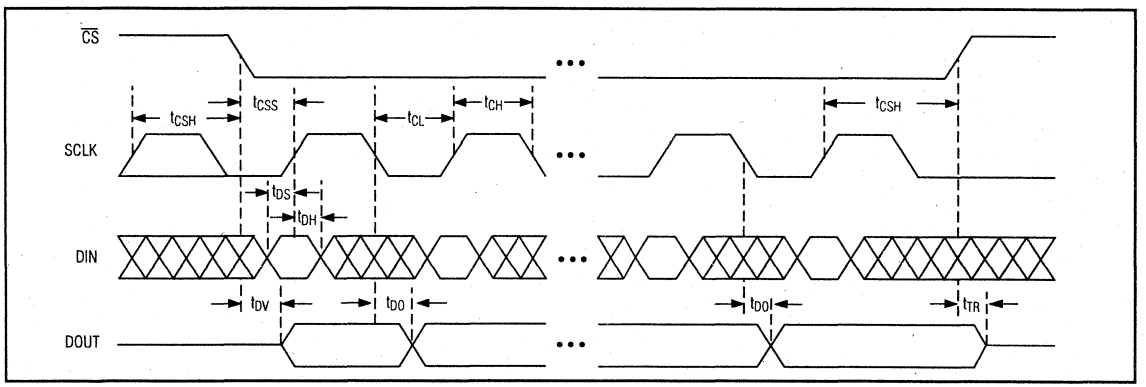


Figure 8. Detailed Serial-Interface Timing

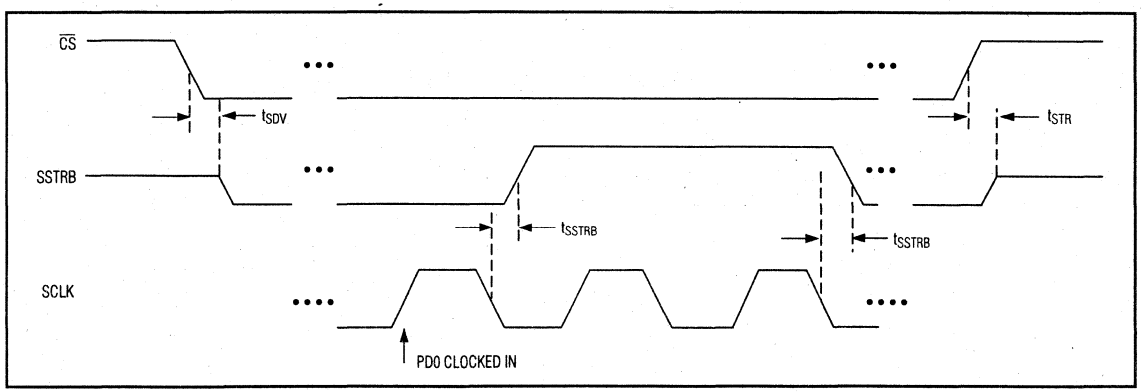


Figure 9. External Clock Mode SSTRB Detailed Timing

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

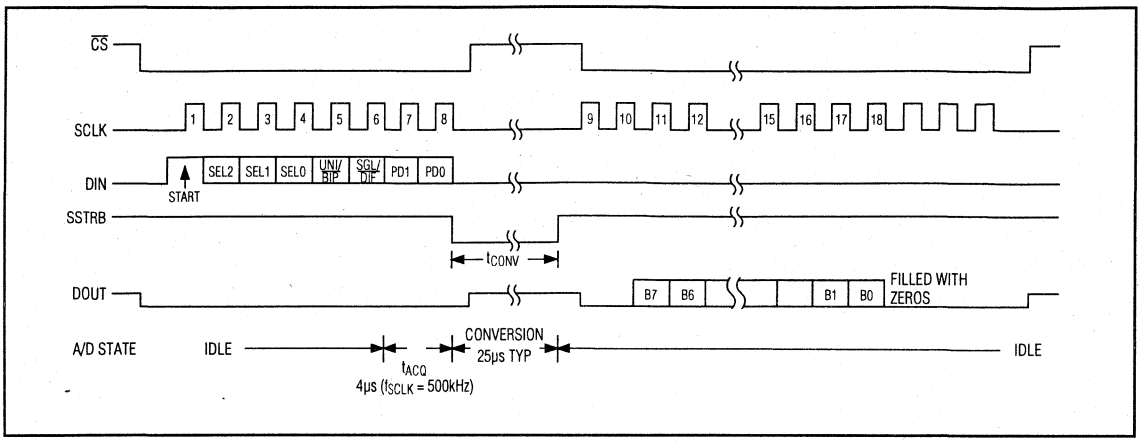


Figure 10. Internal Clock Mode Timing

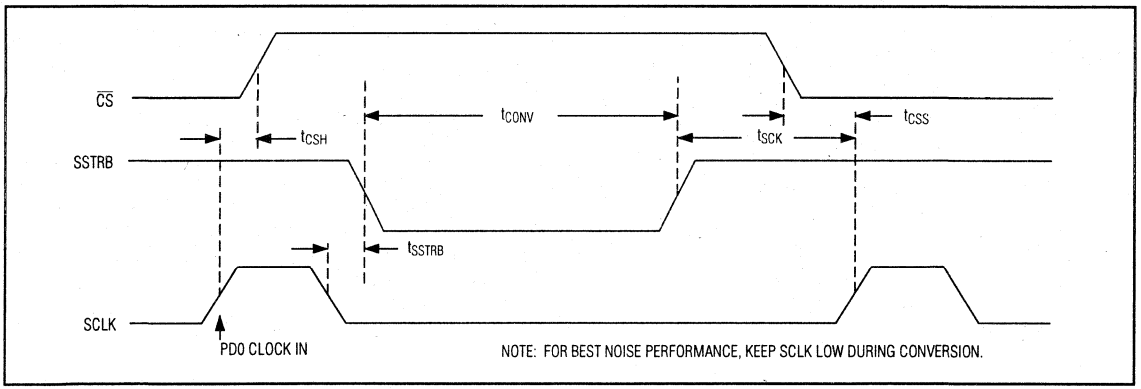


Figure 11. Internal Clock Mode SSTRB Detailed Timing

Internal Clock

Internal clock mode frees the µP from the burden of running the SAR conversion clock. This allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for 25µs (typically), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 10). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1110/MAX1111 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 11 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1110/MAX1111 at clock rates up to 2MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1µs.

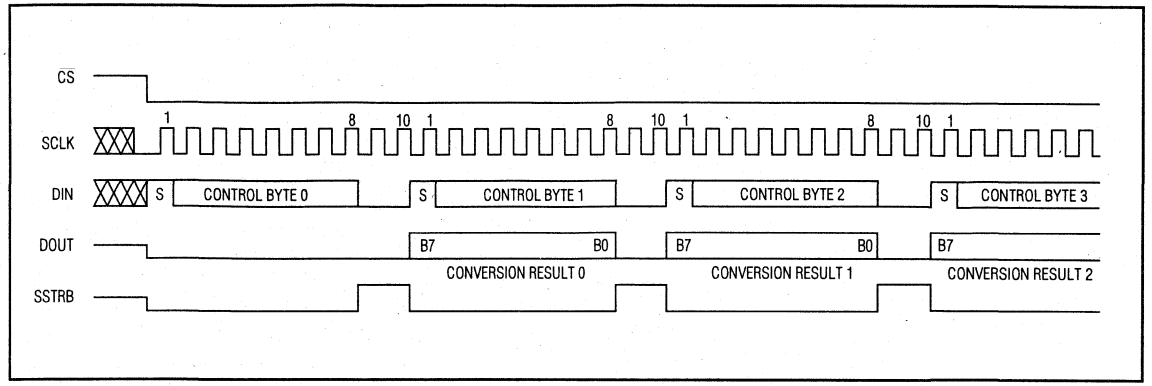


Figure 12a. Continuous Conversions, External Clock Mode, 10 Clocks/Conversion Timing

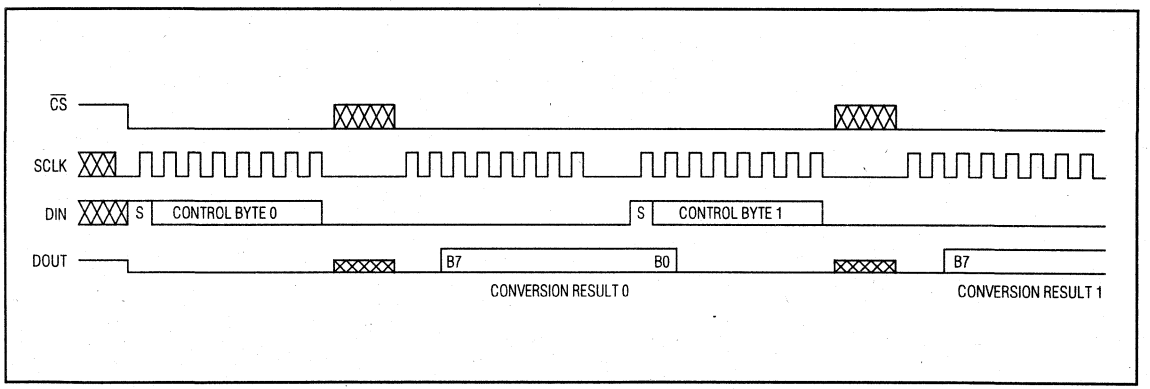


Figure 12b. Continuous Conversions, External Clock Mode, 16 Clocks/Conversion Timing

Data Framing

The falling edge of $\overline{CS}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after the MSB of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1110/MAX1111 can run is 10 clocks per conversion. Figure 12a shows the serial-interface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1110/MAX1111. Figure 12b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1110/MAX1111 in internal clock mode. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. No conversions should be performed until the reference voltage has stabilized (see *Electrical Characteristics*).

Power-Down

When operating at speeds below the maximum sampling rate, the MAX1110/MAX1111's automatic power-down mode can save considerable power by placing the converters in a low-current shutdown state between conversions. Figure 13 shows the average supply current as a function of the sampling rate.

Select power-down with PD1 of the DIN control byte with $\overline{SHDN}$ high or floating (Table 3). Pull $\overline{SHDN}$ low at any time to shut down the converters completely. $\overline{SHDN}$ overrides PD1 of the control byte. Figures 14a and 14b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bit PD1 of the control byte. When software power-down is asserted, the ADCs continue to operate in the last specified clock mode until the conversion is complete. The ADCs then power down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1110/MAX1111 have entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, which powers up the MAX1110/MAX1111. If the DIN byte contains PD1 = 1, then the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Hard-Wired Power-Down and Internal Reference State

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL REFERENCE
1	Enabled	Disabled
Floating	Enabled	Enabled
0	Power-Down	Disabled

Hard-Wired Power-Down

Pulling $\overline{SHDN}$ low places the converters in hard-wired power-down. Unlike software power-down, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the state of the internal reference (Table 5). Letting $\overline{SHDN}$ float enables the internal 2.048V voltage reference. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 1MΩ x C_{LOAD}, where C_{LOAD} is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high disables the internal reference, which saves power when using an external reference.

External Reference

An external reference between 1V and V_{DD} should be connected directly at the REFIN terminal. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20µA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1µF capacitor.

If an external reference is used with the MAX1110/MAX1111, tie $\overline{SHDN}$ to V_{DD} to disable the internal reference and decrease power consumption.

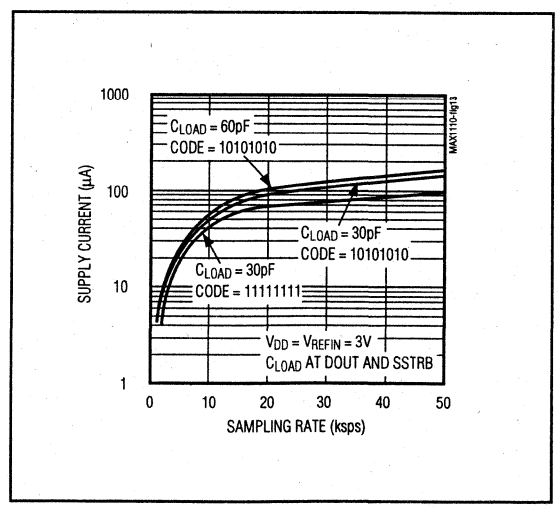


Figure 13. Average Supply Current vs. Sampling Rate

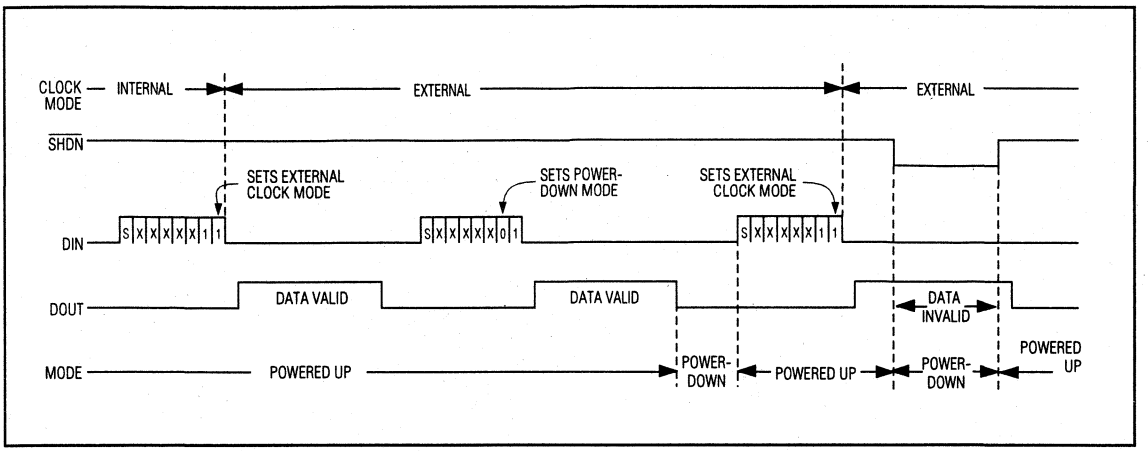


Figure 14a. Power-Down Modes, External Clock Timing Diagram

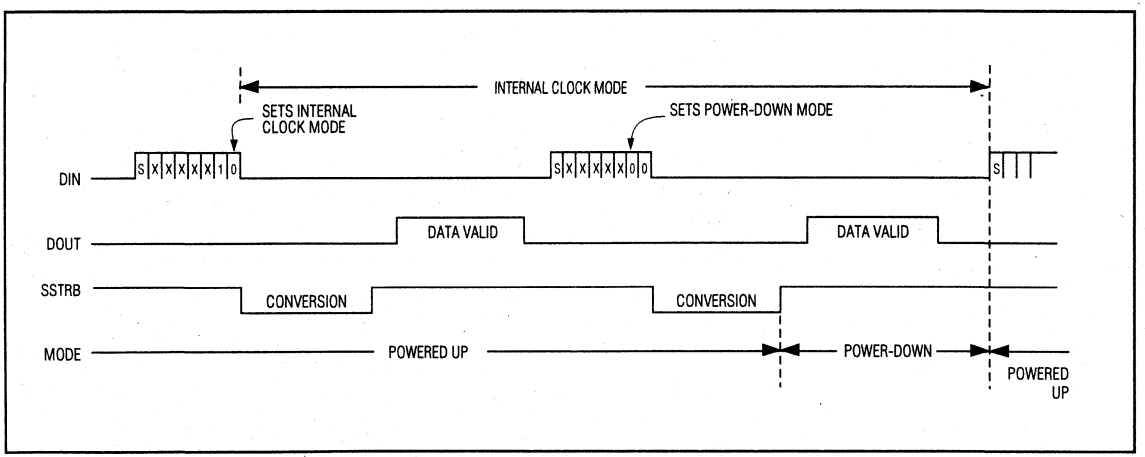


Figure 14b. Power-Down Modes, Internal Clock Timing Diagram

Internal Reference

To use the MAX1110/MAX1111 with the internal reference, connect REFIN to REFOUT. The full-scale range of the MAX1110/MAX1111 with the internal reference is typically 2.048V with unipolar inputs, and ±1.024V with bipolar inputs. The internal reference should be bypassed to AGND with a 1µF capacitor placed as close to the REFIN pin as possible.

Transfer Function

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 15 depicts the nominal, unipolar I/O transfer function, and Figure 16 shows the bipolar I/O transfer function when using a 2.048V reference. Code transitions occur at integer LSB values. Output coding is binary, with 1LSB = 8mV (2.048V/256) for unipolar operation and 1LSB = 8mV [(2.048V/2 - -2.048V/2)/256] for bipolar operation.

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

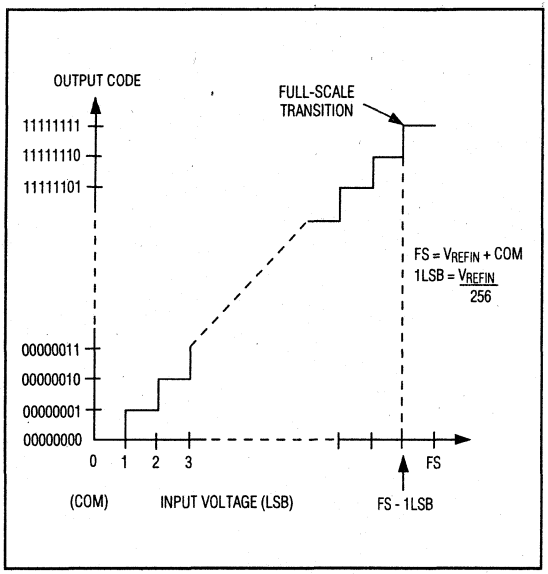


Figure 15. Unipolar Transfer Function

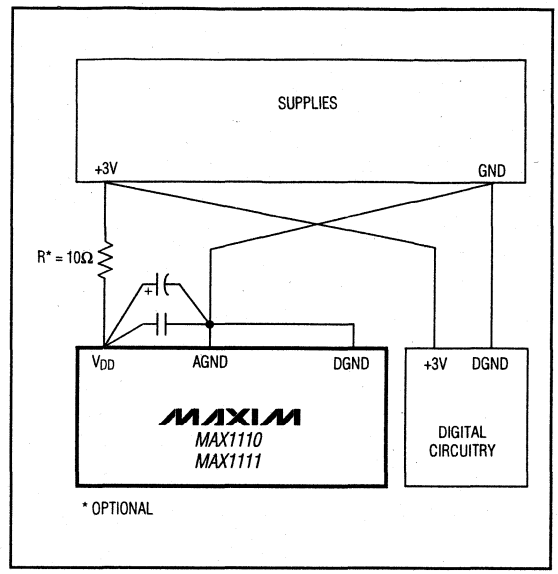


Figure 17. Power-Supply Grounding Connections

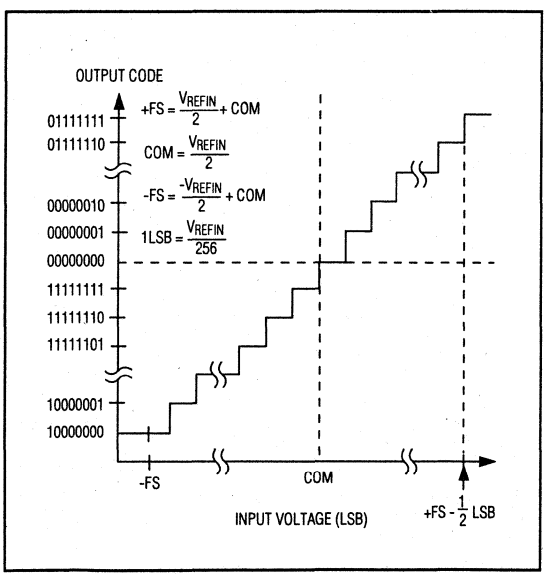


Figure 16. Bipolar Transfer Function

Layout, Grounding, and Bypassing

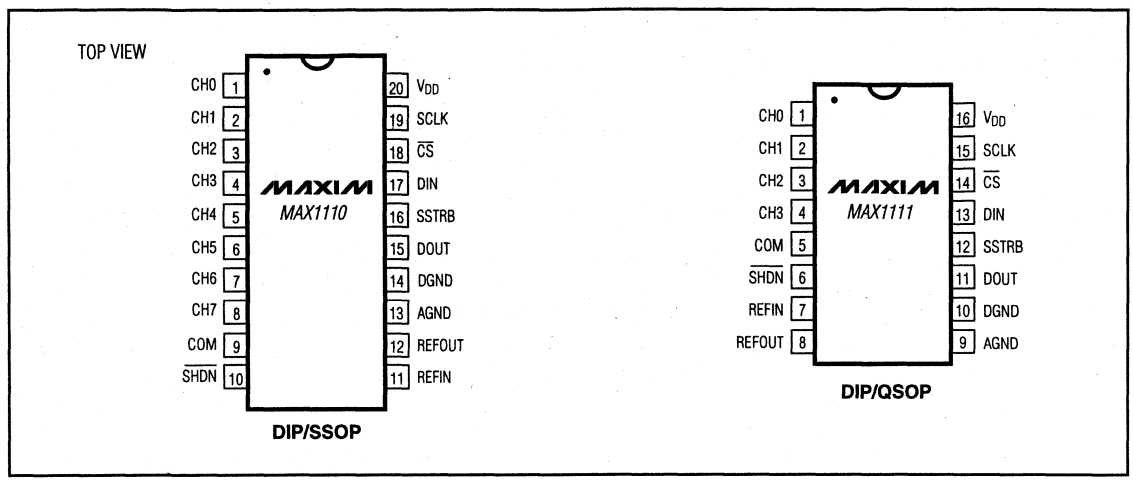
For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the V_{DD} pin of the MAX1110/MAX1111. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected to form a lowpass filter.

+2.7V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Pin Configurations



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1110EPP	-40°C to +85°C	20 Plastic DIP
MAX1110EAP	-40°C to +85°C	20 SSOP
MAX1110MJP	-55°C to +125°C	20 CERDIP**
MAX1111CPE	0°C to +70°C	16 Plastic DIP
MAX1111CEE	0°C to +70°C	16 QSOP
MAX1111EPE	-40°C to +85°C	16 Plastic DIP
MAX1111EEE	-40°C to +85°C	16 QSOP
MAX1111MJE	-55°C to +125°C	16 CERDIP**

***Contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 1996

SUBSTRATE CONNECTED TO DGND

7

19-1231; Rev 0; 6/97

EVALUATION KIT AVAILABLE

MAXIM

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

General Description

The MAX1112/MAX1113 are low-power, 8-bit, 8-channel analog-to-digital converters (ADCs) that feature an internal track/hold, voltage reference, clock, and serial interface. They operate from a single +4.5V to +5.5V supply and consume only 135µA while sampling at rates up to 50ksps. The MAX1112's 8 analog inputs and the MAX1113's 4 analog inputs are software-configurable, allowing unipolar/bipolar and single-ended/differential operation.

Successive-approximation conversions are performed using either the internal clock or an external serial-interface clock. The full-scale analog input range is determined by the 4.096V internal reference, or by an externally applied reference ranging from 1V to V_{DD}. The 4-wire serial interface is compatible with the SPI™, QSPI™, and Microwire™ serial-interface standards. A serial-strobe output provides the end-of-conversion signal for interrupt-driven processors.

The MAX1112/MAX1113 have a software-programmable, 2µA automatic power-down mode to minimize power consumption. Using power-down, the supply current is reduced to 13µA at 1ksps, and only 82µA at 10ksps. Power-down can also be controlled using the $\overline{SHDN}$ input pin. Accessing the serial interface automatically powers up the device.

The MAX1112 is available in 20-pin SSOP and DIP packages. The MAX1113 is available in small 16-pin QSOP and DIP packages.

Applications

Portable Data Logging

Hand-Held Measurement Devices

Medical Instruments

System Diagnostics

Solar-Powered Remote Systems

4–20mA-Powered Remote Data-Acquisition Systems

Pin Configurations appear at end of data sheet.

SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

Features

- **+4.5V to +5.5V Single Supply**
- **Low Power: 135µA at 50ksps**
  13µA at 1ksps
- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1112)**
- **4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1113)**
- **Internal Track/Hold; 50kHz Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/QSPI/Microwire-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Available in a Small 16-Pin QSOP Package (MAX1113)**

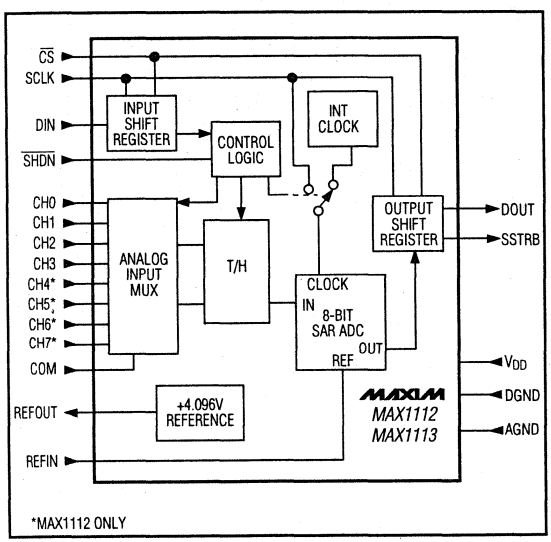
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1112CPP	0°C to +70°C	20 Plastic DIP
MAX1112CAP	0°C to +70°C	20 SSOP
MAX1112C/D	0°C to +70°C	Dice*

**Dice are specified at T_A = +25°C, DC parameters only.*

Ordering Information continued at end of data sheet.

Functional Diagram



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For small orders, phone 408-737-7600 ext. 3468.

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to 6V
AGND to DGND .....-0.3V to 0.3V
CH0–CH7, COM, REFIN,
REFOUT to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to 6V
Digital Outputs to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
16 Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16 QSOP (derate 8.30mW/°C above +70°C) 667mW
16 CERDIP (derate 10.00mW/°C above +70°C) 800mW
20 Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20 SSOP (derate 8.00mW/°C above +70°C) 640mW
20 CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX1112C_P/MAX1113C_E .....0°C to +70°C
MAX1112E_P/MAX1113E_E .....-40°C to +85°C
MAX1112MJP/MAX1113MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.5V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY						
Resolution			8			Bits
Relative Accuracy (Note 1)	INL			±0.1	±0.5	LSB
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error				±0.3	±1	LSB
Gain Error (Note 2)		Internal or external reference			±1	LSB
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
Total Unadjusted Error	TUE	MAX111_C/E		±1		LSB
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10.034kHz sine-wave input, 4.096Vp-p, 50ksps, 500kHz external clock)						
Signal-to-Noise and Distortion Ratio	SINAD			49		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			68		dB
Channel-to-Channel Crosstalk		$V_{CH_}$ = 4.096Vp-p, 25kHz (Note 3)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		1.5		MHz
Full-Power Bandwidth				800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CONVERSION RATE							
Conversion Time (Note 4)	t_{CONV}	Internal clock			25	55	µs
		External clock, 500kHz, 10 clocks/conversion		20			
Track/Hold Acquisition Time	t_{ACQ}	External clock, 2MHz		1			µs
Aperture Delay					10		ns
Aperture Jitter					<50		ps
Internal Clock Frequency					400		kHz
External Clock-Frequency Range		(Note 5)		50		500	kHz
		Used for data transfer only				2	MHz
ANALOG INPUT							
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar input, COM = 0V		0		V_{REFIN}	V
		Bipolar input, COM = V_{REFIN} / 2				COM ± V_{REFIN} / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}			±0.01	±1	µA
Input Capacitance					18		pF
INTERNAL REFERENCE							
REFOUT Voltage				3.936	4.096	4.256	V
REFOUT Short-Circuit Current					6		mA
REFOUT Temperature Coefficient					±50		ppm/°C
Load Regulation (Note 7)		0mA to 0.5mA output load			4.5		mV
Capacitive Bypass at REFOUT				1			µF
EXTERNAL REFERENCE AT REFIN							
Input Voltage Range				1		V_{DD} + 50mV	V
Input Current		(Note 8)			1	20	µA
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.5		5.5	V
Supply Current	I_{DD}	Full-scale input C_{LOAD} = 10pF	Operating mode		135	250	µA
			Reference disabled		95		
		Power-down	Software		2		
			$\overline{SHDN}$ at DGND		3.2	10	
Power-Supply Rejection (Note 9)	PSR	V_{DD} = 4.5V to 5.5V; external reference, 4.096V; full-scale input			±0.4	±4	mV

7

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.5V to +5.5V; unipolar input mode; COM = 0V; f_{SCLK} = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}		3			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	Digital inputs = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 5)			15	pF
$\overline{SHDN}$ INPUT						
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		V_{DD} / 2		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}			±4	µA
$\overline{SHDN}$ Maximum Allowed Leakage for Mid-Input		$\overline{SHDN}$ = open			±100	nA
DIGITAL OUTPUTS: DOUT, SSTRB						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 5)			15	pF

TIMING CHARACTERISTICS (Figures 8 and 9)

(V_{DD} = +4.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Track/Hold Acquisition Time	t_{ACQ}			1			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}			0			ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 100pF	MAX111_C/E	20		200	ns
			MAX111_M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 5)	t_{SDV}	Figure 1, external clock mode only, C_{LOAD} = 100pF				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 5)	t_{STR}	Figure 2, external clock mode only, C_{LOAD} = 100pF				240	ns
SSTRB Rise to SCLK Rise (Note 5)	t_{SCK}	Figure 11, internal clock mode only		0			ns
Wakeup Time	t_{WAKE}	External reference			20		µs
		Internal reference (Note 10)			24		ms

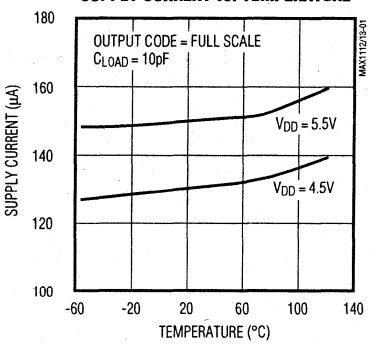
Note 1: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
Note 2: V_{REFIN} = 4.096V, offset nulled.
Note 3: On-channel grounded; sine wave applied to all off-channels.
Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 5: Guaranteed by design. Not subject to production testing.
Note 6: Common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: External load should not change during the conversion for specified accuracy.
Note 8: External reference at 4.096V, full-scale input, 500kHz external clock.
Note 9: Measured as | V_{FS} (4.5V) - V_{FS} (5.5V) |.
Note 10: 1µF at REFOUT; internal reference settling to 0.5LSB.

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

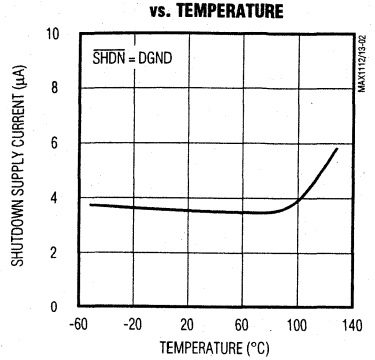
Typical Operating Characteristics

(V_{DD} = +5.0V; f_{SCLK} = 500kHz; external clock (50% duty cycle); R_L = ∞; T_A = +25°C, unless otherwise noted.)

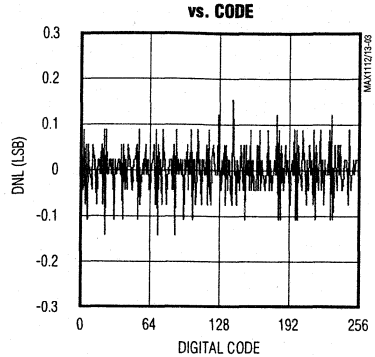
SUPPLY CURRENT vs. TEMPERATURE



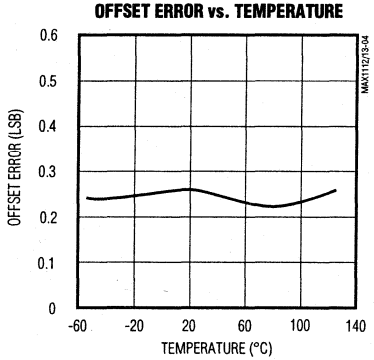
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



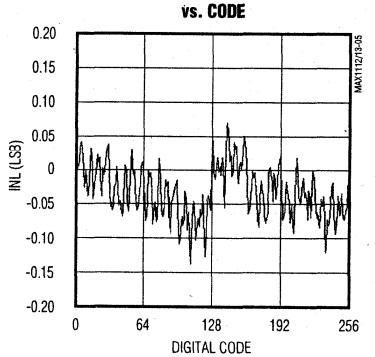
DIFFERENTIAL NONLINEARITY vs. CODE



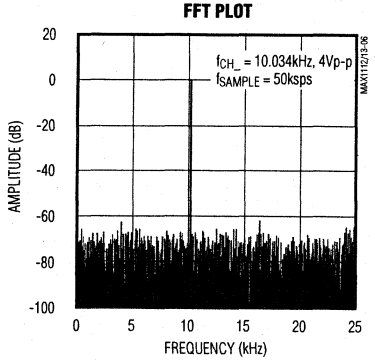
OFFSET ERROR vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



FFT PLOT



Pin Description

PIN		NAME	FUNCTION
MAX1112	MAX1113		
1–4	1–4	CH0–CH3	Sampling Analog Inputs
5–8	—	CH4–CH7	Sampling Analog Inputs
9	5	COM	Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
10	6	$\overline{SHDN}$	Three-Level Shutdown Input. Normally floats. Pulling $\overline{SHDN}$ low shuts the MAX1112/MAX1113 down to 10µA (max) supply current; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high shuts down the internal reference.
11	7	REFIN	Reference Voltage Input for Analog-to-Digital Conversion. Connect to REFOUT to use the internal reference.
12	8	REFOUT	Internal Reference Generator Output. Bypass with a 1µF capacitor to AGND.
13	9	AGND	Analog Ground
14	10	DGND	Digital Ground
15	11	DOUT	Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	12	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1112/MAX1113 begin the A/D conversion and goes high when the conversion is complete. In external clock mode, SSTRB pulses high for two clock periods before the MSB is shifted out. High impedance when $\overline{CS}$ is high (external clock mode only).
17	13	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge.
18	14	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	15	SCLK	Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 45% to 55%).
20	16	V_{DD}	Positive Supply Voltage, +4.5V to +5.5V

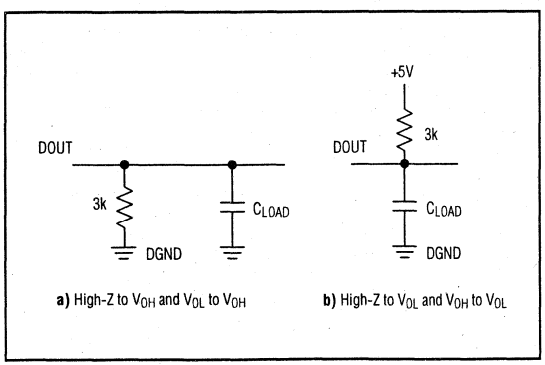


Figure 1. Load Circuits for Enable Time

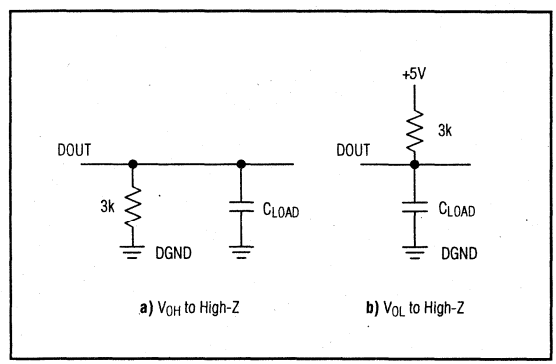


Figure 2. Load Circuits for Disable Time

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Detailed Description

The MAX1112/MAX1113 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows the Typical Operating Circuit.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in Figure 4, the equivalent input circuit. In single-ended mode, IN+ is internally switched to the selected input channel, CH_, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the MAX1112 channels with Table 1 and the MAX1113 channels with Table 2.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND if necessary.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans two SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF x (V_{IN+} - V_{IN-}) from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the sixth bit of the 8-bit control byte has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control byte has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input; if it is set up for differential inputs, IN- connects to the "-" input, and the difference (IN+ - IN-) is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

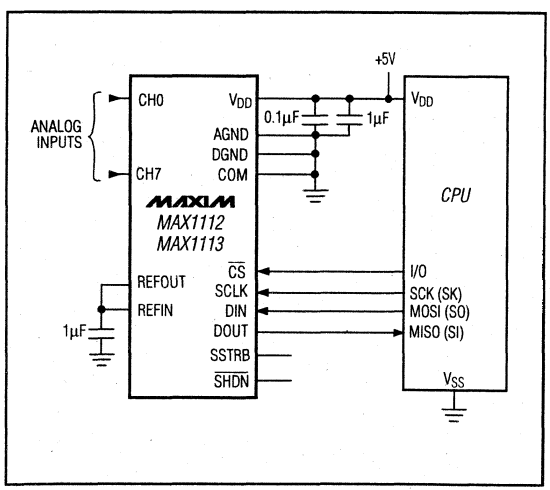


Figure 3. Typical Operating Circuit

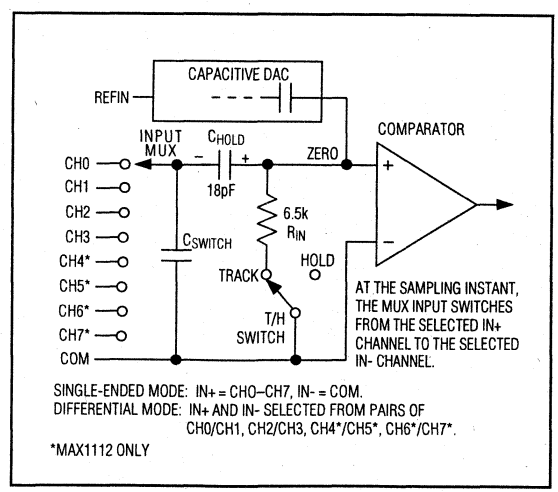


Figure 4. Equivalent Input Circuit

Table 1a. MAX1112 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 1b. MAX1112 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

Table 2a. MAX1113 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	X	+				–
1	0	X		+			–
0	1	X			+		–
1	1	X				+	–

Table 2b. MAX1113 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	X	+	–		
0	1	X			+	–
1	0	X	–	+		
1	1	X			–	+

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 6 \times (R_S + R_{IN}) \times 18pF$$

where R_{IN} = 6.5kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1µs. Note that source impedances below 2.4kΩ do not significantly affect the AC performance of the ADC.

Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Inputs

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from (AGND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.

The MAX1112/MAX1113 can be configured for differential or single-ended inputs with bits 2 and 3 of the control byte (Table 3). In single-ended mode, analog inputs are internally referenced to COM with a full-scale input range from COM to V_{REFIN} + COM. For bipolar operation, set COM to V_{REFIN} / 2.

In differential mode, choosing unipolar mode sets the differential input range at 0V to V_{REFIN}. In unipolar mode, the output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to ±V_{REFIN} / 2. Note that in this mode, the common-mode input range includes both supply rails. Refer to Table 4 for input voltage ranges.

Quick Look

To quickly evaluate the MAX1112/MAX1113's analog performance, use the circuit of Figure 5. The MAX1112/MAX1113 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds

Table 3. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7 (MSB)	START	The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	Select which of the input channels are to be used for the conversion (Tables 1 and 2).
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode (Table 4).
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured. See Tables 1 and 2.
1	PD1	**1** = fully operational, **0** = power-down. Selects fully operational or power-down mode.
0 (LSB)	PD0	**1** = external clock mode, **0** = internal clock mode. Selects external or internal clock mode.

Table 4. Full-Scale and Zero-Scale Voltages

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
V_{REFIN} + COM	COM	+V_{REFIN} / 2 + COM	COM	-V_{REFIN} / 2 + COM

in control bytes of $FF (hex), which trigger single-ended, unipolar conversions on CH7 (MAX1112) or CH3 (MAX1113) in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the most significant bit (MSB) of the 8-bit conversion result is shifted out of DOUT. Varying the analog input alters the output code. A total of 10 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on SCLK's falling edge.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1112/MAX1113's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit at DIN defines the MSB of the control byte. Until this first start bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 3 shows the control-byte format.

The MAX1112/MAX1113 are compatible with Microwire, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the Typical Operating Circuit (Figure 3), the simplest software interface requires three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the

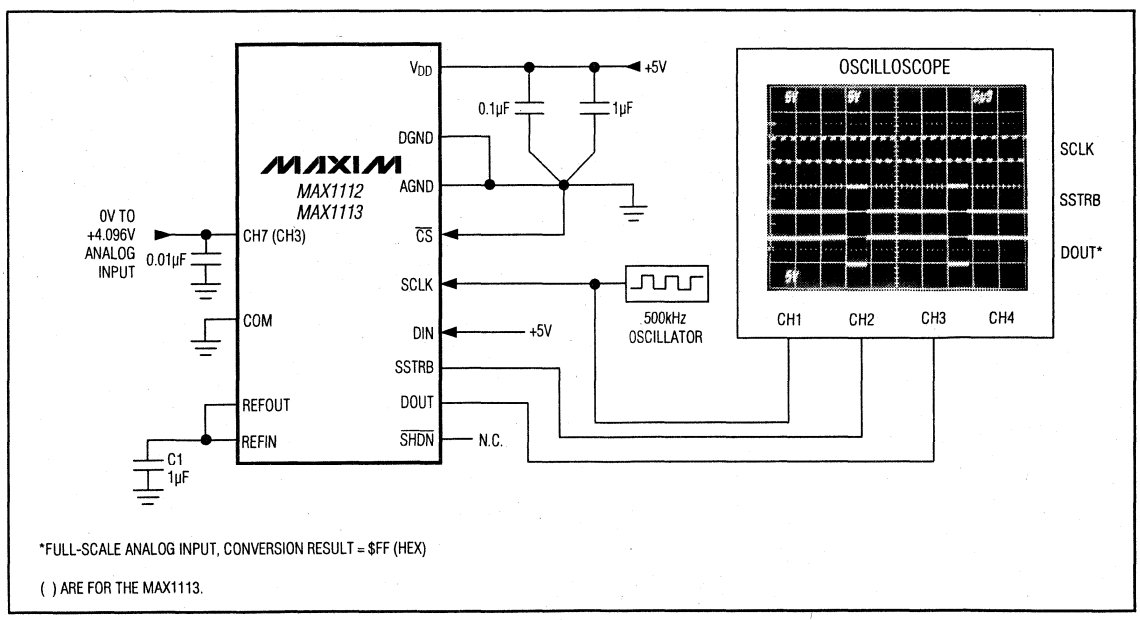


Figure 5. Quick-Look Circuit

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

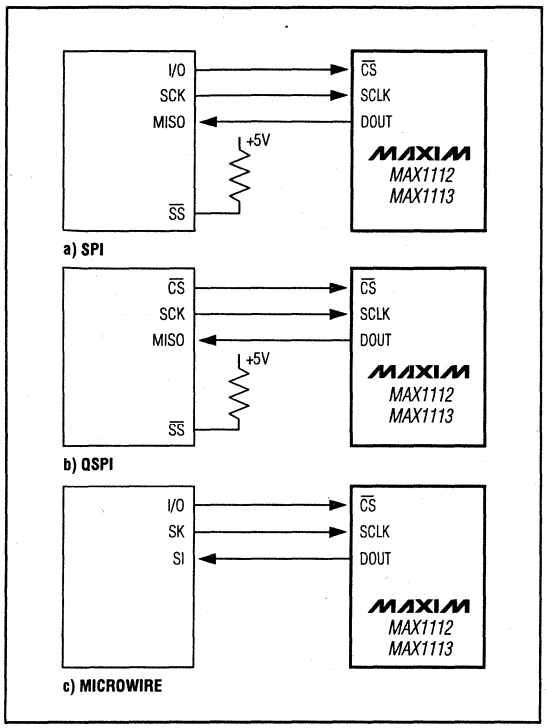


Figure 6. Common Serial-Interface Connections to the MAX1112/MAX1113

8-bit conversion result). Figure 6 shows the MAX1112/MAX1113 common serial-interface connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 50kHz to 500kHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 7 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with two leading zeros and six trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 1ms, to avoid excessive T/H droop.

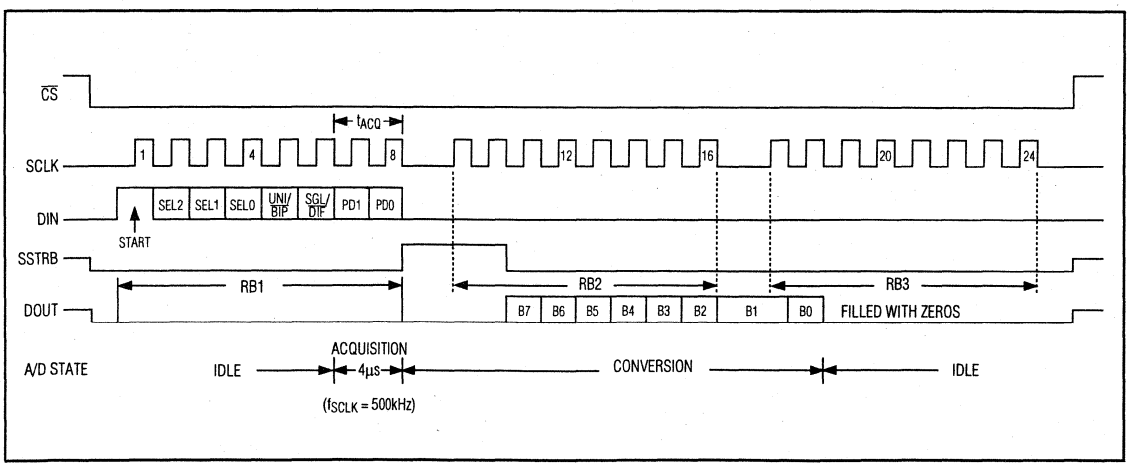


Figure 7. Single-Conversion Timing, External Clock Mode, 24 Clocks

Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format.

Clock Modes

The MAX1112/MAX1113 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit PD0 of the control byte programs the clock mode. Figures 8–11 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next eight SCLK falling edges (Figure 7). After the eight data bits are clocked out, subsequent clock pulses clock out zeros from the DOUT pin.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 9 shows the SSTRB timing in external clock mode.

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.

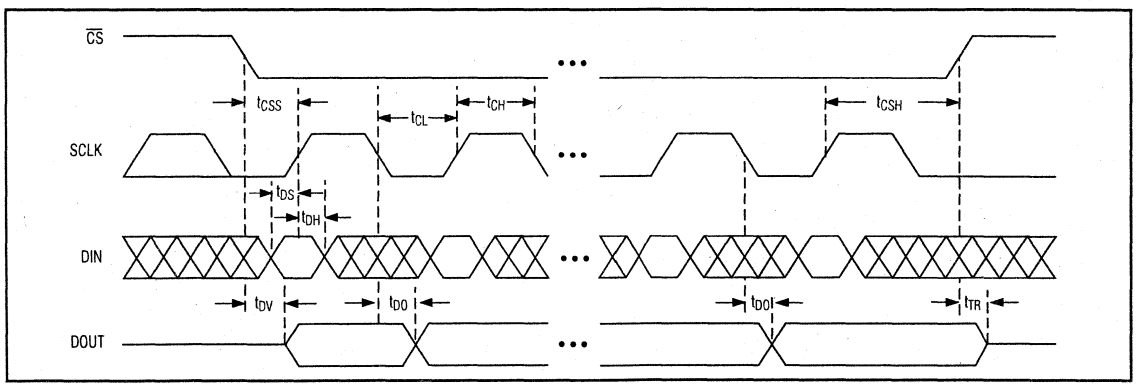


Figure 8. Detailed Serial-Interface Timing

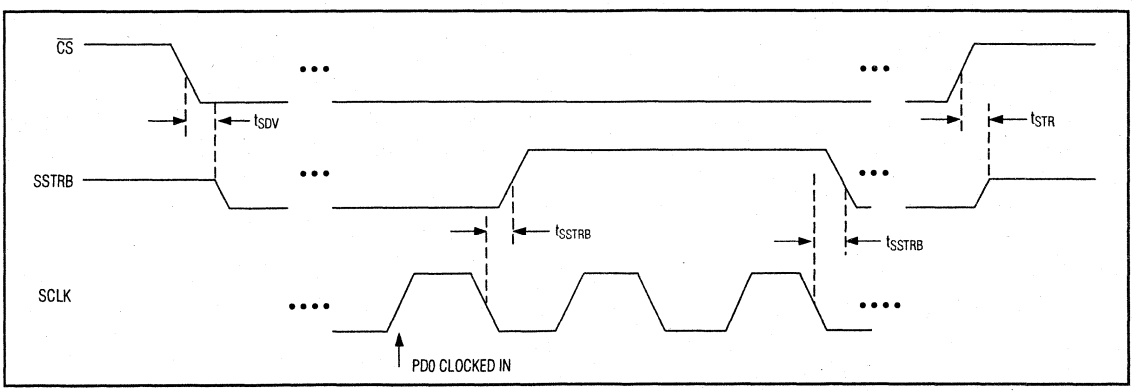


Figure 9. External Clock Mode SSTRB Detailed Timing

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

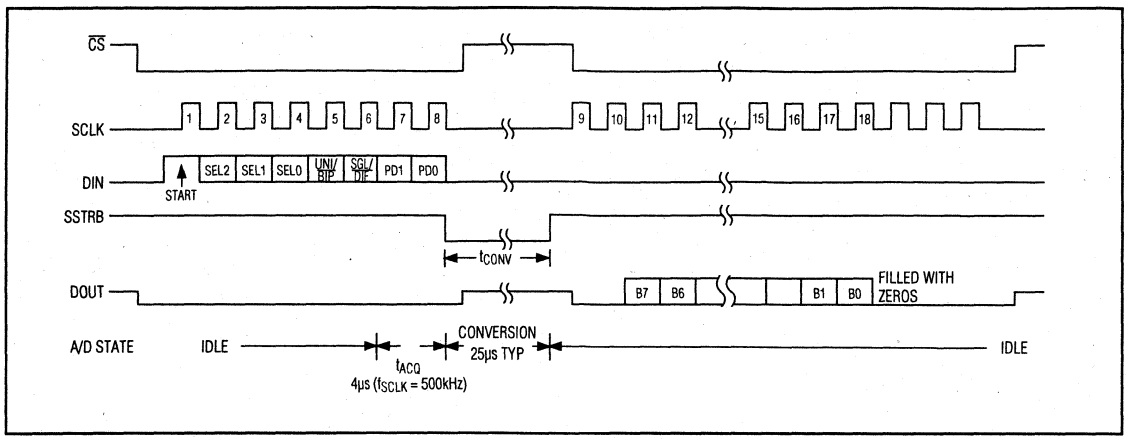


Figure 10. Internal Clock Mode Timing

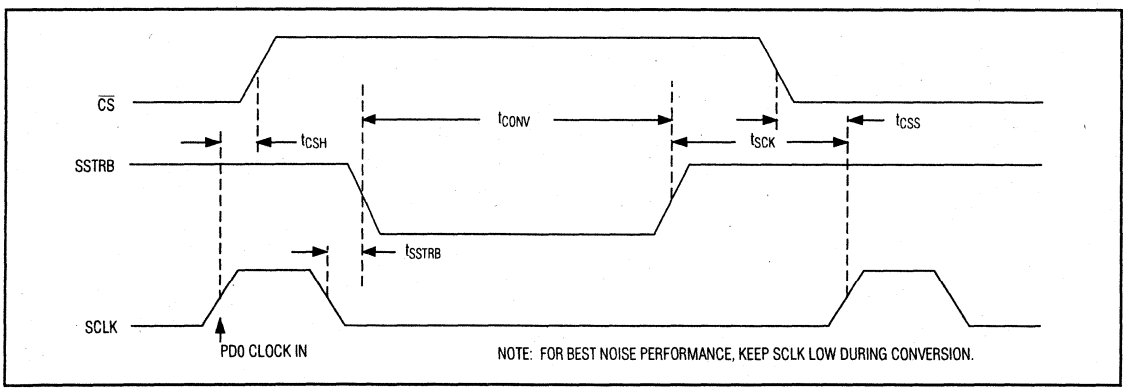


Figure 11. Internal Clock Mode SSTRB Detailed Timing

Internal Clock

Internal clock mode frees the µP from the burden of running the SAR conversion clock. This allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for 25µs (typically), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 10). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1112/MAX1113 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 11 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1112/MAX1113 at clock rates up to 2MHz, provided that the minimum acquisition time, t_{ACQ}, is kept above 1µs.

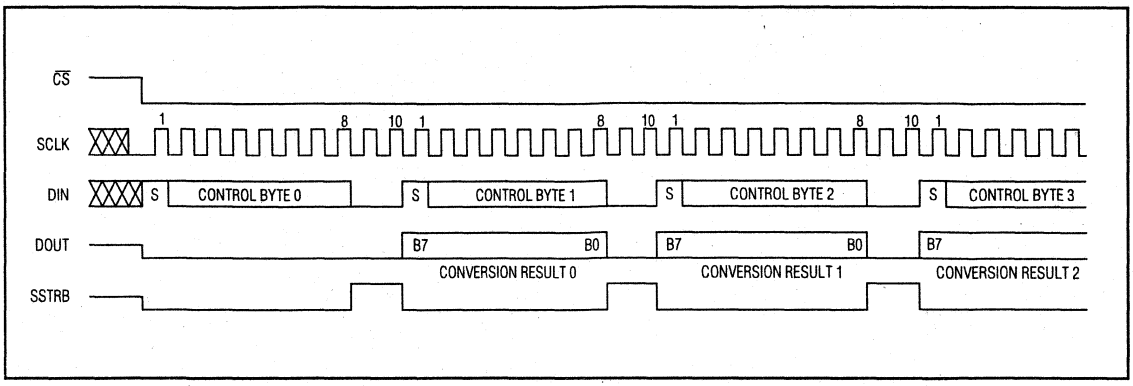


Figure 12a. Continuous Conversions, External Clock Mode, 10 Clocks/Conversion Timing

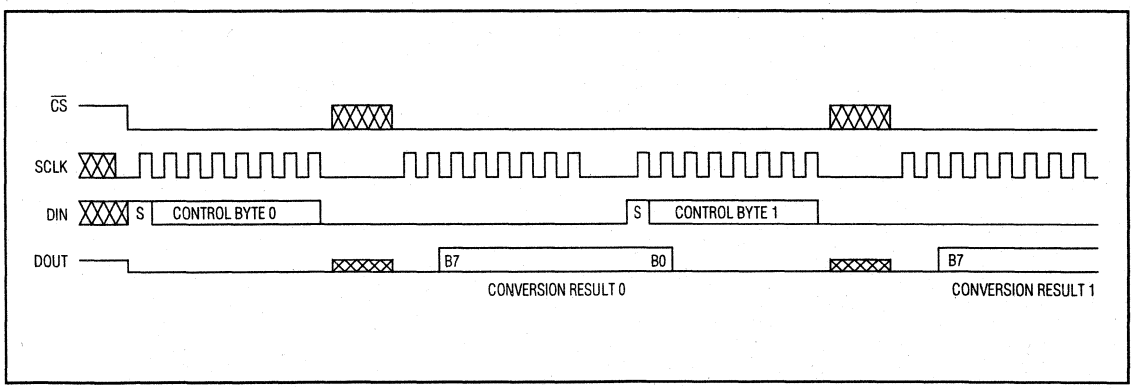


Figure 12b. Continuous Conversions, External Clock Mode, 16 Clocks/Conversion Timing

Data Framing

The falling edge of $\overline{CS}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle, e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after the MSB of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1112/MAX1113 can run is 10 clocks per conversion. Figure 12a shows the serial-interface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1112/MAX1113. Figure 12b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1112/MAX1113 in internal clock mode. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. No conversions should be performed until the reference voltage has stabilized (see the Wakeup Time specifications in the *Timing Characteristics*).

Power-Down

When operating at speeds below the maximum sampling rate, the MAX1112/MAX1113's automatic power-down mode can save considerable power by placing the converters in a low-current shutdown state between conversions. Figure 13 shows the average supply current as a function of the sampling rate.

Select power-down with PD1 of the DIN control byte with $\overline{SHDN}$ high or floating (Table 3). Pull $\overline{SHDN}$ low at any time to shut down the converters completely. $\overline{SHDN}$ overrides PD1 of the control byte. Figures 14a and 14b illustrate the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bit PD1 of the control byte. When software power-down is asserted, the ADCs continue to operate in the last specified clock mode until the conversion is complete. The ADCs then power down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1112/MAX1113 have entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, which powers up the MAX1112/MAX1113. If the DIN byte contains PD1 = 1, then the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Hard-Wired Power-Down and Internal Reference State

$\overline{SHDN}$ STATE	DEVICE MODE	INTERNAL REFERENCE
1	Enabled	Disabled
Floating	Enabled	Enabled
0	Power-Down	Disabled

Hard-Wired Power-Down

Pulling $\overline{SHDN}$ low places the converters in hard-wired power-down. Unlike software power-down, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the state of the internal reference (Table 5). Letting $\overline{SHDN}$ float enables the internal 4.096V voltage reference. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 1MΩ x C_{LOAD}, where C_{LOAD} is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high disables the internal reference, which saves power when using an external reference.

External Reference

An external reference between 1V and V_{DD} should be connected directly at the REFIN terminal. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20µA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1µF capacitor.

If an external reference is used with the MAX1112/MAX1113, tie $\overline{SHDN}$ to V_{DD} to disable the internal reference and decrease power consumption.

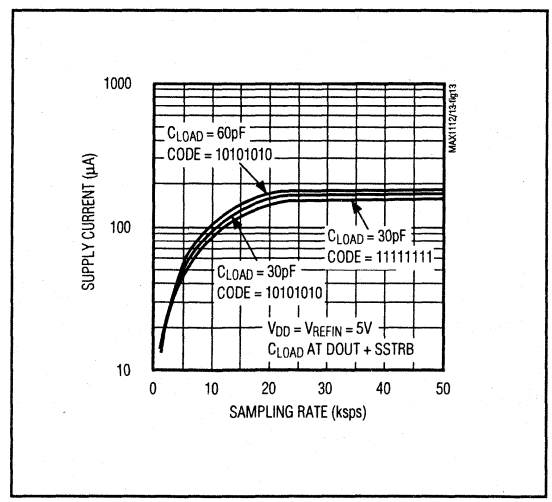


Figure 13. Average Supply Current vs. Sampling Rate

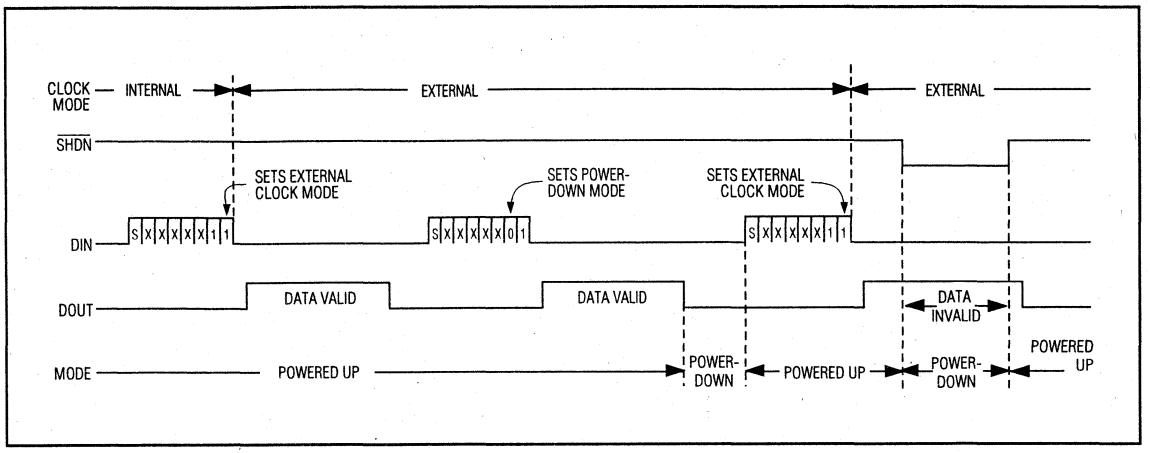


Figure 14a. Power-Down Modes, External Clock Timing Diagram

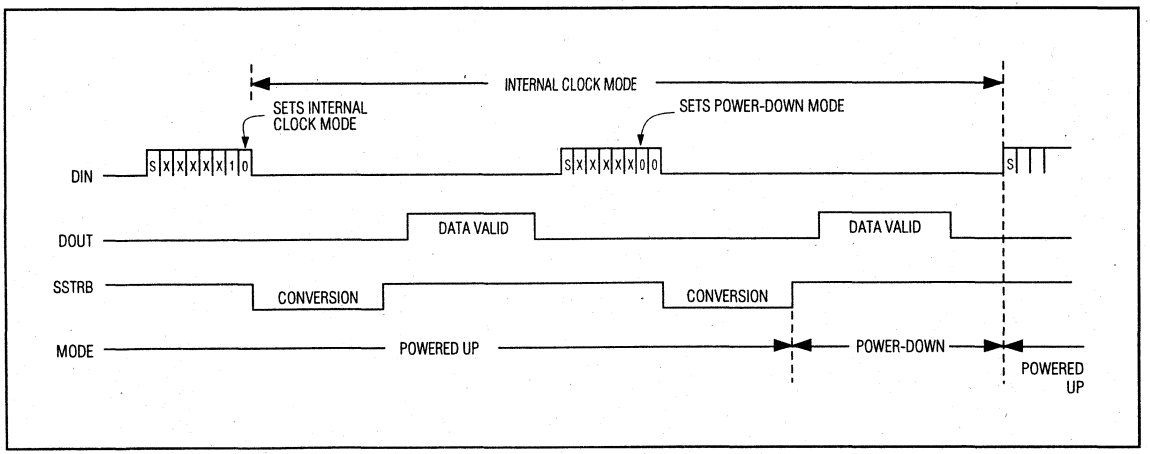


Figure 14b. Power-Down Modes, Internal Clock Timing Diagram

Internal Reference

To use the MAX1112/MAX1113 with the internal reference, connect REFIN to REFOUT. The full-scale range of the MAX1112/MAX1113 with the internal reference is typically 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference should be bypassed to AGND with a 1µF capacitor placed as close to the REFIN pin as possible.

Transfer Function

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 15 depicts the nominal, unipolar I/O transfer function, and Figure 16 shows the bipolar I/O transfer function when using a 4.096V reference. Code transitions occur at integer LSB values. Output coding is binary, with 1LSB = 16mV (4.096V/256) for unipolar operation and 1LSB = 16mV [(4.096V/2 - -4.096V/2)/256] for bipolar operation.

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

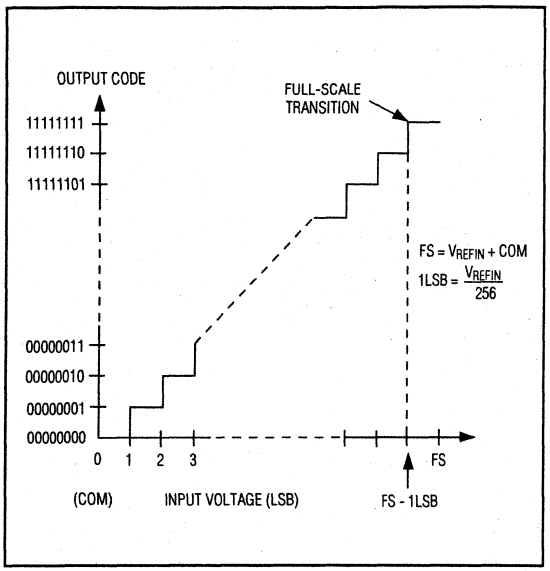


Figure 15. Unipolar Transfer Function

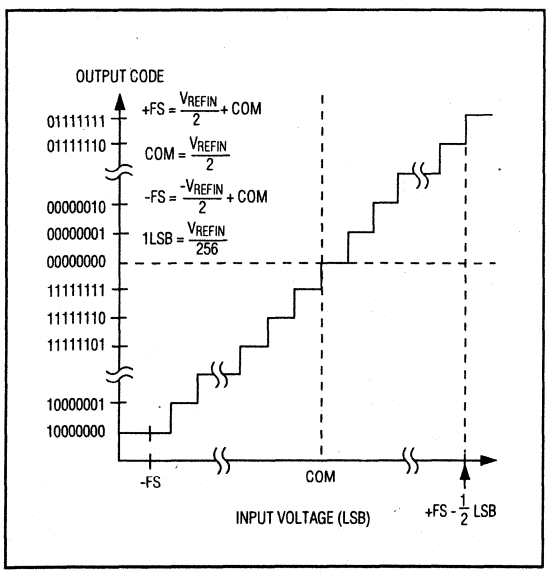


Figure 16. Bipolar Transfer Function

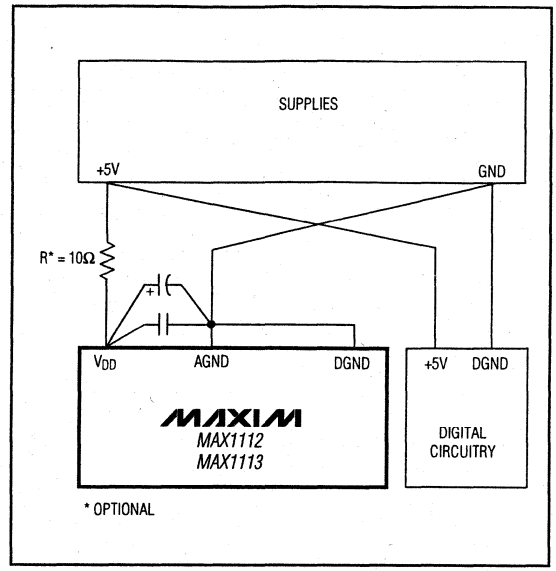


Figure 17. Power-Supply Grounding Connections

Layout, Grounding, and Bypassing

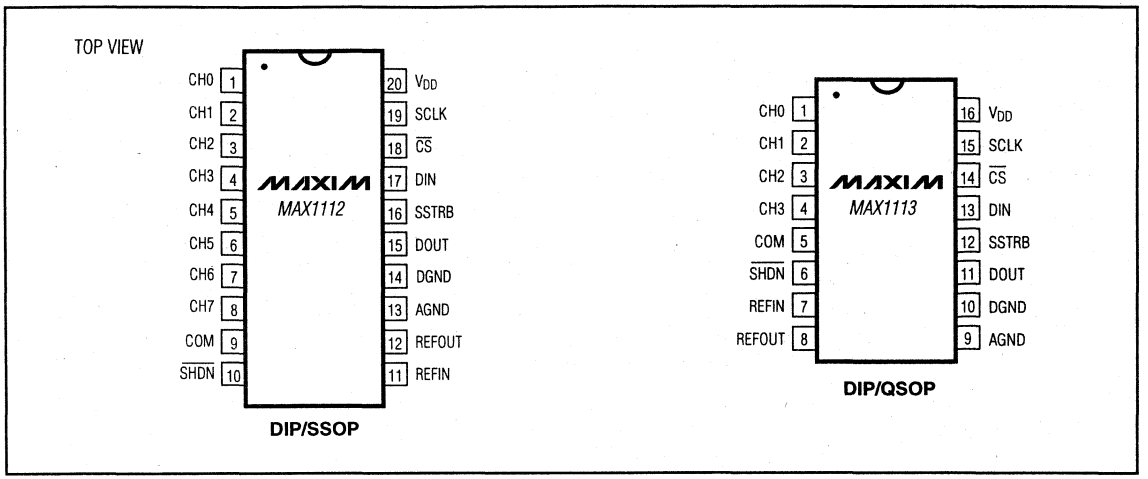
For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the V_{DD} pin of the MAX1112/MAX1113. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected to form a lowpass filter.

+5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs

Pin Configurations



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1112EPP	-40°C to +85°C	20 Plastic DIP
MAX1112EAP	-40°C to +85°C	20 SSOP
MAX1112MJP	-55°C to +125°C	20 CERDIP**
MAX1113CPE	0°C to +70°C	16 Plastic DIP
MAX1113CEE	0°C to +70°C	16 QSOP
MAX1113EPE	-40°C to +85°C	16 Plastic DIP
MAX1113EEE	-40°C to +85°C	16 QSOP
MAX1113MJE	-55°C to +125°C	16 CERDIP**

***Contact factory for availability.*

Chip Information

TRANSISTOR COUNT: 1996

SUBSTRATE CONNECTED TO DGND

7

19-1189; Rev 0; 3/97

EVALUATION KIT AVAILABLE

10-Bit, 20Msps, TTL-Output ADC

General Description

The MAX1160 10-bit, monolithic analog-to-digital converter (ADC) is capable of 20Msps minimum word rates. An on-board track/hold ensures excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes drive requirement problems.

Inputs and outputs are TTL compatible. An overrange output is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is low at only 1W with +5V and -5.2V power-supply voltages. The MAX1160 also accepts wide ±2V input voltages.

The MAX1160 is available in 28-pin DIP and SO packages in the commercial temperature range.

Applications

Medical Imaging
Professional Video
Radar Receivers
Instrumentation
Digital Communications

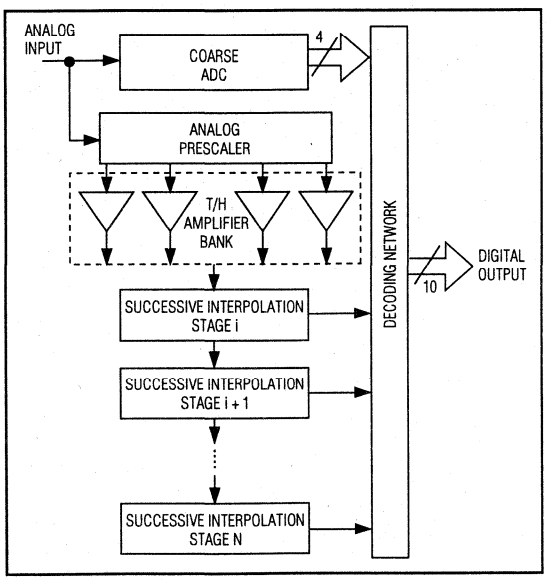
Features

- ♦ **Monolithic 20Msps Converter**
- ♦ **On-Chip Track/Hold**
- ♦ **Bipolar, ±2V Analog Input**
- ♦ **60dB SNR at 1MHz Input**
- ♦ **5pF Input Capacitance**
- ♦ **TTL Outputs**

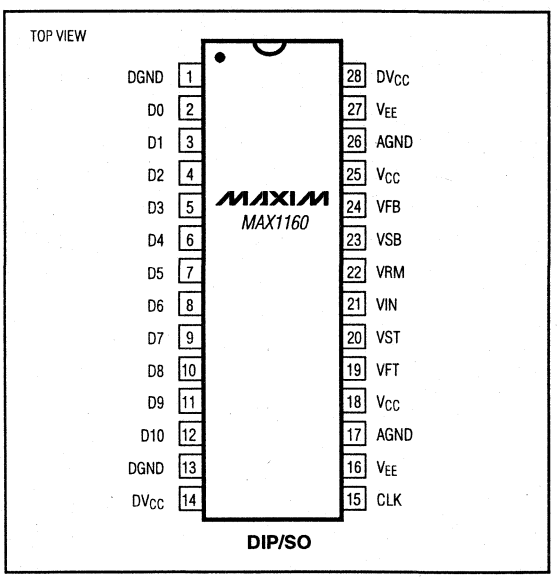
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1160ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1160ACWI	0°C to +70°C	28 SO
MAX1160BCWI	0°C to +70°C	28 SO

Functional Diagram



Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

10-Bit, 20Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} 6V
V_{EE} ..... -6V
Analog Input ..... $V_{FB} \le V_{IN} \le V_{FT}$
V_{FT}, V_{FB} ..... 3V, -3V
Reference-Ladder Current 12mA
CLK Input ..... V_{CC}
Digital Outputs ..... 30mA to -30mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP 1.14W
SO 1W
Operating Temperature Range ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1160A			MAX1160B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			10			10			Bits
DC ACCURACY (± full scale, 250kHz sample rate, T_A = +25°C)									
Integral Nonlinearity		I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN} = 0V	VI		30	60		30	60	µA
Input Bias Current	T_A = -55°C to +125°C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	T_A = -55°C to +125°C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3dB small signal	V		120			120		MHz
Positive Full-Scale Error		V		±2.0			±2.0		LSB
Negative Full-Scale Error		V		±2.0			±2.0		LSB
REFERENCE INPUT									
Reference-Ladder Resistance		VI	500	800		500	800		Ω
Reference-Ladder Tempco		V		0.8			0.8		Ω/°C
TIMING CHARACTERISTICS									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1			1		ns
Aperture Jitter Time	T_A = +25°C	V		5			5		ps-RMS
Acquisition Time	T_A = +25°C	V		20			20		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MAX1160A MIN	MAX1160A TYP	MAX1160A MAX	MAX1160B MIN	MAX1160B TYP	MAX1160B MAX	UNITS
DYNAMIC PERFORMANCE										
Effective Number of Bits (ENOB)	f_{IN} = 1MHz				9.2			8.7		Bits
	f_{IN} = 3.58MHz				8.8			8.3		
	f_{IN} = 10MHz				7.5			7.0		
Signal-to-Noise Ratio (without harmonics) (SNR)	f_{IN} = 1MHz	T_A = +25°C	I	57	60		54	57		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	55	58		52	55		
	f_{IN} = 3.58MHz	T_A = +25°C	I	56	58		53	55		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	54	56		51	53		
	f_{IN} = 10MHz	T_A = +25°C	I	50	53		47	49		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	47	50		44	46		
Total Harmonic Distortion (THD)	f_{IN} = 1MHz	T_A = +25°C	I	57	60		54	57		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	54	57		51	54		
	f_{IN} = 3.58MHz	T_A = +25°C	I	56	58		53	55		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	53	55		50	52		
	f_{IN} = 10MHz	T_A = +25°C	I	46	48		43	45		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	45	47		42	44		
Signal-to-Noise and Distortion Ratio (SINAD)	f_{IN} = 1MHz	T_A = +25°C	I	55	57		52	54		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	52			49			
	f_{IN} = 3.58MHz	T_A = +25°C	I	54	55		51	52		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	51			48			
	f_{IN} = 10MHz	T_A = +25°C	I	44	47		41	44		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	43			40			
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1MHz	T_A = +25°C	V		67			67		dB
Differential Phase	f_{IN} = 3.58MHz and 4.35MHz	T_A = +25°C	V		0.2			0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz and 4.35MHz	T_A = +25°C	V		0.5			0.7		%

10-Bit, 20Msps, TTL-Output ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 20MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1160A MIN	MAX1160A TYP	MAX1160A MAX	MAX1160B MIN	MAX1160B TYP	MAX1160B MAX	UNITS
DIGITAL INPUTS									
Logic 1 Voltage		V	2.4		4.5	2.4		4.0	V
Logic 0 Voltage		V			0.8			0.8	V
Maximum Input Current Low	T_A = +25°C	IV	0	5	20	0	5	20	µA
Maximum Input Current High	T_A = +25°C	IV	0	5	20	0	5	20	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
DIGITAL OUTPUTS									
Logic 1 Voltage		IV	2.4			2.4			V
Logic 0 Voltage		IV			0.6			0.6	V
POWER-SUPPLY REQUIREMENTS									
Voltages	V_{CC}	IV	4.75		5.25	4.75		5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	
Currents	I_{CC}	VI		118	145		118	145	mA
	DI_{CC}	VI		40	55		40	55	
	$-I_{EE}$	VI		40	57		40	57	
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power-Supply Rejection	V_{CC} = 5V ±0.25V, V_{EE} = -5.2V ±0.25V	V		1.0			1.0		LSB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

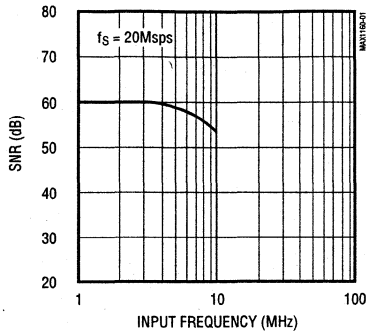
PIN	NAME	FUNCTION
1, 13	DGND	Digital Ground
2	D0	TTL Output (LSB)
3–10	D1–D8	TTL Outputs
11	D9	TTL Output (MSB)
12	D10	TTL Output Overrange
14, 28	DV_{CC}	+5V Supply (digital)
15	CLK	Clock
16, 27	V_{EE}	-5.2V Supply (analog)

PIN	NAME	FUNCTION
17, 26	AGND	Analog Ground
18, 25	V_{CC}	+5V Supply (analog)
19	VFT	Force for Top of Reference Ladder
20	VST	Sense for Top of Reference Ladder
21	VIN	Analog Input
22	VRM	Middle of Voltage Reference Ladder
23	VSB	Sense for Bottom of Reference Ladder
24	VFB	Force for Bottom of Reference Ladder

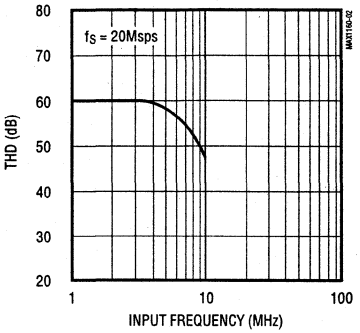
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

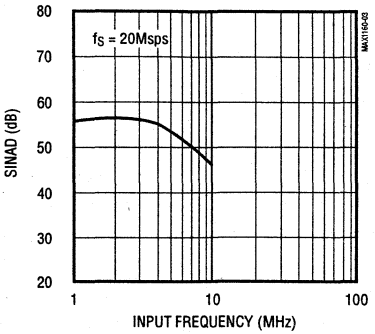
SIGNAL-TO-NOISE RATIO vs. INPUT FREQUENCY



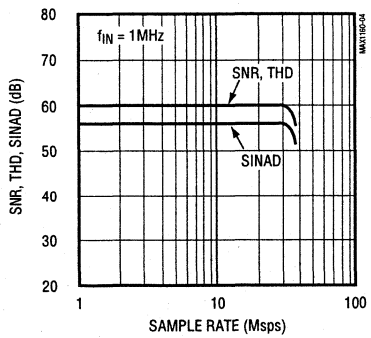
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



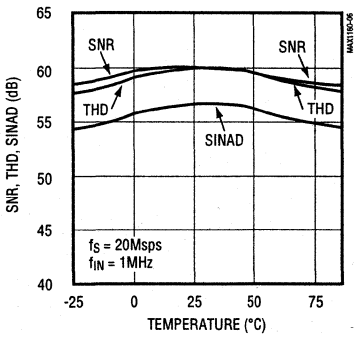
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



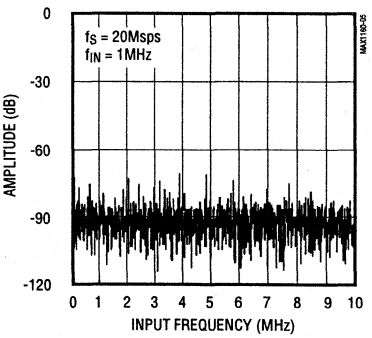
SNR, THD, SINAD vs. SAMPLE RATE



SNR, THD, SINAD vs. TEMPERATURE



SPECTRAL RESPONSE



Detailed Description

The MAX1160 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1160 in normal circuit operation. The following section provides a description of the pin functions, and outlines critical performance criteria to consider for achieving the optimal device performance.

Power Supplies and Grounding

The MAX1160 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. Connect these beads as close to the device as possible. The connection between the beads and the MAX1160 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are recommended).

10-Bit, 20Msps, TTL-Output ADC

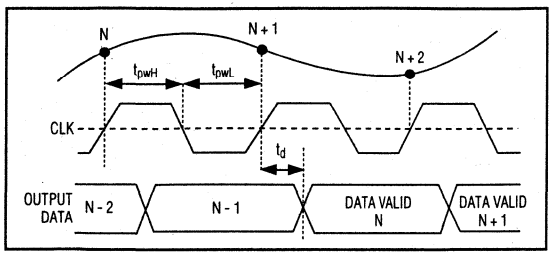


Figure 1a. Timing Diagram

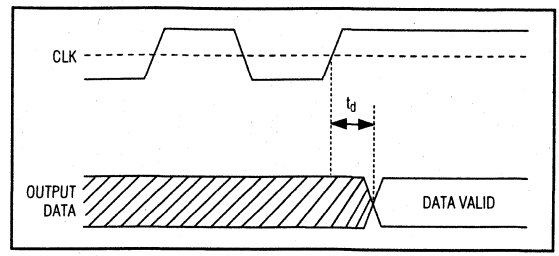


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Propagation Delay		14	18	ns
t_{pwH}	CLK High Pulse Width	20		300	ns
t_{pwL}	CLK Low Pulse Width	20			ns

The MAX1160 has two grounds: AGND and DGND. These internal grounds are isolated on the device. Use ground planes for optimum device performance. Use DGND for the DV_{CC} return path (typically 40mA) and for the return path for all digital output logic interfaces. Separate AGND and DGND from each other, connecting them together only through a ferrite bead at the device.

Connect a Schottky or hot carrier diode between AGND and V_{EE}. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply-sequencing latchup conditions. For optimum performance, use the recommended circuit shown in Figure 2.

Voltage Reference

The MAX1160 requires the use of two voltage references: VFT and VFB. VFT is the force for the top of the voltage-reference ladder (typically +2.5V); VFB (typically -2.5V) is the force for the bottom of the voltage-reference ladder. Both voltages are applied across an 800Ω internal reference-ladder resistance. The +2.5V voltage source for reference VFT must be current limited to 20mA (max) if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3. In addition, there are three reference-ladder taps (VST, VRM, and VSB). VST is the sense for the top of the reference ladder (+2V), VRM is the midpoint of the ladder (typically 0V), and VSB is the sense for the bottom of the reference ladder (-2V). The voltages at VST and VSB are the device's true full-scale input voltages when VFT and VFB are driven to the recommended voltages (typically +2.5V and -2.5V, respectively). These points should be used to monitor the device's actual full-scale input range. When not being used, a decoupling capacitor of 0.01µF (chip capacitor preferred) connected to AGND from each tap is recommended to minimize high-frequency noise injection.

Figure 2 shows an example of a recommended reference-driver circuit. IC1 is a MAX6225, a 2.5V reference with an accuracy of 0.2%. The 10kΩ potentiometer R1 supports a minimum adjustable range of 0.6%. Use an OP07 or equivalent device for IC2. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain 0.3LSB matching between VFT and VFB. If 0.1% matching is not met, then R4 can be used to adjust the VFB voltage to the desired level. Adjust VFT and VFB such that VST and VSB are exactly +2V and -2V, respectively.

The analog input range scales proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of VFT and VFB. However, because the device is laser trimmed to optimize performance with ±2.5V references, its accuracy degrades if operated beyond a ±2% range.

The following errors are defined:

+FS error = top of ladder offset voltage
= Δ(+FS - VST + 1LSB)

-FS error = bottom of ladder offset voltage
= Δ(-FS - VSB - 1LSB)

where the +FS (full-scale) input voltage is defined as the output transition between 11 1111 1110 and 11 1111 1111, and the -FS input voltage is defined as the output transition between 00 0000 0000 and 00 0000 0001 (Table 2).

Analog Input

VIN is the analog input. The full-scale input range will be 80% of the reference voltage, or ±2V with VFB = -2.5V and VFT = +2.5V.

The analog input's drive requirements are minimal when compared to conventional flash converters. This is due to the MAX1160's extremely low (5pF) input capacitance and very high (300kΩ) input resistance. For example, for an input signal of ±2Vp-p with a 10MHz input frequency, the peak output current required for the driving circuit is only 628µA.

Clock Input

The MAX1160 is driven from a single-ended TTL input (CLK). The CLK pulse width (t_{PWH}) must be kept between 20ns and 300ns to ensure proper operation of the internal track/hold amplifier (Figure 1a). When operating the MAX1160 at sampling rates above 3Msps, it is recommended that the clock input duty cycle be kept at

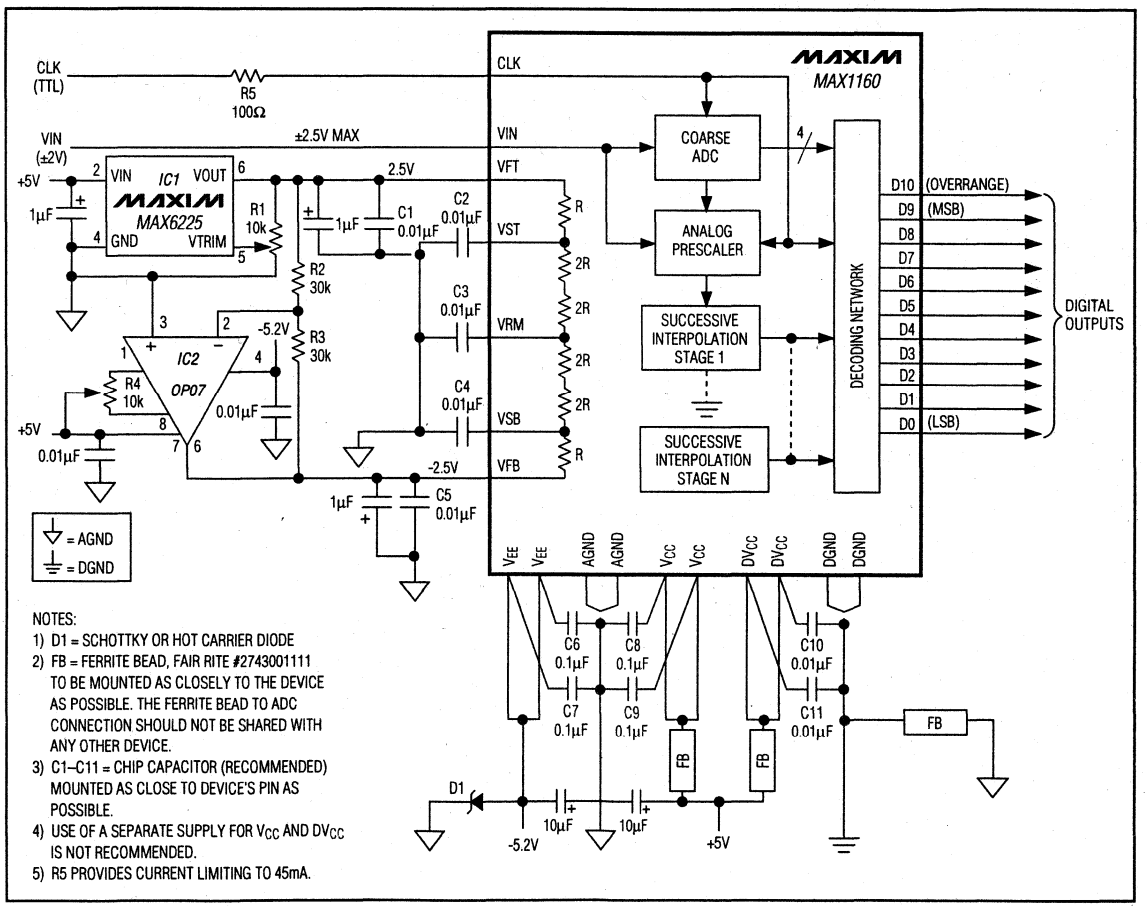


Figure 2. Typical Operating Circuit

10-Bit, 20Msps, TTL-Output ADC

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2V + 1/2LSB	1	11 1111 1111
+2V - 1LSB	0	11 1111 111Ø
0V	0	ØØ ØØØØ ØØØØ
-2V + 1LSB	0	00 0000 000Ø
< 2V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1.)

50% to optimize performance, but performance will not be degraded if kept within the 40% to 60% range. The analog input signal is latched on the rising edge of CLK.

The clock input must be driven from fast TTL logic (VIH ≤ 4.5V, t_{RISE} < 6ns). In the event the clock is driven from a high current source, use a 100Ω resistor (R5) in series to limit current to approximately 45mA.

Digital Outputs

The format of the output data (D0–D9) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a typical propagation delay of 14ns. There is a one-clock-cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise and fall times are not symmetrical. Typical propagation delay is 14ns for the rise time and 6ns for the fall time (Figure 4). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Overrange Output

The overrange output (D10) is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0–D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the MAX1160 in higher-resolution systems.

Evaluation Board

The MAX1160 EV kit is available to help designers demonstrate the MAX1160's full performance. This board includes a reference circuit, a clock-driver circuit, output data latches, and an on-board reconstruction of the digital data. A separate data sheet describing the operation of this board is also available. Contact the factory for price and availability.

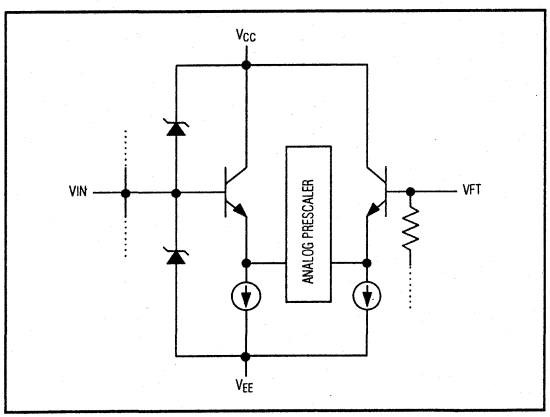


Figure 3. Analog Equivalent Input Circuit

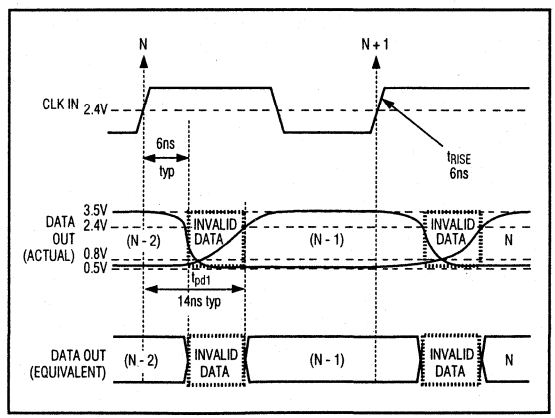


Figure 4. Digital Output Characteristics

19-1190; Rev 0; 3/97

EVALUATION KIT AVAILABLE

10-Bit, 40Msps, TTL-Output ADC

General Description

The MAX1161 10-bit, monolithic analog-to-digital converter (ADC) is capable of 40Msps minimum word rates. An on-board track/hold ensures excellent dynamic performance without the need for external components. A 5pF input capacitance minimizes drive requirement problems.

Inputs and outputs are TTL compatible. An overrange output is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is low at only 1W with +5V and -5.2V power-supply voltages. The MAX1161 also accepts wide, ±2V input voltages.

The MAX1161 is available in 28-pin DIP and SO packages in the commercial temperature range.

Features

- ♦ **Monolithic 40Msps Converter**
- ♦ **On-Chip Track/Hold**
- ♦ **Bipolar, ±2V Analog Input**
- ♦ **57dB SNR at 3.58MHz Input**
- ♦ **5pF Input Capacitance**
- ♦ **TTL Outputs**

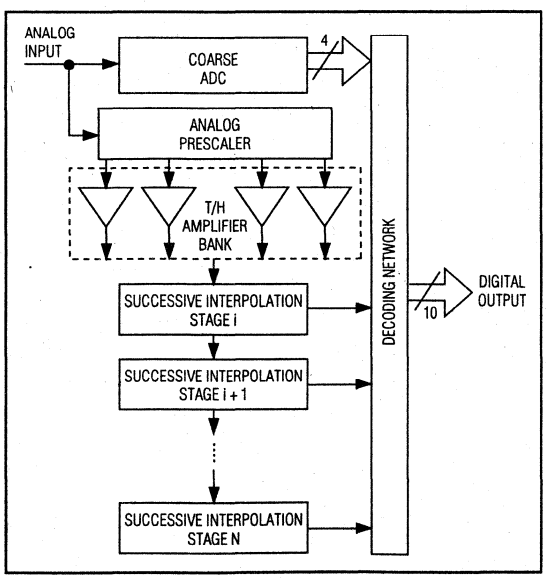
Applications

Medical Imaging
Professional Video
Radar Receivers
Instrumentation
Digital Communications

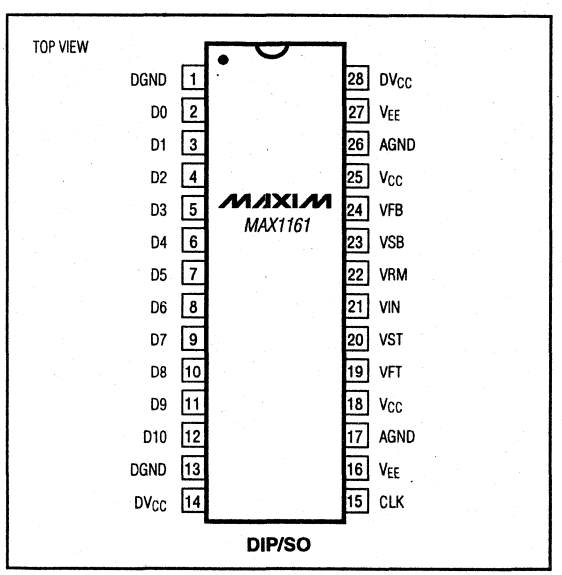
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1161ACPI	0°C to +70°C	28 Wide Plastic DIP
MAX1161BCPI	0°C to +70°C	28 Wide Plastic DIP
MAX1161ACWI	0°C to +70°C	28 SO
MAX1161BCWI	0°C to +70°C	28 SO

Functional Diagram



Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

10-Bit, 40Msps, TTL-Output ADC

ABSOLUTE MAXIMUM RATINGS

V_{CC} .....+6V
V_{EE} .....-6V
Analog Input.....VFB ≤ VIN ≤ VFT
VFT, VFB .....3V, -3V
Reference-Ladder Current.....12mA
CLK Input.....V_{CC}
Digital Outputs.....30mA to -30mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP.....1.14W
SO 1W
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 40MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1161A MIN	MAX1161A TYP	MAX1161A MAX	MAX1161B MIN	MAX1161B TYP	MAX1161B MAX	UNITS
Resolution			10			10			Bits
DC ACCURACY (±full scale, 250kHz sample rate, T_A = +25°C)									
Integral Nonlinearity		I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN} = 0V	VI		30	60		30	60	µA
Input Bias Current	T_A = -55°C to +125°C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	T_A = -55°C to +125°C	VI	75	300		75	300		kΩ
Input Capacitance		VI		5			5		pF
Input Bandwidth	3dB small signal	V		120			120		MHz
Positive Full-Scale Error		V		±2.0			±2.0		LSB
Negative Full-Scale Error		V		±2.0			±2.0		LSB
REFERENCE INPUT									
Reference-Ladder Resistance		VI	500	800		500	800		Ω
Reference-Ladder Tempco		V			0.8			0.8	Ω/°C
TIMING CHARACTERISTICS									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A = +25°C	V		14	18		14	18	ns
Aperture Delay Time	T_A = +25°C	V		1			1		ns
Aperture Jitter Time	T_A = +25°C	V		5			5		ps-RMS
Acquisition Time	T_A = +25°C	V		12			12		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 40MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		TEST LEVEL	MAX1161A MIN	MAX1161A TYP	MAX1161A MAX	MAX1161B MIN	MAX1161B TYP	MAX1161B MAX	UNITS
DYNAMIC PERFORMANCE										
Effective Number of Bits (ENOB)	f_{IN} = 1MHz					8.7			8.2	Bits
	f_{IN} = 3.58MHz					8.7			8.2	
	f_{IN} = 10.0MHz					7.3			6.9	
Signal-to-Noise Ratio (without harmonics) (SNR)	f_{IN} = 1MHz	T_A = +25°C	I	55	57		52	54		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	53	55		50	52		
	f_{IN} = 3.58MHz	T_A = +25°C	I	55	57		52	54		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	53	55		50	52		
	f_{IN} = 10.0MHz	T_A = +25°C	I	48	50		46	48		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	45	47		43	45		
Total Harmonic Distortion (THD)	f_{IN} = 1MHz	T_A = +25°C	I	54	56		52	54		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	51	53		49	51		
	f_{IN} = 3.58MHz	T_A = +25°C	I	54	56		52	54		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	51	53		49	51		
	f_{IN} = 10.0MHz	T_A = +25°C	I	46	48		43	45		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	45	47		41	44		
Signal-to-Noise and Distortion Ratio (SINAD)	f_{IN} = 1MHz	T_A = +25°C	I	52	54		49	51		dB
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	49			46			
	f_{IN} = 3.58MHz	T_A = +25°C	I	52	54		49	51		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	49			46			
	f_{IN} = 10.0MHz	T_A = +25°C	I	44	46		41	43		
		T_A = 0°C to +70°C, T_A = -25°C to +85°C	IV	43			40			
Spurious-Free Dynamic Range (SFDR)	f_{IN} = 1MHz	T_A = +25°C	V		67			67		dB
Differential Phase	f_{IN} = 3.58MHz, 4.35MHz	T_A = +25°C	V		0.2			0.2		Degrees
Differential Gain	f_{IN} = 3.58MHz, 4.35MHz	T_A = +25°C	V		0.5			0.7		%

10-Bit, 40Msps, TTL-Output ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, DV_{CC} = +5.0V, V_{IN} = ±2.0V, VSB = -2.0V, VST = +2.0V, f_{CLK} = 40MHz, 50% clock duty cycle, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX1161A MIN	MAX1161A TYP	MAX1161A MAX	MAX1161B MIN	MAX1161B TYP	MAX1161B MAX	UNITS
DIGITAL INPUTS									
Logic 1 Voltage		V	2.4		4.5	2.4		4.0	V
Logic 0 Voltage		V			0.8			0.8	V
Maximum Input Current Low	T_A = +25°C	IV	0	5	20	0	5	20	µA
Maximum Input Current High	T_A = +25°C	IV	0	5	20	0	5	20	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
DIGITAL OUTPUTS									
Logic 1 Voltage		IV	2.4			2.4			V
Logic 0 Voltage		IV			0.6			0.6	V
POWER-SUPPLY REQUIREMENTS									
Voltages	V_{CC}	IV	4.75		5.25	4.75		5.25	V
	DV_{CC}	IV	4.75	5.0	5.25	4.75	5.0	5.25	
	$-V_{EE}$	IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	
Currents	I_{CC}	VI		118	145		118	145	mA
	DI_{CC}	VI		40	55		40	55	
	$-I_{EE}$	VI		40	57		40	57	
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power-Supply Rejection	V_{CC} = 5V ±0.25V, V_{EE} = -5.2V ±0.25V	V		1.0			1.0		LSB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.
Unless otherwise noted, all tests are pulsed; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

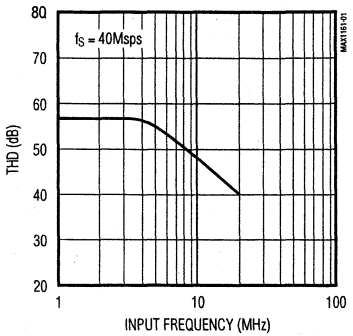
PIN	NAME	FUNCTION
1, 13	DGND	Digital Ground
2	D0	TTL Output (LSB)
3–10	D1–D8	TTL Outputs
11	D9	TTL Output (MSB)
12	D10	TTL Output Overrange
14, 28	DV_{CC}	+5V Supply (digital)
15	CLK	Clock
16, 27	V_{EE}	-5.2V Supply (analog)

PIN	NAME	FUNCTION
17, 26	AGND	Analog Ground
18, 25	V_{CC}	+5V Supply (analog)
19	VFT	Force for Top of Reference Ladder
20	VST	Sense for Top of Reference Ladder
21	VIN	Analog Input
22	VRM	Middle of Voltage Reference Ladder
23	VSB	Sense for Bottom of Reference Ladder
24	VFB	Force for Bottom of Reference Ladder

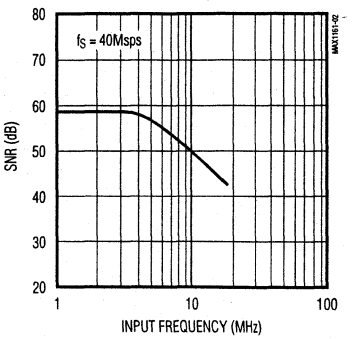
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

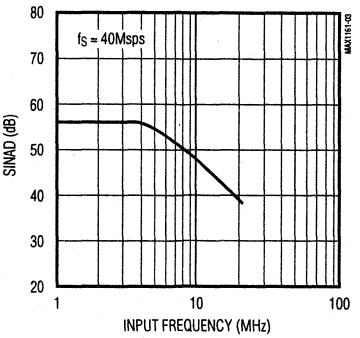
TOTAL HARMONIC DISTORTION vs. INPUT FREQUENCY



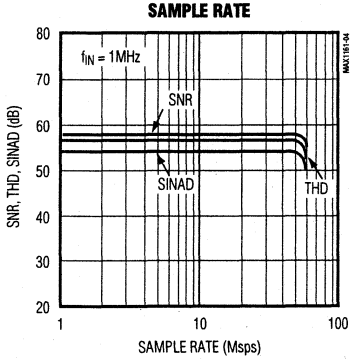
SIGNAL-TO-NOISE vs. INPUT FREQUENCY



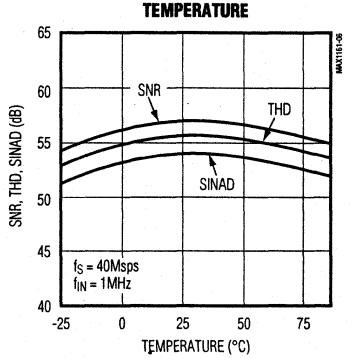
SIGNAL-TO-NOISE AND DISTORTION vs. INPUT FREQUENCY



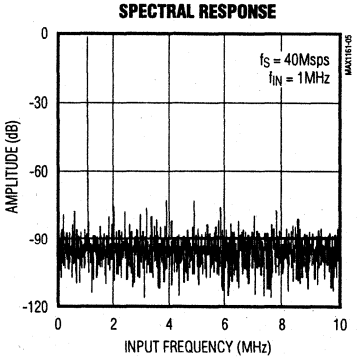
SNR, THD, SINAD vs. SAMPLE RATE



SNR, THD, SINAD vs. TEMPERATURE



SPECTRAL RESPONSE



Detailed Description

The MAX1161 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the MAX1161 in normal circuit operation. The following section provides a description of the pin functions, and outlines critical performance criteria to consider for achieving optimal device performance.

Power Supplies and Grounding

The MAX1161 requires -5.2V and +5V analog supply voltages. The +5V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line reduces the transient noise injected into the analog V_{CC}. These beads should be connected as close to the device as possible. The connection between the beads and the MAX1161 should not be shared with any other device. Bypass each power-supply pin as close to the device as possible. Use 0.1µF for V_{EE} and V_{CC}, and 0.01µF for DV_{CC} (chip capacitors are recommended).

The MAX1161 has two grounds: AGND and DGND. These internal grounds are isolated on the device. Use ground planes for optimum device performance. Use DGND for the DV_{CC} return path (typically 40mA) and for the return path for all digital output logic interfaces. Separate AGND and DGND from each other, connecting them together only through a ferrite bead at the device.

10-Bit, 40Msps, TTL-Output ADC

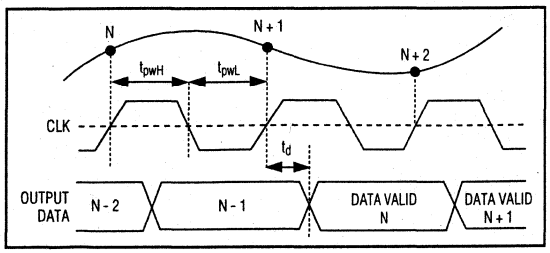


Figure 1a. Timing Diagram

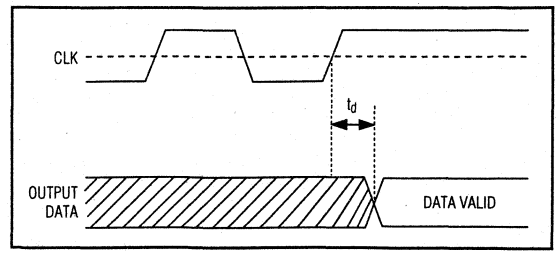


Figure 1b. Single-Event Clock

Table 1. Timing Parameters

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Propagation Delay		14	18	ns
t_{pwH}	CLK High Pulse Width	10		300	ns
t_{pwL}	CLK Low Pulse Width	10			ns

Connect a Schottky or hot carrier diode between AGND and V_{EE}. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power-supply-sequencing latchup conditions. For optimum performance, use the recommended circuit shown in Figure 2.

Voltage Reference

The MAX1161 requires the use of two voltage references: VFT and VFB. VFT is the force for the top of the voltage-reference ladder (typically +2.5V); VFB (typically -2.5V) is the force for the bottom of the voltage-reference ladder. Both voltages are applied across an 800Ω internal reference-ladder resistance. The +2.5V voltage source for reference VFT must be current limited to 20mA (max) if a different driving circuit is used in place of the recommended reference circuit shown in Figures 2 and 3. In addition, there are three reference-ladder taps (VST, VRM, and VSB). VST is the sense for the top of the reference ladder (+2V), VRM is the midpoint of the ladder (typically 0V), and VSB is the sense for the bottom of the reference ladder (-2V). The voltages at VST and VSB are the device's true full-scale input voltages when VFT and VFB are driven to the recommended voltages (+2.5V and -2.5V, respectively). These points should be used to monitor the device's actual full-scale input range. When not being used, a decoupling capacitor of 0.01µF (chip carrier preferred) connected to AGND from each tap is recommended to minimize high-frequency noise injection.

Figure 2 shows an example of a recommended reference-driver circuit. IC1 (MAX6225) is a +2.5V reference with 0.2% accuracy. Potentiometer R1 is 10kΩ and supports a minimum adjustable range of 0.6%. Use an OP07 or equivalent device for IC2. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain 0.3LSB matching between VFT and VFB. If 0.1% matching is not met, then R4 can be used to adjust the VFB voltage to the desired level. Adjust VFT and VFB such that VST and VSB are exactly +2V and -2V, respectively.

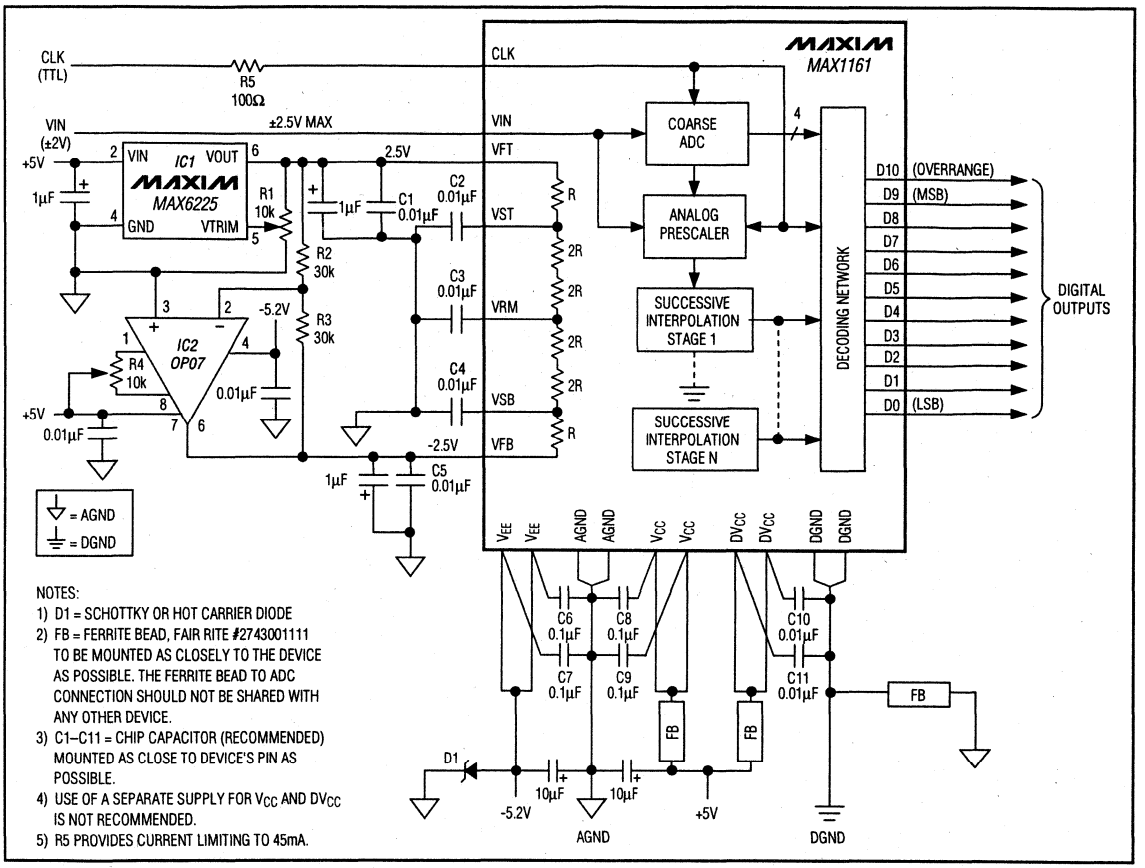
The analog input range scales proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ±20% of the recommended reference voltages of VFT and VFB. However, because the device is laser trimmed to optimize performance with ±2.5V references, its accuracy degrades if operated beyond a ±2% range.

The following errors are defined:

+FS error = top of ladder offset voltage
= Δ (+FS - VST + 1LSB)

-FS error = bottom of ladder offset voltage
= Δ (-FS - VSB - 1LSB)

where the +FS (full-scale) input voltage is defined as the output transition between 11 1111 1110 and 11 1111 1111, and the -FS input voltage is defined as the output transition between 00 0000 0000 and 00 0000 0001 (Table 2).



NOTES:
1) D1 = SCHOTTKY OR HOT CARRIER DIODE
2) FB = FERRITE BEAD, FAIR RITE #2743001111 TO BE MOUNTED AS CLOSELY TO THE DEVICE AS POSSIBLE. THE FERRITE BEAD TO ADC CONNECTION SHOULD NOT BE SHARED WITH ANY OTHER DEVICE.
3) C1–C11 = CHIP CAPACITOR (RECOMMENDED) MOUNTED AS CLOSE TO DEVICE'S PIN AS POSSIBLE.
4) USE OF A SEPARATE SUPPLY FOR V_{CC} AND DV_{CC} IS NOT RECOMMENDED.
5) R5 PROVIDES CURRENT LIMITING TO 45mA.

Figure 2. Typical Operating Circuit

Analog Input

VIN is the analog input. The full-scale input range will be 80% of the reference voltage, or ±2V with VFB = -2.5V and VFT = +2.5V.

The analog input's drive requirements are minimal when compared to conventional flash converters. This is due to the MAX1161's extremely low (5pF) input capacitance and very high (300kΩ) input resistance. For example, for an input signal of ±2Vp-p with a 10MHz input frequency, the peak output current required for the driving circuit is only 628µA.

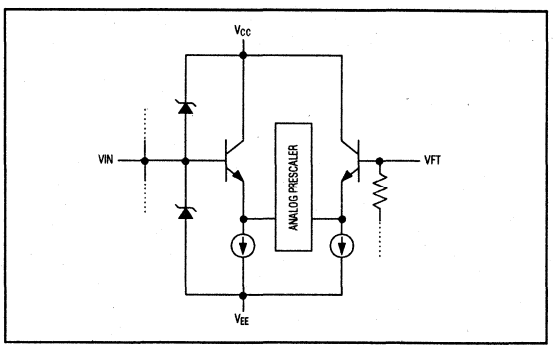


Figure 3. Analog Equivalent Input Circuit

Table 2. Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9–D0
> +2V + 1/2LSB	1	11 1111 1111
+2V - 1LSB	0	11 1111 111Ø
0.0V	0	ØØ ØØØØ ØØØØ
-2V + 1LSB	0	00 0000 000Ø
< 2V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1.)

Clock Input

The MAX1161 is driven from a single-ended TTL input (CLK). The CLK pulse width (t_{pwH}) must be kept between 10ns and 300ns to ensure proper operation of the internal track/hold amplifier (Figure 1a). When operating the MAX1161 at sampling rates above 3Msps, it is recommended that the clock input duty cycle be kept at 50% to optimize performance (Figure 4). The analog input signal is latched on the rising edge of CLK.

The clock input must be driven from fast TTL logic (VIH ≤ 4.5V, t_{RISE} <6ns). In the event the clock is driven from a high current source, use a 100Ω resistor (R5) in series to limit current to approximately 45mA.

Digital Outputs

The format of the output data (D0–D9) is straight binary (Table 2). The outputs are latched on the rising edge of CLK with a propagation delay typically at 14ns. There is a one-clock-cycle latency between CLK and the valid output data (Figure 1a).

The digital outputs' rise and fall times are not symmetrical. Typical propagation delay is 14ns for the rise time and 6ns for the fall time (Figure 5). The nonsymmetrical rise and fall times create approximately 8ns of invalid data.

Overrange Output

The overrange output (D10) is an indication that the analog input signal has exceeded the positive full-scale input voltage by 1LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0–D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the MAX1161 in higher-resolution systems.

Evaluation Board

The MAX1160 EV kit is available to help designers demonstrate the MAX1160 or MAX1161's full performance. This board includes a reference circuit, clock-driver circuit, output data latches, and an on-board reconstruction of the digital data. A separate data sheet describing the operation of this board is also available. Contact the factory for price and availability.

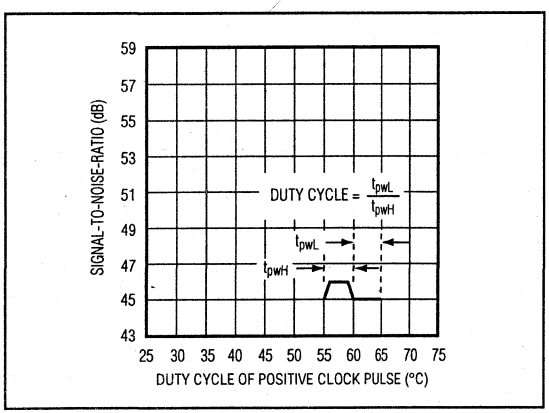


Figure 4. SNR vs. Clock Duty Cycle

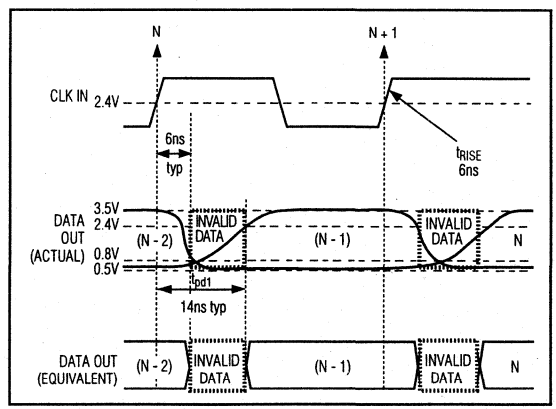


Figure 5. Digital Output Characteristics

19-1173; Rev 1; 3/97

EVALUATION KIT AVAILABLE

MAXIM

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

General Description

The MAX1202/MAX1203 are 12-bit data-acquisition systems specifically designed for use in applications with mixed +5V (analog) and +3V (digital) supply voltages. They operate with a single +5V analog supply or dual ±5V analog supplies, and combine an 8-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption.

A 4-wire serial interface connects directly to SPI™/Microwire™ devices without external logic, and a serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1202/MAX1203 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions. The serial interface operates at up to 2MHz.

The MAX1202 features an internal 4.096V reference, while the MAX1203 requires an external reference. Both parts have a reference-buffer amplifier that simplifies gain trim. They also have a VL pin that is the power supply for the digital outputs. Output logic levels (3V, 3.3V, or 5V) are determined by the value of the voltage applied to this pin.

These devices provide a hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes. Accessing the serial interface automatically powers up the devices. A quick turn-on time enables the MAX1202/MAX1203 to be shut down between conversions, allowing the user to optimize supply currents. By customizing power-down between conversions, supply current can drop below 10µA at reduced sampling rates.

The MAX1202/MAX1203 are available in 20-pin SSOP and DIP packages, and are specified for the commercial, extended, and military temperature ranges.

Applications

5V/3V Mixed-Supply Systems
Data Acquisition
High-Accuracy Process Control
Battery-Powered Instruments
Medical Instruments

Typical Operating Circuit appears at end of data sheet.

SPI is a registered trademark of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

- **8-Channel Single-Ended or 4-Channel Differential Inputs**
- **Operates from Single +5V or Dual ±5V Supplies**
- **User-Adjustable Output Logic Levels (2.7V to 5.25V)**
- **Low Power: 1.5mA (operating mode) 2µA (power-down mode)**
- **Internal Track/Hold, 133kHz Sampling Rate**
- **Internal 4.096V Reference (MAX1202)**
- **SPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar/Bipolar Inputs**
- **20-Pin DIP/SSOP**

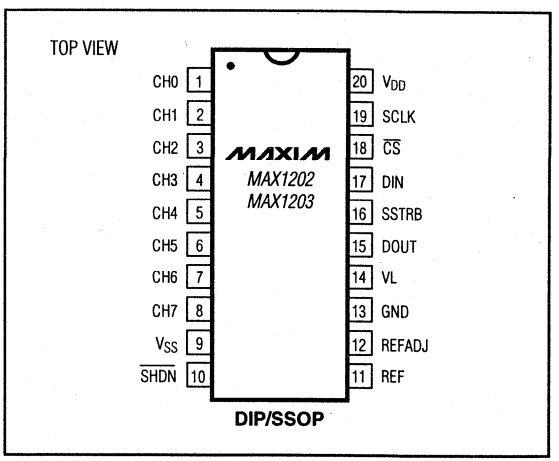
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1202ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1202BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1202ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1202BCAP	0°C to +70°C	20 SSOP	±1
MAX1202BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration



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5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to 6V
VL .....-0.3V to (V_{DD} + 0.3V)
V_{SS} to GND .....0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to 12V
CH0–CH7 to GND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current.....±20mA
REF to GND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND .....-0.3V to (VL + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW°C above +70°C).....889mW
Operating Temperature Ranges
MAX1202_C_P/MAX1203_C_P .....0°C to +70°C
MAX1202_E_P/MAX1203_E_P.....-40°C to +85°C
MAX1202BMJP/MAX1203BMJP.....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)	INL	MAX1202A/MAX1203A				±0.5	LSB
		MAX1202B/MAX1203B				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1.0	LSB
Offset Error						±3.0	LSB
Gain Error (Note 3)		MAX1202 (all grades)				±3	LSB
		External reference, 4.096V	MAX1203A			±0.5	
			MAX1203B			±3	
Gain Temperature Coefficient		External reference, 4.096V			±0.8		ppm/°C
Channel-to-Channel Offset Matching					±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 4.096Vp-p, 133ksps, 2.0MHz external clock, bipolar-input mode)							
Signal-to-Noise + Distortion Ratio	SINAD			70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD					-80	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		V_{IN} = 4.096Vp-p, 65kHz (Note 4)			-85		dB
Small-Signal Bandwidth		-3dB rolloff			4.5		MHz
Full-Power Bandwidth					800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}		1.5			µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock Frequency Range		External compensation mode, 4.7µF	0.1		2.0	MHz
		Internal compensation mode (Note 6)	0.1		0.4	
		Used for data transfer only	0		2.0	
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 7)		Unipolar, V_{SS} = 0V			V_{REF}	V
		Bipolar, V_{SS} = -5V			$\pm V_{REF}/2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE (MAX1202 only, reference-buffer enabled)						
REF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
REF Short-Circuit Current					30	mA
V_{REF} Temperature Coefficient		MAX1202AC		±30	±50	ppm/°C
		MAX1202AE		±30	±60	
		MAX1202B		±30		
Load Regulation (Note 8)		0mA to 0.5mA output load		2.5		mV
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT REF (Reference buffer disabled, V_{REF} = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V		1.5	10	µA
REFADJ Buffer Disable Threshold			V_{DD} - 50mV			V

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX1202		1.68		V/V
		MAX1203		1.64		
REFADJ Input Current		MAX1202			±50	µA
		MAX1203			±5	
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down (Note 9)		30	70	µA
		Full power-down (Note 9)		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	
Logic Supply Voltage	VL		2.70		5.25	V
Logic Supply Current (Notes 6, 10)	I_{VL}	VL = V_{DD} = 5V			10	µA
Positive Supply Rejection (Note 11)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 11)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV
Logic Supply Rejection (Note 12)	PSR	External reference, 4.096V; full-scale input		±0.06	±0.5	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}		2.0			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.5		V_{DD} - 1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{SH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{SL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Maximum Allowed Leakage, Mid-Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS: DOUT, SSTRB (VL = 2.7V to 3.6V)						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	VL - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = VL			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = VL (Note 6)			15	pF
DIGITAL OUTPUTS: DOUT, SSTRB (VL = 4.75V to 5.25V)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 8mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

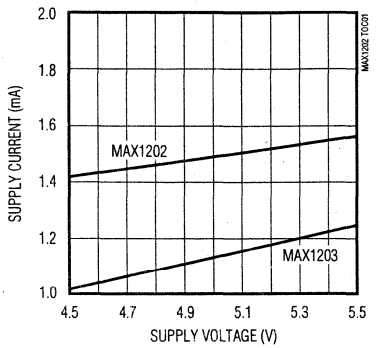
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.5			µs
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	20		240	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External-clock mode only, C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External-clock mode only, C_{LOAD} = 100pF			240	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal-clock mode only	0			ns

Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar-input mode.
Note 2: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
Note 3: MAX1202—internal reference, offset nulled; MAX1203—external reference (V_{REF} = 4.096V), offset nulled.
Note 4: On-channel grounded; sine wave applied to all off-channels.
Note 5: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: Common-mode range for analog inputs is from V_{SS} to V_{DD}.
Note 8: External load should not change during the conversion for specified accuracy.
Note 9: Shutdown supply current is measured with VL at 3.3V, and with all digital inputs tied to either VL or GND; REFADJ = GND. Shutdown supply current is also dependent on V_{IH} (Figure 12c).
Note 10: Logic supply current is measured with the digital outputs (DOUT and SSTRB) disabled ($\overline{CS}$ high). When the outputs are active ($\overline{CS}$ low), the logic supply current depends on f_{SCLK}, and on the static and capacitive load at DOUT and SSTRB.
Note 11: Measured at V_{SUPPLY} + 5% and V_{SUPPLY} - 5% only.
Note 12: Measured at VL = 2.7V and VL = 3.6V.

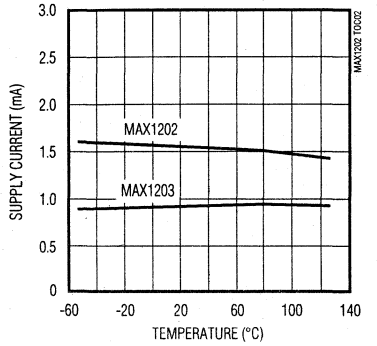
Typical Operating Characteristics

(V_{DD} = 5V ±5%; VL = 2.7V to 3.6V; V_{SS} = 0V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = +25°C; unless otherwise noted.)

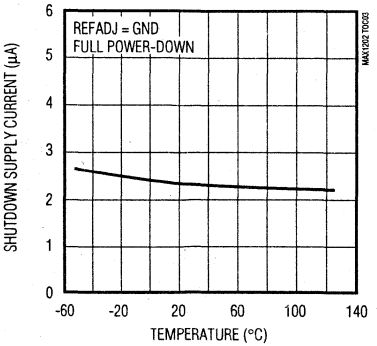
SUPPLY CURRENT vs. SUPPLY VOLTAGE



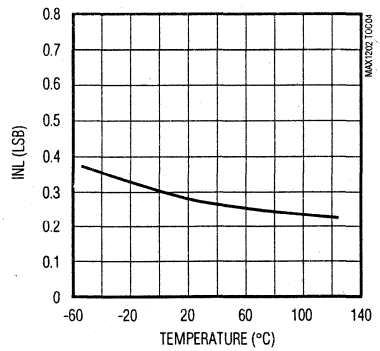
SUPPLY CURRENT vs. TEMPERATURE



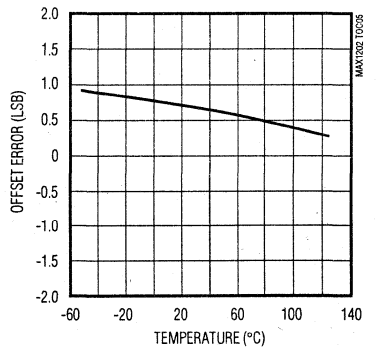
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



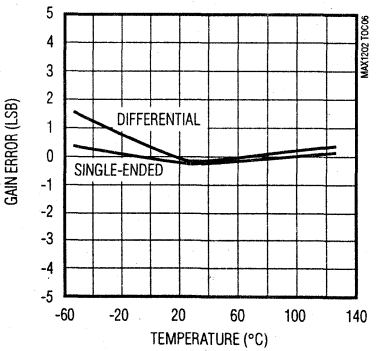
INTEGRAL NONLINEARITY vs. TEMPERATURE



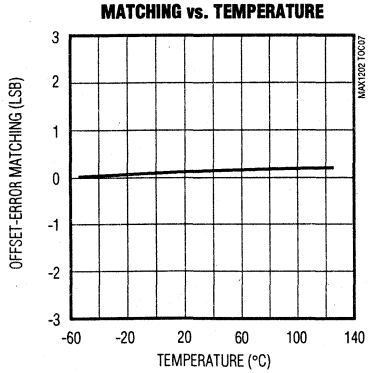
OFFSET ERROR vs. TEMPERATURE



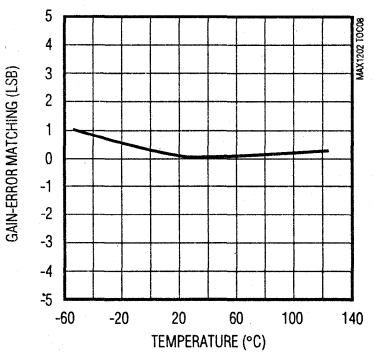
GAIN ERROR vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE

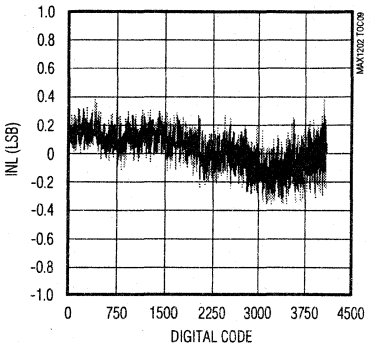


5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

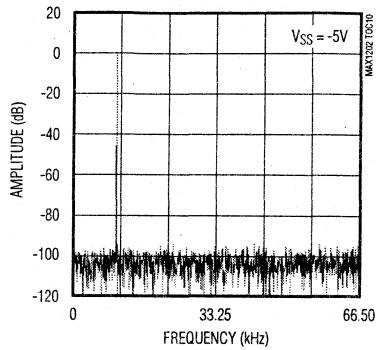
Typical Operating Characteristics (continued)

(V_{DD} = 5V ±5%; VL = 2.7V to 3.6V; V_{SS} = 0V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1202—4.7µF capacitor at REF pin; MAX1203—external reference, V_{REF} = 4.096V applied to REF pin; T_A = +25°C; unless otherwise noted.)

INTEGRAL NONLINEARITY vs. DIGITAL



FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie V_{SS} to -5V ±5% or to GND.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1202/MAX1203 down to 10µA (max) supply current; otherwise, the MAX1202/MAX1203 are fully operational. Pulling $\overline{SHDN}$ to V_{DD} puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	REF	Reference-Buffer Output/ADC Reference Input. In internal reference mode (MAX1202 only), the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the Reference-Buffer Amplifier. Tie REFADJ to V_{DD} to disable the reference-buffer amplifier.
13	GND	Ground; IN- Input for Single-Ended Conversions
14	VL	Supply Voltage for Digital Output Pins. Voltage applied to VL determines the positive output swing of the Digital Outputs (DOUT, SSTRB). 2.7V ≤ VL ≤ 5.25V.
15	DOUT	Serial-Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1202/MAX1203 begin the analog-to-digital conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial-Clock Input. SCLK clocks data in and out of the serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

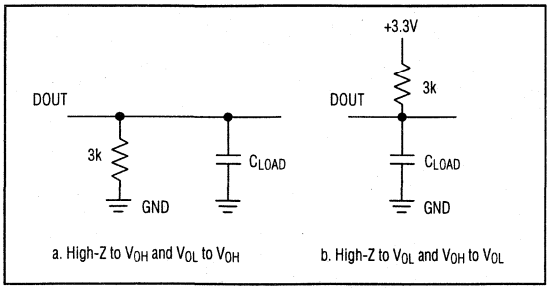


Figure 1. Load Circuits for Enable Time

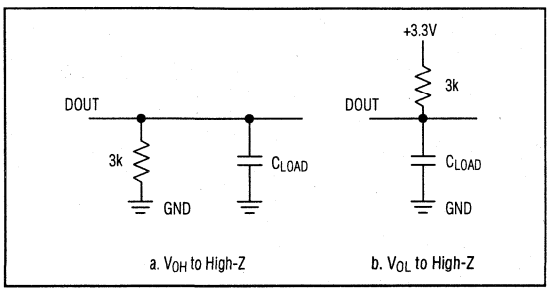


Figure 2. Load Circuits for Disable Time

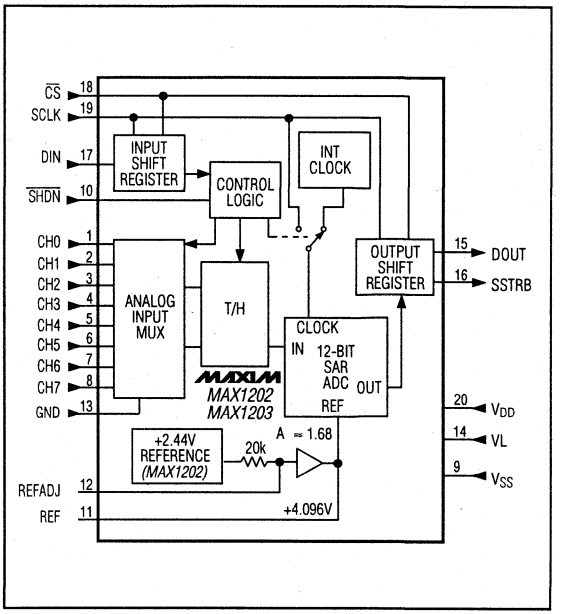


Figure 3. Block Diagram

Detailed Description

The MAX1202/MAX1203 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to 3V microprocessors (µPs). Figure 3 is the MAX1202/MAX1203 block diagram.

Pseudo-Differential Input

Figure 4 shows the ADC's analog comparator's sampling architecture. In single-ended mode, IN+ is internally switched to CH0–CH7 and IN- is switched to GND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels using Tables 3 and 4.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential such that only the signal at IN+ is sampled. The return side (IN-) must remain stable (typically within ±0.5LSB, within ±0.1LSB for best results) with respect to GND during a conversion. To do this, connect a 0.1µF capacitor from IN- (of the selected analog input) to GND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the input control word's last bit is entered. The T/H switch opens at the end of the acquisition interval, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply GND. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge of 16pF x [(V_{IN+}) - (V_{IN-})] from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

Track/Hold

The T/H enters tracking mode on the falling clock edge after the fifth bit of the 8-bit control word is shifted in. The T/H enters hold mode on the falling clock edge after the eighth bit of the control word is shifted in. IN- is connected to GND if the converter is set up for single-ended inputs, and the converter samples the "+" input. IN- connects to the "-" input if the converter is set up for differential inputs, and the difference of $|IN+ - IN-|$ is sampled. The positive input connects back to IN+, at the end of the conversion, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, acquisition time increases and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where $R_{IN} = 9k\Omega$, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Source impedances below 1kΩ do not significantly affect the ADC's AC performance. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

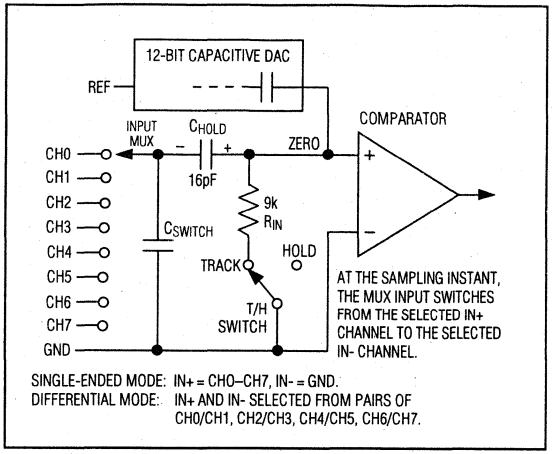


Figure 4. Equivalent Input Circuit

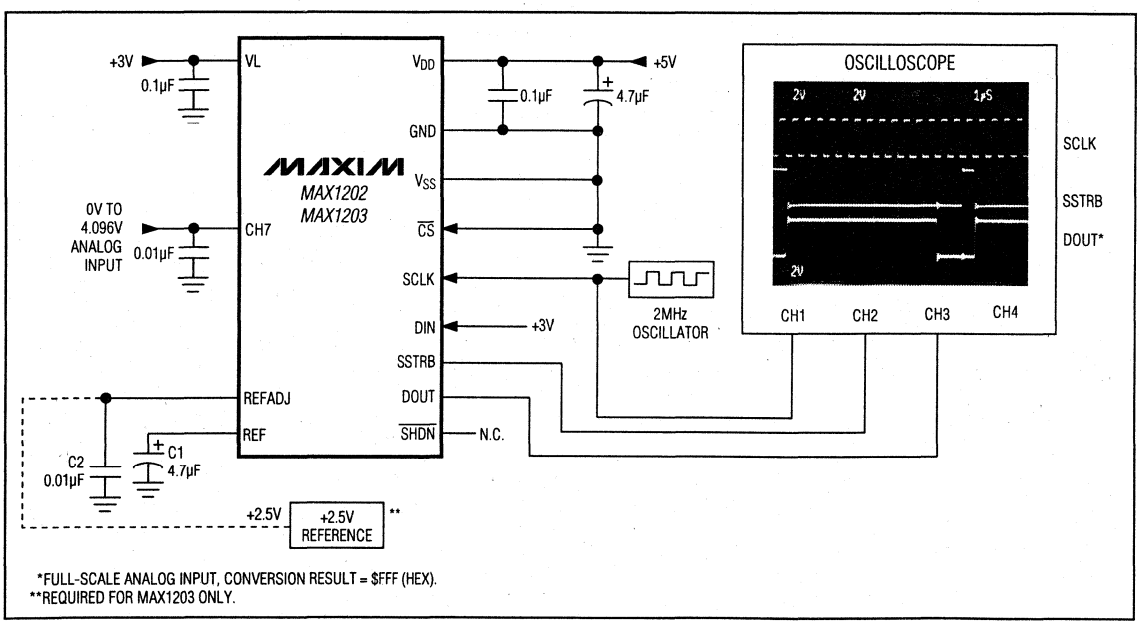


Figure 5. Quick-Look Circuit

Table 1a. Unipolar Full Scale and Zero Scale

REFERENCE		ZERO SCALE	FULL SCALE
Internal		0V	+4.096V
External	at REFADJ	0V	V_{REFADJ} x A*
	at REF	0V	V_{REF}

A = 1.68 for the MAX1202, 1.64 for the MAX1203.

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

REFERENCE		NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
Internal		-4.096V / 2	0V	+4.096V / 2
External	at REFADJ	-1/2 V_{REFADJ} x A*	0V	+1/2 V_{REFADJ} x A*
	at REF	-1/2 V_{REF}	0V	+1/2 V_{REF}

A = 1.68 for the MAX1202, 1.64 for the MAX1203.

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth. Therefore it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog inputs to V_{DD} and V_{SS}, allow the analog input pins to swing from (V_{SS} - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels more than 2mA.

The full-scale input voltage depends on the voltage at REF (Tables 1a and 1b).

Quick Look

Use the circuit of Figure 5 to quickly evaluate the MAX1202/MAX1203's analog performance. The MAX1202/MAX1203 require a control byte to be written to DIN before each conversion. Tying DIN to +3V feeds in control byte $FF hex, which triggers single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the 12-bit conversion result shifts out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 15 clock cycles per conversion is required. All SSTRB and DOUT output transitions occur on SCLK's falling edge.

How to Start a Conversion

Clocking a control byte into DIN starts conversion on the MAX1202/MAX1203. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1202/MAX1203's internal shift register. After $\overline{CS}$ falls, the first logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX1202/MAX1203 are fully compatible with SPI/Microwire devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result).

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL 2	SEL 1	SEL 0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7 (MSB)	START	The first logic **1** bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels is used for the conversion (Tables 3 and 4).
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to V_{REF} can be converted; in bipolar mode, the signal can range from $-V_{REF}/2$ to $+V_{REF}/2$.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to GND. In differential mode, the voltage difference between two channels is measured. (Tables 3 and 4.)
1 0 (LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_{DD} = 2µA, internal reference) **0** **1** Fast power-down (I_{DD} = 30µA, internal reference) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	GND
0	0	0	+								−
1	0	0		+							−
0	0	1			+						−
1	0	1				+					−
0	1	0					+				−
1	1	0						+			−
0	1	1							+		−
1	1	1								+	−

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	−						
0	0	1			+	−				
0	1	0					+	−		
0	1	1							+	−
1	0	0	−	+						
1	0	1			−	+				
1	1	0					−	+		
1	1	1							−	+

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1's format should be: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX1202/MAX1203 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX1202/MAX1203 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure that the total conversion time does not exceed 120µs.

Digital Output

In unipolar-input mode, the output is straight binary (Figure 15); for bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format. The digital output logic level is adjusted with the VL pin. This allows DOUT and SSTRB to interface with 3V logic without the risk of overdrive. The MAX1202/MAX1203's digital inputs are designed to be compatible with 5V CMOS logic as well as 3V logic.

Internal and External Clock Modes

The MAX1202/MAX1203 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1202/MAX1203. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the A/D conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows SSTRB timing in external clock mode.

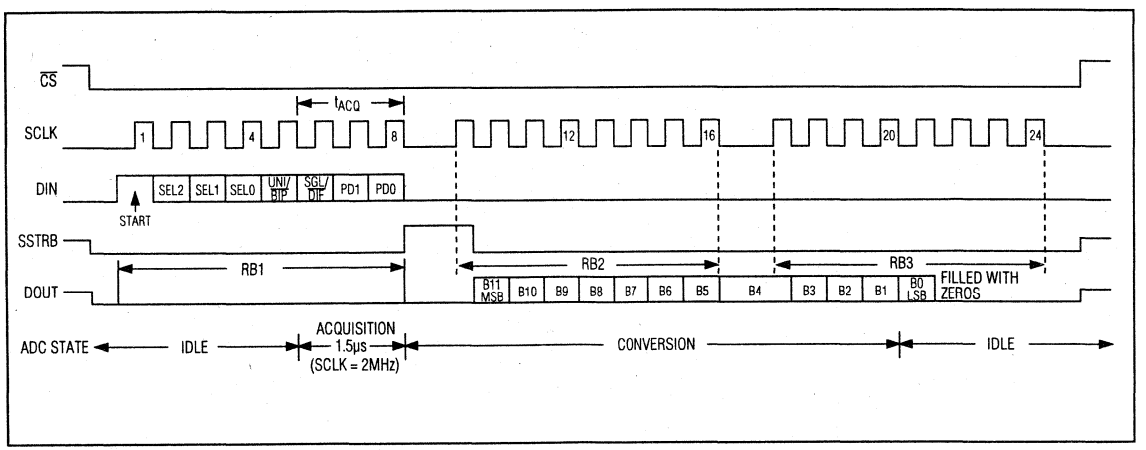


Figure 6. 24-Bit External Clock Mode Conversion Timing (Microwire and SPI Compatible)

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

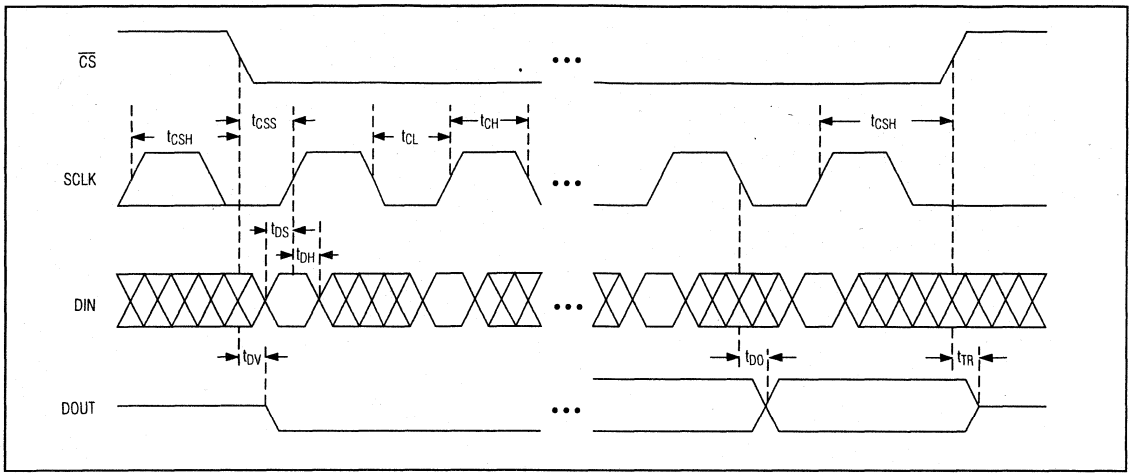


Figure 7. Detailed Serial-Interface Timing

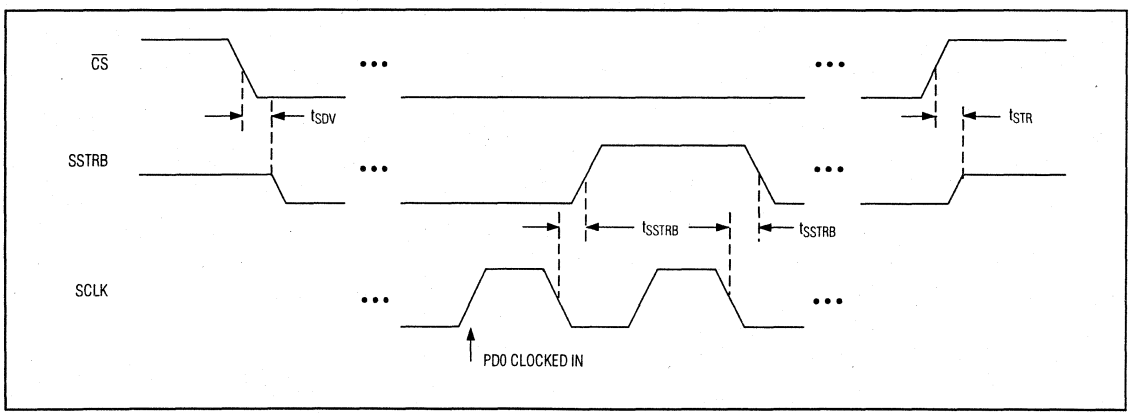


Figure 8. External Clock Mode SSTRB Detailed Timing

The conversion must complete in some minimum time or droop on the sample-and-hold capacitors might degrade conversion results. Use internal clock mode if the clock period exceeds 10µs or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX1202/MAX1203 generate their own conversion clock. This frees the µP from running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 2MHz. SSTRB goes low at the start of the conversion, then goes high when the conversion is complete. SSTRB is low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data while the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a

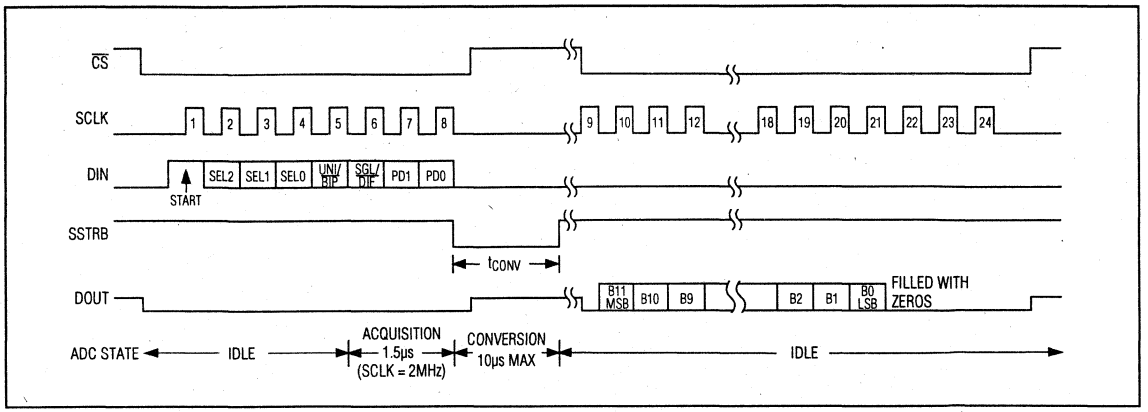


Figure 9. Internal Clock Mode Timing

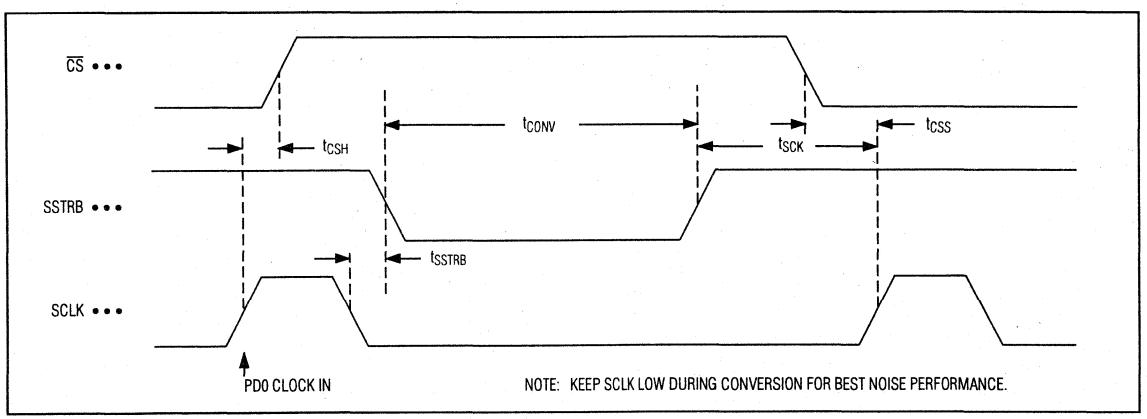


Figure 10. Internal Clock Mode SSTRB Detailed Timing

conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1202/MAX1203 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 10 shows SSTRB timing in internal clock mode. Data can be shifted in and out of the MAX1202/MAX1203 at clock rates up to 2.0MHz, if t_{ACQ} is kept above 1.5µs.

Data Framing

$\overline{CS}$'s falling edge does **not** start a conversion on the MAX1202/MAX1203. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as one of the following:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle (e.g., after V_{DD} is applied).

or

The first high bit clocked into DIN after bit 5 (B5) of a conversion in progress appears at DOUT.

If a falling edge on $\overline{CS}$ forces a start bit before B5 becomes available, the current conversion is terminated and a new one started. Thus, the fastest the MAX1202/MAX1203 can run is 15 clocks/conversion.

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that data transfers occur in multiples of eight clock cycles; 16 clocks per conversion is typically the fastest that a µC can drive the MAX1202/MAX1203. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1202/MAX1203 in internal clock mode, ready to convert with SSTRB = high. After the power supplies are stabilized, the internal reset time is 100µs. No conversions should be performed during this phase. SSTRB is high on power-up, and if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at REF. A value of 4.7µF or greater ensures stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the section *Choosing Power-Down Mode,* and Table 5).

Internal compensation requires no external capacitor at REF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for the shortest power-up times, but the external clock must be limited to 400kHz during the conversion.

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

For the MAX1202, fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Since the MAX1203 does not have an internal reference, power-up times coming out of full or fast power-down are identical.

I_{DD} shutdown current can increase if any digital input (DIN, SCLK, $\overline{CS}$) is held high in either power-down mode. The actual shutdown current depends on the state of the digital inputs, the voltage applied to the digital inputs (V_{IH}), the supply voltage (V_{DD}), and the operating temperature. Figure 12c shows the maximum I_{DD} increase for each digital input held high in power-down mode for different operating conditions. This current is cumulative, so if all three digital inputs are held high, the additional shutdown current is three times the value shown in Figure 12c.

In both software power-down modes, the serial interface remains operational, but the ADC does not convert.

Table 5 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, the capacitor has to supply the current into the reference (typically 1.5µA) and the transient currents at power-up.

Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify the clock mode. When software power-down is asserted, the ADC continues to operate in the last specified clock mode until the conversion is complete. The ADC then powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results can be clocked out even though the MAX1202/MAX1203 have already entered software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1202/MAX1203. Following the start bit, the control byte also determines clock and power-down modes. For example, if the DIN word contains PD1 = 1, the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

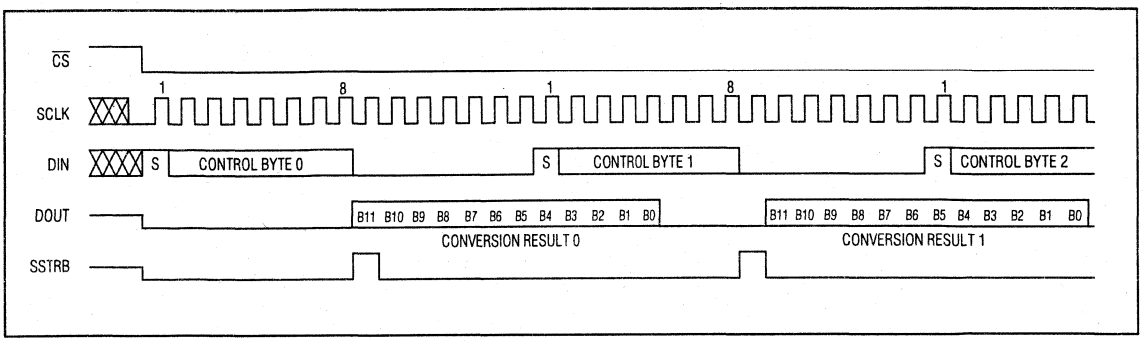


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

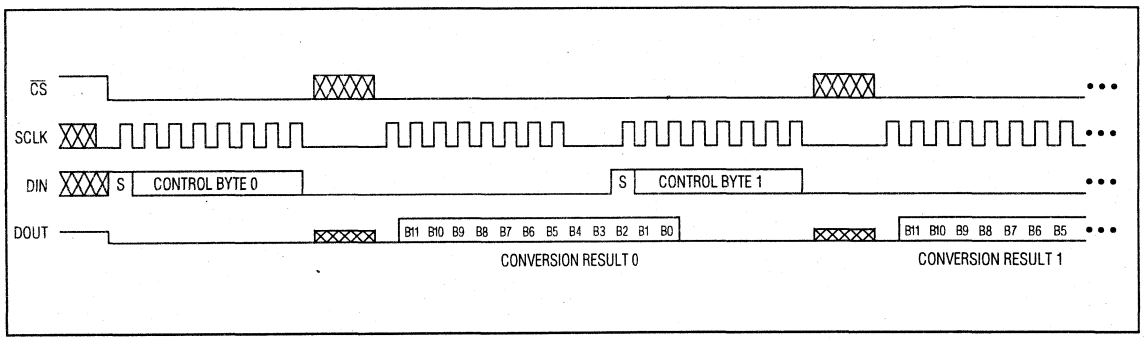


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into full power-down mode. Unlike the software power-down modes, conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference, which is not shut down, is used. $\overline{SHDN}$ also selects internal or external reference compensation (Table 7).

Power-Down Sequencing

The MAX1202/MAX1203's automatic power-down modes can save considerable power when operating at less than maximum sample rates. The following sections discuss the various power-down sequences.

Lowest Power at up to 500 Conversions per Channel per Second

Figure 14a depicts MAX1202 power consumption for one or eight channel conversions using full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor, with a 0.2ms time constant. To achieve full 12-bit accuracy, 10 time constants (or 2ms in this example) are required for the reference buffer to settle. When exiting FULLPD, waiting this 2ms in FASTPD mode (instead of just exiting FULLPD mode and returning to normal operating mode) reduces power consumption by a factor of 10 or more (Figure 13).

Lowest Power at Higher Throughputs

Figure 14b shows power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up. This circuit combines fast multichannel conversion with the lowest power consumption possible. Full power-down mode can increase power savings in applications where the MAX1202/MAX1203 are inactive for long periods of time, but where intermittent bursts of high-speed conversion are required.

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

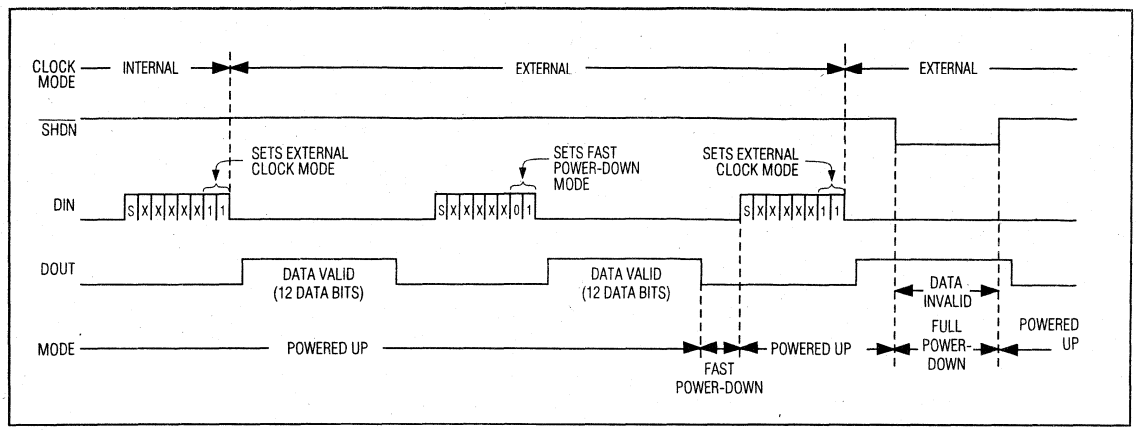


Figure 12a. Timing Diagram for Power-Down Modes, External Clock

Table 5. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	REF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal		Fast	5	26
Enabled	Internal		Full	300	26
Enabled	External	4.7	Fast/Full	See Figure 14c	133
Disabled			Fast	2	133
Disabled			Full	2	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	DEVICE MODE
0	0	Full power-down mode
0	1	Fast power-down mode
1	0	Internal clock mode
1	1	External clock mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION
V_{DD}	Enabled	Internal compensation
Floating	Enabled	External compensation
GND	Full Power-Down	N/A

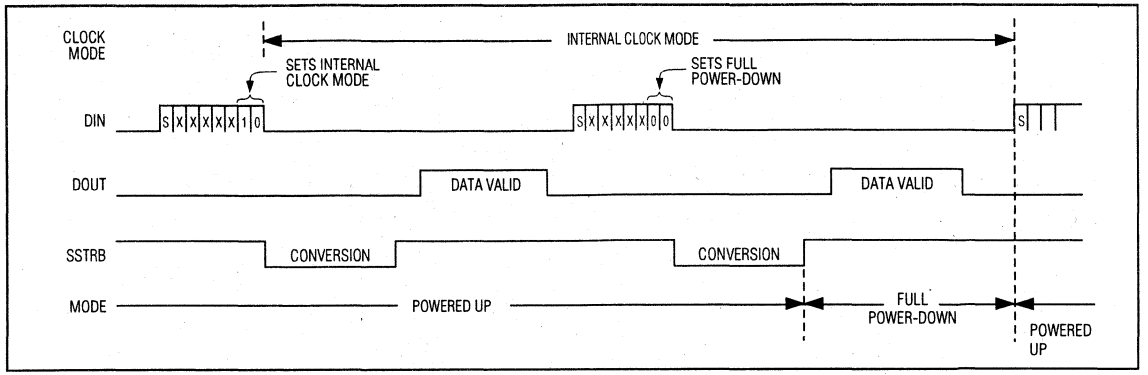


Figure 12b. Timing Diagram for Power-Down Modes, Internal Clock

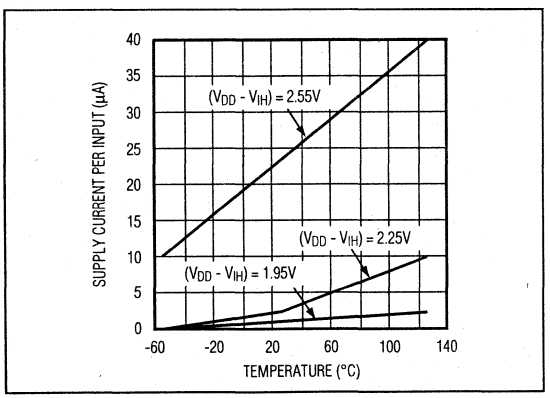


Figure 12c. Additional I_{DD} Shutdown Supply Current vs. V_{IH} for Each Digital Input at a Logic 1

External and Internal References

The MAX1202 can be used with an internal or external reference, whereas an external reference is required for the MAX1203. An external reference can be connected directly at the REF terminal, or at the REFADJ pin.

An internal buffer is designed to provide 4.096V at REF for both the MAX1202 and the MAX1203. The MAX1202's internally trimmed 2.44V reference is buffered with a gain of 1.68. The MAX1203's REFADJ pin is buffered with a gain of 1.64, to scale an external 2.5V reference at REFADJ to 4.096V at REF.

MAX1202 Internal Reference

The MAX1202's full-scale range using the internal reference is 4.096V with unipolar inputs and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit of Figure 17.

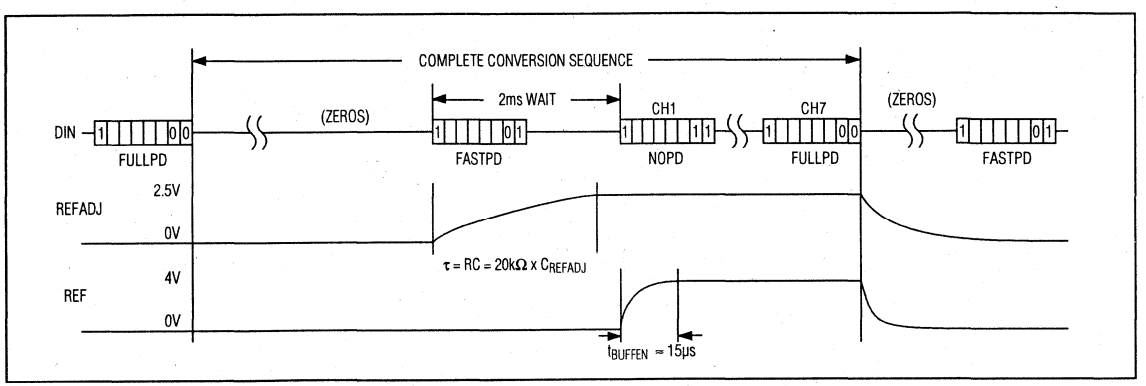


Figure 13. MAX1202 FULLPD/FASTPD Power-Up Sequence

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

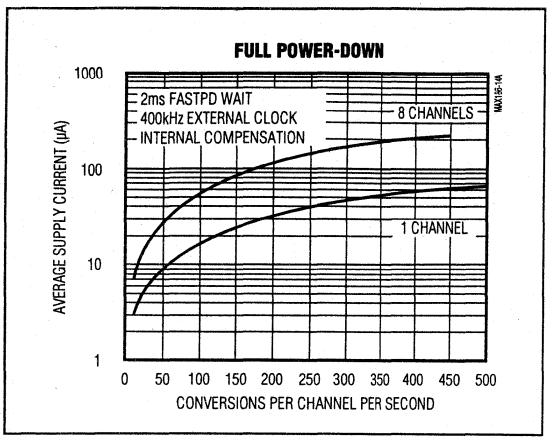


Figure 14a. MAX1202 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

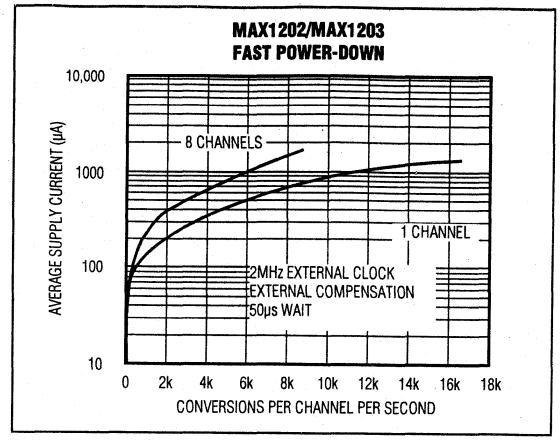


Figure 14b. MAX1202/MAX1203 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

External Reference

With both the MAX1202 and MAX1203, an external reference can be placed at either the input (REFADJ) or the output (REF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX1202, and higher than 100kΩ for the MAX1203, where the internal reference is omitted. At REF, the DC input resistance is a minimum of 12kΩ. During conversion, an external reference at REF must deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Using the buffered REFADJ input makes buffering of the external reference unnecessary. When connecting an external reference directly at REF, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to GND to minimize the input bias current in power-down.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar I/O transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary with 1LSB = 1.00mV (4.096V/4096) for unipolar operation, and 1LSB = 1.00mV [(4.096V/2 - -4.096V/2)/4096] for bipolar operation.

Figure 17 shows how to adjust the ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±65LSBs) of gain adjustment range.

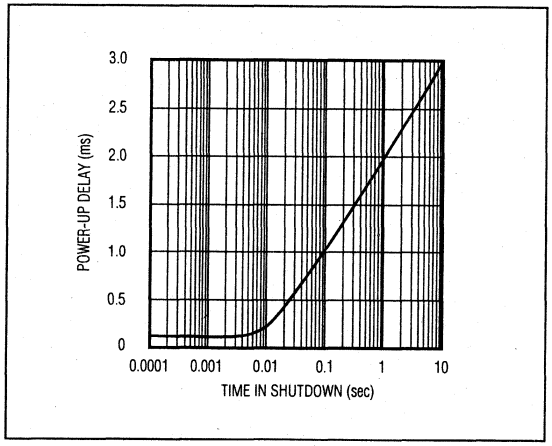


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. Establish a single-point analog ground

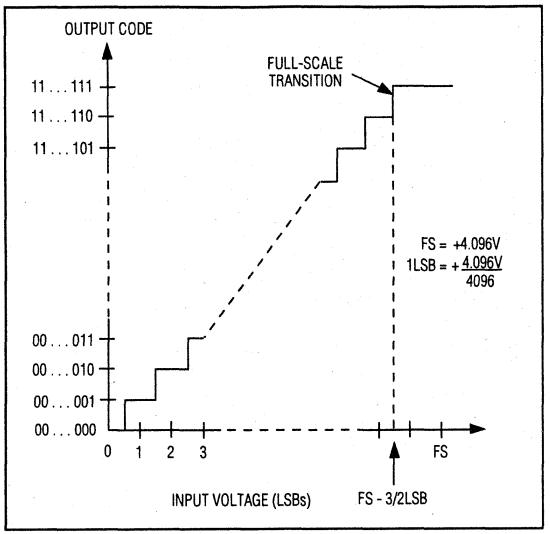


Figure 15. Unipolar Transfer Function, 4.096V = Full Scale

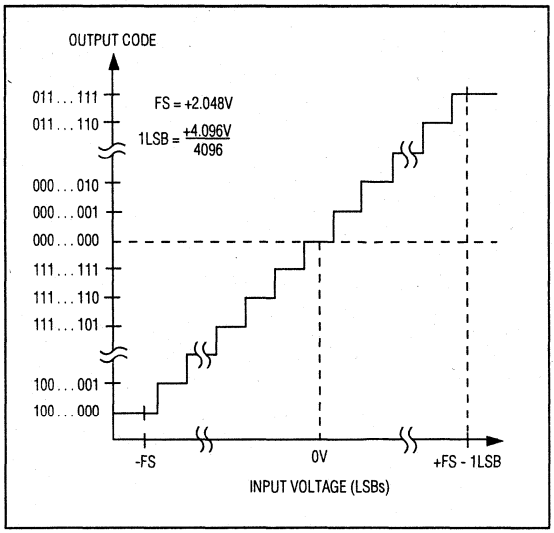


Figure 16. Bipolar Transfer Function, ±4.096V/2 = Full Scale

("star" ground point) at GND. Connect all other analog grounds to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the power supplies can affect the ADC's high-speed comparator. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX1202/MAX1203. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter, as shown in Figure 18.

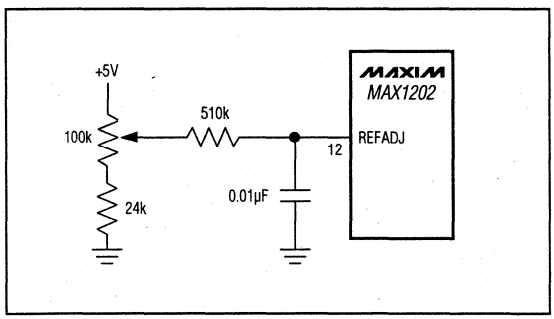


Figure 17. MAX1202 Reference-Adjust Circuit

5V, 8-Channel, Serial, 12-Bit ADCs with 3V Digital Interface

TMS320CL3x to MAX1202/ MAX1203 Interface

Figure 19 shows an application circuit to interface the MAX1202/MAX1203 to the TMS320 in external clock mode. Figure 20 shows the timing diagram for this interface circuit.

Use the following steps to initiate a conversion in the MAX1202/MAX1203 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. The TMS320's CLKX and CLKR are tied together with the MAX1202/MAX1203's SCLK input.
2) The MAX1202/MAX1203's $\overline{CS}$ is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX1202/MAX1203's DIN.
3) Write an 8-bit word (1XXXXX11) to the MAX1202/MAX1203 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The MAX1202/MAX1203's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1202/MAX1203.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1202/MAX1203 until the next conversion is initiated.

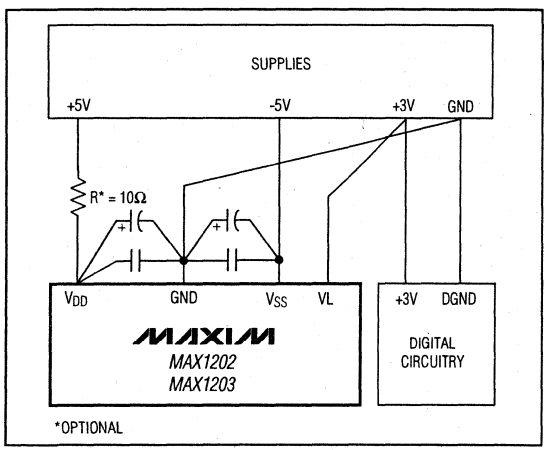


Figure 18. Power-Supply Grounding Connection

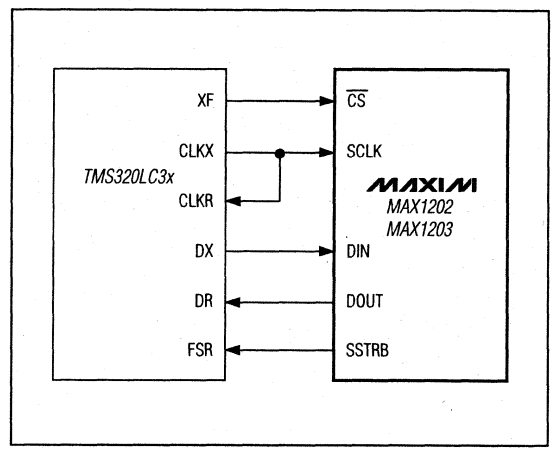


Figure 19. MAX1202/MAX1203-to-TMS320 Serial Interface

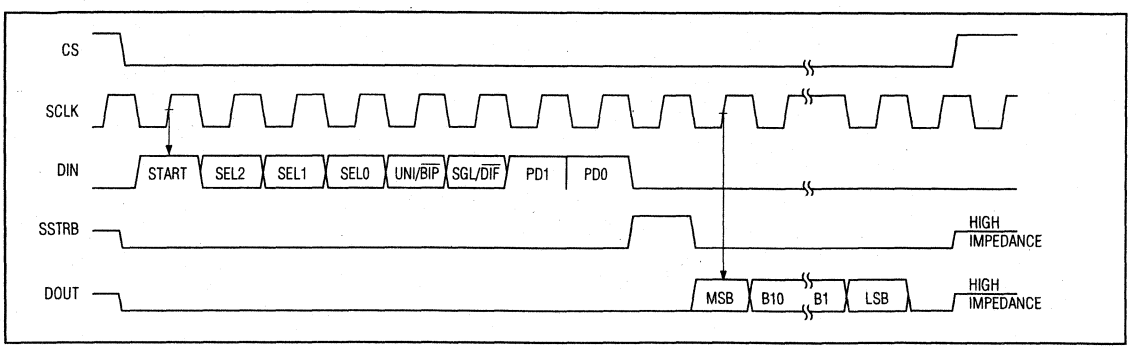


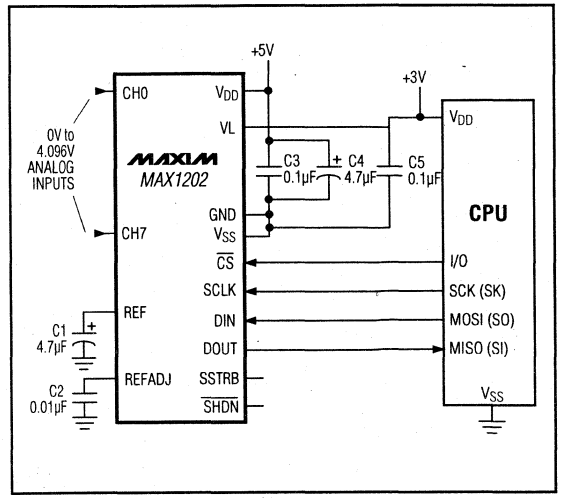
Figure 20. TMS320 Serial-Interface Timing Diagram

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1202AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1202BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1202AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1202BEAP	-40°C to +85°C	20 SSOP	±1
MAX1202BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX1203ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1203BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1203ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1203BCAP	0°C to +70°C	20 SSOP	±1
MAX1203BC/D	0°C to +70°C	Dice*	±1
MAX1203AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1203BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1203AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1203BEAP	-40°C to +85°C	20 SSOP	±1
MAX1203BMJP	-55°C to +125°C	20 CERDIP**	±1

*Dice are specified at T_A = +25°C, DC parameters only.
**Contact factory for availability.

_____Typical Operating Circuit



_____Chip Information

TRANSISTOR COUNT: 2503
SUBSTRATE CONNECTED TO V_{SS}

19-1179; Rev 0; 1/97

MAXIM

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

General Description

The MAX1204 is a 10-bit data-acquisition system specifically designed for use in applications with mixed +5V (analog) and +3V (digital) supply voltages. It operates with a single +5V analog supply or dual ±5V analog supplies, and combines an 8-channel multiplexer, internal track/hold, and serial interface with high conversion speed and low power consumption.

A 4-wire serial interface connects directly to SPI™/Microwire™ devices without external logic, and a serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1204 uses either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions. The serial interface operates at up to 2MHz.

The MAX1204 features an internal 4.096V reference and a reference-buffer amplifier that simplifies gain trim. It also has a VL pin that supplies power to the digital outputs. Output logic levels (3V, 3.3V, or 5V) are determined by the value of the voltage applied to this pin.

A hard-wired $\overline{SHDN}$ pin and two software-selectable power-down modes are provided. Accessing the serial interface automatically powers up the device. A quick turn-on time allows the MAX1204 to be shut down between conversions, enabling the user to optimize supply currents. By customizing power-down between conversions, supply current can drop below 10µA at reduced sampling rates.

The MAX1204 is available in 20-pin SSOP and DIP packages, and is specified for the commercial, extended, and military temperature ranges.

Applications

5V/3V Mixed-Supply Systems
Data Acquisition
Process Control
Battery-Powered Instruments
Medical Instruments

Typical Operating Circuit appears on last page.

SPI is a registered trademark of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

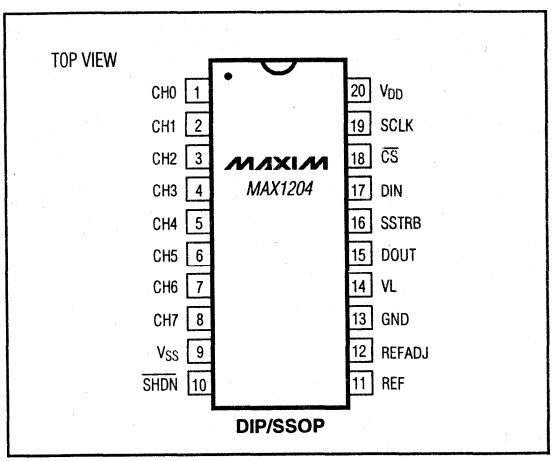
- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Operates from +5V Single or ±5V Dual Supplies**
- ♦ **User-Adjustable Output Logic Levels (2.7V to 5.25V)**
- ♦ **Low Power: 1.5mA (operating mode) 2µA (power-down mode)**
- ♦ **Internal Track/Hold, 133kHz Sampling Rate**
- ♦ **Internal 4.096V Reference**
- ♦ **SPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar/Bipolar Inputs**
- ♦ **20-Pin DIP/SSOP**
- ♦ **Pin-Compatible 12-Bit Upgrade: MAX1202**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1204ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX1204BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX1204ACAP	0°C to +70°C	20 SSOP	±1/2
MAX1204BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued at end of data sheet.

Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
VL .....-0.3V to (V_{DD} + 0.3V)
V_{SS} to GND .....+0.3V to -6V
V_{DD} to V_{SS} .....-0.3V to +12V
CH0–CH7 to GND .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
CH0–CH7 Total Input Current .....±20mA
REF to GND .....-0.3V to (V_{DD} + 0.3V)
REFADJ to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Outputs to GND .....-0.3V to (VL + 0.3V)
Digital Output Sink Current 25mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW°C above +70°C) 889mW
Operating Temperature Ranges
MAX1204_C_P .....0°C to +70°C
MAX1204_E_P .....-40°C to +85°C
MAX1204BMJP .....-55°C to +125°C
Storage Temperature Range .....-60°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX1204A			±0.5	LSB
		MAX1204B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1.0	LSB
Offset Error		MAX1204A			±1.0	LSB
		MAX1204B			±2.0	
Gain Error (Note 3)		MAX1204A			±1.0	LSB
		MAX1204B			±2.0	
Gain Temperature Coefficient		External reference, 4.096V		±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.1		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 4.096Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion (up to the 5th harmonic)	THD			-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		V_{IN} = 4.096Vp-p, 65kHz (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		4.5		MHz
Full-Power Bandwidth				800		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock	5.5		10	µs
		External clock, 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}		1.5			µs
Aperture Delay				10		ns
Aperture Jitter				<50		ps
Internal Clock Frequency				1.7		MHz
External Clock-Frequency Range		External compensation mode, 4.7µF	0.1		2.0	MHz
		Internal compensation mode (Note 6)	0.1		0.4	
		Used for data transfer only	0		2.0	
ANALOG INPUT						
Input Voltage Range, Single-Ended and Differential (Note 7)		Unipolar, V_{SS} = 0V			V_{REF}	V
		Bipolar, V_{SS} = -5V			$\pm V_{REF}/2$	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = ±5V		±0.01	±1	µA
Input Capacitance		(Note 6)		16		pF
INTERNAL REFERENCE						
REF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
REF Short-Circuit Current					30	mA
V_{REF} Temperature Coefficient		MAX1204AC		±30	±50	ppm/°C
		MAX1204AE		±30	±60	
		MAX1204B		±30		
Load Regulation (Note 8)		0mA to 0.5mA output load		2.5		mV
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT REF (Buffer disabled, V_{REF} = 4.096V)						
Input Voltage Range			2.50		V_{DD} + 50mV	V
Input Current				200	350	µA
Input Resistance			12	20		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V		1.5	10	µA
REFADJ Buffer Disable Threshold			V_{DD} - 50mV			V

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at REF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain				1.68		V/V
REFADJ Input Current					±50	µA
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}			5 ±5%		V
Negative Supply Voltage	V_{SS}			0 or -5 ±5%		V
Positive Supply Current	I_{DD}	Operating mode		1.5	2.5	mA
		Fast power-down (Note 9)		30	70	µA
		Full power-down (Note 9)		2	10	
Negative Supply Current	I_{SS}	Operating mode and fast power-down			50	µA
		Full power-down			10	
Logic Supply Voltage	VL		2.70		5.25	V
Logic Supply Current (Notes 6, 10)	I_{VL}	VL = V_{DD} = 5V			10	µA
Positive Supply Rejection (Note 11)	PSR	V_{DD} = 5V ±5%; external reference, 4.096V; full-scale input		±0.06	±0.5	mV
Negative Supply Rejection (Note 11)	PSR	V_{SS} = -5V ±5%; external reference, 4.096V; full-scale input		±0.01	±0.5	mV
Logic Supply Rejection (Note 12)	PSR	External reference, 4.096V; full-scale input		±0.06	±0.5	mV

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, VL = 2.7V to 5.25V; V_{SS} = 0V or -5V ±5%; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}		2.0			V
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.15		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.5			V
$\overline{SHDN}$ Input Mid-Voltage	V_{SM}		1.5		V_{DD} - 1.5	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = open		2.75		V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.5	V
$\overline{SHDN}$ Input Current, High	I_{SH}	$\overline{SHDN}$ = V_{DD}			4.0	µA
$\overline{SHDN}$ Input Current, Low	I_{SL}	$\overline{SHDN}$ = 0V	-4.0			µA
$\overline{SHDN}$ Maximum Allowed Leakage, Mid-Input		$\overline{SHDN}$ = open	-100		100	nA
DIGITAL OUTPUTS: DOUT, SSTRB (VL = 2.7V to 3.6V)						
Output Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
		I_{SINK} = 6mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	VL - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = VL			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = VL (Note 6)			15	pF
DIGITAL OUTPUTS: DOUT, SSTRB (VL = 4.75V to 5.25V)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 8mA		0.3		
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	4			V
Three-State Leakage Current	I_L	$\overline{CS}$ = 5V			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = 5V (Note 6)			15	pF

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

TIMING CHARACTERISTICS

(V_{DD} = +5V ±5%, VL = 2.7V to 3.6V, V_{SS} = 0V or -5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}		1.5			µs
DIN to SCLK Setup	t_{DS}		100			ns
DIN to SCLK Hold	t_{DH}				0	ns
SCLK Fall to Output Data Valid	t_{DO}	C_{LOAD} = 100pF	20		240	ns
$\overline{CS}$ Fall to Output Enable	t_{DV}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}		100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}		0			ns
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Fall to SSTRB	t_{SSTRB}	C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Fall to SSTRB Output Enable (Note 6)	t_{SDV}	External clock mode only, C_{LOAD} = 100pF			240	ns
$\overline{CS}$ Rise to SSTRB Output Disable (Note 6)	t_{STR}	External clock mode only, C_{LOAD} = 100pF			240	ns
SSTRB Rise to SCLK Rise (Note 6)	t_{SCK}	Internal clock mode only	0			ns

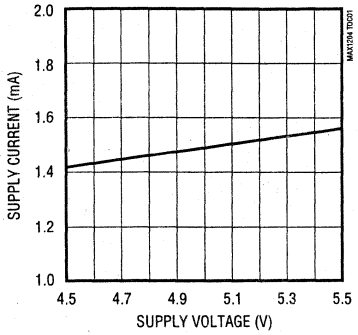
Note 1: Tested at V_{DD} = 5.0V; V_{SS} = 0V; unipolar input mode.
Note 2: Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
Note 3: Internal reference, offset nulled.
Note 4: On-channel grounded; sine-wave applied to all off-channels.
Note 5: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: Common-mode range for analog inputs is from V_{SS} to V_{DD}.
Note 8: External load should not change during the conversion for specified accuracy.
Note 9: Shutdown supply current is measured with VL at 3.3V, and with all digital inputs tied to either VL or GND (Figure 12c); REFADJ = GND.
Note 10: Logic supply current is measured with the digital outputs (DOUT and SSTRB) disabled ($\overline{CS}$ high). When the outputs are active ($\overline{CS}$ low), the logic supply current depends on f_{SCLK}, and on the static and capacitive load at DOUT and SSTRB.
Note 11: Measured at V_{SUPPLY} +5% and V_{SUPPLY} -5% only.
Note 12: Measured at VL = 2.7V and VL = 3.6V.

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

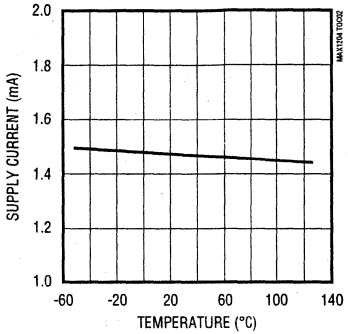
Typical Operating Characteristics

(V_{DD} = 5V ±5%; VL = 2.7V to 3.6V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); 4.7µF capacitor at REF; T_A = +25°C; unless otherwise noted.)

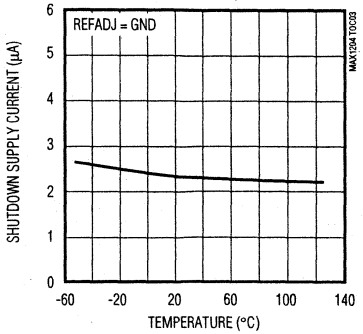
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1–8	CH0–CH7	Sampling Analog Inputs
9	V_{SS}	Negative Supply Voltage. Tie V_{SS} to -5V ±5% or GND.
10	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1204 down to 10µA (max) supply current; otherwise, the MAX1204 is fully operational. Pulling $\overline{SHDN}$ to V_{DD} puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
11	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
12	REFADJ	Input to the Reference-Buffer Amplifier. Tie REFADJ to V_{DD} to disable the reference-buffer amplifier.
13	GND	Ground; IN- Input for Single-Ended Conversions
14	VL	Supply Voltage for Digital Output Pins. Voltage applied to VL determines the positive output swing of the Digital Outputs (DOUT, SSTRB).
15	DOUT	Serial-Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
16	SSTRB	Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1204 begins the analog-to-digital conversion and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
17	DIN	Serial-Data Input. Data is clocked in at SCLK's rising edge.
18	$\overline{CS}$	Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
19	SCLK	Serial-Clock Input. SCLK clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60% in external clock mode.)
20	V_{DD}	Positive Supply Voltage, +5V ±5%

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

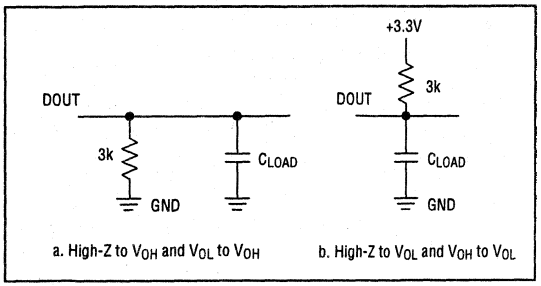


Figure 1. Load Circuits for Enable Time

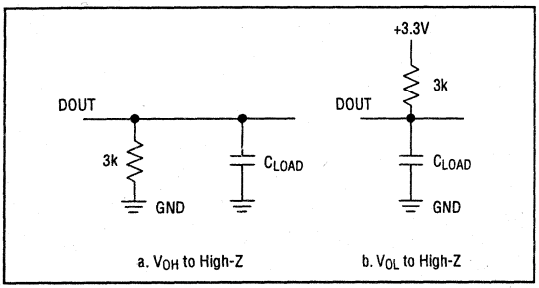


Figure 2. Load Circuits for Disable Time

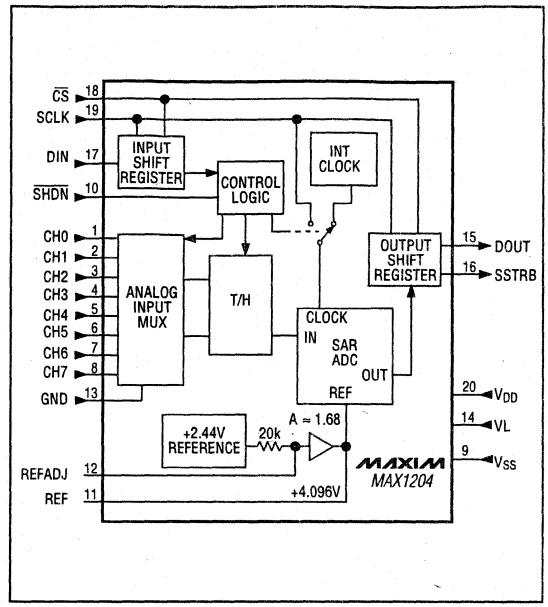


Figure 3. Block Diagram

Detailed Description

The MAX1204 uses a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to 3V microprocessors (µPs). Figure 3 is the MAX1204 block diagram.

Pseudo-Differential Input

Figure 4 shows the analog-to-digital converter's (ADC's) analog comparator's sampling architecture. In single-ended mode, IN+ is internally switched to CH0–CH7 and IN- is switched to GND. In differential mode, IN+ and IN- are selected from pairs of CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the channels using Tables 3 and 4.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential such that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to GND during a conversion. To do this, connect a 0.1µF capacitor from IN- (of the selected analog input) to GND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the input control word's last bit is entered. The T/H switch opens at the end of the acquisition interval, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply GND. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN+}) - (V_{IN-})]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters tracking mode on the falling clock edge after the fifth bit of the 8-bit control word is shifted in. The T/H enters hold mode on the falling clock edge after the eighth bit of the control word is shifted in. IN- is connected to GND if the converter is set up for single-ended inputs, and the converter samples the "+" input. IN- connects to the "-" input if the converter is set up for differential inputs, and the difference of |IN+ - IN-| is sampled. The positive input connects back to IN+ at the end of the conversion, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, acquisition time increases and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following:

$$t_{ACQ} = 7 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 4kΩ do not significantly affect the ADC's AC performance. Higher source impedances can be used if an input capacitor is connected to the analog inputs, as shown in Figure 5. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

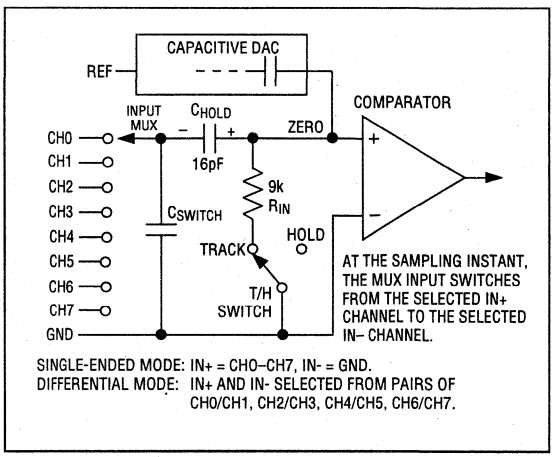


Figure 4. Equivalent Input Circuit

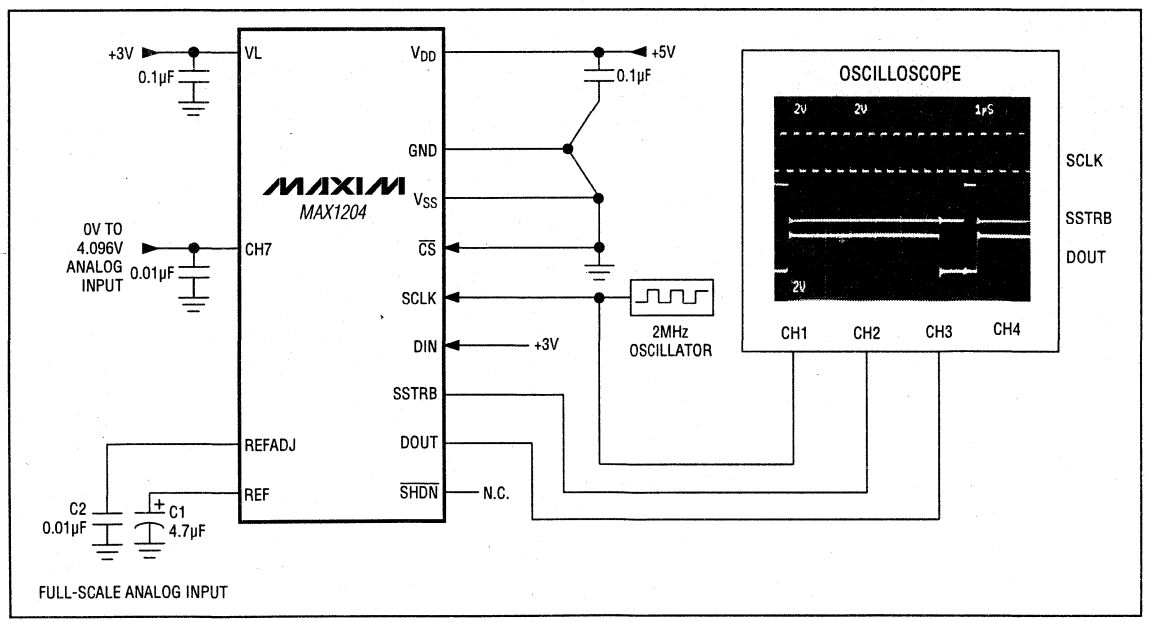


Figure 5. Quick-Look Circuit

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

Table 1a. Unipolar Full Scale and Zero Scale

REFERENCE		ZERO SCALE	FULL SCALE
Internal		0V	+4.096V
External	at REFADJ	0V	V_{REFADJ} x 1.68
	at REF	0V	V_{REF}

Table 1b. Bipolar Full Scale, Zero Scale, and Negative Full Scale

REFERENCE		NEGATIVE FULL SCALE	ZERO SCALE	FULL SCALE
Internal		-4.096V/2	0V	+4.096V / 2
External	at REFADJ	-1/2 V_{REFADJ} x 1.68	0V	+1/2 V_{REFADJ} x 1.68
	at REF	-1/2 V_{REF}	0V	+1/2 V_{REF}

Input Bandwidth

The ADC's input tracking circuitry has a 4.5MHz small-signal bandwidth. Therefore, it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Range and Input Protection

Internal protection diodes, which clamp the analog inputs to V_{DD} and V_{SS}, allow the analog input pins to swing from (V_{SS} - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV, or be lower than V_{SS} by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off-channels over 2mA, as excessive current degrades on-channel conversion accuracy.

The full-scale input voltage depends on the voltage at REF (Tables 1a and 1b).

Quick Look

Use the circuit of Figure 5 to quickly evaluate the MAX1204's analog performance. The MAX1204 requires that a control byte be written to DIN before each conversion. Tying DIN to +3V feeds in control byte $FF hex, which triggers single-ended unipolar conversions on CH7 in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for one clock period before the most significant bit of the conversion result shifts out of DOUT. Varying the analog input to CH7 alters the sequence of bits from DOUT. A total of 15 clock cycles per conversion is required. All SSTRB and DOUT output transitions occur on SCLK's falling edge.

How to Start a Conversion

Clocking a control byte into DIN starts conversion on the MAX1204. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1204's internal shift register. After $\overline{CS}$ falls, the first logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 2 shows the control-byte format.

The MAX1204 is fully compatible with Microwire and SPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire and SPI both transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit*, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the conversion result).

Table 2. Control-Byte Format

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
START	SEL 2	SEL 1	SEL 0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

Bit	Name	Description
7 (MSB)	START	The first logic **1** bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the eight channels is used for the conversion (Tables 3 and 4).
3	UNI/$\overline{BIP}$	**1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to V_{REF} can be converted; in bipolar mode, the signal can range from -V_{REF} / 2 to +V_{REF} / 2.
2	SGL/$\overline{DIF}$	**1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to GND. In differential mode, the voltage difference between two channels is measured. (Tables 3 and 4.)
1 0 (LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode **0** **0** Full power-down (I_{DD} = 2µA, internal reference) **0** **1** Fast power-down (I_{DD} = 30µA, internal reference) **1** **0** Internal clock mode **1** **1** External clock mode

Table 3. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	GND
0	0	0	+								–
1	0	0		+							–
0	0	1			+						–
1	0	1				+					–
0	1	0					+				–
1	1	0						+			–
0	1	1							+		–
1	1	1								+	–

Table 4. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+	–						
0	0	1			+	–				
0	1	0					+	–		
0	1	1							+	–
1	0	0	–	+						
1	0	1			–	+				
1	1	0					–	+		
1	1	1							–	+

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1's format should be: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ on the MAX1204 low.
3) Transmit TB1 and simultaneously receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and simultaneously receive byte RB3.
6) Pull $\overline{CS}$ on the MAX1204 high.

Figure 6 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with one leading zero, two trailing sub-bits (S1 and S0), and three trailing zeros. Total conversion time is a function of the serial clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure that the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 15); for bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format. The digital output logic level is adjusted with the VL pin. This allows DOUT and SSTRB to interface with 3V logic without the risk of overdrive. The MAX1204's digital inputs are designed to be compatible with 3V CMOS logic as well as 5V logic.

Internal and External Clock Modes

The MAX1204 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1204. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 7–10 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the A/D conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 6). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 8 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time or droop on the sample-and-hold can degrade conversion results. Use internal clock mode if the clock period exceeds 10µs or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

Internal Clock

In internal clock mode, the MAX1204 generates its own conversion clock. This frees the µP from running the SAR conversion clock, and allows the conversion results to be read back at the processor's convenience, at any clock rate from zero to 2MHz. SSTRB goes low at the start of the conversion, then goes high when the conversion is complete. SSTRB is low for a maximum of 10µs, during which time SCLK should remain low for best noise performance. An internal register stores data while the conversion is in progress. SCLK clocks the data out at this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 9). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1204 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go high impedance when $\overline{CS}$ goes high.

Figure 10 shows the SSTRB timing in internal clock mode. Data can be shifted in and out of the MAX1204 at clock rates up to 2.0MHz if the acquisition time, t_{ACQ}, is kept above 1.5µs.

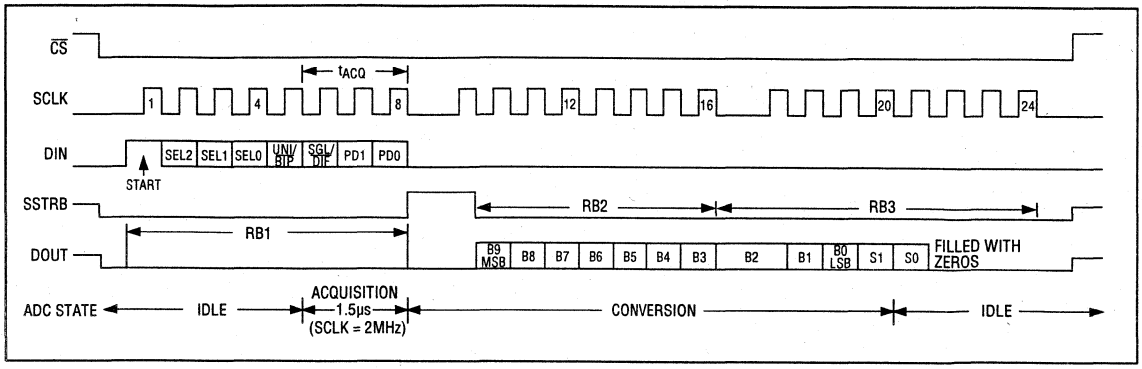


Figure 6. 24-Bit External-Clock-Mode Conversion Timing (Microwire/SPI Compatible)

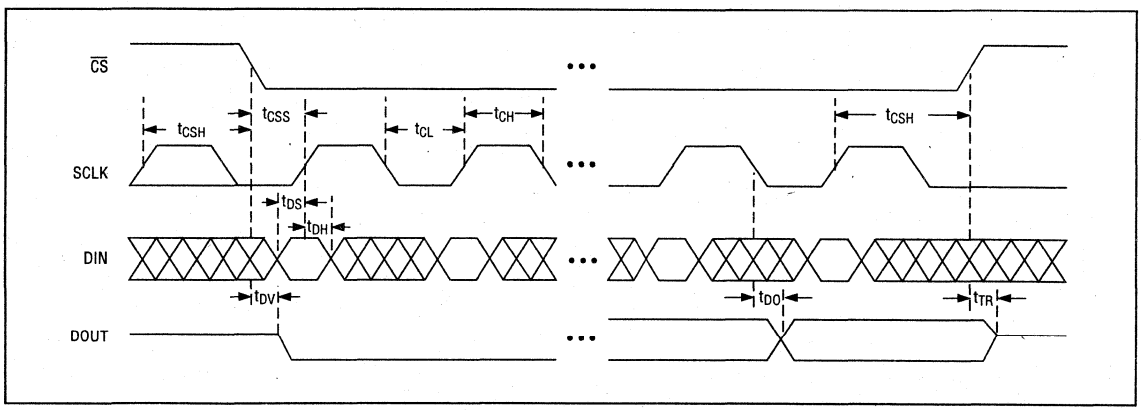


Figure 7. Detailed Serial-Interface Timing

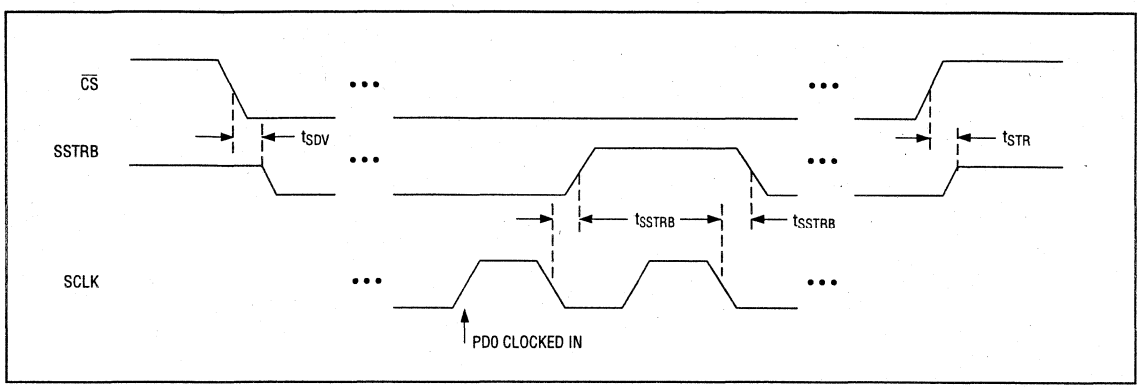


Figure 8. External Clock-Mode SSTRB Detailed Timing

7

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

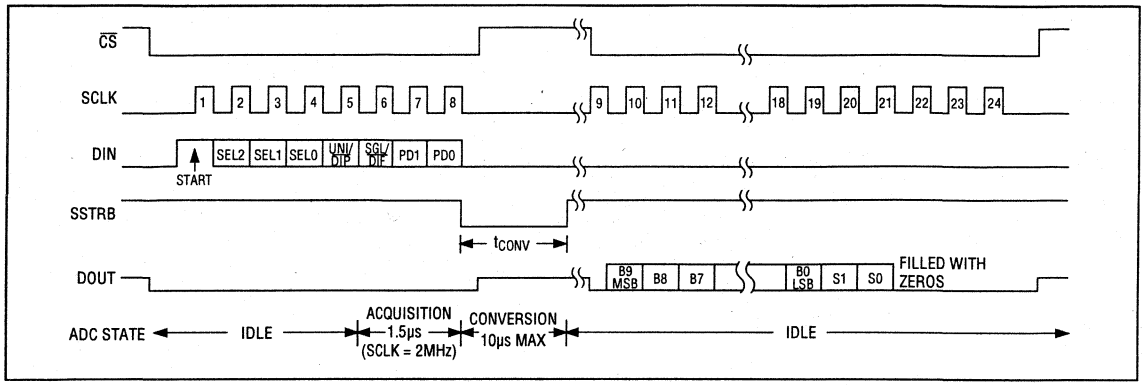


Figure 9. Internal Clock Mode Timing

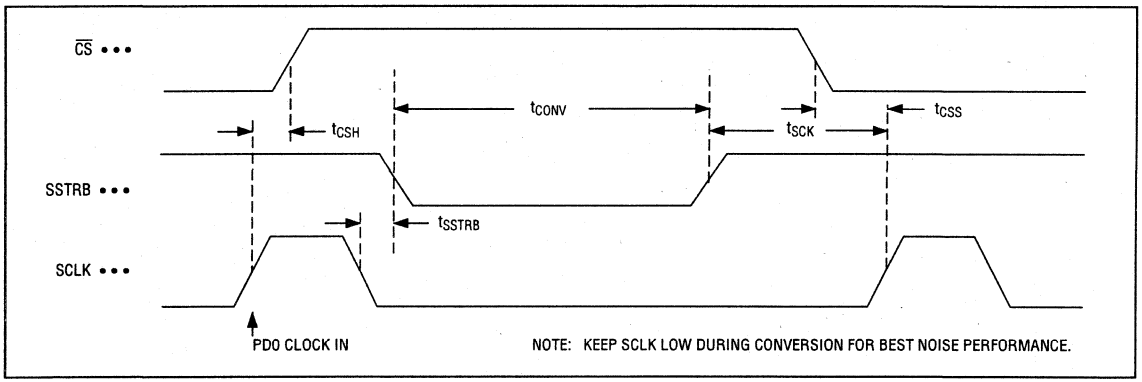


Figure 10. Internal Clock Mode SSTRB Detailed Timing

Data Framing

$\overline{CS}$'s falling edge does **not** start a conversion on the MAX1204. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low anytime the converter is idle; (e.g., after V_{DD} is applied).

or

The first high bit clocked into DIN after bit 3 (B3) of a conversion in progress appears at DOUT.

If a falling edge on $\overline{CS}$ forces a start bit before B3 becomes available, the current conversion is terminated and a new one started. Thus, the fastest the MAX1204 can run is 15 clocks/conversion. Figure 11a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX1204. Figure 11b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

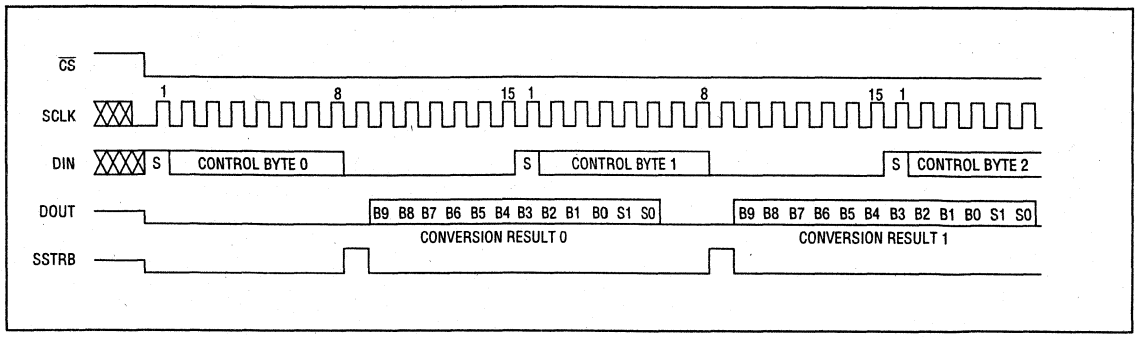


Figure 11a. External Clock Mode, 15 Clocks/Conversion Timing

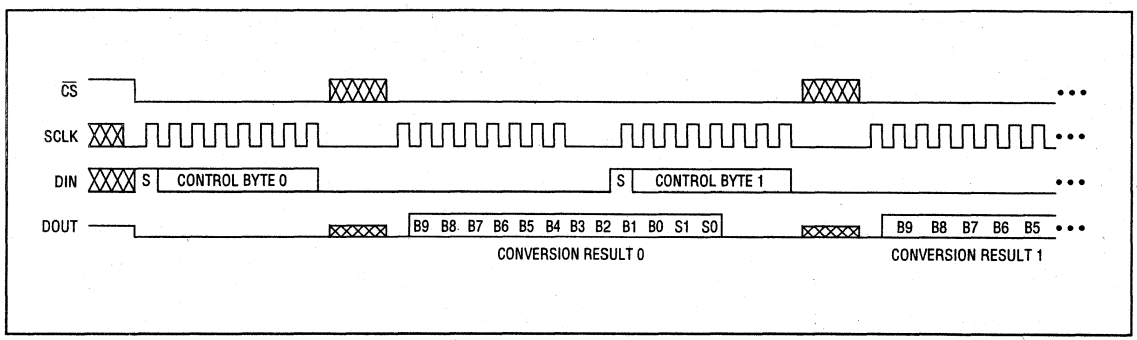


Figure 11b. External Clock Mode, 16 Clocks/Conversion Timing

Applications Information

Power-On Reset

When power is first applied and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1204 in internal clock mode, ready to convert with SSTRB = high. After the power supplies are stabilized, the internal reset time is 100µs. No conversions should be performed during this phase. SSTRB is high on power-up, and if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros.

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ also selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. Compensated or not, the minimum clock rate is 100kHz due to droop on the sample-and-hold.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at REF. A value of 4.7µF or greater ensures stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the section *Choosing Power-Down Mode,* and Table 5).

Internal compensation requires no external capacitor at REF, and is selected by pulling $\overline{SHDN}$ high. Internal compensation allows for the shortest power-up times, but is only available using an external clock up to 400kHz.

Power-Down

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 2 and 6). Pull $\overline{SHDN}$ low at any time to

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing I_{DD} and I_{SS} typically to 2µA.

Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

The I_{DD} shutdown current can increase if any digital input (DIN, SCLK, $\overline{CS}$) is held high in either power-down mode. The actual shutdown current depends on the state of the digital inputs, the voltage applied to the digital inputs (V_{IH}), the supply voltage (V_{DD}), and the operating temperature. Figure 12c shows the maximum I_{DD} increase for each digital input held high in power-down mode for different operating conditions. This current is cumulative, so if all three digital inputs are held high, the additional shutdown current is three times the value shown in Figure 12c.

In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Table 5 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate.

In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor (200ms with a 33µF capacitor) when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, the capacitor has to supply the current into the reference (typically 1.5µA) and the transient currents at power-up.

Figures 12a and 12b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 6, PD1 and PD0 also specify clock mode. When software power-down is asserted, the ADC continues to operate in the last specified clock mode until the conversion is complete. The ADC then powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results can be clocked out even though the MAX1204 has already entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1204. Following the start bit, the control byte also determines clock and power-down modes. For example, if the control byte contains PD1 = 1, the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

Table 5. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	REFERENCE CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal		Fast	5	26
Enabled	Internal		Full	300	26
Enabled	External	4.7	Fast/Full	See Figure 14c	133
Disabled			Fast	2	133
Disabled			Full	2	133

Table 6. Software Shutdown and Clock Mode

PD1	PD0	DEVICE MODE
1	1	External clock mode
1	0	Internal clock mode
0	1	Fast power-down mode
0	0	Full power-down mode

Table 7. Hard-Wired Shutdown and Compensation Mode

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION
V_{DD}	Enabled	Internal compensation
Floating	Enabled	External compensation
GND	Full Power-Down	N/A

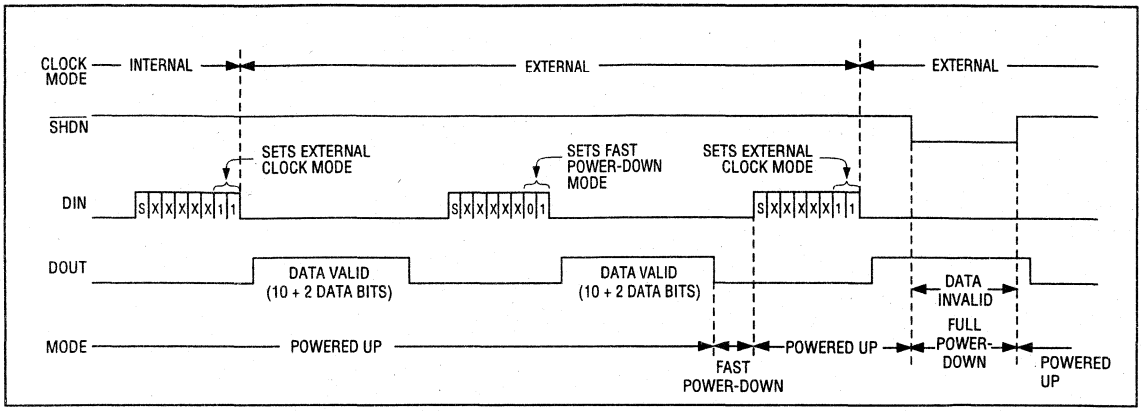


Figure 12a. Timing Diagram for Power-Down Modes (External Clock)

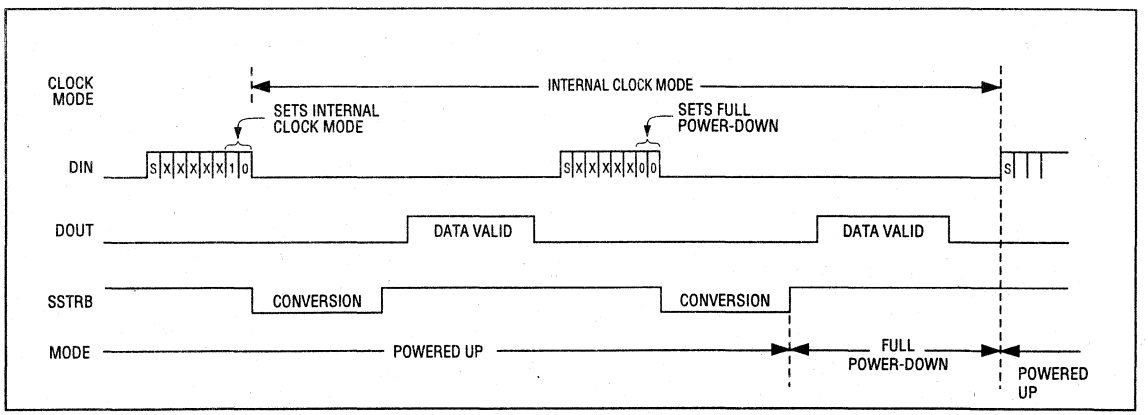


Figure 12b. Timing Diagram for Power-Down Modes (Internal Clock)

Hardware Power-Down

The $\overline{SHDN}$ pin places the converter into full power-down mode. Unlike the software power-down modes, conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. There is no power-up delay if an external reference, which is not shut down, is used. $\overline{SHDN}$ also selects internal or external reference compensation (Table 7).

Power-Down Sequencing

The MAX1204's automatic power-down modes can save considerable power when operating at less than maximum sample rates. The following sections discuss the various power-down sequences.

Lowest Power at up to 500 Conversions per Channel per Second

Figure 14a depicts MAX1204's power consumption for one or eight channel conversions using full power-down mode and internal reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor, with a 0.2ms time constant. To achieve full 10-bit accuracy, 10 time constants (or 2ms in this example) are required for the reference buffer to settle. When exiting FULLPD, waiting this 2ms in FASTPD mode (instead of just exiting FULLPD mode and returning to normal operating mode) reduces power consumption by a factor of 10 or more (Figure 13).

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

Lowest Power at Higher Throughputs

Figure 14b shows power consumption with external-reference compensation in fast power-down, with one and eight channels converted. The external 4.7µF compensation requires a 50µs wait after power-up. This circuit combines fast multichannel conversion with the lowest power consumption possible. Full power-down mode can increase power savings in applications where the MAX1204 is inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

External and Internal References

The MAX1204 can be used with an internal or external reference. An external reference can be connected directly at the REF terminal or at the REFADJ pin.

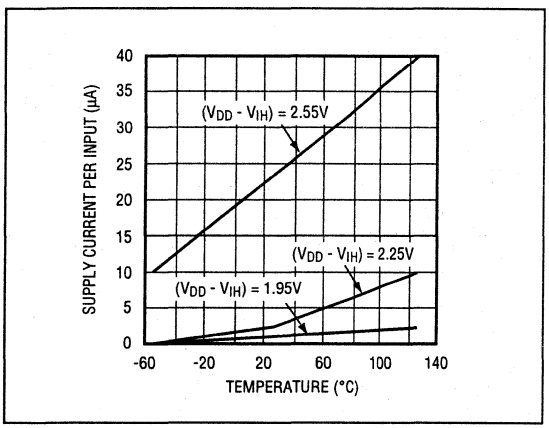


Figure 12c. Additional I_{DD} Shutdown Supply Current vs. V_{IH} for Each Digital Input at a Logic 1

An internal buffer is designed to provide 4.096V at REF for the MAX1204. Its internally trimmed 2.44V reference is buffered with a 1.68 nominal gain.

Internal Reference

The MAX1204's full-scale range with internal reference is 4.096V with unipolar inputs and ±2.048V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit of Figure 17.

External Reference

An external reference can be placed at either the input (REFADJ) or the output (REF) of the MAX1204's internal buffer amplifier. The REFADJ input impedance is typically 20kΩ. At REF, the input impedance is a minimum of 12kΩ for DC currents. During conversion, an external reference at REF must deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Using the buffered REFADJ input makes buffering of the external reference unnecessary. To use the direct REF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to GND to minimize the input bias current in power-down.

Transfer Function and Gain Adjust

Figure 15 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 16 shows the bipolar I/O transfer function. Code transitions occur halfway between successive integer LSB values. Output coding is binary with 1 LSB = 4mV (4.096V/1024) for unipolar operation and 1 LSB = 4mV [(4.096V/2 - -4.096V/2)/1024] for bipolar operation.

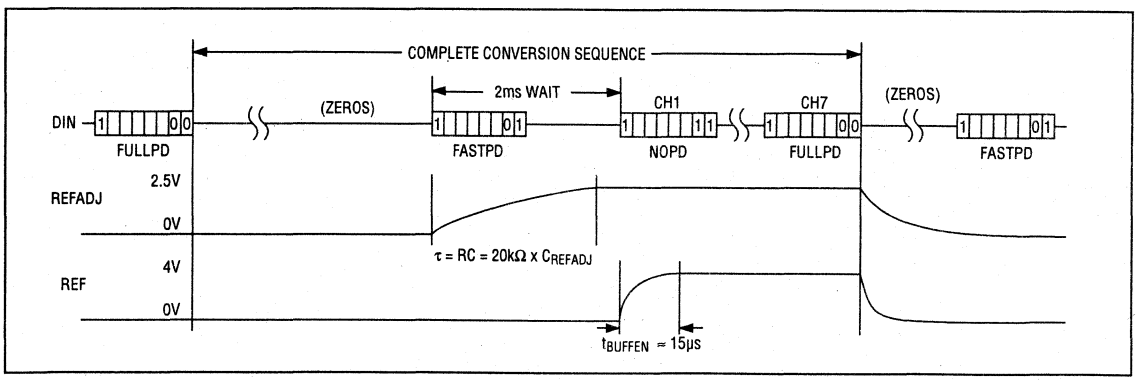


Figure 13. MAX1204 FULLPD/FASTPD Power-Up Sequence

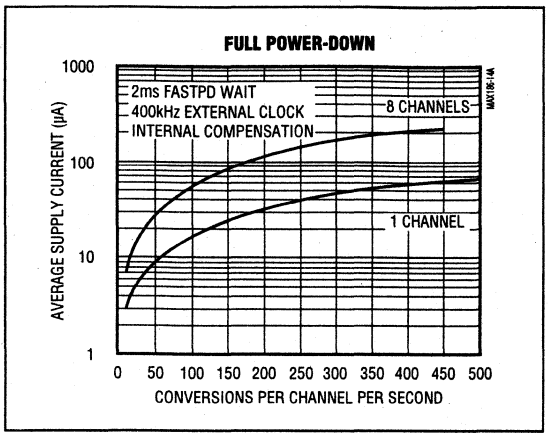


Figure 14a. MAX1204 Supply Current vs. Sample Rate/Second, FULLPD, 400kHz Clock

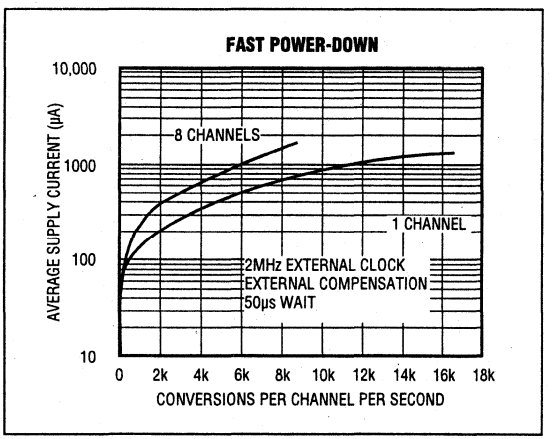


Figure 14b. MAX1204 Supply Current vs. Sample Rate/Second, FASTPD, 2MHz Clock

Figure 17, the Reference-Adjust Circuit, shows how to adjust ADC gain in applications that use the internal reference. The circuit provides ±1.5% (±16LSBs) of gain-adjustment range.

Layout, Grounding, Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital

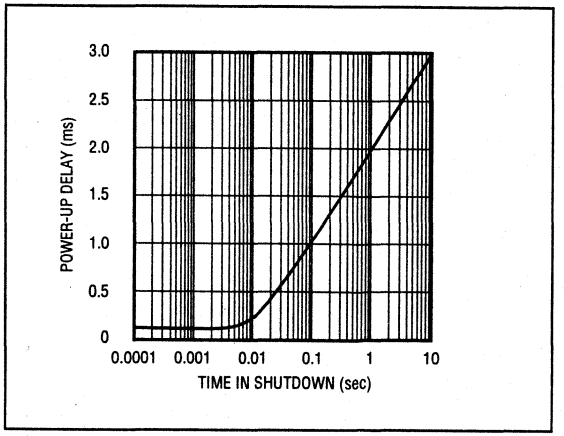


Figure 14c. Typical Power-Up Delay vs. Time in Shutdown

(especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system-ground connections. Establish a single-point analog ground (star ground point) at GND. Connect all other analog grounds to this ground. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass these supplies to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors close to the MAX1204. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter, as shown in Figure 18.

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

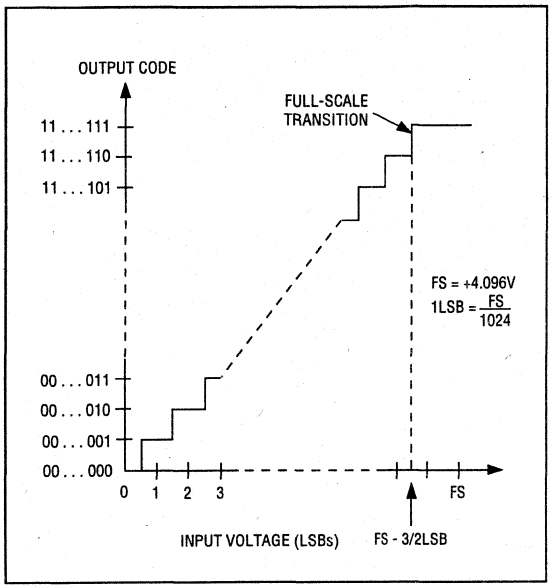


Figure 15. Unipolar Transfer Function, 4.096V = Full Scale

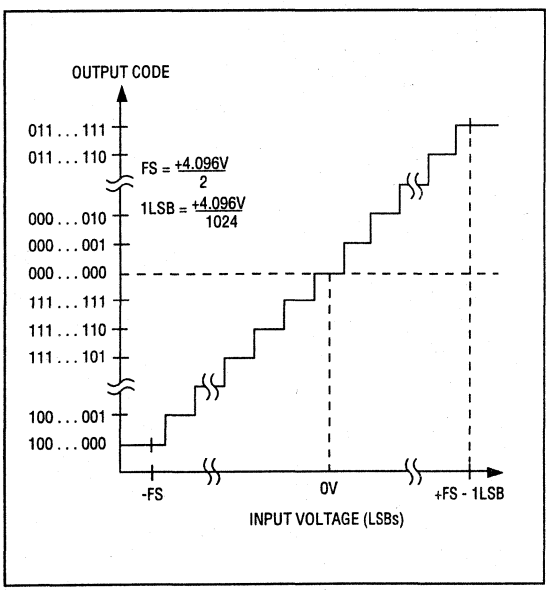


Figure 16. Bipolar Transfer Function, ±4.096V/2 = Full Scale

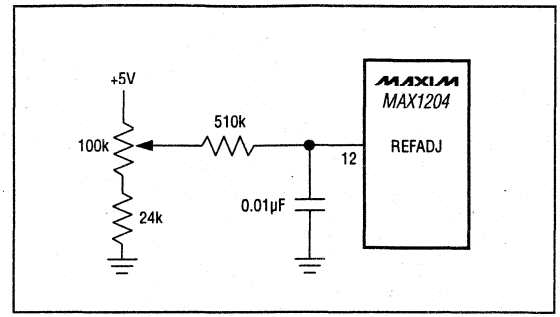


Figure 17. Reference-Adjust Circuit

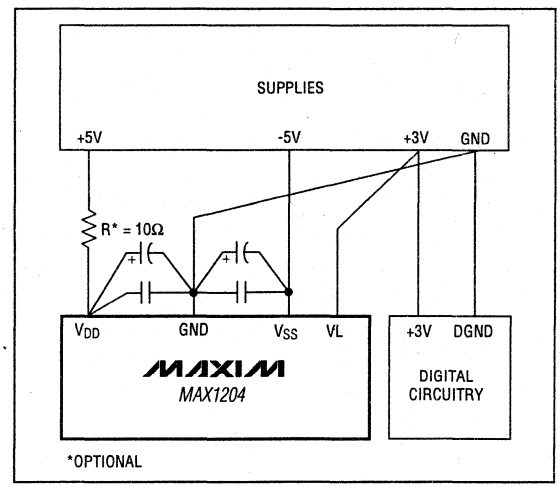


Figure 18. Power-Supply Grounding Connection

TMS320CL3x to MAX1204 Interface

Figure 19 shows an application circuit to interface the MAX1204 to the TMS320 in external clock mode. Figure 20 is the timing diagram for this interface circuit.

Use the following steps to initiate a conversion in the MAX1204 and to read the results.

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. The TMS320's CLKX and CLKR are tied together with the MAX1204's SCLK input.
2) The MAX1204's $\overline{CS}$ is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX1204's DIN.
3) Write an 8-bit word (1XXXXX11) to the MAX1204 to initiate a conversion and place the device into external clock mode. Refer to Table 2 to select the proper XXXXX bit values for your specific application.
4) The MAX1204's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1204.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10-bit conversion result followed by two sub-bits and four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1204 until the next conversion is initiated.

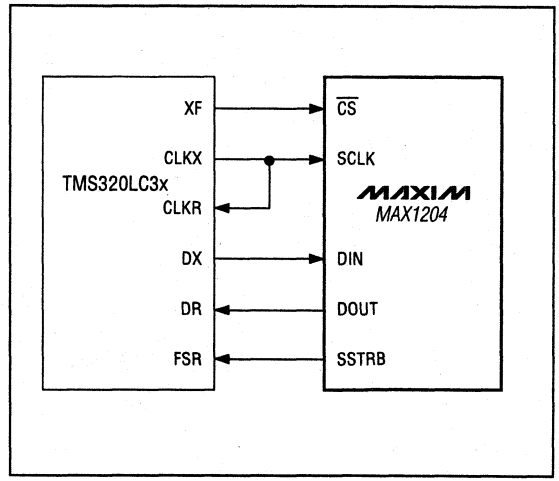


Figure 19. MAX1204 to TMS320 Serial Interface

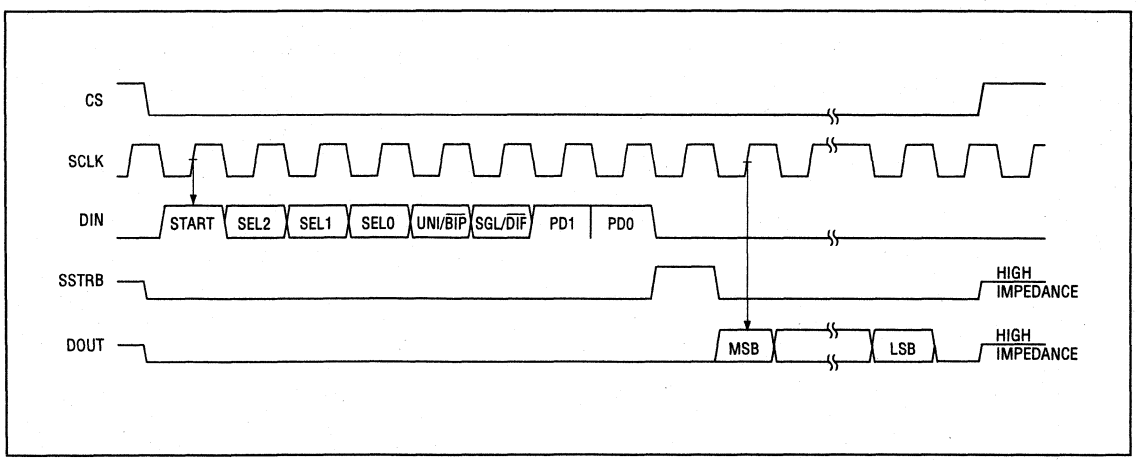


Figure 20. TMS320 Serial-Interface Timing Diagram

5V, 8-Channel, Serial, 10-Bit ADC with 3V Digital Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1204AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX1204BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX1204AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX1204BEAP	-40°C to +85°C	20 SSOP	±1
MAX1204BMJP	-55°C to +125°C	20 CERDIP*	±1

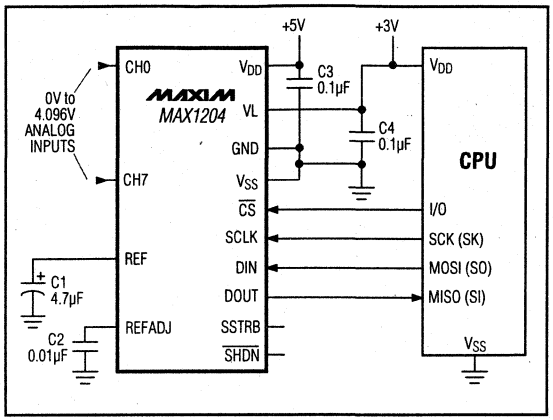
Contact factory for availability.

_____Chip Information

TRANSISTOR COUNT: 2503

SUBSTRATE CONNECTED TO V_{SS}

_____Typical Operating Circuit



19-1155; Rev 1; 9/97

EVALUATION KIT AVAILABLE

MAXIM

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

General Description

The MAX1240/MAX1241 are low-power, 10-bit analog-to-digital converters (ADCs) available in 8-pin packages. The MAX1240 operates with a single +2.7V to +3.6V supply, and the MAX1241 operates with a single +2.7V to +5.25V supply. Both devices feature a 7.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 37mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. A 2µA shutdown mode reduces power at slower throughput rates.

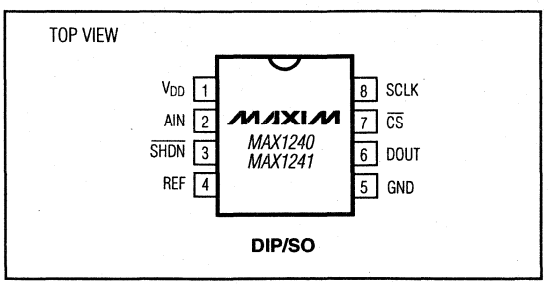
The MAX1240 has an internal 2.5V reference, while the MAX1241 requires an external reference. The MAX1241 accepts signals from 0V to V_{REF}, and the reference input range includes the positive supply rail. An external clock accesses data from the 3-wire interface, which connects directly to standard microcontroller I/O ports. The interface is compatible with SPI™, QSPI™, and Microwire™.

Excellent AC characteristics and very low power combined with ease of use and small package size make these converters ideal for remote-sensor and data-acquisition applications, or for other circuits with demanding power consumption and space requirements. The MAX1240/MAX1241 are available in 8-pin DIP and SO packages.

Applications

Battery-Powered Systems
Portable Data Logging
Isolated Data Acquisition
Process Control
Instrumentation

Pin Configuration



Features

- **Single-Supply Operation:**
  +2.7V to +3.6V (MAX1240)
  +2.7V to +5.25V (MAX1241)
- **12-Bit Resolution**
- **Internal 2.5V Reference (MAX1240)**
- **Small Footprint: 8-Pin DIP/SO Packages**
- **Low Power: 3.7µW (73ksps, MAX1240)**
  3mW (73ksps, MAX1241)
  66µW (1ksps, MAX1241)
  5µW (power-down mode)
- **Internal Track/Hold**
- **SPI/QSPI/Microwire 3-Wire Serial Interface**
- **Internal Clock**

Ordering Information

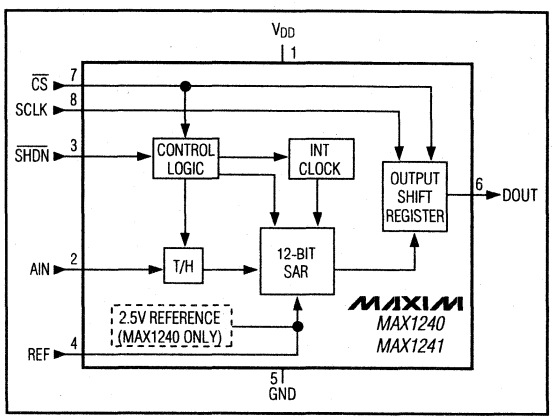
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1240ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1240BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1240CCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1240ACSA	0°C to +70°C	8 SO	±1/2
MAX1240BCSA	0°C to +70°C	8 SO	±1
MAX1240CCSA	0°C to +70°C	8 SO	±1
MAX1240BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*

7

Functional Diagram



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+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND.....-0.3V to +6V
DOUT to GND .....-0.3V to (V_{DD} + 0.3V)
DOUT Current .....±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX1240_C_A/MAX1241_C_A .....0°C to +70°C
MAX1240_E_ A/MAX1241_E_ A.....-40°C to +85°C
MAX1240_MJA/MAX1241_MJA .....-55°C to +125°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1240); V_{DD} = +2.7V to +5.25V (MAX1241); 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); MAX1240—4.7µF capacitor at REF pin, MAX1241—external reference; V_{REF} = 2.500V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)							
Resolution				12			Bits
Relative Accuracy (Note 2)	INL	MAX124_A				±0.5	LSB
		MAX124_B/C				±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature				±1	LSB
Offset Error		MAX124_A			±0.5	±3.0	LSB
		MAX124_B/C			±0.5	±4.0	
Gain Error (Note 3)					±0.5	±4.0	LSB
Gain Temperature Coefficient					±0.25		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 73ksps, f_{SCLK} = 2.1MHz)							
Signal-to-Noise Plus Distortion Ratio	SINAD	MAX124_A/B		70			dB
		MAX124_C			71.5		
Total Harmonic Distortion	THD	Up to the 5th harmonic	MAX124_A/B			-80	dB
			MAX124_C		-88		
Spurious-Free Dynamic Range	SFDR	MAX124_A/B		80			dB
		MAX124_C			-88		
Small-Signal Bandwidth		-3dB rolloff			2.25		MHz
Full-Power Bandwidth					1.0		MHz
CONVERSION RATE							
Conversion Time	t_{CONV}			5.5		7.5	µs
Track/Hold Acquisition Time	t_{ACQ}					1.5	µs
Throughput Rate		f_{SCLK} = 2.1MHz				73	ksps
Aperture Delay	t_{APR}	Figure 8			30		ns
Aperture Jitter					<50		ps
ANALOG INPUT							
Input Voltage Range				0		V_{REF}	V
Input Capacitance					16		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1240); V_{DD} = +2.7V to +5.25V (MAX1241); 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); MAX1240—4.7µF capacitor at REF pin, MAX1241—external reference; V_{REF} = 2.500V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERNAL REFERENCE (MAX1240 only)						
REF Output Voltage		T_A = +25°C	2.480	2.500	2.520	V
REF Short-Circuit Current					30	mA
REF Temperature Coefficient		MAX1240AC/BC		±30	±50	ppm/°C
		MAX1240AE/BE		±30	±60	
		MAX1240AM/BM		±30	±80	
		MAX1240C		±30		
Load Regulation (Note 4)		0mA to 0.2mA output load		0.35		
Capacitive Bypass at REF			4.7			µF
EXTERNAL REFERENCE (V_{REF} = 2.500V)						
Input Voltage Range			1.00		V_{DD} + 50mV	V
Input Current				100	150	µA
Input Resistance			18	25		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V		±0.01	10	µA
Capacitive Bypass at REF			0.1			µF
DIGITAL INPUTS: SCLK, $\overline{CS}$, $\overline{SHDN}$						
SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \leq 3.6V$	2.0			V
		V_{DD} > 3.6V (MAX1241)	3.0			
SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 5)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = float		V_{DD}/2		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = float			±100	nA
DIGITAL OUTPUT: DOUT						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 5)			15	pF

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1240); V_{DD} = +2.7V to +5.25V (MAX1241); 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); MAX1240—4.7µF capacitor at REF pin, MAX1241—external reference; V_{REF} = 2.500V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
POWER REQUIREMENTS								
Supply Voltage	V_{DD}	MAX1240			2.7		3.6	V
		MAX1241			2.7		5.25	
Supply Current	I_{DD}	Operating mode	MAX1240A/B	V_{DD} = 3.6V		1.4	2.0	mA
			MAX1240C			1.4	3.5	
			MAX1241A/B	V_{DD} = 3.6V		0.9	1.5	
				V_{DD} = 5.25V		1.6	2.5	
			MAX1241C	V_{DD} = 3.6V		0.9	2.8	
				V_{DD} = 5.25V		1.6	3.8	
		Power-down, digital inputs at 0V or V_{DD}		V_{DD} = 3.6V		1.9	10	µA
				V_{DD} = 5.25V		3.5	15	
Supply Rejection	PSR	(Note 5)				±0.3		mV

TIMING CHARACTERISTICS (Figure 8)

(V_{DD} = +2.7V to +3.6V (MAX1240); V_{DD} = +2.7V to +5.25V (MAX1241); T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	$\overline{CS}$ = V_{DD} (Note 6)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX124_ _C/E	20		200	ns
			MAX124_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
SCLK Clock Frequency	f_{SCLK}			0		2.1	MHz
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CS0}			50			ns
DOUT Rise to SCLK Rise (Note 5)	t_{STR}			0			ns
$\overline{CS}$ Pulse Width	t_{CS}			240			ns

Note 1: Tested at V_{DD} = +2.7V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.
Note 3: MAX1240—internal reference, offset nulled; MAX1241—external reference (V_{REF} = +2.500V), offset nulled.
Note 4: External load should not change during conversion for specified accuracy.
Note 5: Guaranteed by design. Not subject to production testing.
Note 6: Measured as [V_{FS}(2.7V) - V_{FS}($V_{DD(MAX)}$)].
Note 7: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

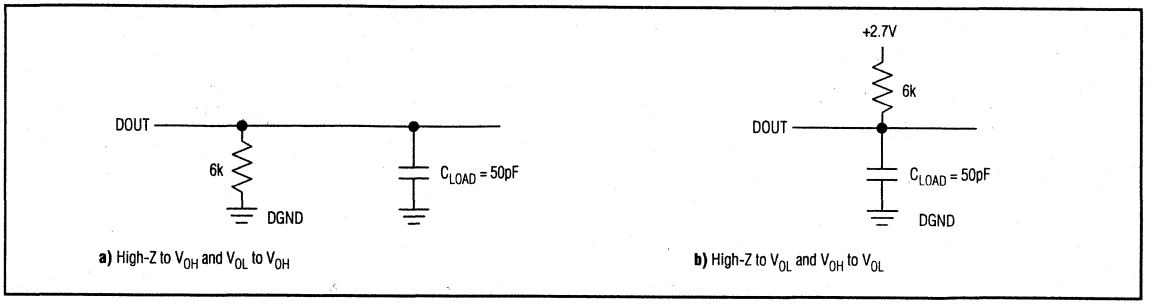


Figure 1. Load Circuits for DOUT Enable Time

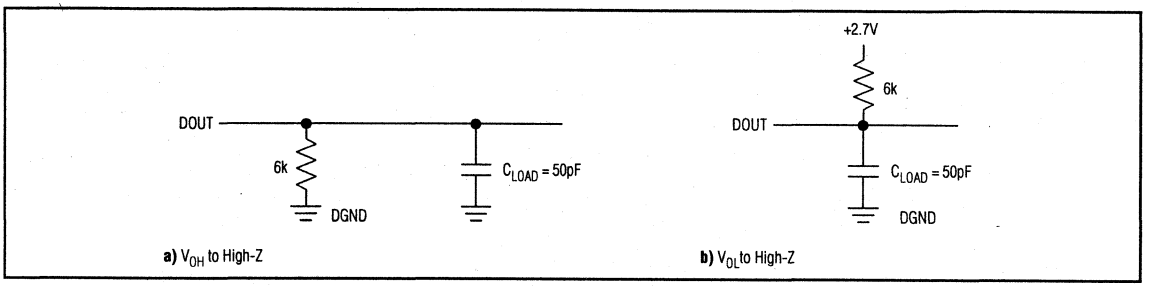
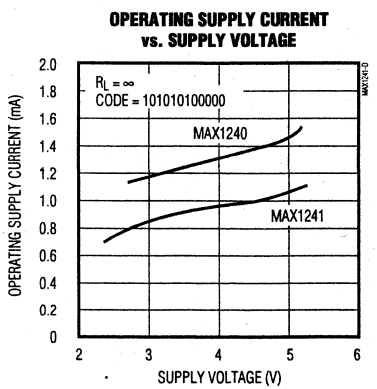
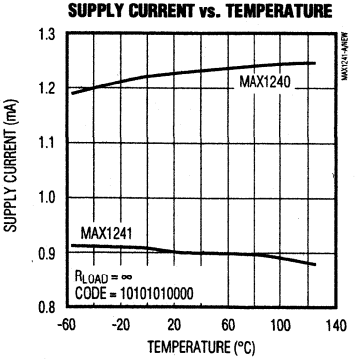


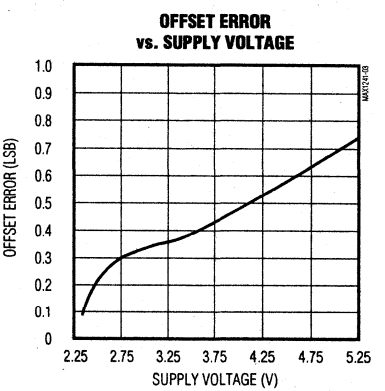
Figure 2. Load Circuits for DOUT Disable Time

Typical Operating Characteristics

(V_{DD} = 3.0V, V_{REF} = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)







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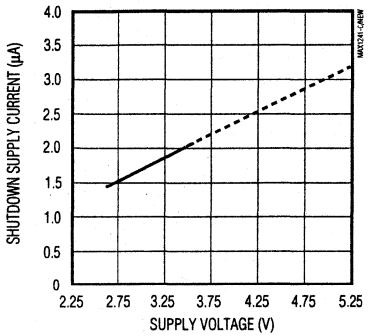
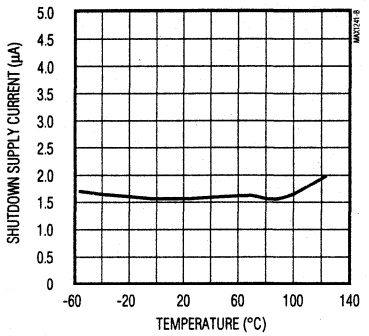
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, V_{REF} = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

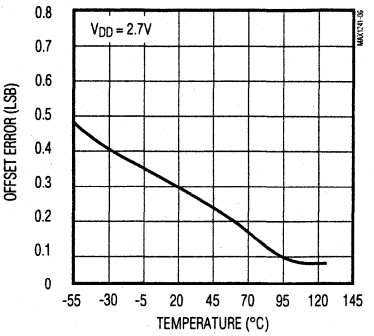
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



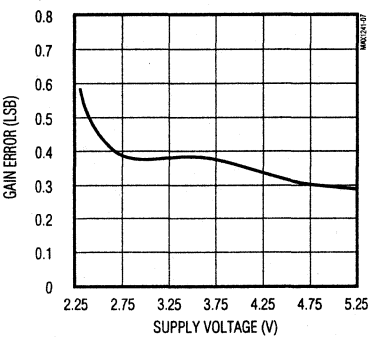
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



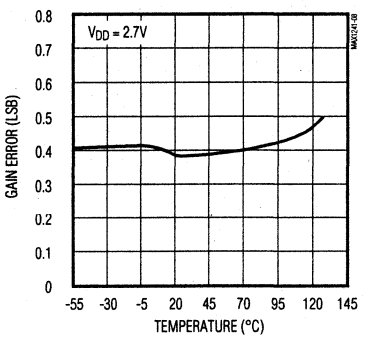
OFFSET ERROR vs. TEMPERATURE



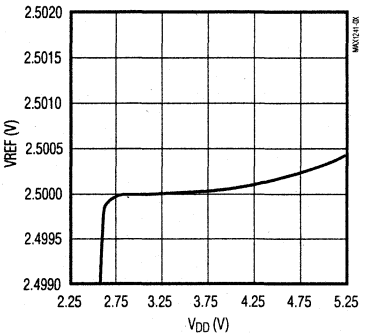
GAIN ERROR vs. SUPPLY VOLTAGE



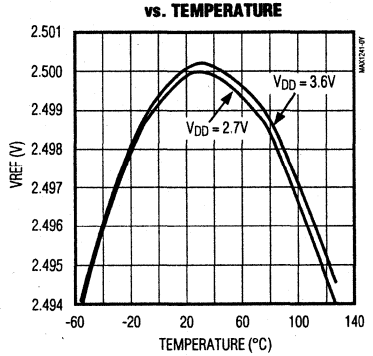
GAIN ERROR vs. TEMPERATURE



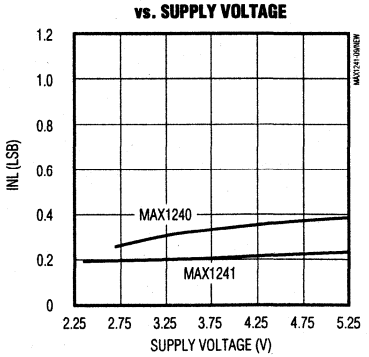
MAX1240 INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



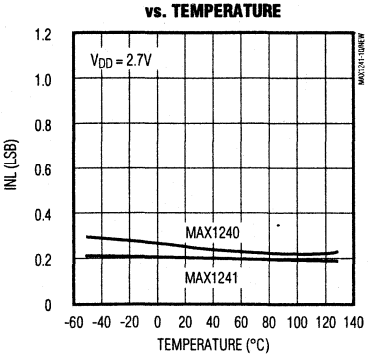
MAX1240 INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



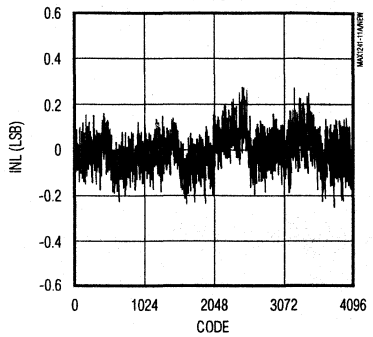
INTEGRAL NONLINEARITY vs. TEMPERATURE



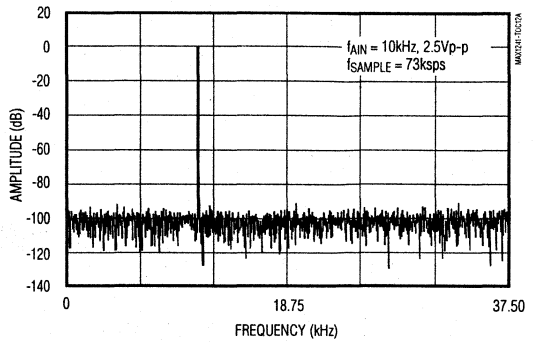
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, REF = 2.5V, f_{SCLK} = 2.1MHz, C_L = 20pF, T_A = +25°C, unless otherwise noted.)

INTEGRAL NONLINEARITY vs. CODE



FFT PLOT



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage: 2.7V to 3.6V, (MAX1240); 2.7 to 5.25V (MAX1241)
2	AIN	Sampling Analog Input, 0V to V_{REF} range
3	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1240/MAX1241 down to 15µA (max) supply current. Both the MAX1240 and MAX1241 are fully operational with either $\overline{SHDN}$ high or floating. For the MAX1240, pulling $\overline{SHDN}$ high enables the internal reference, and letting $\overline{SHDN}$ float disables the internal reference and allows for the use of an external reference.
4	REF	Reference Voltage for Analog-to-Digital Conversion. Internal 2.5V reference output for MAX1240; bypass with 4.7µF capacitor. External reference voltage input for MAX1241, or for MAX1240 with the internal reference disabled. Bypass REF with a minimum of 0.1µF when using an external reference.
5	GND	Analog and Digital Ground
6	DOUT	Serial Data Output. Data changes state at SCLK's falling edge. DOUT is high impedance when $\overline{CS}$ is high.
7	$\overline{CS}$	Active-Low Chip Select initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	SCLK	Serial Clock Input. SCLK clocks data out at rates up to 2.1MHz.

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

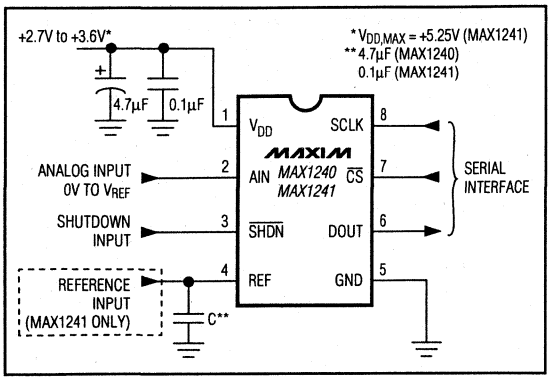


Figure 3. Operational Diagram

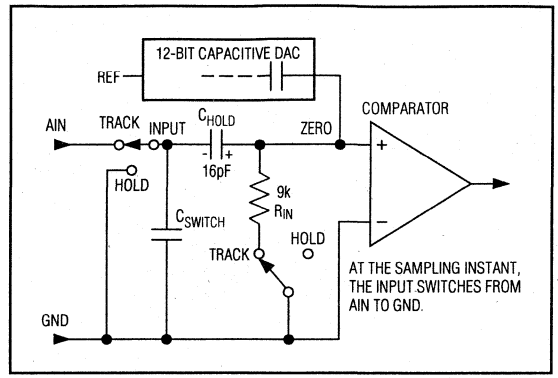


Figure 4. Equivalent Input Circuit

Detailed Description

Converter Operation

The MAX1240/MAX1241 use an input track/hold (T/H) and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. No external-hold capacitor is needed for the T/H. Figure 3 shows the MAX1240/MAX1241 in its simplest configuration. The MAX1240/MAX1241 convert input signals in the 0V to V_{REF} range in 9µs, including T/H acquisition time. The MAX1240's internal reference is trimmed to 2.5V, while the MAX1241 requires an external reference. Both devices accept voltages from 1.0V to V_{DD}. The serial interface requires only three digital lines (SCLK, $\overline{CS}$, and DOUT) and provides an easy interface to microprocessors (µPs).

The MAX1240/MAX1241 have two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current below 10µA ($V_{DD} \leq 3.6V$), while pulling $\overline{SHDN}$ high or leaving it open puts the device into operational mode. Pulling $\overline{CS}$ low initiates a conversion. The conversion result is available at DOUT in unipolar serial format. The serial data stream consists of a high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first).

Analog Input

Figure 4 illustrates the sampling architecture of the analog-to-digital converter's (ADC's) comparator. The full-scale input voltage is set by the voltage at REF.

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input (AIN) charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing node ZERO at the comparator's input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. Acquisition time is calculated by:

$$t_{ACQ} = 9(R_S + R_{IN}) \times 16pF$$

where $R_{IN} = 9k\Omega$, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.5µs. Source impedances below 1kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's input signal bandwidth.

Input Bandwidth

The ADCs' input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA.

Internal Reference (MAX1240)

The MAX1240 has an on-chip voltage reference trimmed to 2.5V. The internal reference output is connected to REF and also drives the internal capacitive DAC. The output can be used as a reference voltage source for other components and can source up to 400µA. Bypass REF with a 4.7µF capacitor. Larger capacitors increase wake-up time when exiting shutdown (see the section *Using $\overline{SHDN}$ to Reduce Supply Current*). The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX1240/MAX1241 operate with an external reference at the REF pin. To use the MAX1240 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the +1.0V to V_{DD} voltage range to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents. During conversion, the external reference must be able to deliver up to 250µA of DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

Serial Interface

Initialization after Power-Up and Starting a Conversion

When power is first applied, and if $\overline{SHDN}$ is not pulled low, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With an external reference, the internal reset time is 10µs after the power supplies have stabilized. No conversions should be performed during these times.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiat-

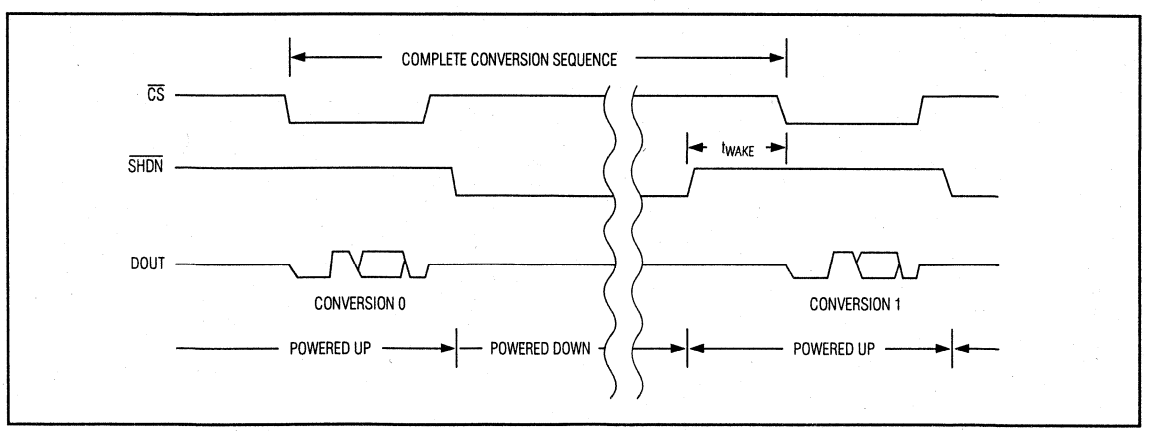


Figure 5. Shutdown Sequence

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

ed. After an internally timed conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1240/MAX1241 between conversions. Figure 6 shows a plot of average supply current versus conversion rate. Because the MAX1241 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly (in 4µs) and therefore provides lower average supply currents. The wake-up time (t_{WAKE}) is the time from when $\overline{SHDN}$ is deasserted to the time when a conversion may be initiated (Figure 5). For the MAX1240, this time depends on the time in shutdown (Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown.

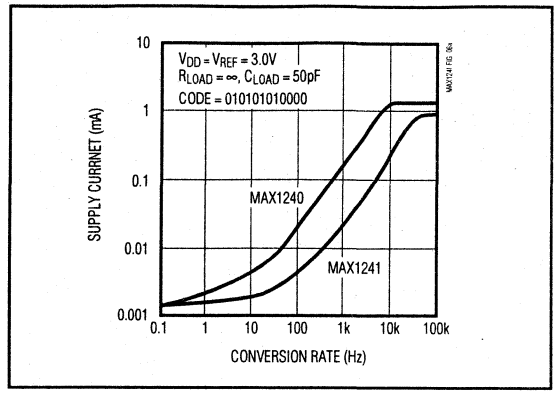


Figure 6. Average Supply Current vs. Conversion Rate

External Clock

The actual conversion does not require the external clock. This allows the conversion result to be read back at the µP's convenience at any clock rate from up to 2.1MHz. The clock duty cycle is unrestricted if each clock phase is at least 200ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline serial-interface operation.

A $\overline{CS}$ falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept low during the conversion. An internal register stores the data when the conversion is in progress.

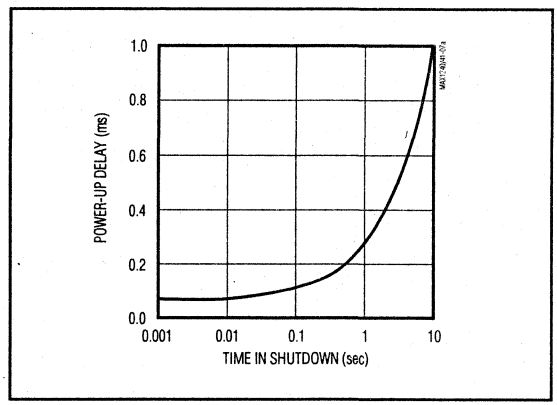


Figure 7. Typical Reference Power-Up Delay vs. Time in Shutdown

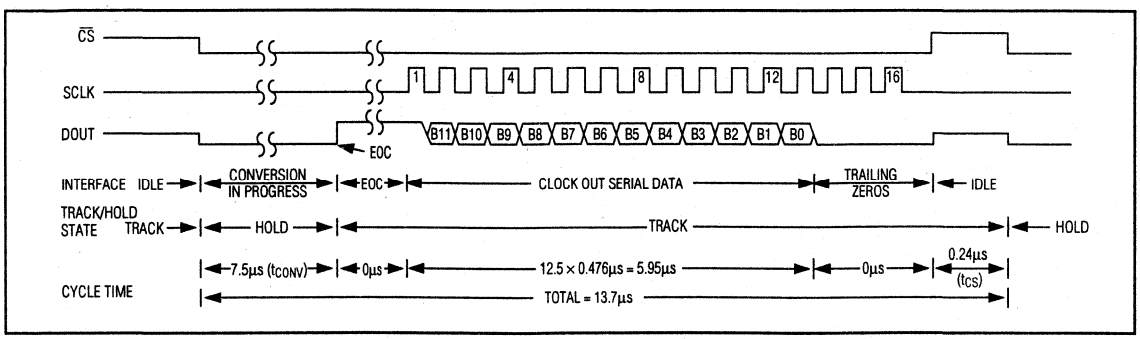


Figure 8. Interface Timing Sequence

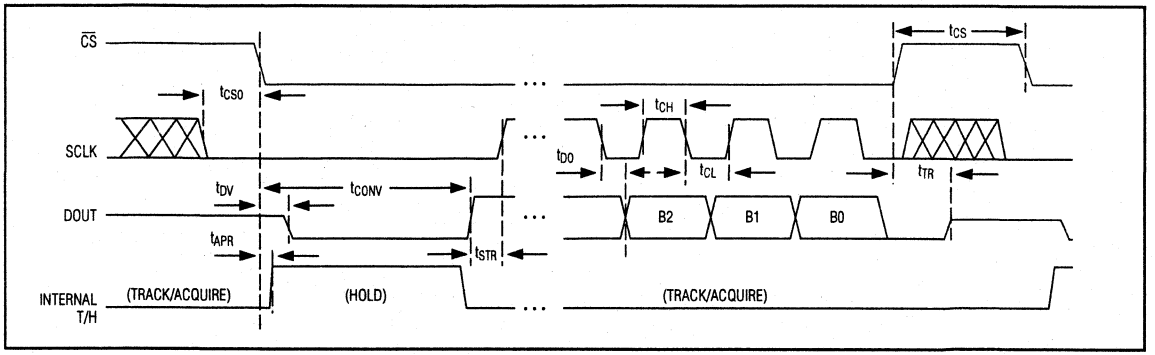


Figure 9. Detailed Serial-Interface Timing

End of conversion (EOC) is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing zeros at DOUT and have no effect on converter operation.

Minimum cycle time is accomplished by using DOUT's rising edge as the EOC signal. Clock out the data with 12.5 clock cycles at full speed. Pull $\overline{CS}$ high after reading the conversion's LSB. After the specified minimum time (t_{CS}), $\overline{CS}$ can be pulled low again to initiate the next conversion.

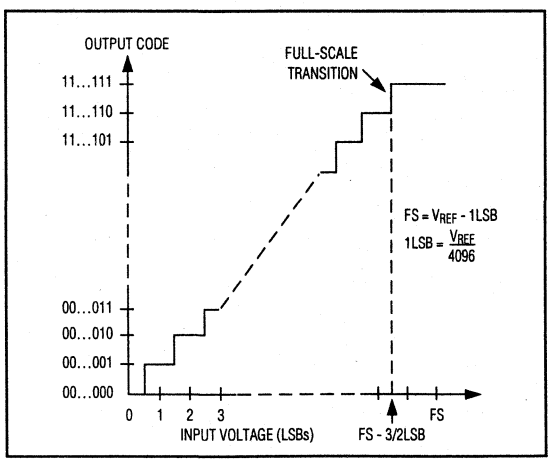


Figure 10. Unipolar Transfer Function, Full Scale (FS) = V_{REF} - 1LSB, Zero Scale (ZS) = GND

Output Coding and Transfer Function

The data output from the MAX1240/MAX1241 is binary, and Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values. If V_{REF} = +2.500V, then 1 LSB = 610µV or 2.500V/4096.

Applications Information

Connection to Standard Interfaces

The MAX1240/MAX1241 serial interface is fully compatible with SPI/QSPI and Microwire standard serial interfaces (Figure 11).

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.1MHz.

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the for the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 13 clock cycles. The first falling clock edge produces the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 13th falling clock edge. If $\overline{CS}$ remains low, trailing zeros are clocked out after the LSB.

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

5) With $\overline{CS}$ = high, wait the minimum specified time, tCS, before initiating a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversion's end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

$\overline{CS}$ must be held low until all data bits are clocked out. Data can be output in two bytes or continuously, as shown in Figure 8. The bytes contain the result of the conversion padded with one leading 1, and trailing 0s.

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion in progress. Wait until DOUT goes high or until the maximum specified 7.5µs conversion time elapses. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1, and seven bits of conversion result. The second byte contains the remaining five bits and three trailing zeros. See Figure 11 for connections and Figure 12 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1240/MAX1241 requires 13 clock cycles from the µP to clock out the 12 bits of data with no trailing zeros (Figure 13). The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 14 shows the recommended system ground connections. Establish a single-point analog ground ("star" ground point) at GND, separate from the logic ground. Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass this supply to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (Figure 14).

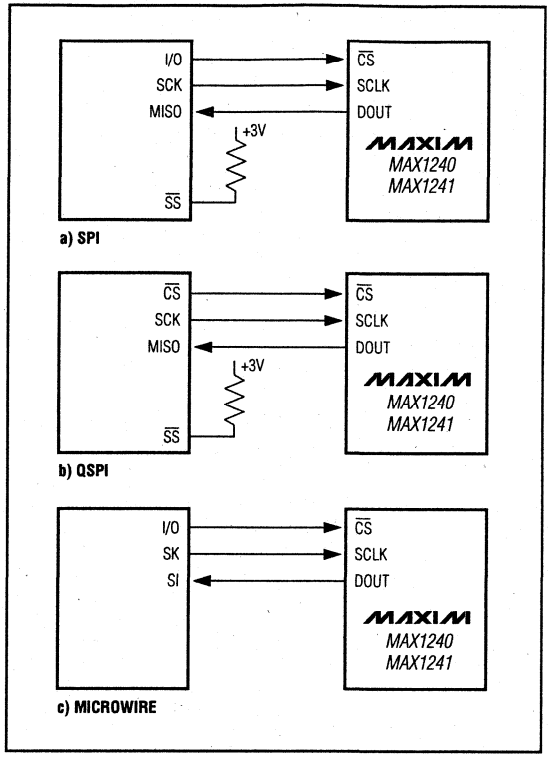


Figure 11. Common Serial-Interface Connections to the MAX1241

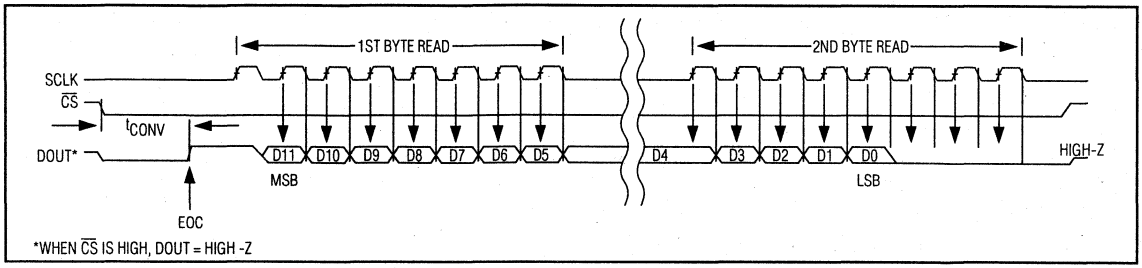


Figure 12. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)

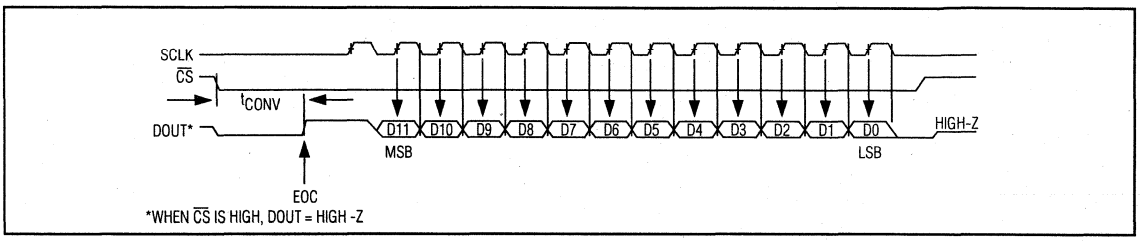


Figure 13. QSPI Serial Interface Timing (CPOL = CPHA = 0)

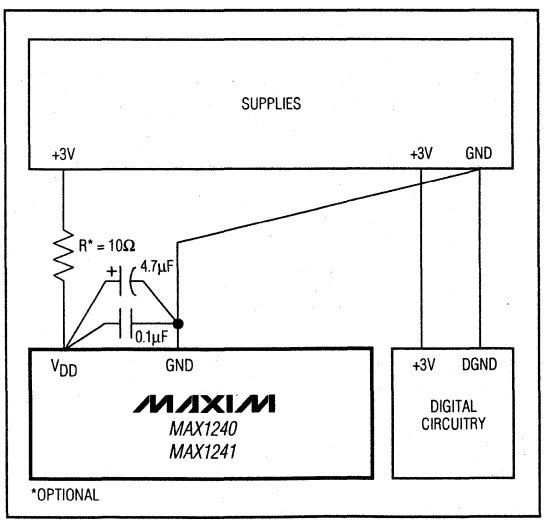


Figure 14. Power-Supply Grounding Condition

+2.7V, Low-Power, 12-Bit Serial ADCs in 8-Pin SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1240AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1240BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1240CEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1240AESA	-40°C to +85°C	8 SO	±1/2
MAX1240BESA	-40°C to +85°C	8 SO	±1
MAX1240CESA	-40°C to +85°C	8 SO	±1
MAX1240AMJA	-55°C to +125°C	8 CERDIP**	±1/2
MAX1240BMJA	-55°C to +125°C	8 CERDIP**	±1
MAX1240CMJA	-55°C to +125°C	8 CERDIP**	±1
MAX1241ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1241BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1241CCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1241ACSA	0°C to +70°C	8 SO	±1/2
MAX1241BCSA	0°C to +70°C	8 SO	±1
MAX1241CCSA	0°C to +70°C	8 SO	±1
MAX1241BC/D	0°C to +70°C	Dice*	±1
MAX1241AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1241BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1241CEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1241AESA	-40°C to +85°C	8 SO	±1/2
MAX1241BESA	-40°C to +85°C	8 SO	±1
MAX1241CESA	-40°C to +85°C	8 SO	±1
MAX1241AMJA	-55°C to +125°C	8 CERDIP**	±1/2
MAX1241BMJA	-55°C to +125°C	8 CERDIP**	±1
MAX1241CMJA	-55°C to +125°C	8 CERDIP**	±1

** Dice are specified at T_A = +25°C, DC parameters only.*

*** Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 2558

SUBSTRATE CONNECTED TO GND

19-1156; Rev 1; 7/97

MAXIM

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

General Description

The MAX1242/MAX1243 are low-power, 10-bit analog-to-digital converters (ADCs) available in 8-pin packages. The MAX1242 operates with a single +2.7V to +3.6V supply, and the MAX1243 operates with a single +2.7V to +5.25V supply. Both devices feature a 7.5µs successive-approximation ADC, a fast track/hold (1.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 3mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. A 2µA shutdown mode reduces power at slower throughput rates.

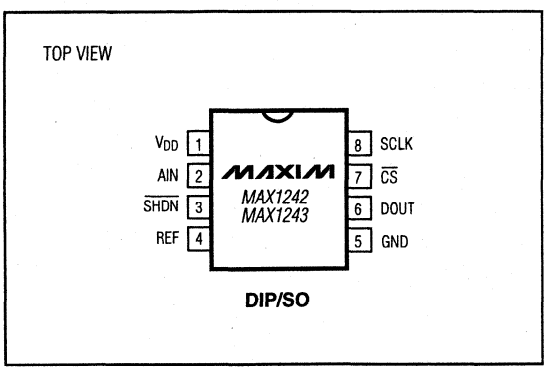
The MAX1242 has an internal 2.5V reference, while the MAX1243 requires an external reference. The MAX1243 accepts signals from 0V to V_{REF}, and the reference input range includes the positive supply rail. An external clock accesses data from the 3-wire interface, which connects directly to standard microcontroller I/O ports. The interface is compatible with SPI™, QSPI™, and Microwire™.

Excellent AC characteristics and very low power combined with ease of use and small package size make these converters ideal for remote-sensor and data-acquisition applications, or for other circuits with demanding power consumption and space requirements. The MAX1242/MAX1243 are available in 8-pin DIP and SO packages.

Applications

Portable Data Logging
Test Equipment
Isolated Data Acquisition
Process Control Monitoring
Temperature Measurement

Pin Configuration



Features

- **Single-Supply Operation:**
  +2.7V to +3.6V (MAX1242)
  +2.7V to +5.25V (MAX1243)
- **10-Bit Resolution**
- **Internal 2.5V Reference (MAX1242)**
- **Small Footprint: 8-Pin DIP and SO Packages**
- **Low Power: 3.7mW (73ksps, MAX1242)**
  3mW (73ksps, MAX1243)
  66µW (1ksps, MAX1243)
  5µW (power-down mode)
- **Internal Track/Hold**
- **SPI™/QSPI™/Microwire™ 3-Wire Serial Interface**
- **Pin-Compatible 12-Bit Upgrades:**
  MAX1240/MAX1241

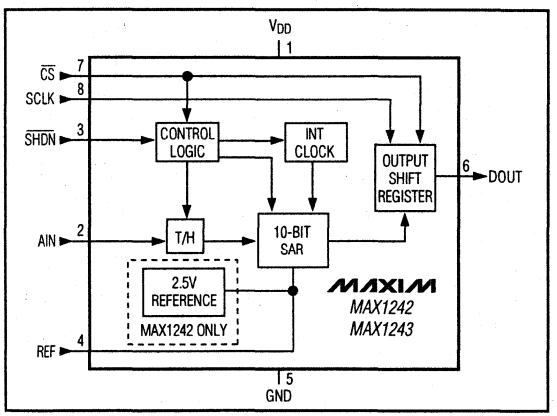
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1242CCPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1242DCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1242CCSA	0°C to +70°C	8 SO	±1/2
MAX1242DCSA	0°C to +70°C	8 SO	±1
MAX1242CEPA	-40°C to +85°C	8 Plastic DIP*	±1/2
MAX1242DEPA	-40°C to +85°C	8 Plastic DIP*	±1

*Contact factory for availability.

Ordering Information continued at end of data sheet.

Functional Diagram



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For small orders, phone 408-737-7600 ext. 3468.

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
AIN to GND .....-0.3V to (V_{DD} + 0.3V)
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND.....-0.3V to +6V
DOUT to GND.....-0.3V to (V_{DD} + 0.3V)
DOUT Current.....±25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C).....471mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX1242/MAX1243_C_A.....0°C to +70°C
MAX1242/MAX1243_E_ A .....-40°C to +85°C
MAX1242/MAX1243_MJA .....-55°C to +125°C
Storage Temperature Range.....-60°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1242), V_{DD} = +2.7V to +5.25V (MAX1243); 73ksps; f_{SCLK} = 2.1MHz (50% duty cycle); MAX1242—4.7µF capacitor at REF pin, MAX1243—external reference; V_{REF} = 2.5V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)		MAX1242C/MAX1243A			±0.5	LSB
		MAX1242D/MAX1243B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX1242C/MAX1243A			±1	LSB
		MAX1242D/MAX1243B			±2	
Gain Error (Note 3)		MAX1242C/MAX1243A			±1	LSB
		MAX1242D/MAX1243B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.5Vp-p, 73ksps, f_{SCLK} = 2.1MHz)						
Signal-to-Noise Plus Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Small-Signal Bandwidth		- 3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time	t_{CONV}		5.5		7.5	µs
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Throughput Rate		f_{SCLK} = 2.1MHz			73	ksps
Aperture Delay	t_{AP}	Figure 9		30		ns
Aperture Jitter				<50		ps
ANALOG INPUT						
Input Voltage Range			0		V_{REF}	V
Input Capacitance				16		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1242), V_{DD} = +2.7V to +5.25V (MAX1243); 73ksps; f_{SCLK} = 2.1MHz (50% duty cycle); MAX1242—4.7µF capacitor at REF pin, MAX1243—external reference; V_{REF} = 2.5V applied to REF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INTERNAL REFERENCE (MAX1242 only)							
REF Output Voltage		T_A = +25°C (Note 4)		2.470	2.500	2.530	V
REF Short-Circuit Current						30	mA
REF Temperature Coefficient		MAX1242			±30		ppm/°C
Load Regulation (Note 5)		0mA to 0.2mA output load			0.35		mV
Capacitive Bypass at REF				4.7			µF
EXTERNAL REFERENCE (V_{REF} = 2.5V)							
Input Voltage Range				1.00		V_{DD} + 50mV	V
Input Current					100	150	µA
Input Resistance				18	25		kΩ
REF Input Current in Shutdown		$\overline{SHDN}$ = 0V			±0.01	10	µA
Capacitive Bypass at REF				0.1			µF
DIGITAL INPUTS: SCLK, CS, SHDN							
SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$		2.0			V
		V_{DD} > 3.6V (MAX1243)		3.0			
SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}					0.8	V
SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}				0.2		V
SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}			±0.01	±1	µA
SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 6)				15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}			V_{DD} - 0.4			V
$\overline{SHDN}$ Input Low Voltage	V_{SL}					0.4	V
$\overline{SHDN}$ Input Current		$\overline{SHDN}$ = 0V or V_{DD}				±4.0	µA
$\overline{SHDN}$ Input Mid Voltage	V_{SM}			1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = float			V_{DD} / 2		V
$\overline{SHDN}$ Max Allowed Leakage, Mid Input		$\overline{SHDN}$ = float				±100	nA
DIGITAL OUTPUT: DOUT							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 6)				15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	MAX1242		2.7		3.6	V
		MAX1243		2.7		5.25	
Supply Current	I_{DD}	Operating mode (MAX1242)	V_{DD} = 3.6V		1.4	2.0	mA
		Operating mode (MAX1243)	V_{DD} = 3.6V		0.9	1.5	
			V_{DD} = 5.25V		1.6	2.5	
		Power-down	V_{DD} = 3.6V		1.9	10	µA
			V_{DD} = 5.25V		3.5	15	
Supply Rejection (Note 7)	PSR	V_{DD} = $V_{DD, min}$ to $V_{DD, max}$, full-scale input			±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1242), V_{DD} = +2.7V to +5.25V (MAX1243); T_A = T_{MIN} to T_{MAX}; unless otherwise noted.) (Figure 9)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}	$\overline{CS}$ = V_{DD} (Note 8)		1.5			µs
SCLK Fall to Output Data Valid	t_{DO}	Figure 1, C_{LOAD} = 50pF	MAX124_ _C/E	20		200	ns
			MAX124_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1, C_{LOAD} = 50pF				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2, C_{LOAD} = 50pF				240	ns
SCLK Clock Frequency	f_{SCLK}			0		2.1	MHz
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Low to $\overline{CS}$ Fall Setup Time	t_{CS0}			50			ns
DOUT Rise to SCLK Rise (Note 6)	t_{STR}			0			ns
$\overline{CS}$ Pulse Width	t_{CS}			240			ns

Note 1: Tested at V_{DD} = +2.7V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.
Note 3: Offset nulled.
Note 4: Sample tested to 0.1% AQL.
Note 5: External load should not change during conversion for specified accuracy.
Note 6: Guaranteed by design. Not subject to production testing.
Note 7: Measured as [V_{FS} ($V_{DD, min}$) - V_{FS} ($V_{DD, max}$)].
Note 8: To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired.

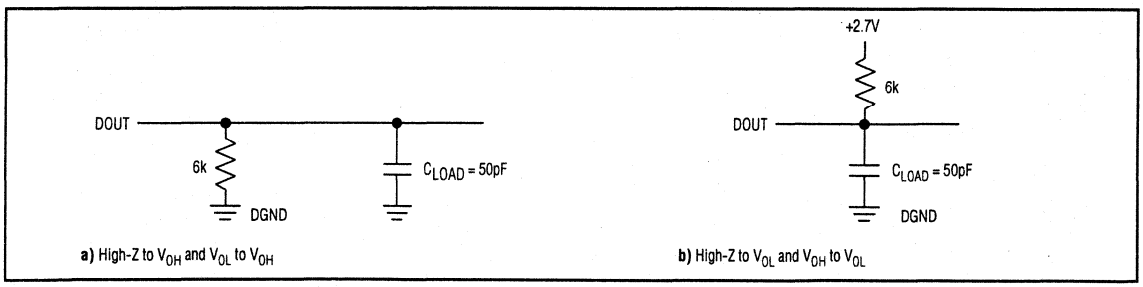


Figure 1. Load Circuits for DOUT Enable Time

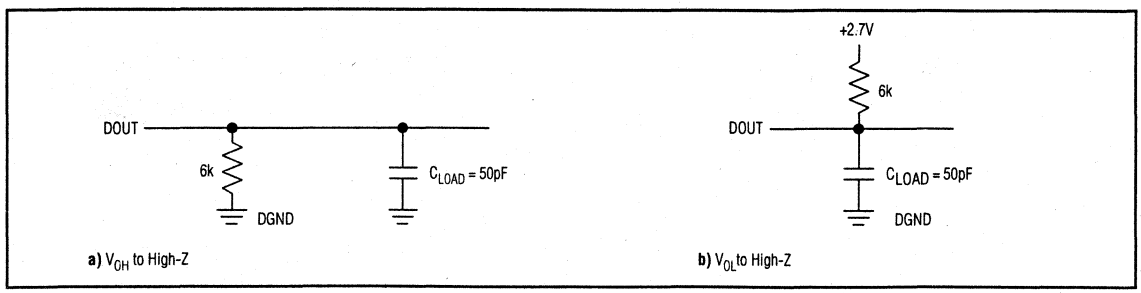
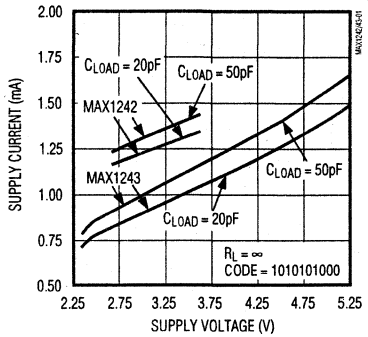


Figure 2. Load Circuits for DOUT Disable Time

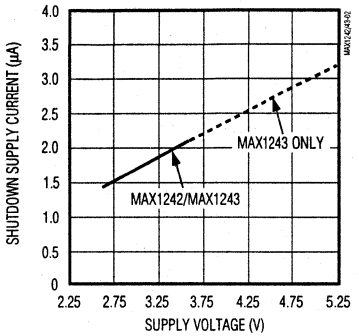
Typical Operating Characteristics

(V_{DD} = +3.0V, V_{REF} = 2.5V, f_{SCLK} = 2.1MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

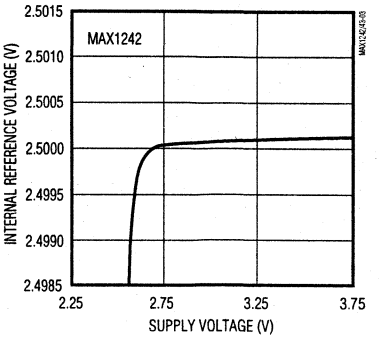
SUPPLY CURRENT vs. SUPPLY VOLTAGE



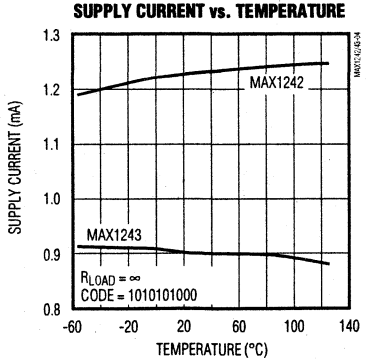
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



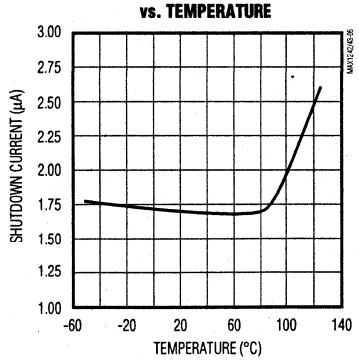
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



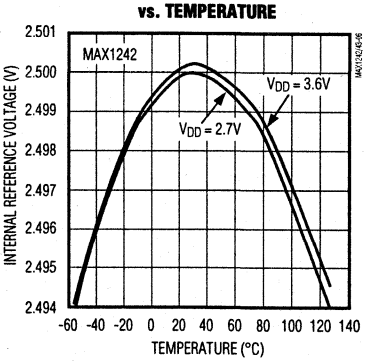
SUPPLY CURRENT vs. TEMPERATURE



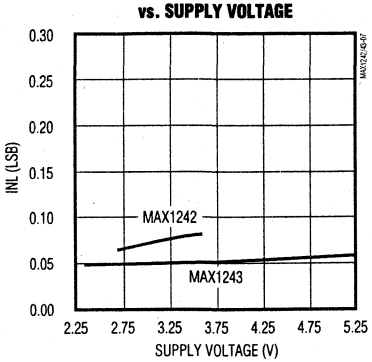
SHUTDOWN CURRENT vs. TEMPERATURE



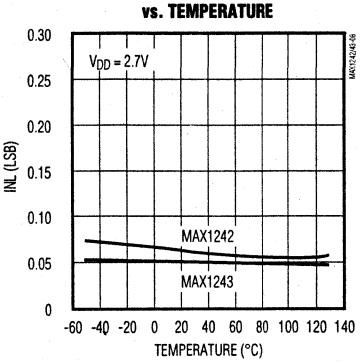
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



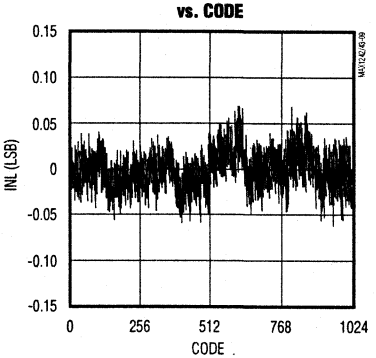
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



7

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage: +2.7V to +3.6V (MAX1242); +2.7V to +5.25V (MAX1243)
2	AIN	Sampling Analog Input, 0V to V_{REF} range
3	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1242/MAX1243 down to 15µA (max) supply current. Both MAX1242 and MAX1243 are fully operational with either $\overline{SHDN}$ high or floating. For the MAX1242, pulling $\overline{SHDN}$ high enables the internal reference, and letting $\overline{SHDN}$ float disables the internal reference and allows for the use of an external reference.
4	REF	Reference Voltage for Analog-to-Digital Conversion. Internal 2.5V reference output for MAX1242; bypass with a 4.7µF capacitor. External reference voltage input for MAX1243, or for MAX1242 with the internal reference disabled. Bypass REF with a minimum of 0.1µF when using an external reference.
5	GND	Analog and Digital Ground
6	DOUT	Serial-Data Output. Data changes state at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
7	$\overline{CS}$	Active-Low Chip Select. Initiates conversions on the falling edge. When $\overline{CS}$ is high, DOUT is high impedance.
8	SCLK	Serial-Clock Input. SCLK clocks data out at rates up to 2.1MHz.

Detailed Description

Converter Operation

The MAX1242/MAX1243 use an input track/hold (T/H) and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 10-bit output. Figure 3 shows the MAX1242/MAX1243 in their simplest configuration. The MAX1242/MAX1243 convert input signals in the 0V to V_{REF} range in 9µs, including T/H acquisition time. The MAX1242's internal reference is trimmed to 2.5V, while the MAX1243 requires an external reference. Both devices accept external reference voltages from 1.0V to V_{DD}. The serial interface requires only three digital lines (SCLK, $\overline{CS}$, and DOUT) and provides an easy interface to microprocessors (µPs).

The MAX1242/MAX1243 have two modes: normal and shutdown. Pulling $\overline{SHDN}$ low shuts the device down and reduces supply current below 10µA ($V_{DD} \leq 3.6V$), while pulling $\overline{SHDN}$ high or leaving it open puts the devices into operational mode. A conversion is initiated by pulling $\overline{CS}$ low. The conversion result is available at DOUT in unipolar serial format. The serial-data stream consists of a high bit, signaling the end of conversion (EOC), followed by the data bits (MSB first).

Analog Input

Figure 4 illustrates the sampling architecture of the analog-to-digital converter's (ADC's) comparator. The full-scale input voltage is set by the voltage at REF.

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input AIN charges capacitor C_{HOLD}. Bringing $\overline{CS}$ low ends the acquisition interval. At this instant, the T/H switches the input side of C_{HOLD} to GND. The retained charge on C_{HOLD} represents a sample of the input, unbalancing node ZERO at the comparator's input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input side of C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal and the minimum time needed for the signal to be acquired. Acquisition time is calculated by:

$$t_{ACQ} = 7(R_S + R_{IN}) \times 16pF$$

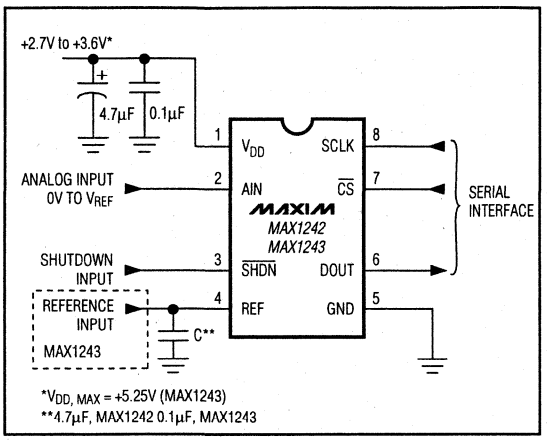


Figure 3. Operational Diagram

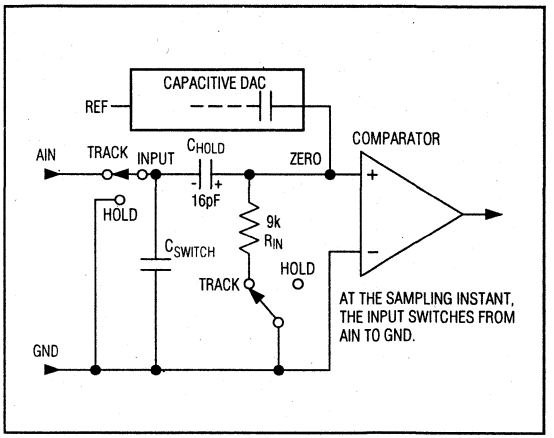


Figure 4. Equivalent Input Circuit

where R_{IN} = 9kΩ, R_S = the input signal's source impedance, and t_{ACQ} is never less than 1.5µs. Source impedances below 4kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's input signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from GND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA.

Internal Reference (MAX1242)

The MAX1242 has an on-chip voltage reference trimmed to 2.5V. The internal reference output is connected to REF and also drives the internal capacitive DAC. The output can be used as a reference voltage source for other components and can source up to 400µA. Bypass REF with a 4.7µF capacitor. Larger capacitors increase wake-up time when exiting shutdown (see *Using $\overline{SHDN}$ to Reduce Supply Current*). The internal reference is enabled by pulling the $\overline{SHDN}$ pin high. Letting $\overline{SHDN}$ float disables the internal reference, which allows the use of an external reference, as described in the *External Reference* section.

External Reference

The MAX1242/MAX1243 operate with an external reference at the REF pin. To use the MAX1242 with an external reference, disable the internal reference by letting $\overline{SHDN}$ float. Stay within the voltage range 1.0V to V_{DD} to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents. During conversion, the external reference must be able to deliver up to 250µA of DC load current and have an output impedance of 10Ω or less. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor.

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

Serial Interface

Initialization after Power-Up and Starting a Conversion

When power is first applied, and if $\overline{SHDN}$ is not pulled low, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy. With an external reference, the internal reset time is 10µs after the power supplies have stabilized. No conversions should be performed during these times.

To start a conversion, pull $\overline{CS}$ low. At $\overline{CS}$'s falling edge, the T/H enters its hold mode and a conversion is initiated. After an internally timed conversion period, the end of conversion is signaled by DOUT pulling high. Data can then be shifted out serially with the external clock.

Using $\overline{SHDN}$ to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1242/MAX1243 between conversions. Figure 6 shows a plot of average supply current vs. conversion rate. Because the MAX1243 uses an external reference voltage (assumed to be present continuously), it "wakes up" from shutdown more quickly, providing lower average supply currents. The wake-up time, t_{WAKE}, is the time from $\overline{SHDN}$ deasserted to the time when a conversion may be initiated (Figure 5). For the MAX1242, this time depends on the time in shutdown (Figure 7) because the external 4.7µF reference bypass capacitor loses charge slowly during shutdown. The MAX1243's wake-up time is largely dependent on the external reference's power-up time. If the external reference is not shut down, the wake-up time is approximately 4µs.

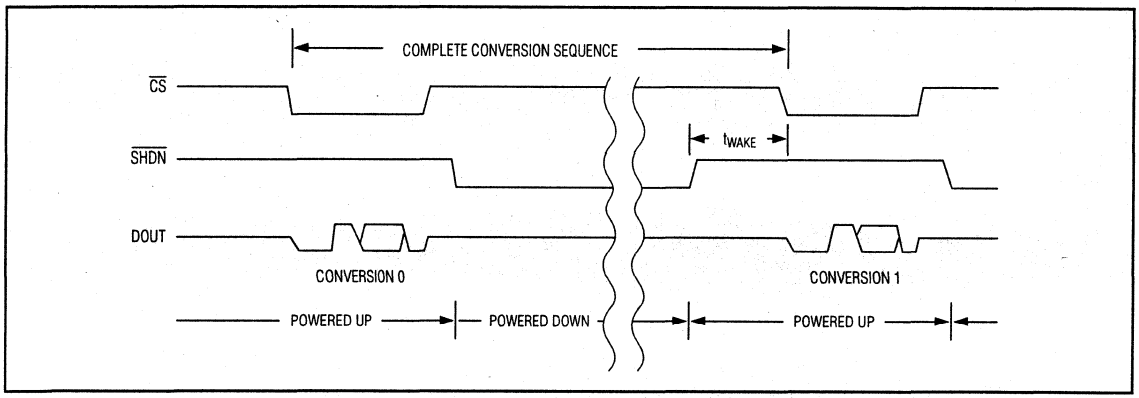


Figure 5. Shutdown Sequence

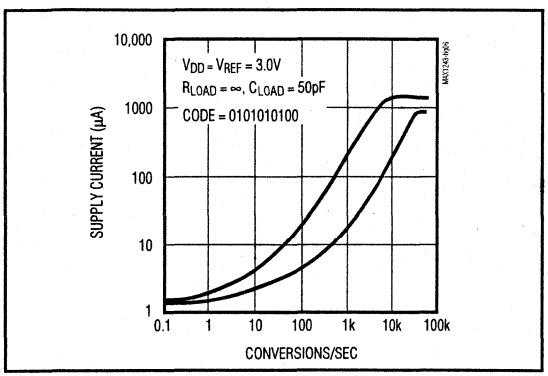


Figure 6. Average Supply Current vs. Conversion Rate

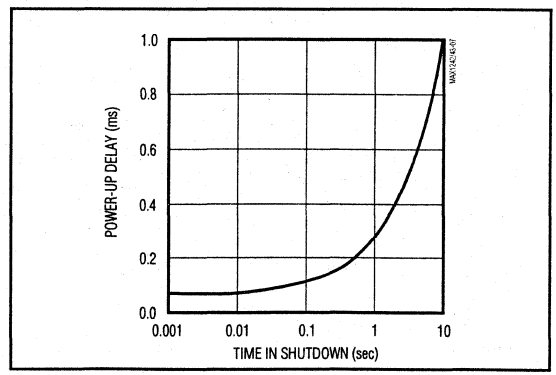


Figure 7. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

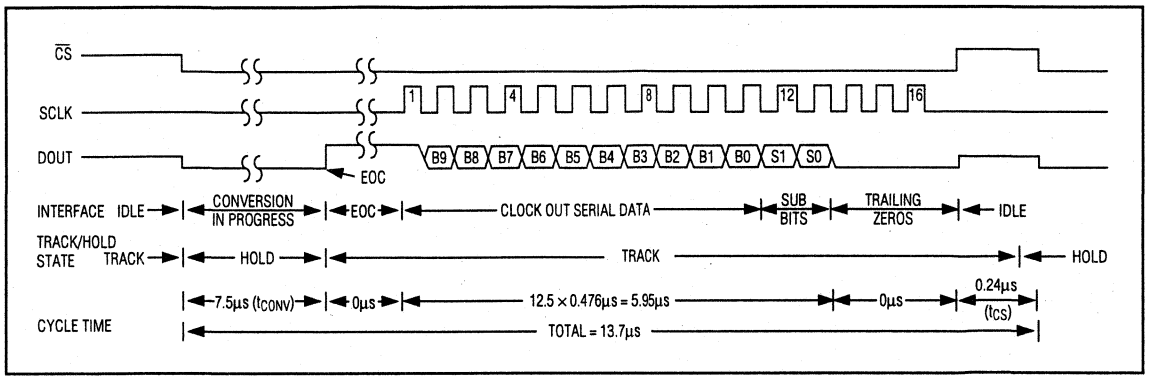


Figure 8a. Interface Timing Sequence

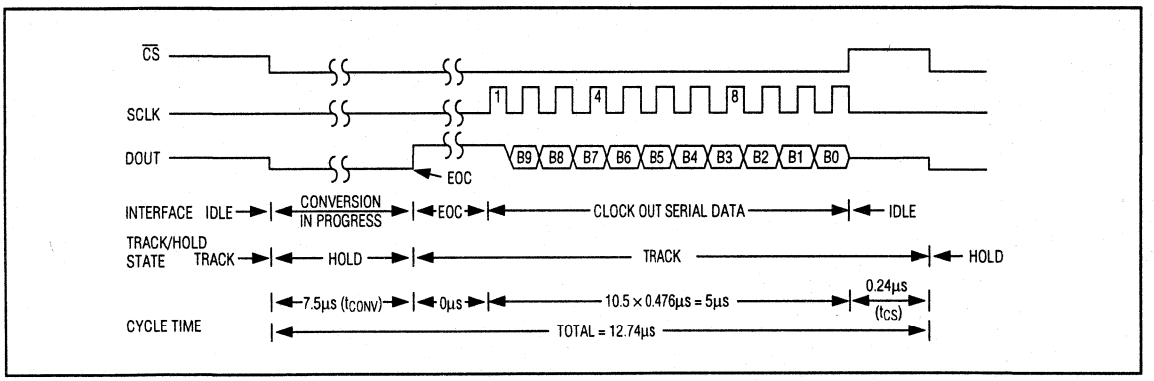


Figure 8b. Interface Timing Sequence—Minimum Cycle Time

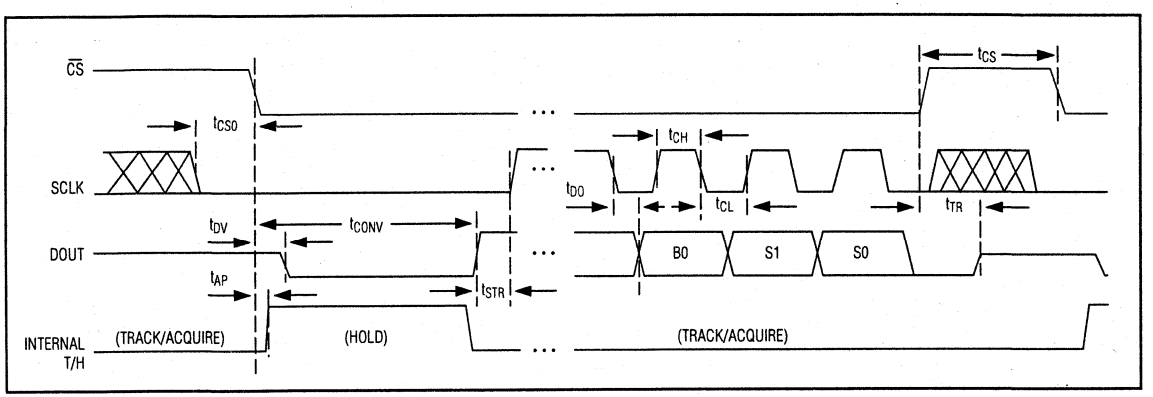


Figure 9. Detailed Serial-Interface Timing

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

External Clock

The actual conversion does not require the external clock. This allows the conversion result to be read back at the µP's convenience at any clock rate up to 2.1MHz. The clock duty cycle is unrestricted if each clock phase is at least 200ns. Do not run the clock while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by the $\overline{CS}$ and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline serial-interface operation.

A $\overline{CS}$ falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK must be kept low during the conversion. An internal register stores the data when the conversion is in progress.

EOC is signaled by DOUT going high. DOUT's rising edge can be used as a framing signal. SCLK shifts the data out of this register any time after the conversion is complete. DOUT transitions on SCLK's falling edge. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 10 data bits, two sub-bits, and one leading high bit, at least 13 falling clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of $\overline{CS}$, produce trailing zeros at DOUT and have no effect on converter operation.

For minimum cycle time, use DOUT's rising edge as the EOC signal and then clock out the data with 10.5 clock cycles at full speed (Figure 8b). Pull $\overline{CS}$ high after reading the conversion's LSB. After the specified minimum time, t_{CS}, pull $\overline{CS}$ low again to initiate the next conversion.

Output Coding and Transfer Function

The data output from the MAX1242/MAX1243 is binary. Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB values. If V_{REF} = 2.5V, then 1LSB = 2.44mV or 2.5V / 1024.

Applications Information

Connection to Standard Interfaces

The MAX1242/MAX1243 serial interface is fully compatible with SPI, QSPI, and Microwire standard serial interfaces (Figure 11).

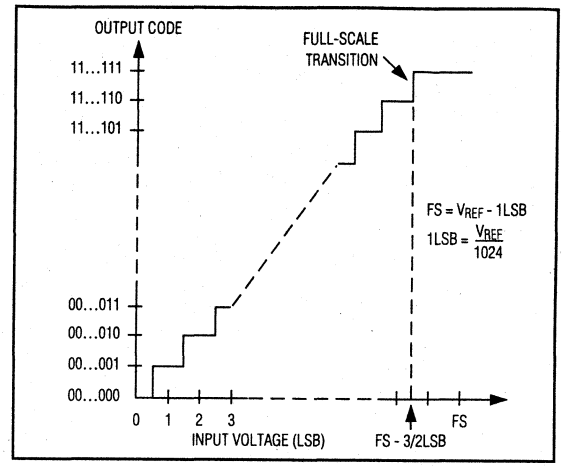


Figure 10. Unipolar Transfer Function, Full Scale (FS) = V_{REF} - 1LSB, Zero Scale (ZS) = GND

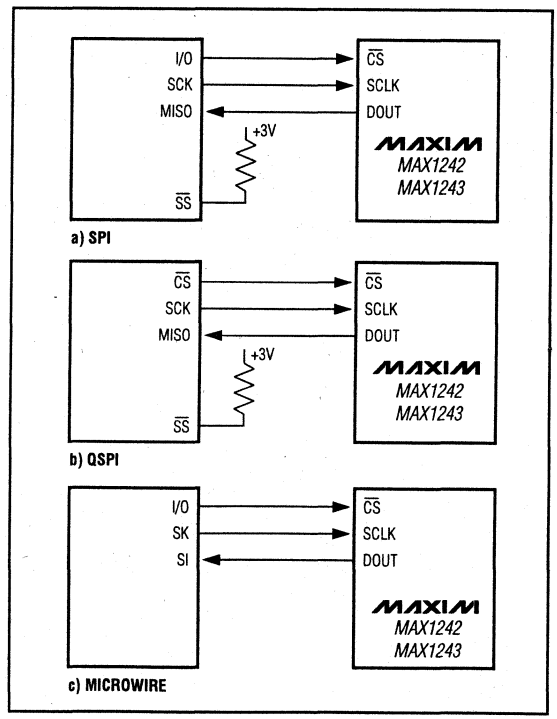


Figure 11. Common Serial-Interface Connections to the MAX1242/MAX1243

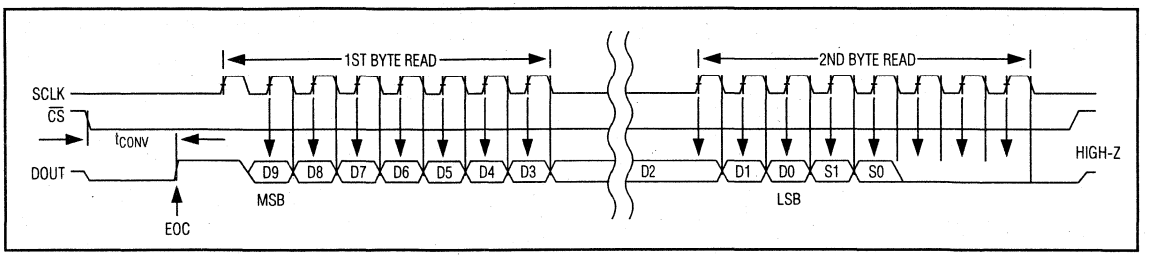


Figure 12. SPI/Microwire Serial-Interface Timing (CPOL = CPHA = 0)

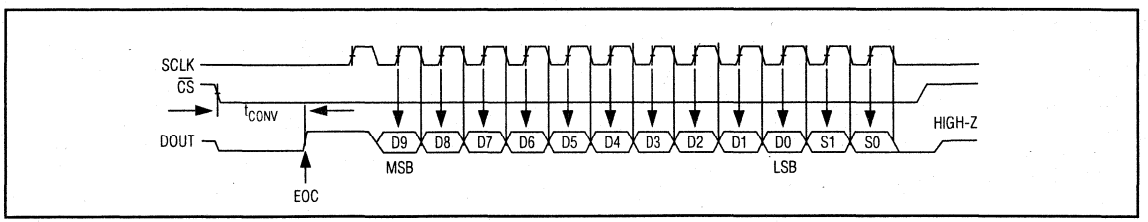


Figure 13. QSPI Serial-Interface Timing (CPOL = CPHA = 0)

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 2.1MHz.

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low. Keep SCLK low.
2) Wait the maximum conversion time specified before activating SCLK. Alternatively, look for a DOUT rising edge to determine the end of conversion.
3) Activate SCLK for a minimum of 11 clock cycles. The first falling clock edge produces the MSB of the DOUT conversion. DOUT output data transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK-to-DOUT valid timing characteristic. Data can be clocked into the µP on SCLK's rising edge.
4) Pull $\overline{CS}$ high at or after the 11th falling clock edge. If $\overline{CS}$ remains low, the two sub-bits and trailing zeros are clocked out after the LSB.
5) With $\overline{CS}$ = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling $\overline{CS}$ low. If a conversion is aborted by pulling $\overline{CS}$ high before the conversion's end, wait the minimum acquisition time, t_{ACQ}, before starting a new conversion.

Data can be output in two bytes or continuously, as shown in Figures 8a and 8b. The bytes contain the result of the conversion padded with one leading 1, two sub-bits, and trailing 0s if SCLK is still active with $\overline{CS}$ kept low.

SPI and Microwire

When using SPI or QSPI, set CPOL = 0 and CPHA = 0. Conversion begins with a $\overline{CS}$ falling edge. DOUT goes low, indicating a conversion is in progress. Wait until DOUT goes high or until the maximum specified 7.5µs conversion time elapses. Two consecutive 1-byte reads are required to get the full 10+2 bits from the ADC. DOUT output data transitions on SCLK's falling edge and is clocked into the µP on SCLK's rising edge.

The first byte contains a leading 1, and seven bits of conversion result. The second byte contains the remaining three bits, two sub-bits, and three trailing zeros. See Figure 11 for connections and Figure 12 for timing.

QSPI

Set CPOL = CPHA = 0. Unlike SPI, which requires two 1-byte reads to acquire the 10 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1242/MAX1243 require 11 clock cycles from the µP to clock out the 10 bits of data. Additional clock cycles clock out the two sub-bits followed by trailing zeros (Figure 13). The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Layout and Grounding

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

+2.7V, Low-Power, 10-Bit Serial ADCs in SO-8

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1242CESA	-40°C to +85°C	8 SO*	±1/2
MAX1242DESA	-40°C to +85°C	8 SO*	±1
MAX1242CMJA	-55°C to +125°C	8 CERDIP**	±1/2
MAX1242DMJA	-55°C to +125°C	8 CERDIP**	±1
MAX1243ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX1243BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX1243ACSA	0°C to +70°C	8 SO	±1/2
MAX1243BCSA	0°C to +70°C	8 SO	±1
MAX1243AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX1243BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX1243AESA	-40°C to +85°C	8 SO	±1/2
MAX1243BESA	-40°C to +85°C	8 SO	±1
MAX1243AMJA	-55°C to +125°C	8 CERDIP**	±1/2
MAX1243BMJA	-55°C to +125°C	8 CERDIP**	±1

*Contact factory for availability.
**Contact factory for availability and processing to MIL-STD-883.

Chip Information

TRANSISTOR COUNT: 2559
SUBSTRATE CONNECTED TO GND

19-1071; Rev 1; 3/97

EVALUATION KIT AVAILABLE

MAXIM

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

General Description

The MAX1246/MAX1247 12-bit data-acquisition systems combine a 4-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption. The MAX1246 operates from a single +2.7V to +3.6V supply; the MAX1247 operates from a single +2.7V to +5.25V supply. Both devices' analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1246/MAX1247 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX1246 has an internal 2.5V reference, while the MAX1247 requires an external reference. Both parts have a reference-buffer amplifier with a ±1.5% voltage-adjustment range.

These devices provide a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX1246/MAX1247, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current to under 60µA at reduced sampling rates.

The MAX1246/MAX1247 are available in a 16-pin DIP and a small QSOP that occupies the same board area as an 8-pin SO.

For 8-channel versions of these devices, see the MAX146/MAX147 data sheet.

Applications

Portable Data Logging
Medical Instruments
Pen Digitizers
Data Acquisition
Battery-Powered Instruments
Process Control

Features

- **4-Channel Single-Ended or 2-Channel Differential Inputs**
- **Single-Supply Operation:**
  +2.7V to +3.6V (MAX1246)
  +2.7V to +5.25V (MAX1247)
- **Internal 2.5V Reference (MAX1246)**
- **Low Power: 1.2mA (133ksps, 3V supply)**
  54µA (1ksps, 3V supply)
  1µA (power-down mode)
- **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **16-Pin QSOP Package (same area as 8-pin SO)**

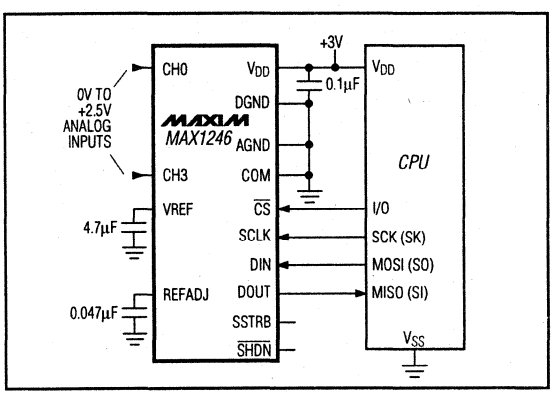
Ordering Information

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1246ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1246BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX1246ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1246BCEE	0°C to +70°C	16 QSOP	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

SPI and QSPI are registered trademarks of Motorola, Inc. Microwire is a registered trademark of National Semiconductor Corp.

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For small orders, phone 408-737-7600 ext. 3468.

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to 6V
AGND to DGND ..... -0.3V to 0.3V
CH0–CH3, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to 6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.36mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX1246_C_E/MAX1247_C_E ..... 0°C to +70°C
MAX1246_E_E/MAX1247_E_E ..... -40°C to +85°C
MAX1246_MJE/MAX1247_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1246); V_{DD} = +2.7V to +5.25V (MAX1247); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1246—4.7µF capacitor at VREF pin; MAX1247—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			12			Bits
Relative Accuracy (Note 2)	INL	MAX124_A			±0.5	LSB
		MAX124_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX124_A		±0.5	±3	LSB
		MAX124_B		±0.5	±4	
Gain Error (Note 3)				±0.5	±4	LSB
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.25		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD		70	73		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-88	-80	dB
Spurious-Free Dynamic Range	SFDR		80	90		dB
Channel-to-Channel Crosstalk		65kHz, 2.500V_{p-p} (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1246); V_{DD} = +2.7V to +5.25V (MAX1247); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1246—4.7µF capacitor at VREF pin; MAX1247—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF / 2			±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX1246 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C	2.480	2.500	2.520	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX1246_C		±30	±50	ppm/°C
		MAX1246_E		±30	±60	
		MAX1246_M		±30	±80	
Load Regulation (Note 8)		0mA to 0.2mA output load		±0.35		mV
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.047			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 9)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
REFADJ Buffer Disable Threshold			V_{DD} - 0.5			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference Buffer Gain		MAX1246		2.06		V/V
		MAX1247		2.00		
REFADJ Input Current		MAX1246			±50	µA
		MAX1247			±10	

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+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +3.6V (MAX1246); V_{DD} = +2.7V to +5.25V (MAX1247); COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1246—4.7µF capacitor at VREF pin; MAX1247—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$	2.0			V
		V_{DD} > 3.6V, MAX1247 only	3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 7)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current	I_S	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = FLOAT		V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = FLOAT			±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)						
Output Voltage Low	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}		±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 7)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	MAX1246	2.70		3.60	V
		MAX1247	2.70		5.25	
Positive Supply Current, MAX1246	I_{DD}	V_{DD} = 3.6V, Operating mode, full-scale input		1.2	2.0	mA
		V_{DD} = 3.6V, Fast power-down		30	70	µA
		V_{DD} = 3.6V, Full power-down		1.2	10	
Positive Supply Current, MAX1247	I_{DD}	Operating mode, full-scale input, V_{DD} = 5.25V		1.8	2.5	mA
		Operating mode, full-scale input, V_{DD} = 3.6V		0.9	1.5	
		Fast power-down		30	70	µA
		Full power-down, V_{DD} = 5.25V		3.5	15	
		Full power-down, V_{DD} = 3.6V		1.2	10	
Supply Rejection (Note 10)	PSR	V_{DD} = 2.7V to $V_{DD(MAX)}$, full-scale input, external reference = 2.500V		±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +3.6V (MAX1246); V_{DD} = +2.7V to +5.25V (MAX1247); T_A = T_{MIN} to T_{MAX}; unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX124_ _C/E	20		200	ns
			MAX124_ _M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 7)		0			ns

Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX1246—internal reference, offset nulled; MAX1247—external reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7: Guaranteed by design. Not subject to production testing.
Note 8: External load should not change during conversion for specified accuracy.
Note 9: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 10: Measured as $|V_{FS}(2.7V) - V_{FS}(V_{DD, MAX})|$.

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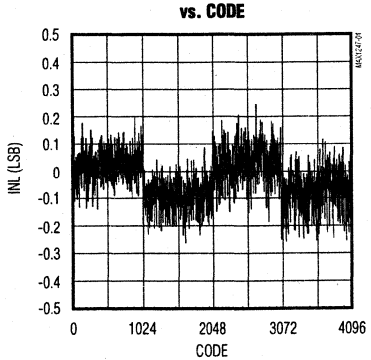
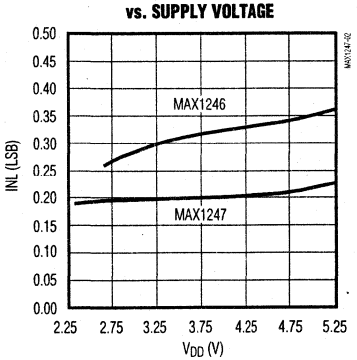
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

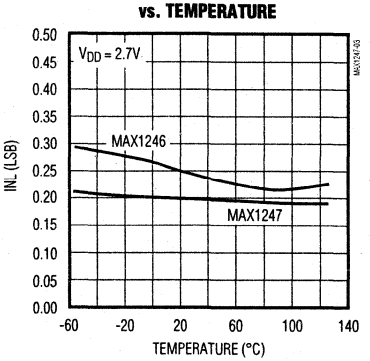
INTEGRAL NONLINEARITY vs. CODE



INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE

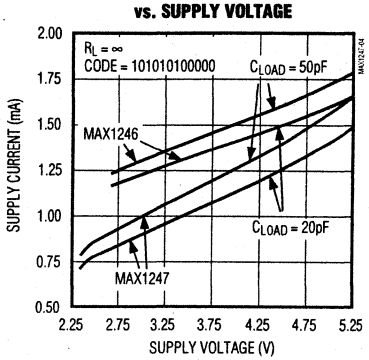


+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

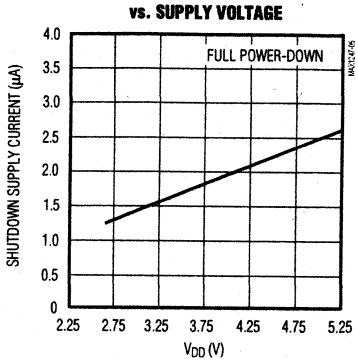
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

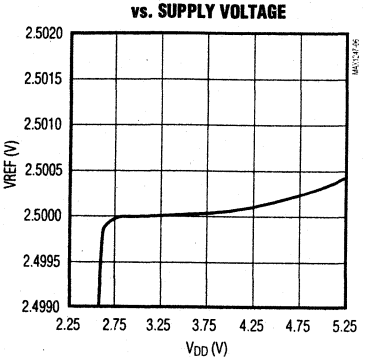
SUPPLY CURRENT vs. SUPPLY VOLTAGE



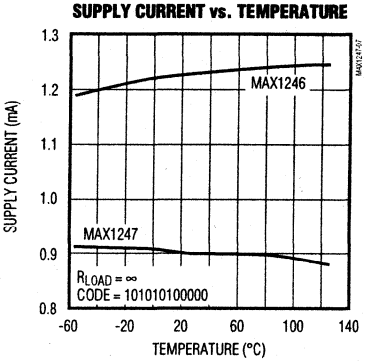
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



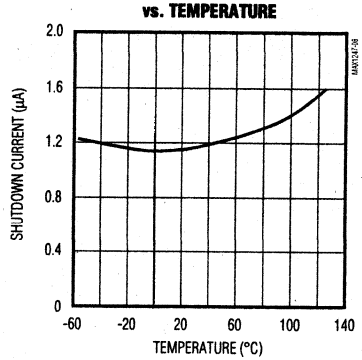
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



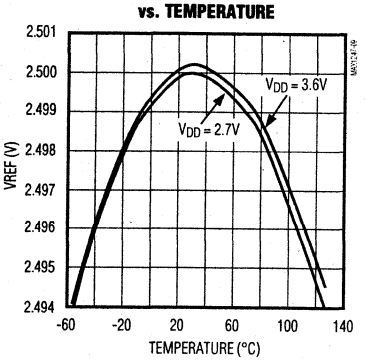
SUPPLY CURRENT vs. TEMPERATURE



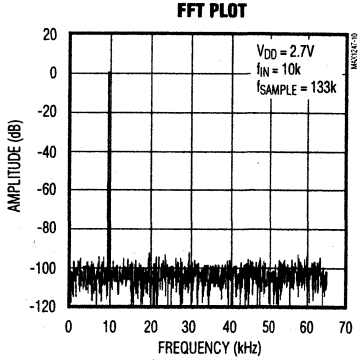
SHUTDOWN CURRENT vs. TEMPERATURE



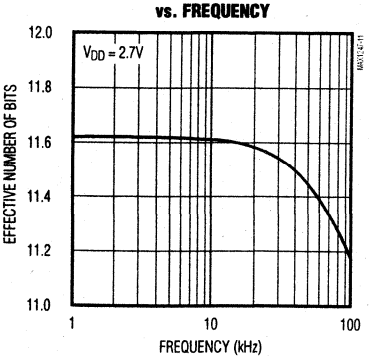
MAX1246 INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



FFT PLOT



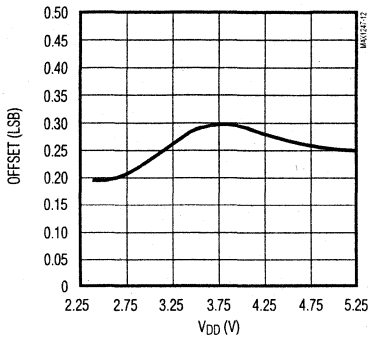
EFFECTIVE NUMBER OF BITS vs. FREQUENCY



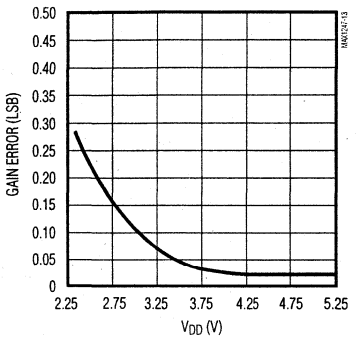
Typical Operating Characteristics (continued)

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

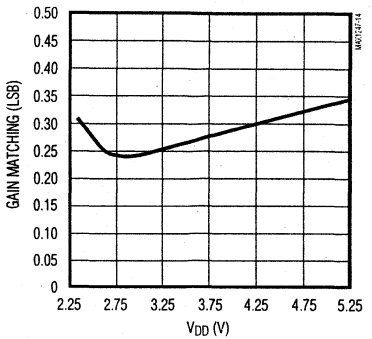
OFFSET vs. SUPPLY VOLTAGE



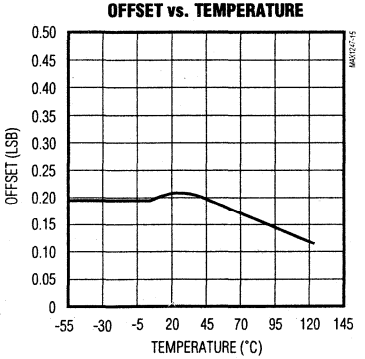
GAIN ERROR vs. SUPPLY VOLTAGE



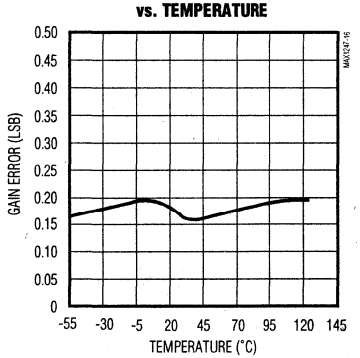
CHANNEL-TO-CHANNEL GAIN MATCHING vs. SUPPLY VOLTAGE



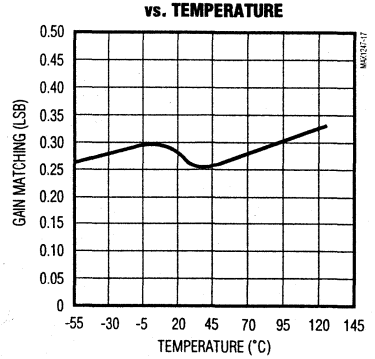
OFFSET vs. TEMPERATURE



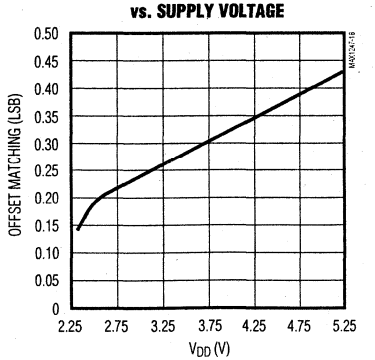
GAIN ERROR vs. TEMPERATURE



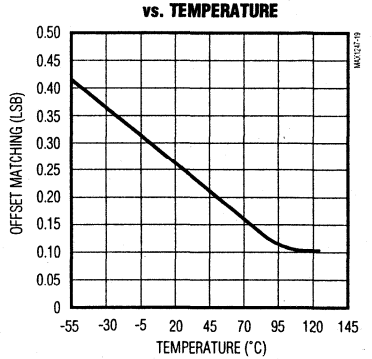
CHANNEL-TO-CHANNEL GAIN MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. SUPPLY VOLTAGE



CHANNEL-TO-CHANNEL OFFSET MATCHING vs. TEMPERATURE



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+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2–5	CH0–CH3	Sampling Analog Inputs
6	COM	Ground reference for analog inputs. COM sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
7	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1246/MAX1247 down; otherwise, they are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
8	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX1246 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
9	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
10	AGND	Analog Ground
11	DGND	Digital Ground
12	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
13	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1246/MAX1247 begin the A/D conversion, and goes high when the conversion is finished. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
14	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
15	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
16	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

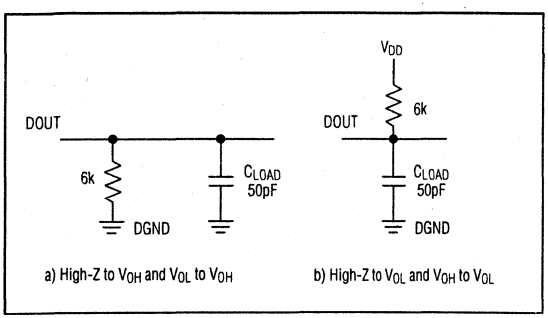

Figure 1. Load Circuits for Enable Time

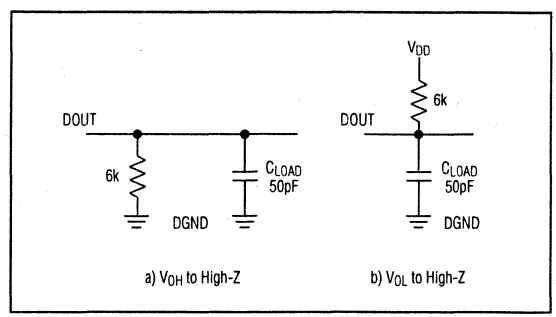

Figure 2. Load Circuits for Disable Time

Detailed Description

The MAX1246/MAX1247 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX1246/MAX1247.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH3, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from two pairs: CH0/CH1 and CH2/CH3. Configure the channels with Tables 2 and 3. Please note that the codes for CH0–CH3 in the MAX1246/MAX1247 correspond to the codes for CH2–CH5 in the eight-channel (MAX146/MAX147) versions.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a 16pF x $[(V_{IN+}) - (V_{IN-})]$ charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be

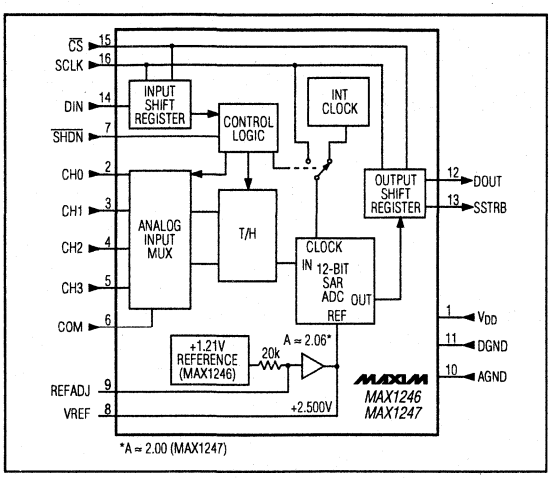

Figure 3. Block Diagram

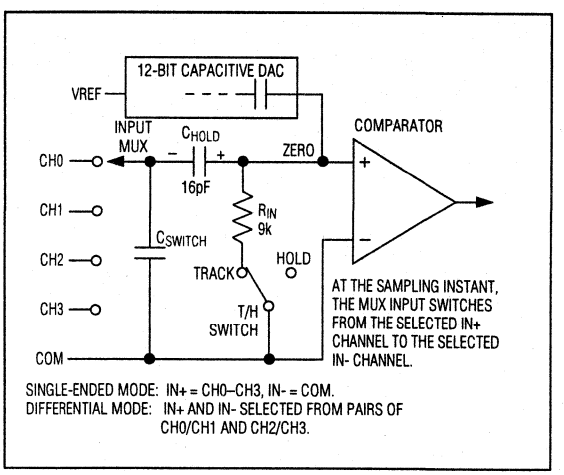

Figure 4. Equivalent Input Circuit

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the four channels are used for the conversion (Tables 2 and 3).
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF / 2 to +VREF / 2.
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 PD0 Mode 0 0 Full power-down 0 1 Fast power-down 1 0 Internal clock mode 1 1 External clock mode

allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by the following equation:

$$t_{ACQ} = 9 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 1kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 4mA.

How to Start a Conversion

Start a conversion by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1246/MAX1247's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1246/MAX1247 are compatible with SPI™/QSPI™ and Microwire™ devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating*

Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	1	+				–
1	0	1		+			–
0	1	0			+		–
1	1	0				+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	1	+	–		
0	1	0			+	–
1	0	1	–	+		
1	1	0			–	+

Circuit, the simplest software interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 12-bit conversion result). See Figure 19 for MAX1246/MAX1247 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 5 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion, padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 16). For bipolar inputs, the output is two's complement (Figure 17). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1246/MAX1247 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1246/MAX1247. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 6–9 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, but it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 12 SCLK falling edges (Figure 5). SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 7 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial clock frequency is less than 100kHz, or if serial clock interruptions could cause the conversion interval to exceed 120µs.

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

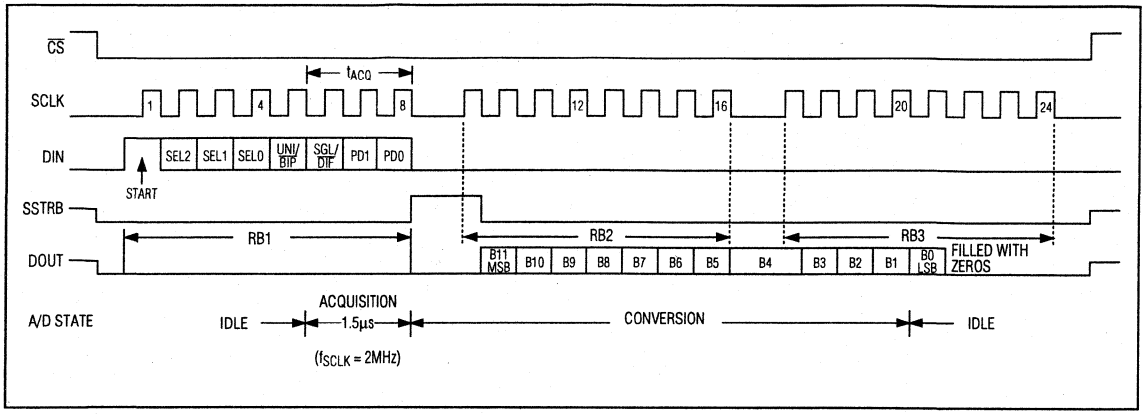

Figure 5. 24-Clock External Clock Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{SCLK} \leq 2MHz$)

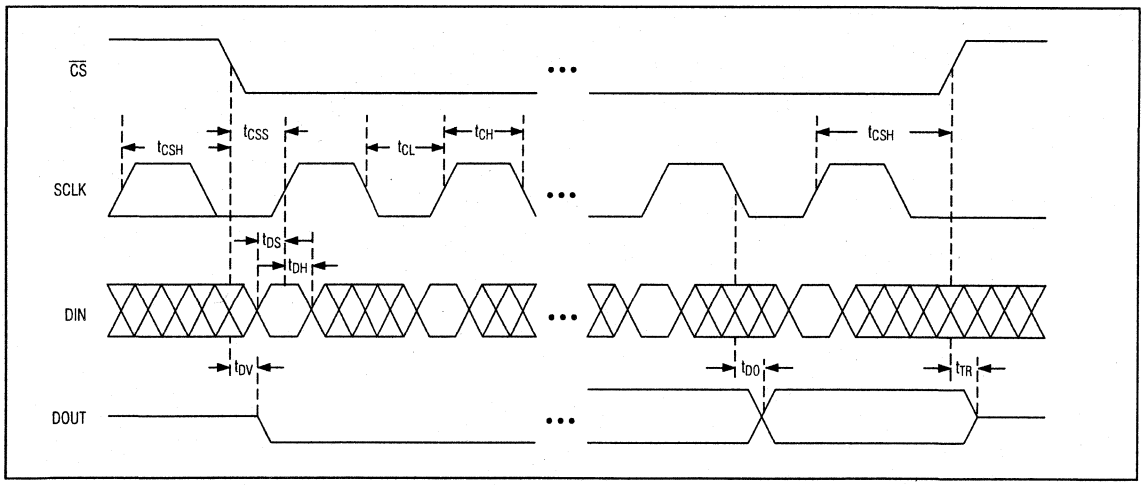

Figure 6. Detailed Serial-Interface Timing

Internal Clock

In internal clock mode, the MAX1246/MAX1247 generate their own conversion clocks internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 8). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1246/MAX1247 and three-states DOUT, but it does not adversely affect an internal clock mode

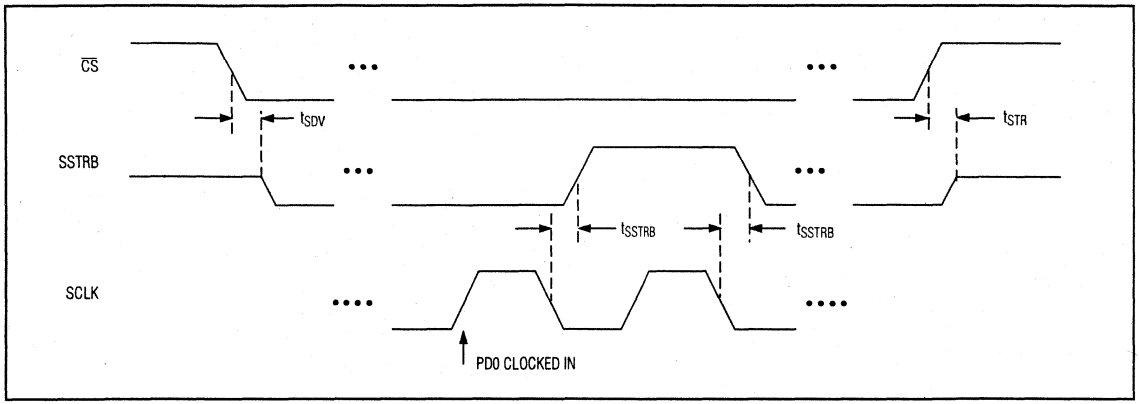

Figure 7. External Clock Mode SSTRB Detailed Timing

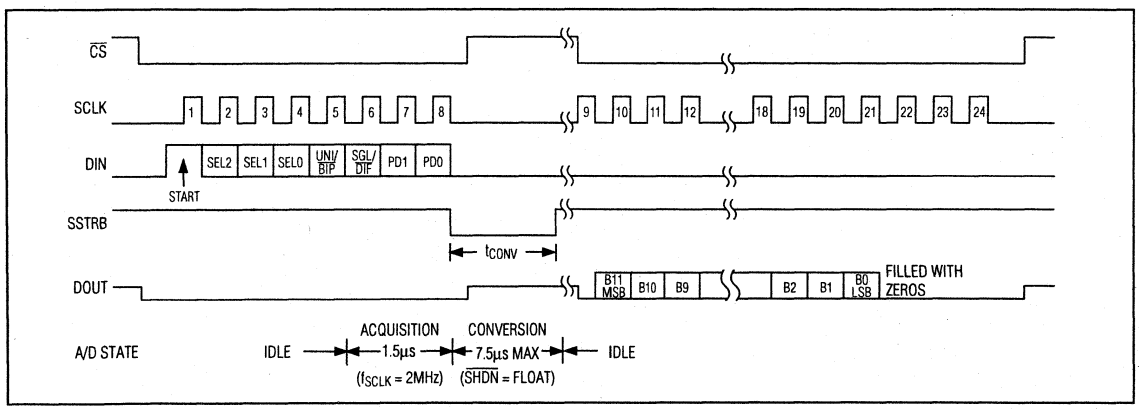

Figure 8. Internal Clock Mode Timing

conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 9 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1246/MAX1247 at clock rates exceeding 2.0MHz if the minimum acquisition time (t_{ACQ}) is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on SCLK's falling edge, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as follows:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 5 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

The fastest the MAX1246/MAX1247 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 10a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers (µCs) require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a µC can drive the MAX1246/MAX1247. Figure 10b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

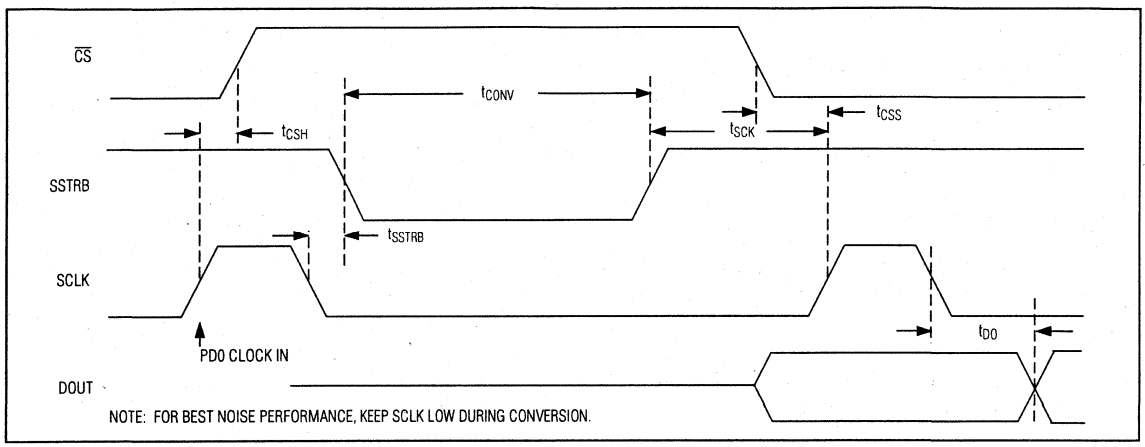

Figure 9. Internal Clock Mode SSTRB Detailed Timing

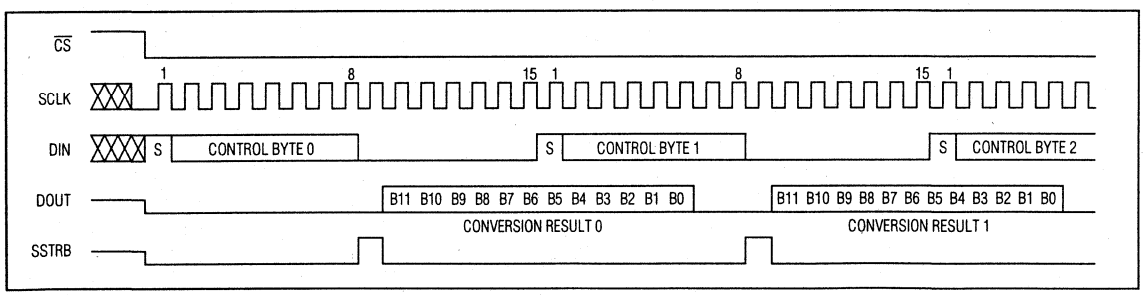

Figure 10a. External Clock Mode, 15 Clocks/Conversion Timing

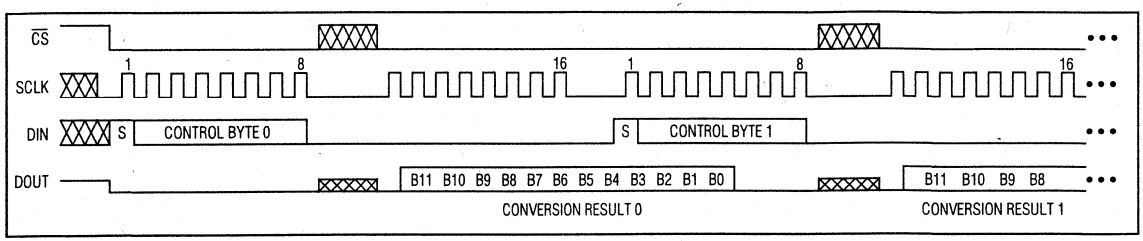

Figure 10b. External Clock Mode, 16 Clocks/Conversion Timing

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1246/MAX1247 in internal clock mode, ready to convert with SSTRB = high. After the power supplies stabilize, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. (Also see Table 4.)

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The100kHz minimum clock rate is limited by droop on the sample-and-hold and is independent of the compensation used.

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at VREF. A 4.7µF value ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see the *Choosing Power-Down Mode* section and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down mode or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current to 2µA (typ). Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 11a and 11b show the various power-down sequences in both external and internal clock modes.

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active and conversion results may be clocked out after the MAX1246/MAX1247 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1246/MAX1247. Following the start bit, the data input word or control byte also

Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal		Fast	5	26
Enabled	Internal		Full	300	26
Enabled	External	4.7	Fast	See Figure 13c	133
Enabled	External	4.7	Full	See Figure 13c	133
Disabled			Fast	2	133
Disabled			Full	2	133

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

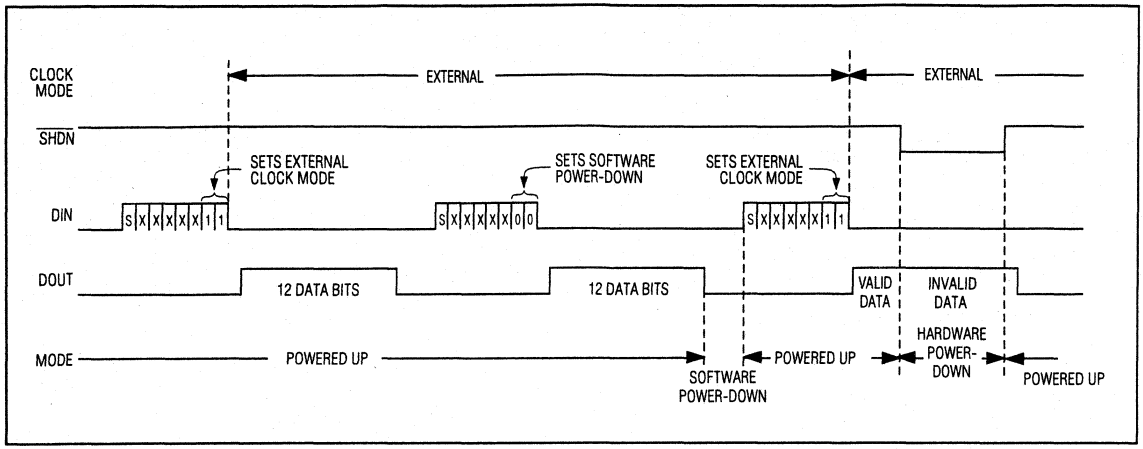

Figure 11a. Timing Diagram Power-Down Modes, External Clock

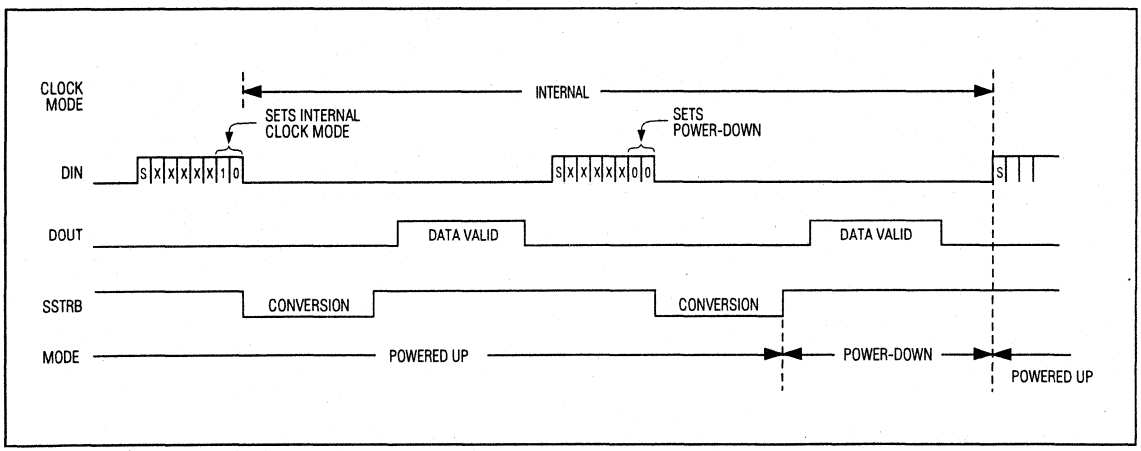

Figure 11b. Timing Diagram Power-Down Modes, Internal Clock

determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets internal clock frequency to 225kHz. This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX1246/MAX1247 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

Power-Down Sequencing

The MAX1246/MAX1247 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 12, 13a, and 13b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples show two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 13a depicts the MAX1246 power consumption for one or four channel conversions utilizing full power-down mode and internal-reference compensation. A 0.047µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.9ms time constant. To achieve full 12-bit accuracy, 10 time constants or 9ms are required after power-up. Waiting this 9ms in FASTPD mode instead of in full power-up can reduce power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 14.

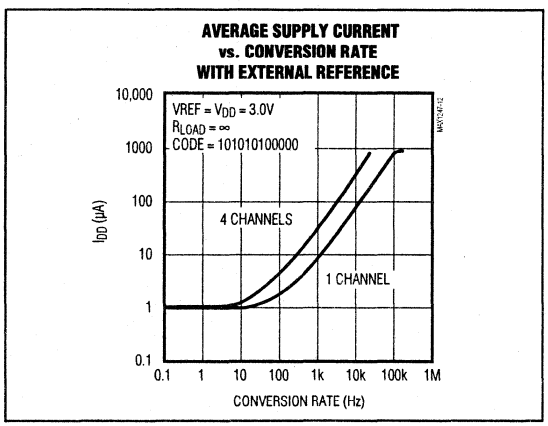

Figure 12. Average Supply Current vs. Conversion Rate with External Reference

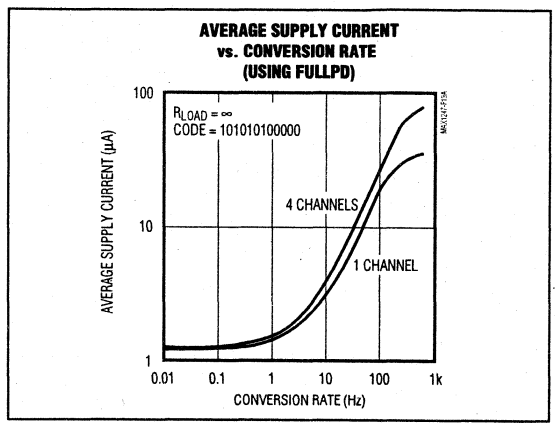

Figure 13a. MAX1246 Supply Current vs. Conversion Rate, FULLPD

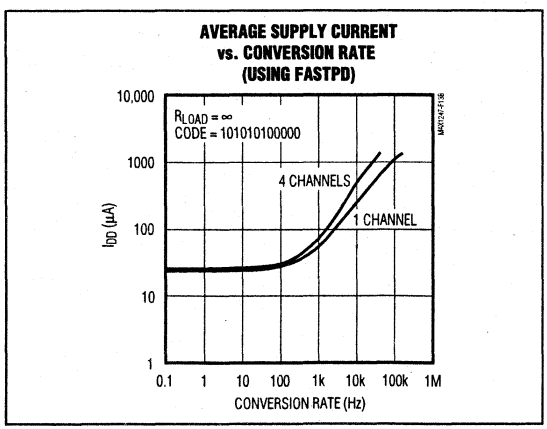

Figure 13b. MAX1246 Supply Current vs. Conversion Rate, FASTPD

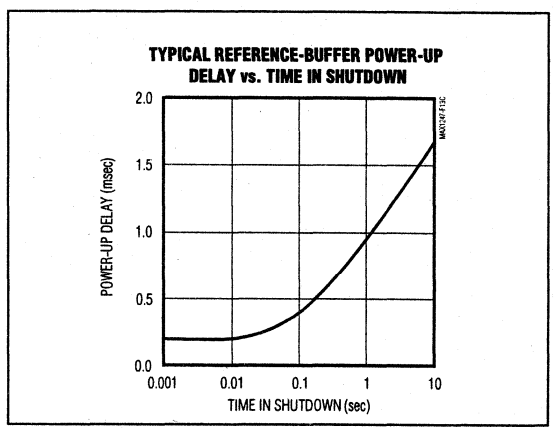

Figure 13c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

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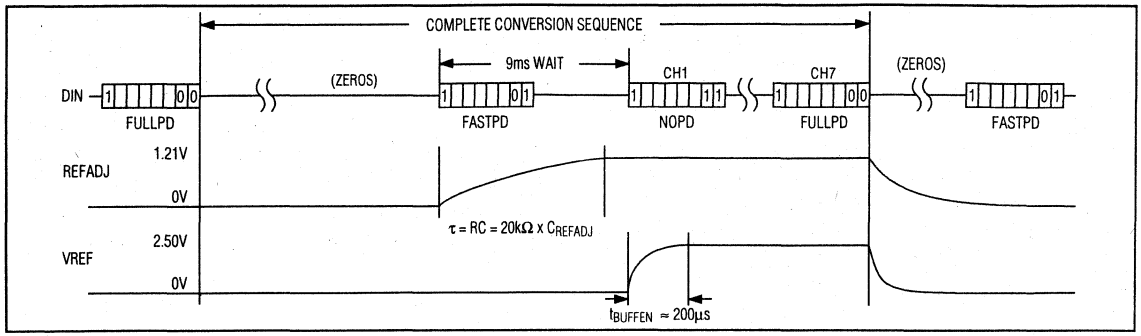


Figure 14. MAX1246 FULLPD/FASTPD Power-Up Sequence

Lowest Power at Higher Throughputs

Figure 13b shows the power consumption with external-reference compensation in fast power-down, with one and four channels converted. The external 4.7µF compensation requires a 200µs wait after power-up with one dummy conversion. This circuit combines fast multi-channel conversion with the lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX1246/MAX1247 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX1246 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX1247. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX1246 and the MAX1247. The MAX1246's internally trimmed 1.21V reference is buffered with a 2.06 gain. The MAX1247's REFADJ pin is also buffered with a 2.00 gain to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

Internal Reference (MAX1246)

The MAX1246's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipolar inputs. The internal reference voltage is adjustable to ±1.5% with the circuit in Figure 15.

External Reference

With both the MAX1246 and MAX1247, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX1246, and higher than 100kΩ for the MAX1247.

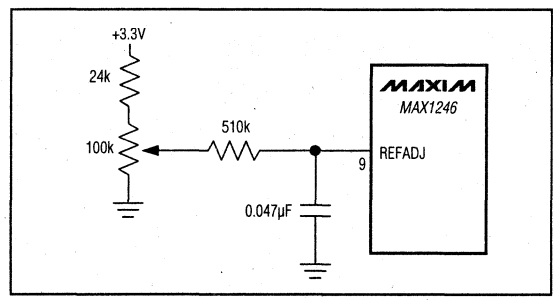


Figure 15. MAX1246 Reference-Adjust Circuit

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE MODE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hard-Wired Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

At VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350µA DC load current and have 10Ω or less output impedance. If the reference has a higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to AGND to minimize the input bias current in power-down.

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 4ppm/°C or less to achieve accuracy to within 1LSB over the 0°C to +70°C commercial temperature range.

Figure 16 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 17 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values. Output coding is binary, with 1LSB = 610µV (2.500V / 4096) for unipolar operation, and 1LSB = 610µV [(2.500V / 2 - -2.500V / 2) / 4096] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest-noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

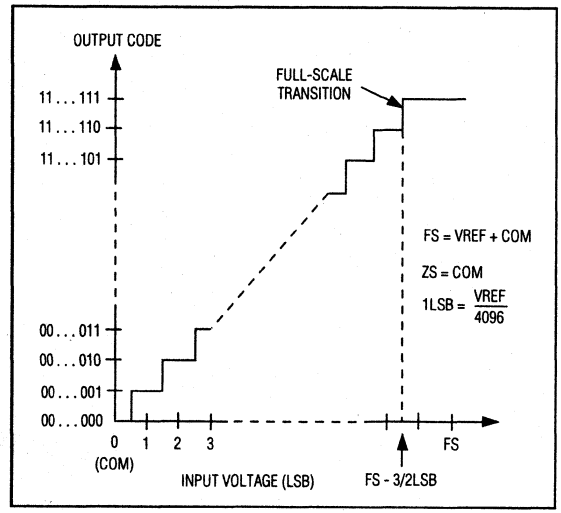


Figure 16. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 1 of the MAX1246/MAX1247. Minimize capacitor lead lengths for best supply-noise rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 18).

High-Speed Digital Interfacing with QSPI

The MAX1246/MAX1247 can interface with QSPI using the circuit in Figure 19 (f_{SCLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the four channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own microsequencer.

The MAX1246/MAX1247 are QSPI compatible up to its maximum external clock frequency of 2MHz.

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

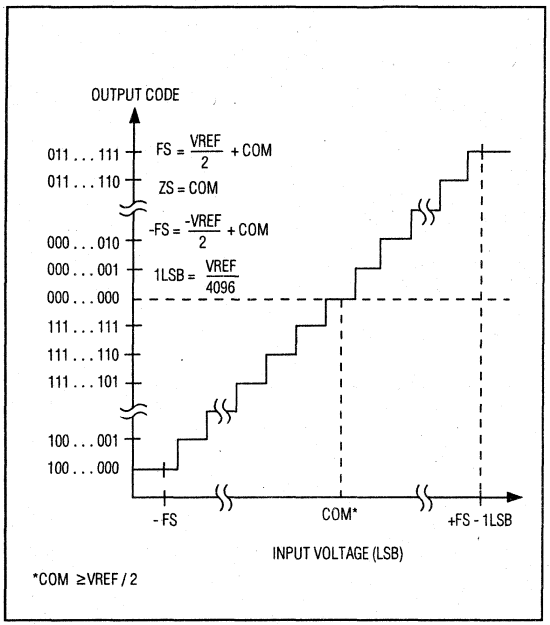


Figure 17. Bipolar Transfer Function, Full Scale (FS) = VREF / 2 + COM, Zero Scale (ZS) = COM

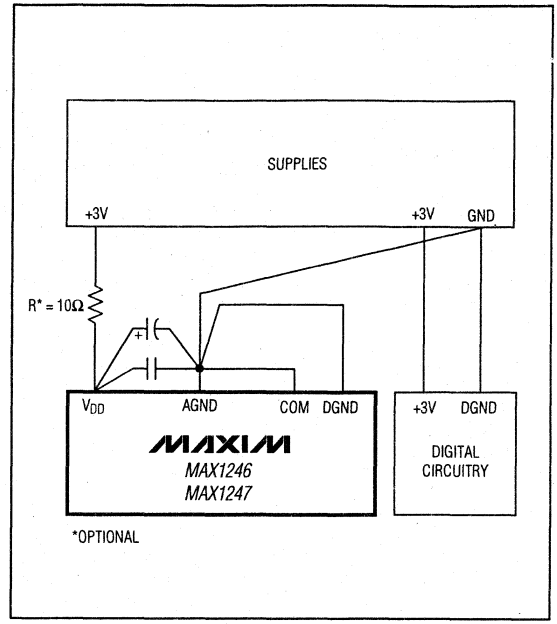


Figure 18. Power-Supply Grounding Connection

TMS320LC3x Interface

Figure 20 shows an application circuit to interface the MAX1246/MAX1247 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 21.

Use the following steps to initiate a conversion in the MAX1246/MAX1247 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1246/MAX1247's SCLK input.
2) The MAX1246/MAX1247's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port to enable data to be clocked into the MAX1246/MAX1247's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1246/MAX1247 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1246/MAX1247's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1246/MAX1247.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 12-bit conversion result followed by four trailing bits, which should be ignored.
6) Pull $\overline{CS}$ high to disable the MAX1246/MAX1247 until the next conversion is initiated.

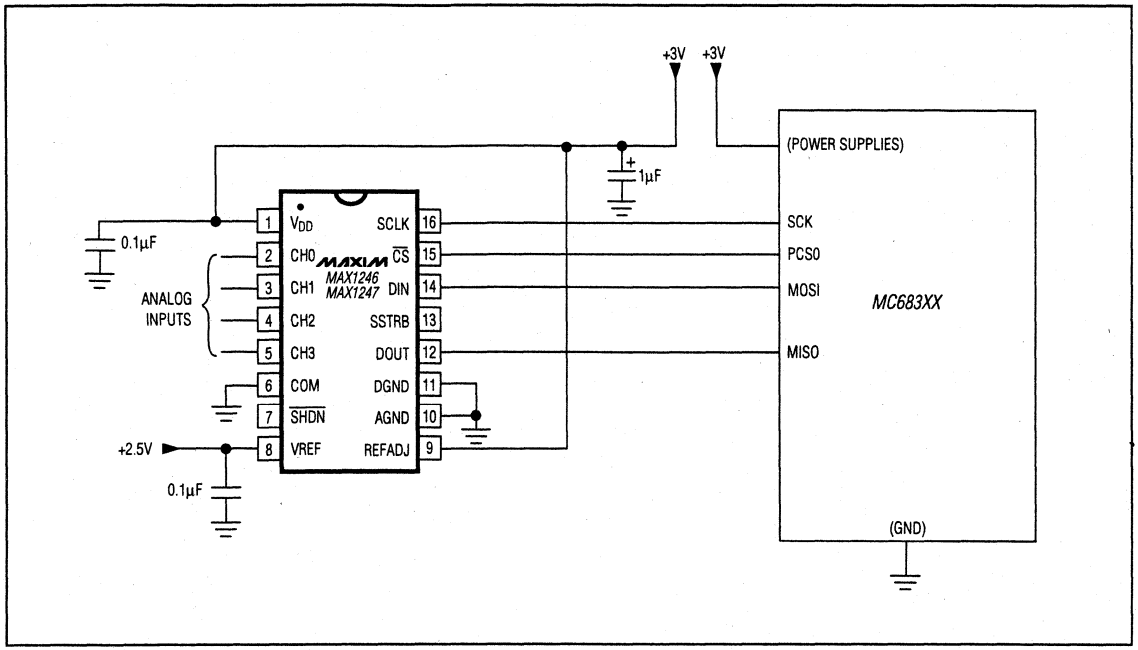


Figure 19. MAX1246/MAX1247 QSPI Connections, External Reference

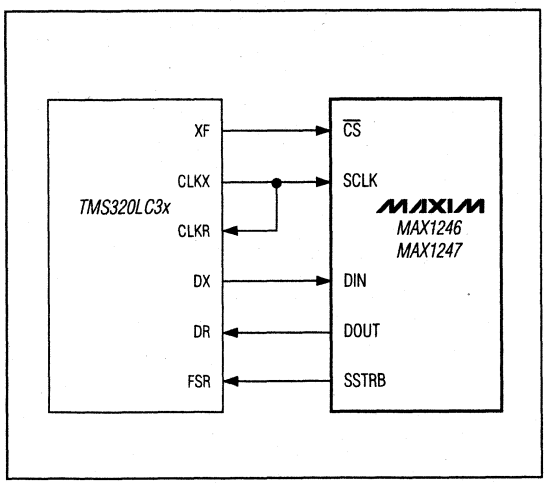


Figure 20. MAX1246/MAX1247-to-TMS320 Serial Interface

+2.7V, Low-Power, 4-Channel, Serial 12-Bit ADCs in QSOP-16

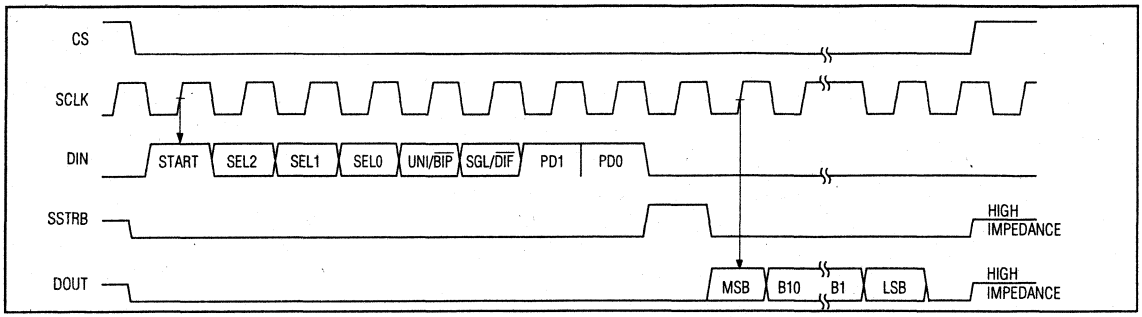


Figure 21. TMS320 Serial-Interface Timing Diagram

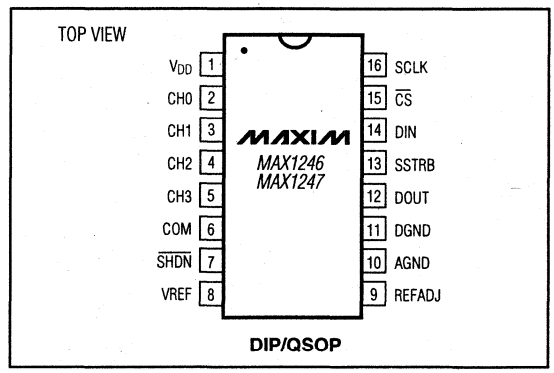
_Ordering Information (continued)

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1246AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1246BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1246AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1246BEEE	-40°C to +85°C	16 QSOP	±1
MAX1246AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1246BMJE	-55°C to +125°C	16 CERDIP*	±1
MAX1247ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1247BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX1247ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1247BCEE	0°C to +70°C	16 QSOP	±1
MAX1247AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1247BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1247AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1247BEEE	-40°C to +85°C	16 QSOP	±1
MAX1247AMJE	-55°C to +125°C	16 CERDIP*	±1/2
MAX1247BMJE	-55°C to +125°C	16 CERDIP*	±1

† *Contact factory for availability of alternate surface-mount packages.*

* *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

_Pin Configuration



_Chip Information

TRANSISTOR COUNT: 2554

19-1072; Rev 1; 6/97

MAXIM

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

General Description

The MAX1248/MAX1249 10-bit data-acquisition systems combine a 4-channel multiplexer, high-bandwidth track/hold, and serial interface with high conversion speed and low power consumption. They operate from a single +2.7V to +5.25V supply, and their analog inputs are software configurable for unipolar/bipolar and single-ended/differential operation.

The 4-wire serial interface connects directly to SPI™/QSPI™ and Microwire™ devices without external logic. A serial strobe output allows direct connection to TMS320-family digital signal processors. The MAX1248/MAX1249 use either the internal clock or an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

The MAX1248 has an internal 2.5V reference, while the MAX1249 requires an external reference. Both parts have a reference-buffer amplifier with a ±1.5% voltage adjustment range.

These devices provide a hard-wired $\overline{SHDN}$ pin and a software-selectable power-down, and can be programmed to automatically shut down at the end of a conversion. Accessing the serial interface automatically powers up the MAX1248/MAX1249, and the quick turn-on time allows them to be shut down between all conversions. This technique can cut supply current to under 60µA at reduced sampling rates.

The MAX1248/MAX1249 are available in a 16-pin DIP and a very small QSOP that occupies the same board area as an 8-pin SO.

For 8-channel versions of these devices, see the MAX148/MAX149 data sheet.

Applications

Portable Data Logging
Medical Instruments
Pen Digitizers
Data Acquisition
Battery-Powered Instruments
System Supervision

Pin Configuration appears at end of data sheet.

SPI and QSPI are registered trademarks of Motorola, Inc.
Microwire is a registered trademark of National Semiconductor Corp.

Features

- ♦ **4-Channel Single-Ended or 2-Channel Differential Inputs**
- ♦ **Single +2.7V to +5.25V Operation**
- ♦ **Internal 2.5V Reference (MAX1248)**
- ♦ **Low Power: 1.2mA (133ksps, +3V supply)**
  54µA (1ksps, +3V supply)
  1µA (power-down mode)
- ♦ **SPI/QSPI/Microwire/TMS320-Compatible 4-Wire Serial Interface**
- ♦ **Software-Configurable Unipolar or Bipolar Inputs**
- ♦ **16-Pin QSOP Package (same area as 8-pin SO)**

Ordering Information

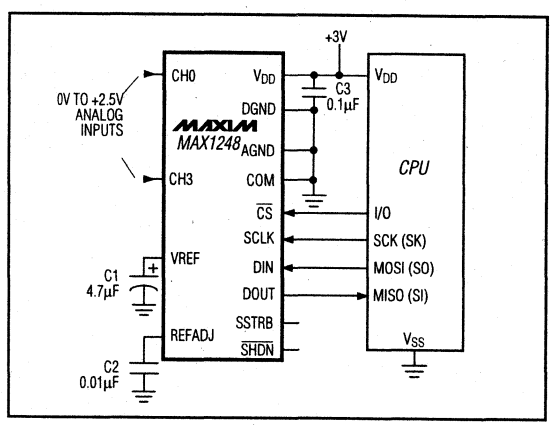
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1248ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1248BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX1248ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1248BCEE	0°C to +70°C	16 QSOP	±1

Ordering Information continued at end of data sheet.

† *Contact factory for availability of alternate surface-mount packages.*

7

Typical Operating Circuit



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+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND, DGND ..... -0.3V to +6V
AGND to DGND ..... -0.3V to +0.3V
CH0–CH3, COM to AGND, DGND ..... -0.3V to (V_{DD} + 0.3V)
VREF to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to +6V
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Output Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
QSOP (derate 8.30mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX1248_C_E/MAX1249_C_E ..... 0°C to +70°C
MAX1248_E_E/MAX1249_E_E ..... -40°C to +85°C
MAX1248_MJE/MAX1249_MJE ..... -55°C to +125°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution			10			Bits
Relative Accuracy (Note 2)	INL	MAX124_A			±0.5	LSB
		MAX124_B			±1.0	
Differential Nonlinearity	DNL	No missing codes over temperature			±1	LSB
Offset Error		MAX124_A			±1	LSB
		MAX124_B			±2	
Gain Error (Note 3)		MAX124_A			±1	LSB
		MAX124_B			±2	
Gain Temperature Coefficient				±0.25		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, 0V to 2.500Vp-p, 133ksps, 2.0MHz external clock, bipolar input mode)						
Signal-to-Noise + Distortion Ratio	SINAD			66		dB
Total Harmonic Distortion	THD	Up to the 5th harmonic		-70		dB
Spurious-Free Dynamic Range	SFDR			70		dB
Channel-to-Channel Crosstalk		65kHz, 2.500Vp-p (Note 4)		-75		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	Internal clock, $\overline{SHDN}$ = FLOAT	5.5		7.5	µs
		Internal clock, $\overline{SHDN}$ = V_{DD}	35		65	
		External clock = 2MHz, 12 clocks/conversion	6			
Track/Hold Acquisition Time	t_{ACQ}				1.5	µs
Aperture Delay				30		ns
Aperture Jitter				<50		ps
Internal Clock Frequency		$\overline{SHDN}$ = FLOAT		1.8		MHz
		$\overline{SHDN}$ = V_{DD}		0.225		
External Clock Frequency			0.1		2.0	MHz
		Data transfer only	0		2.0	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz; external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference, VREF = 2.500V applied to VREF pin; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG/COM INPUTS						
Input Voltage Range, Single-Ended and Differential (Note 6)		Unipolar, COM = 0V			0 to VREF	V
		Bipolar, COM = VREF / 2			±VREF / 2	
Multiplexer Leakage Current		On/off leakage current, $V_{CH_}$ = 0V or V_{DD}		±0.01	±1	µA
Input Capacitance				16		pF
INTERNAL REFERENCE (MAX1248 only, reference buffer enabled)						
VREF Output Voltage		T_A = +25°C (Note 7)	2.470	2.500	2.530	V
VREF Short-Circuit Current					30	mA
VREF Temperature Coefficient		MAX1248		±30		ppm/°C
Load Regulation (Note 8)		0mA to 0.2mA output load		0.35		mV
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Capacitive Bypass at REFADJ			0.01			µF
REFADJ Adjustment Range				±1.5		%
EXTERNAL REFERENCE AT VREF (Buffer disabled)						
VREF Input Voltage Range (Note 9)			1.0		V_{DD} + 50mV	V
VREF Input Current		VREF = 2.500V		100	150	µA
VREF Input Resistance			18	25		kΩ
Shutdown VREF Input Current				0.01	10	µA
REFADJ Buffer-Disable Threshold			V_{DD} - 0.5			V
EXTERNAL REFERENCE AT REFADJ						
Capacitive Bypass at VREF		Internal compensation mode	0			µF
		External compensation mode	4.7			
Reference-Buffer Gain		MAX1248		2.06		V/V
		MAX1249		2.00		
REFADJ Input Current		MAX1248			±50	µA
		MAX1249			±10	
DIGITAL INPUTS (DIN, SCLK, $\overline{CS}$, $\overline{SHDN}$)						
DIN, SCLK, $\overline{CS}$ Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$	2.0			V
		$V_{DD} > 3.6V$	3.0			
DIN, SCLK, $\overline{CS}$ Input Low Voltage	V_{IL}				0.8	V
DIN, SCLK, $\overline{CS}$ Input Hysteresis	V_{HYST}			0.2		V
DIN, SCLK, $\overline{CS}$ Input Leakage	I_{IN}	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
DIN, SCLK, $\overline{CS}$ Input Capacitance	C_{IN}	(Note 10)			15	pF
$\overline{SHDN}$ Input High Voltage	V_{SH}		V_{DD} - 0.4			V
$\overline{SHDN}$ Input Mid Voltage	V_{SM}		1.1		V_{DD} - 1.1	V
$\overline{SHDN}$ Input Low Voltage	V_{SL}				0.4	V
$\overline{SHDN}$ Input Current	I_S	$\overline{SHDN}$ = 0V or V_{DD}			±4.0	µA

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V; COM = 0V; f_{SCLK} = 2.0MHz, external clock (50% duty cycle); 15 clocks/conversion cycle (133ksps); MAX1248—4.7µF capacitor at VREF pin; MAX1249—external reference; VREF = 2.500V applied to VREF pin, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Voltage, Floating	V_{FLT}	$\overline{SHDN}$ = FLOAT			V_{DD} / 2		V
$\overline{SHDN}$ Maximum Allowed Leakage, Mid Input		$\overline{SHDN}$ = FLOAT				±100	nA
DIGITAL OUTPUTS (DOUT, SSTRB)							
Output Voltage Low	V_{OL}	I_{SINK} = 5mA				0.4	V
		I_{SINK} = 16mA				0.8	
Output Voltage High	V_{OH}	I_{SOURCE} = 0.5mA		V_{DD} - 0.5			V
Three-State Leakage Current	I_L	$\overline{CS}$ = V_{DD}			±0.01	±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$ = V_{DD} (Note 10)				15	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}			2.70		5.25	V
Positive Supply Current	I_{DD}	Operating mode, full-scale input (Note 11)	V_{DD} = 5.25V		1.6	3.0	mA
			V_{DD} = 3.6V		1.2	2.0	
		Full power-down	V_{DD} = 5.25V		3.5	15	µA
			V_{DD} = 3.6V		1.2	10	
	I_{DD}	Fast power-down (MAX1248)			30	70	
Supply Rejection (Note 12)	PSR	V_{DD} = 2.7V to 5.25V, full-scale input, external reference = 2.500V			±0.3		mV

TIMING CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Acquisition Time	t_{ACQ}			1.5			µs
DIN to SCLK Setup	t_{DS}			100			ns
DIN to SCLK Hold	t_{DH}					0	ns
SCLK Fall to Output Data Valid	t_{DO}	Figure 1	MAX124__C/E	20		200	ns
			MAX124__M	20		240	
$\overline{CS}$ Fall to Output Enable	t_{DV}	Figure 1				240	ns
$\overline{CS}$ Rise to Output Disable	t_{TR}	Figure 2				240	ns
$\overline{CS}$ to SCLK Rise Setup	t_{CSS}			100			ns
$\overline{CS}$ to SCLK Rise Hold	t_{CSH}			0			ns
SCLK Pulse Width High	t_{CH}			200			ns
SCLK Pulse Width Low	t_{CL}			200			ns
SCLK Fall to SSTRB	t_{SSTRB}	Figure 1				240	ns
$\overline{CS}$ Fall to SSTRB Output Enable	t_{SDV}	External clock mode only, Figure 1				240	ns
$\overline{CS}$ Rise to SSTRB Output Disable	t_{STR}	External clock mode only, Figure 2				240	ns
SSTRB Rise to SCLK Rise	t_{SCK}	Internal clock mode only (Note 10)		0			ns

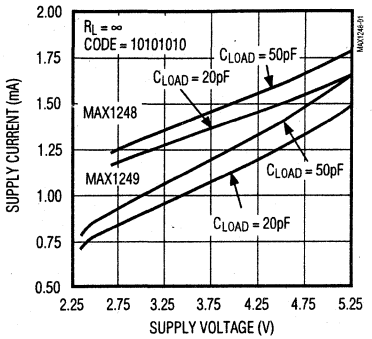
Note 1: Tested at V_{DD} = 2.7V; COM = 0V; unipolar single-ended input mode.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.
Note 3: MAX1248—internal reference, offset nulled; MAX1249—external reference (VREF = +2.500V), offset nulled.
Note 4: Ground "on" channel; sine wave applied to all "off" channels.
Note 5: Conversion time defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from AGND to V_{DD}.
Note 7 Sample tested to 0.1% AQL.
Note 8: External load should not change during conversion for specified accuracy.
Note 9: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 10 Guaranteed by design. Not subject to production testing.
Note 11: The MAX1249 typically draws 400µA less than the values shown.
Note 12: Measured as $|V_{FS}(2.7V) - V_{FS}(5.25V)|$.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

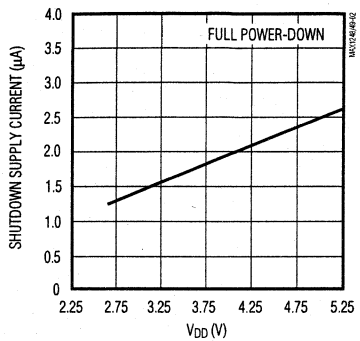
Typical Operating Characteristics

(V_{DD} = 3.0V, VREF = 2.500V, f_{SCLK} = 2.0MHz, C_{LOAD} = 20pF, T_A = +25°C, unless otherwise noted.)

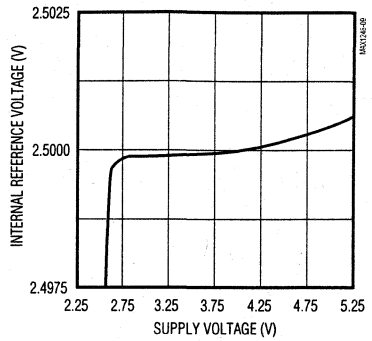
SUPPLY CURRENT vs. SUPPLY VOLTAGE



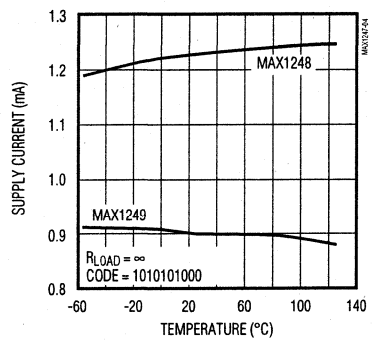
SHUTDOWN SUPPLY CURRENT vs. SUPPLY VOLTAGE



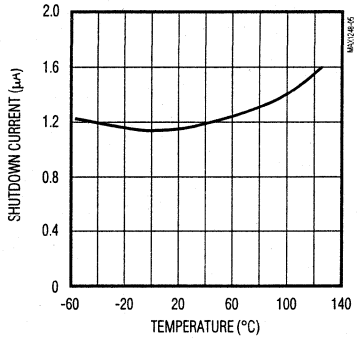
INTERNAL REFERENCE VOLTAGE vs. SUPPLY VOLTAGE



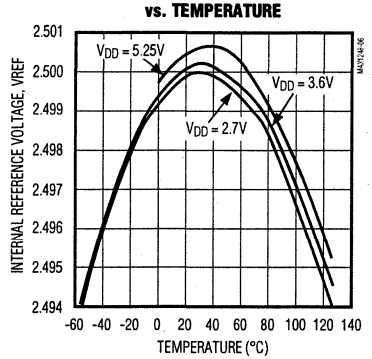
SUPPLY CURRENT vs. TEMPERATURE



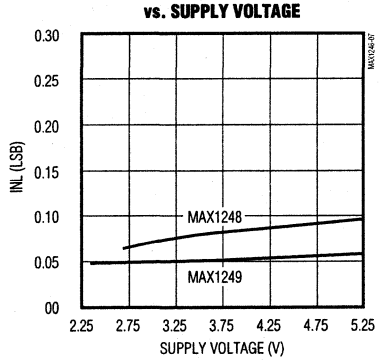
SHUTDOWN CURRENT vs. TEMPERATURE



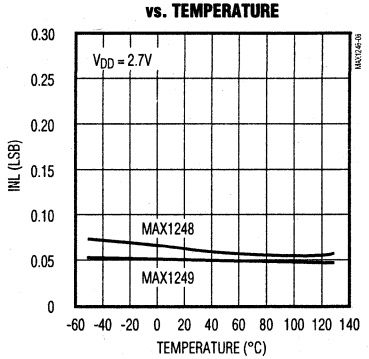
INTERNAL REFERENCE VOLTAGE vs. TEMPERATURE



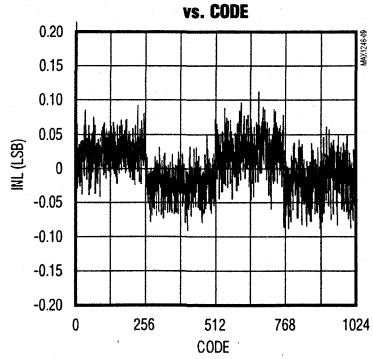
INTERGRAL NONLINEARITY vs. SUPPLY VOLTAGE



INTEGRAL NONLINEARITY vs. TEMPERATURE



INTEGRAL NONLINEARITY vs. CODE



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage
2–5	CH0–CH3	Sampling Analog Inputs
6	COM	Ground reference for analog inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB.
7	$\overline{SHDN}$	Three-Level Shutdown Input. Pulling $\overline{SHDN}$ low shuts the MAX1248/MAX1249 down; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high puts the reference-buffer amplifier in internal compensation mode. Letting $\overline{SHDN}$ float puts the reference-buffer amplifier in external compensation mode.
8	VREF	Reference-Buffer Output/ADC Reference Input. Reference voltage for analog-to-digital conversion. In internal reference mode (MAX1248 only), the reference buffer provides a 2.500V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
9	REFADJ	Input to the Reference-Buffer Amplifier. To disable the reference-buffer amplifier, tie REFADJ to V_{DD}.
10	AGND	Analog Ground
11	DGND	Digital Ground
12	DOUT	Serial Data Output. Data is clocked out at SCLK's falling edge. High impedance when $\overline{CS}$ is high.
13	SSTRB	Serial Strobe Output. In internal clock mode, SSTRB goes low when the MAX1248/MAX1249 begin the A/D conversion and goes high when the conversion is completed. In external clock mode, SSTRB pulses high for one clock period before the MSB decision. High impedance when $\overline{CS}$ is high (external clock mode).
14	DIN	Serial Data Input. Data is clocked in at SCLK's rising edge.
15	$\overline{CS}$	Active-Low Chip Select. Data will not be clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance.
16	SCLK	Serial Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed. (Duty cycle must be 40% to 60%.)

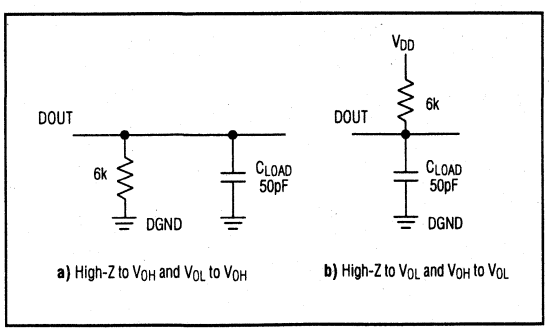


Figure 1. Load Circuits for Enable Time

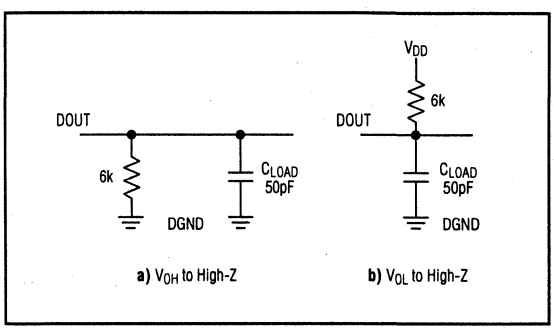


Figure 2. Load Circuits for Disable Time

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

Detailed Description

The MAX1248/MAX1249 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to a 10-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 is a block diagram of the MAX1248/MAX1249.

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit (Figure 4). In single-ended mode, IN+ is internally switched to CH0–CH3, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from two pairs: CH0/CH1 and CH2/CH3. Configure the channels with Tables 2 and 3. Please note that the codes for CH0–CH3 in the MAX1248/MAX1249 correspond to the codes for CH2–CH5 in the eight-channel (MAX148/MAX149) versions.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans three SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the comparator's input. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 10-bit resolution. This action is equivalent to transferring a charge of 16pF x $[(V_{IN+}) - (V_{IN-})]$ from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold

The T/H enters its tracking mode on the falling clock edge after the fifth bit of the 8-bit control word has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control word has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input. If the converter is set up for differential inputs, IN- connects to the "-" input, and the difference of |IN+ - IN-| is sampled. At the end of the conversion, the positive input connects back to IN+, and C_{HOLD} charges to the input signal.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high,

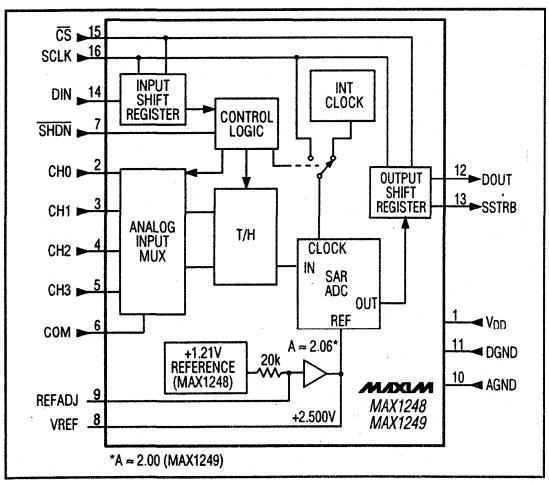


Figure 3. Block Diagram

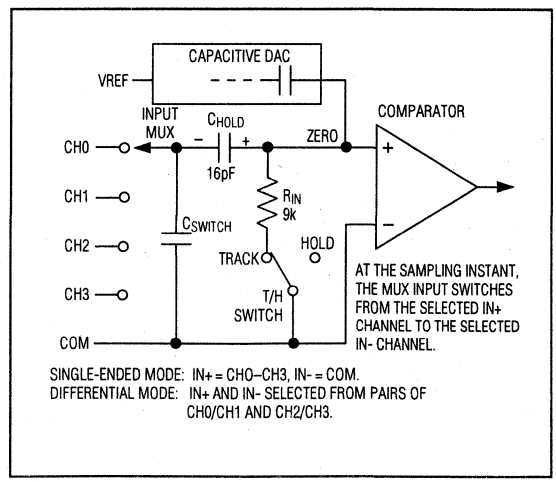


Figure 4. Equivalent Input Circuit

Table 1. Control-Byte Format

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
START	SEL2	SEL1	SEL0	UNI/$\overline{BIP}$	SGL/$\overline{DIF}$	PD1	PD0

BIT	NAME	DESCRIPTION		
7(MSB)	START	The first logic "1" bit after $\overline{CS}$ goes low defines the beginning of the control byte.		
6 5 4	SEL2 SEL1 SEL0	These three bits select which of the four channels are used for the conversion (Tables 2 and 3).		
3	UNI/$\overline{BIP}$	1 = unipolar, 0 = bipolar. Selects unipolar or bipolar conversion mode. In unipolar mode, an analog input signal from 0V to VREF can be converted; in bipolar mode, the signal can range from -VREF / 2 to +VREF / 2.		
2	SGL/$\overline{DIF}$	1 = single ended, 0 = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured (Tables 2 and 3).		
1 0(LSB)	PD1 PD0	Selects clock and power-down modes. PD1 0 0 1 1	 PD0 0 1 0 1	 Mode Full power-down Fast power-down (MAX1248 only) Internal clock mode External clock mode

the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 7.6 \times (R_S + R_{IN}) \times 16pF$$

where R_{IN} = 9kΩ, R_S = the source impedance of the input signal, and t_{ACQ} is never less than 1.5µs. Note that source impedances below 3kΩ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's signal bandwidth.

Input Bandwidth

The ADC's input tracking circuitry has a 2.25MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and AGND, allow the channel input pins to swing from AGND - 0.3V to V_{DD} + 0.3V without damage. However, for accurate conversions near full scale, the inputs must not exceed V_{DD} by more than 50mV or be lower than AGND by 50mV.

If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 4mA.

How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1248/MAX1249's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit defines the control byte's MSB. Until this first "start" bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 1 shows the control-byte format.

The MAX1248/MAX1249 are compatible with SPI/QSPI and Microwire devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the *Typical Operating Circuit,* the simplest soft-

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Table 2. Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3	COM
0	0	1	+				–
1	0	1		+			–
0	1	0			+		–
1	1	0				+	–

Table 3. Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

SEL2	SEL1	SEL0	CH0	CH1	CH2	CH3
0	0	1	+	–		
0	1	0			+	–
1	0	1	–	+		
1	1	0			–	+

ware interface requires only three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the 10-bit conversion result). See Figure 19 for MAX1248/MAX1249 QSPI connections.

Simple Software Interface

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 100kHz to 2MHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format: 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 5 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with one leading zero and three trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. To avoid excessive T/H droop, make sure the total conversion time does not exceed 120µs.

Digital Output

In unipolar input mode, the output is straight binary (Figure 16). For bipolar inputs, the output is two's complement (Figure 17). Data is clocked out at the falling edge of SCLK in MSB-first format.

Clock Modes

The MAX1248/MAX1249 may use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the MAX1248/MAX1249. The T/H acquires the input signal as the last three bits of the control byte are clocked into DIN. Bits PD1 and PD0 of the control byte program the clock mode. Figures 6–9 show the timing characteristics common to both modes.

External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for one clock period after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next 10 SCLK falling edges (Figure 5). SSTRB and DOUT go into a high-impedance state when

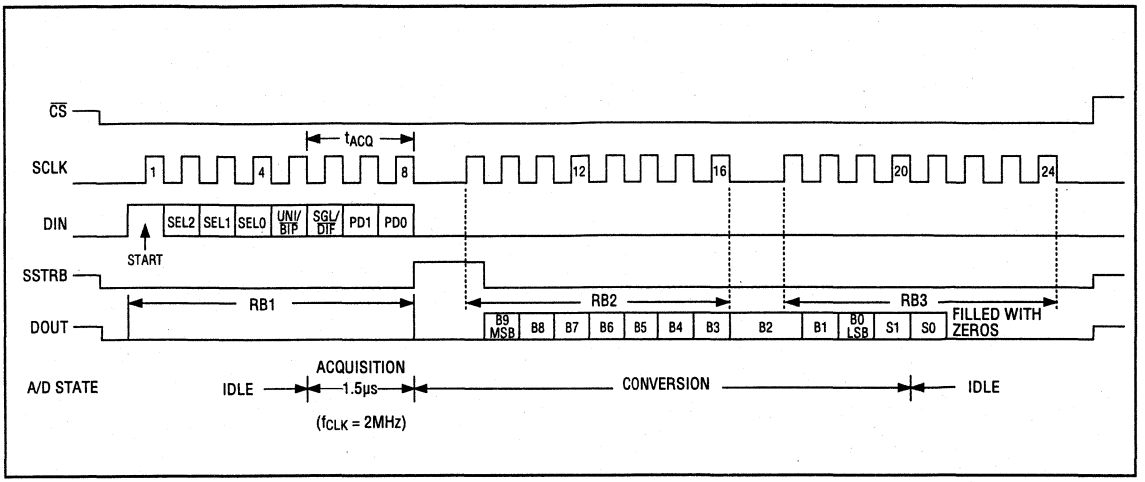

Figure 5. 24-Clock External Clock Mode Conversion Timing (Microwire and SPI Compatible, QSPI Compatible with $f_{SCLK} \leq$ 2MHz)

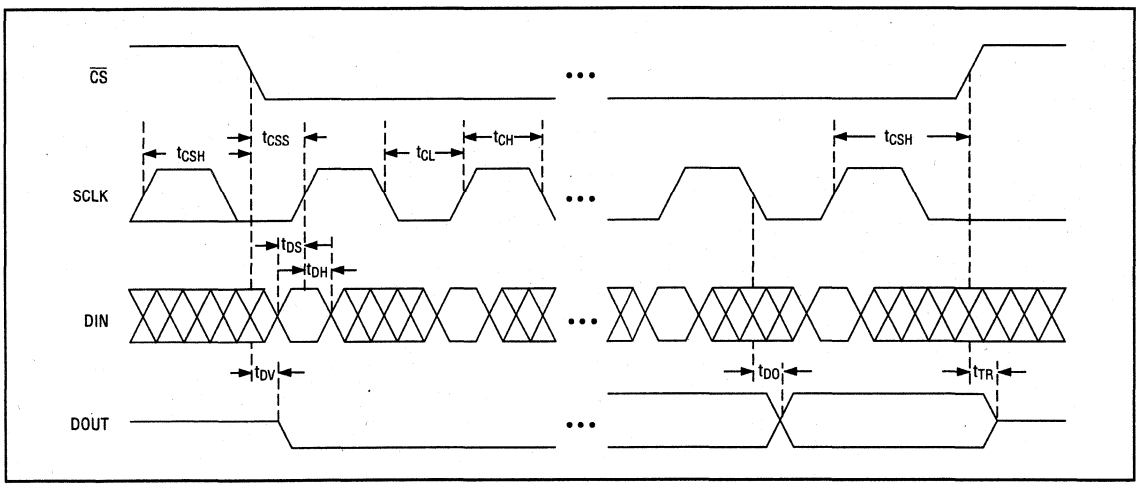

Figure 6. Detailed Serial-Interface Timing

$\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB will output a logic low. Figure 7 shows the SSTRB timing in external clock mode.

The conversion must complete in some minimum time, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 100kHz, or if serial-clock interruptions could cause the conversion interval to exceed 120µs.

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

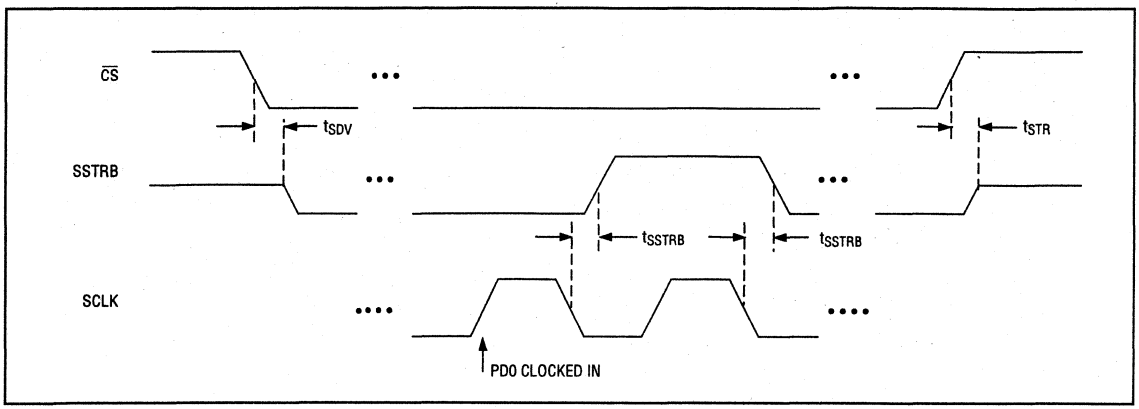

Figure 7. External Clock Mode SSTRB Detailed Timing

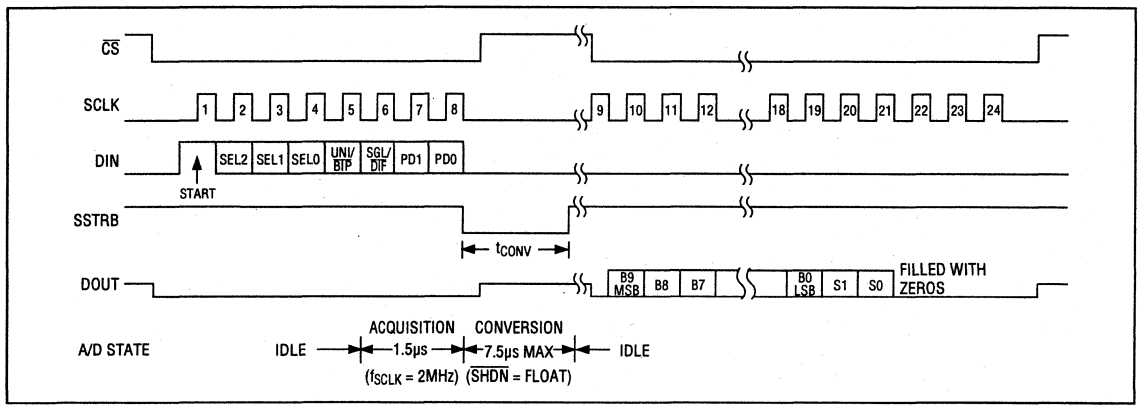

Figure 8. Internal Clock Mode Timing

Internal Clock

In internal clock mode, the MAX1248/MAX1249 generate their own conversion clocks internally. This frees the µP from the burden of running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0MHz to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for a maximum of 7.5µs ($\overline{SHDN}$ = FLOAT), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 8). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1248/MAX1249 and three-states DOUT, but it does not adversely affect an internal clock mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 9 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1248/MAX1249 at clock rates exceeding 2.0MHz if the minimum acquisition time, t_{ACQ}, is kept above 1.5µs.

Data Framing

The falling edge of $\overline{CS}$ does **not** start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle; e.g., after V_{DD} is applied.

OR

The first high bit clocked into DIN after bit 3 of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1248/MAX1249 can run with $\overline{CS}$ held low between conversions is 15 clocks per conversion. Figure 10a shows the serial-interface timing necessary to perform a conversion every 15 SCLK cycles in external clock mode. If $\overline{CS}$ is tied low and SCLK is continuous, guarantee a start bit by first clocking in 16 zeros.

Most microcontrollers require that conversions occur in multiples of 8 SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1248/MAX1249. Figure 10b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

Applications Information

Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1248/MAX1249 in internal clock mode, ready to convert with SSTRB = high. After the power supplies have stabilized, the internal reset time is 10µs, and no conversions should be performed during this phase. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros (also see Table 4).

Reference-Buffer Compensation

In addition to its shutdown function, $\overline{SHDN}$ selects internal or external compensation. The compensation affects both power-up time and maximum conversion speed. The 100kHz minimum clock rate is limited by droop on the sample-and-hold, and is independent of the compensation used.

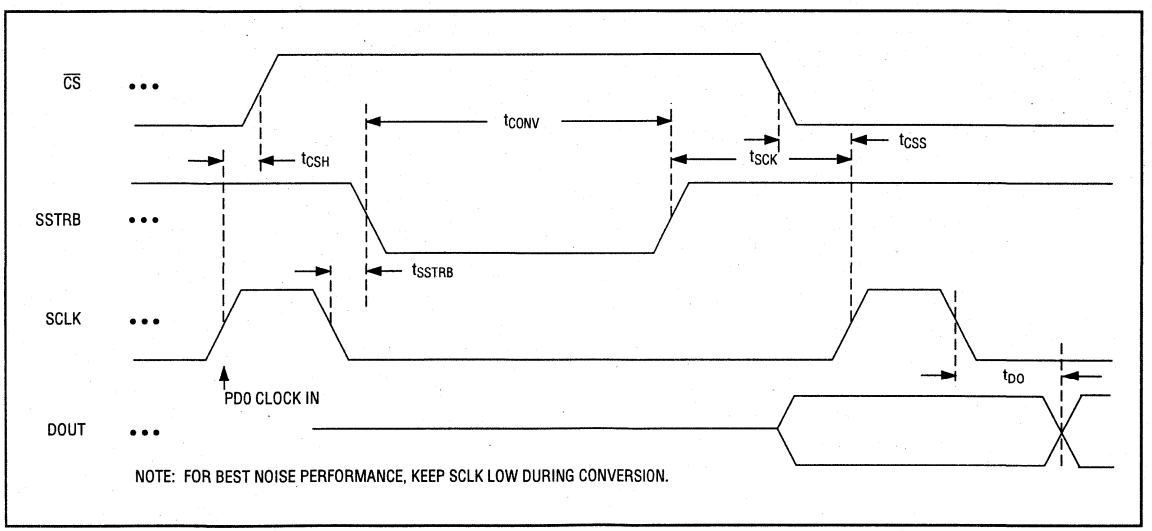

Figure 9. Internal Clock Mode SSTRB Detailed Timing

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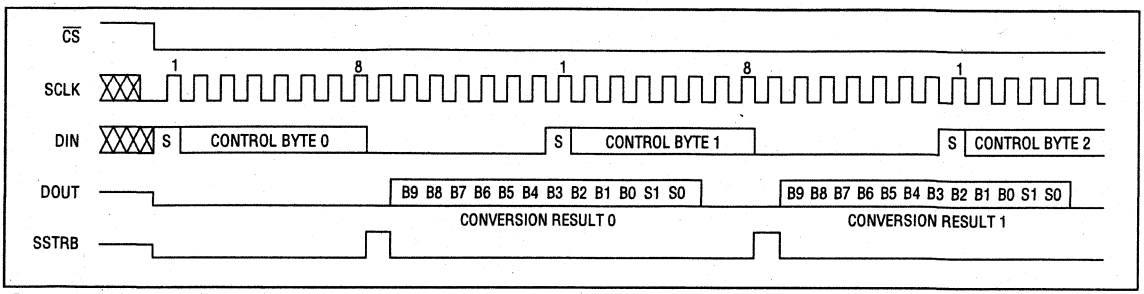


Figure 10a. External Clock Mode, 15 Clocks/Conversion Timing

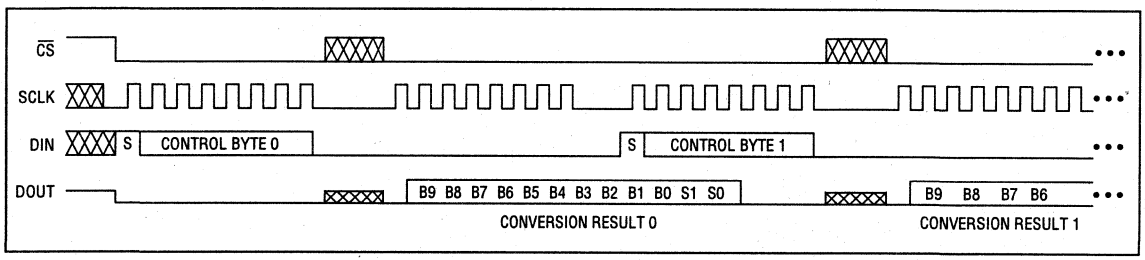


Figure 10b. External Clock Mode, 16 Clocks/Conversion Timing

Float $\overline{SHDN}$ to select external compensation. The *Typical Operating Circuit* uses a 4.7µF capacitor at VREF. A value of 4.7µF or greater ensures reference-buffer stability and allows converter operation at the 2MHz full clock speed. External compensation increases power-up time (see *Choosing Power-Down Mode* and Table 4).

Pull $\overline{SHDN}$ high to select internal compensation. Internal compensation requires no external capacitor at VREF and allows for the shortest power-up times. The maximum clock rate is 2MHz in internal clock mode and 400kHz in external clock mode.

Choosing Power-Down Mode

You can save power by placing the converter in a low-current shutdown state between conversions. Select full power-down or fast power-down mode via bits 1 and 0 of the DIN control byte with $\overline{SHDN}$ high or floating (Tables 1 and 5). In both software power-down modes, the serial interface remains operational, but the ADC does not convert. Pull $\overline{SHDN}$ low at any time to shut down the converter completely. $\overline{SHDN}$ overrides bits 1 and 0 of the control byte.

Full power-down mode turns off all chip functions that draw quiescent current, reducing supply current typically to 2µA. Fast power-down mode turns off all circuitry except the bandgap reference. With fast power-down mode, the supply current is 30µA. Power-up time can be shortened to 5µs in internal compensation mode.

Table 4 shows how the choice of reference-buffer compensation and power-down mode affects both power-up delay and maximum sample rate. In external compensation mode, power-up time is 20ms with a 4.7µF compensation capacitor when the capacitor is initially fully discharged. From fast power-down, start-up time can be eliminated by using low-leakage capacitors that do not discharge more than 1/2LSB while shut down. In power-down, leakage currents at VREF cause droop on the reference bypass capacitor. Figures 11a and 11b show the various power-down sequences in both external and internal clock modes.

Table 4. Typical Power-Up Delay Times

REFERENCE BUFFER	REFERENCE-BUFFER COMPENSATION MODE	VREF CAPACITOR (µF)	POWER-DOWN MODE	POWER-UP DELAY (µs)	MAXIMUM SAMPLING RATE (ksps)
Enabled	Internal	—	Fast	5	26
Enabled	Internal	—	Full	300	26
Enabled	External	4.7	Fast	See Figure 13c	133
Enabled	External	4.7	Full	See Figure 13c	133
Disabled	—	—	Fast	2	133
Disabled	—	—	Full	2	133

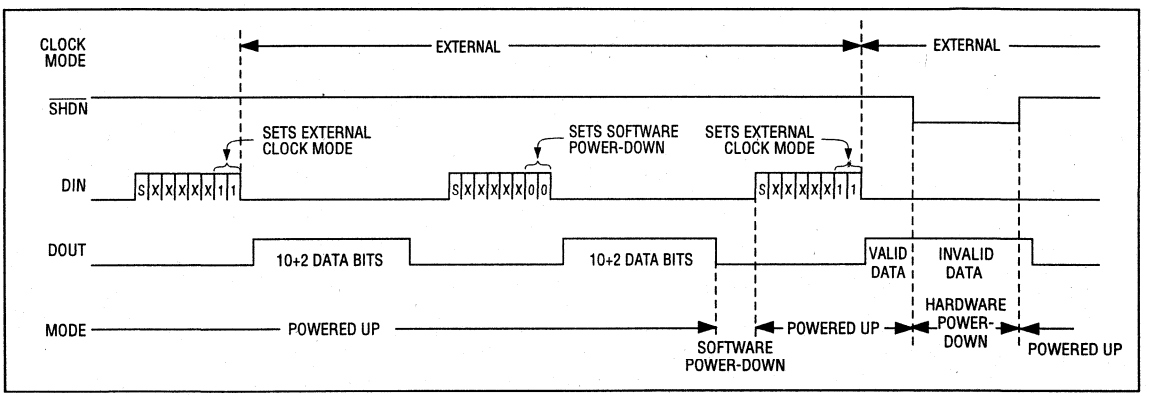


Figure 11a. Timing Diagram Power-Down Modes, External Clock

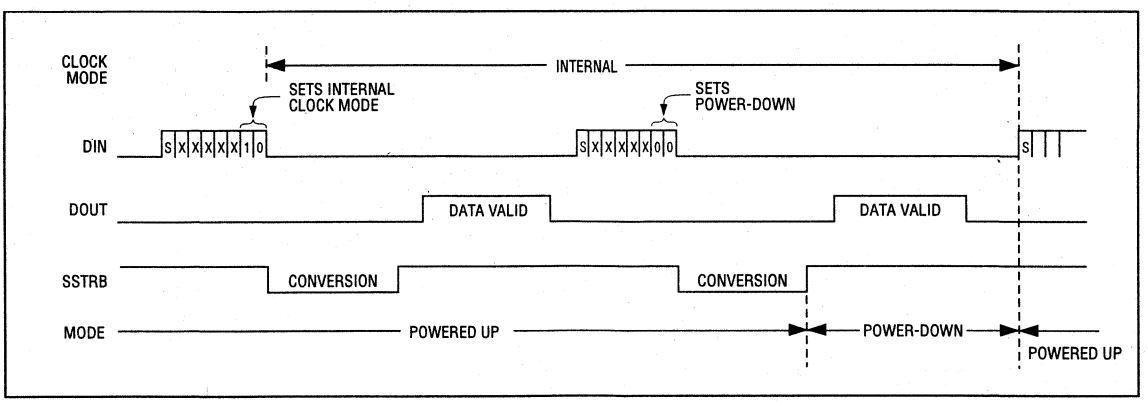


Figure 11b. Timing Diagram Power-Down Modes, Internal Clock

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

Table 5. Software Power-Down and Clock Mode

PD1	PD0	DEVICE
0	0	Full Power-Down
0	1	Fast Power-Down
1	0	Internal Clock
1	1	External Clock

Table 6. Hardware Power-Down and Internal Clock Frequency

$\overline{SHDN}$ STATE	DEVICE MODE	REFERENCE-BUFFER COMPENSATION	INTERNAL CLOCK FREQUENCY
1	Enabled	Internal	225kHz
Floating	Enabled	External	1.8MHz
0	Power-Down	N/A	N/A

Software Power-Down

Software power-down is activated using bits PD1 and PD0 of the control byte. As shown in Table 5, PD1 and PD0 also specify the clock mode. When software shutdown is asserted, the ADC operates in the last specified clock mode until the conversion is complete. Then the ADC powers down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1248/MAX1249 enter a software power-down.

The first logical 1 on DIN is interpreted as a start bit and powers up the MAX1248/MAX1249. Following the start bit, the data input word or control byte also determines clock mode and power-down states. For example, if the DIN word contains PD1 = 1, then the chip remains powered up. If PD0 = PD1 = 0, a power-down resumes after one conversion.

Hardware Power-Down

Pulling $\overline{SHDN}$ low places the converter in hardware power-down (Table 6). Unlike software power-down mode, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the clock frequency in internal clock mode. Letting $\overline{SHDN}$ float sets the internal clock frequency to 1.8MHz. When returning to normal operation with $\overline{SHDN}$ floating, there is a t_{RC} delay of approximately 2MΩ x C_L, where C_L is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high sets the internal clock frequency to 225kHz.

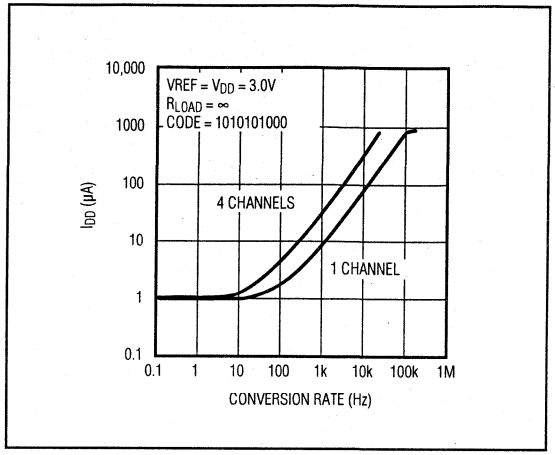


Figure 12. Average Supply Current vs. Conversion Rate with External Reference

This feature eases the settling-time requirement for the reference voltage. With an external reference, the MAX1248/MAX1249 can be considered fully powered up within 2µs of actively pulling $\overline{SHDN}$ high.

Power-Down Sequencing

The MAX1248/MAX1249 auto power-down modes can save considerable power when operating at less than maximum sample rates. Figures 12, 13a, and 13b show the average supply current as a function of the sampling rate. The following discussion illustrates the various power-down sequences.

Lowest Power at up to 500 Conversions/Channel/Second

The following examples illustrate two different power-down sequences. Other combinations of clock rates, compensation modes, and power-down modes may give lowest power consumption in other applications.

Figure 13a depicts the MAX1248 power consumption for one or eight channel conversions, utilizing full power-down mode and internal-reference compensation. A 0.01µF bypass capacitor at REFADJ forms an RC filter with the internal 20kΩ reference resistor with a 0.2ms time constant. To achieve full 10-bit accuracy, 8 time constants or 1.6ms are required after power-up. Waiting 1.6ms in FASTPD mode instead of in full power-up can reduce the power consumption by a factor of 10 or more. This is achieved by using the sequence shown in Figure 14.

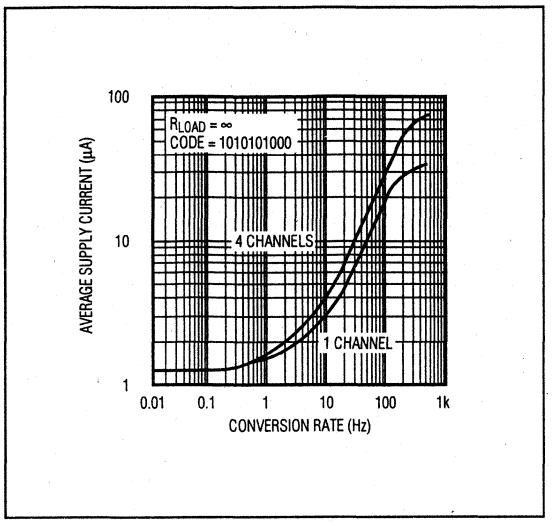


Figure 13a. MAX1248 Supply Current vs. Conversion Rate, FULLPD

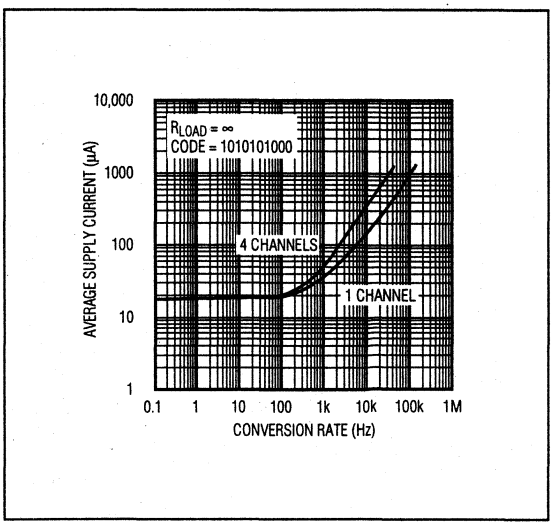


Figure 13b. MAX1248 Supply Current vs. Conversion Rate, FASTPD

Lowest Power at Higher Throughputs

Figure 13b shows the power consumption with external-reference compensation in fast power-down, with one and four channels converted. The external 4.7µF compensation requires a 75µs wait after power-up with one dummy conversion. This circuit combines fast multi-channel conversion with lowest power consumption possible. Full power-down mode may provide increased power savings in applications where the MAX1248/MAX1249 are inactive for long periods of time, but where intermittent bursts of high-speed conversions are required.

Internal and External References

The MAX1248 can be used with an internal or external reference voltage, whereas an external reference is required for the MAX1249. An external reference can be connected directly at VREF or at the REFADJ pin.

An internal buffer is designed to provide 2.5V at VREF for both the MAX1248 and the MAX1249. The MAX1248's internally trimmed 1.21V reference is buffered with a gain of 2.06. The MAX1249's REFADJ pin is also buffered with a gain of 2.06 to scale an external 1.25V reference at REFADJ to 2.5V at VREF.

Internal Reference (MAX1248)

The MAX1248's full-scale range with the internal reference is 2.5V with unipolar inputs and ±1.25V with bipo-

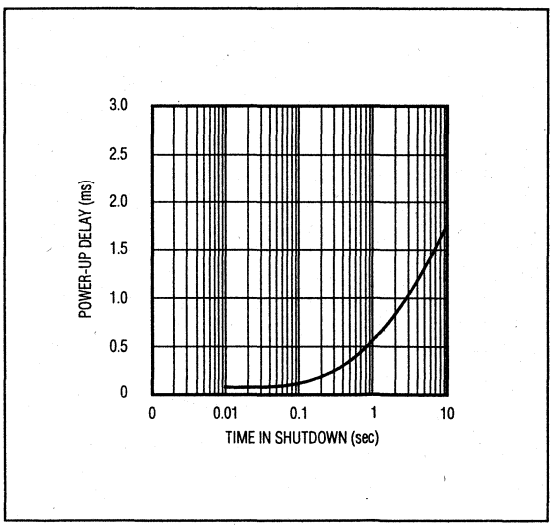


Figure 13c. Typical Reference-Buffer Power-Up Delay vs. Time in Shutdown

7

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

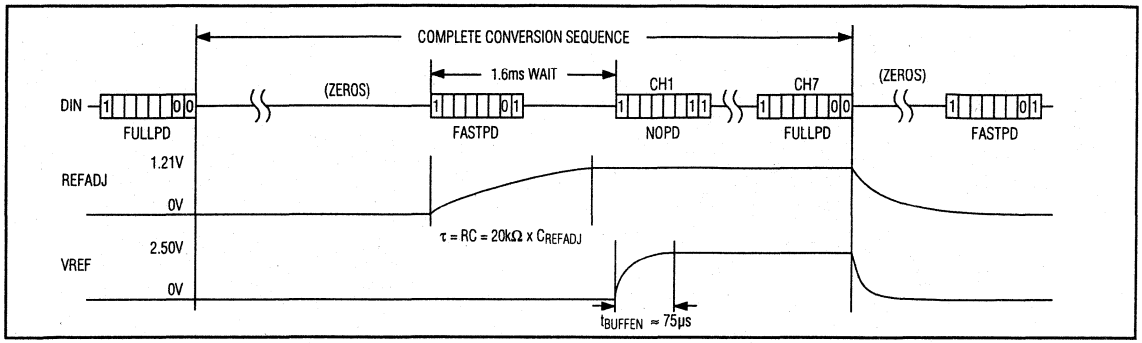


Figure 14. MAX1248 FULLPD/FASTPD Power-Up Sequence

lar inputs. The internal-reference voltage is adjustable to ±1.5% with the circuit of Figure 15.

External Reference

With both the MAX1248 and MAX1249, an external reference can be placed at either the input (REFADJ) or the output (VREF) of the internal reference-buffer amplifier. The REFADJ input impedance is typically 20kΩ for the MAX1248 and higher than 100kΩ for the MAX1249, where the internal reference is omitted. At VREF, the DC input resistance is a minimum of 18kΩ. During conversion, an external reference at VREF must deliver up to 350µA DC load current and have an output impedance of 10Ω or less. If the reference has higher output impedance or is noisy, bypass it close to the VREF pin with a 4.7µF capacitor.

Using the REFADJ input makes buffering the external reference unnecessary. To use the direct VREF input, disable the internal buffer by tying REFADJ to V_{DD}. In power-down, the input bias current to REFADJ can be as much as 25µA with REFADJ tied to V_{DD}. Pull REFADJ to AGND to minimize the input bias current in power-down.

Transfer Function

Table 7 shows the full-scale voltage ranges for unipolar and bipolar modes.

The external reference must have a temperature coefficient of 20ppm/°C or less to achieve accuracy to within 1LSB over the commercial temperature range of 0°C to +70°C.

Figure 16 depicts the nominal, unipolar input/output (I/O) transfer function, and Figure 17 shows the bipolar input/output transfer function. Code transitions occur halfway between successive-integer LSB values.

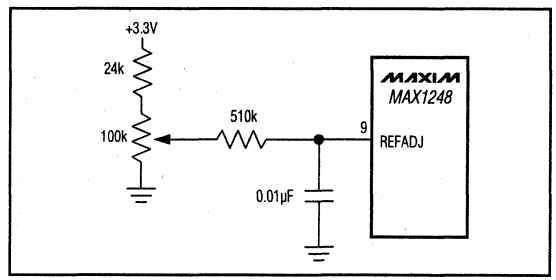


Figure 15. MAX1248 Reference-Adjust Circuit

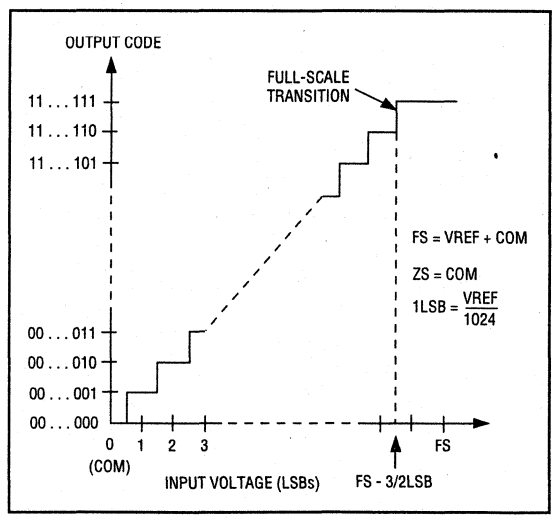


Figure 16. Unipolar Transfer Function, Full Scale (FS) = VREF + COM, Zero Scale (ZS) = COM

Table 7. Full Scale and Zero Scale

UNIPOLAR MODE		BIPOLAR MODE		
Full Scale	Zero Scale	Positive Full Scale	Zero Scale	Negative Full Scale
VREF + COM	COM	VREF / 2 + COM	COM	-VREF / 2 + COM

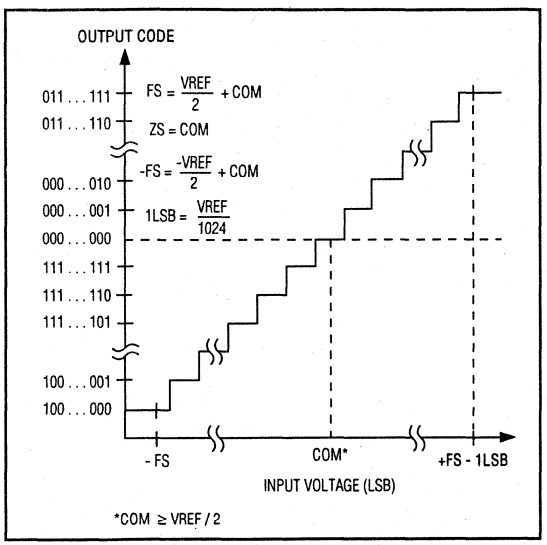


Figure 17. Bipolar Transfer Function, Zero Scale (ZS) = COM, Full Scale (FS) = VREF / 2 + COM

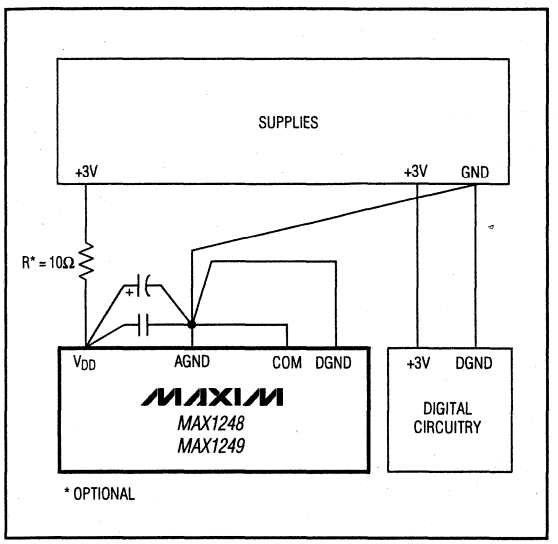


Figure 18. Power-Supply Grounding Connection

Output coding is binary, with 1LSB = 2.44mV (2.500V / 1024) for unipolar operation and 1LSB = 2.44mV [(2.500V / 2 - -2.500V / 2) / 1024] for bipolar operation.

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 18 shows the recommended system ground connections. Establish a single-point analog ground (star ground point) at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. For lowest noise operation, the ground return to the star ground's power supply should be low impedance and as short as possible.

High-frequency noise in the V_{DD} power supply may affect the ADC's high-speed comparator. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to pin 1 of the MAX1248/MAX1249. Minimize capacitor lead lengths for best supply-noise rejection. If the +3V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter (Figure 18).

High-Speed Digital Interfacing with QSPI

The MAX1248/MAX1249 can interface with QSPI using the circuit in Figure 19 (f_{SCLK} = 2.0MHz, CPOL = 0, CPHA = 0). This QSPI circuit can be programmed to do a conversion on each of the four channels. The result is stored in memory without taxing the CPU, since QSPI incorporates its own micro-sequencer.

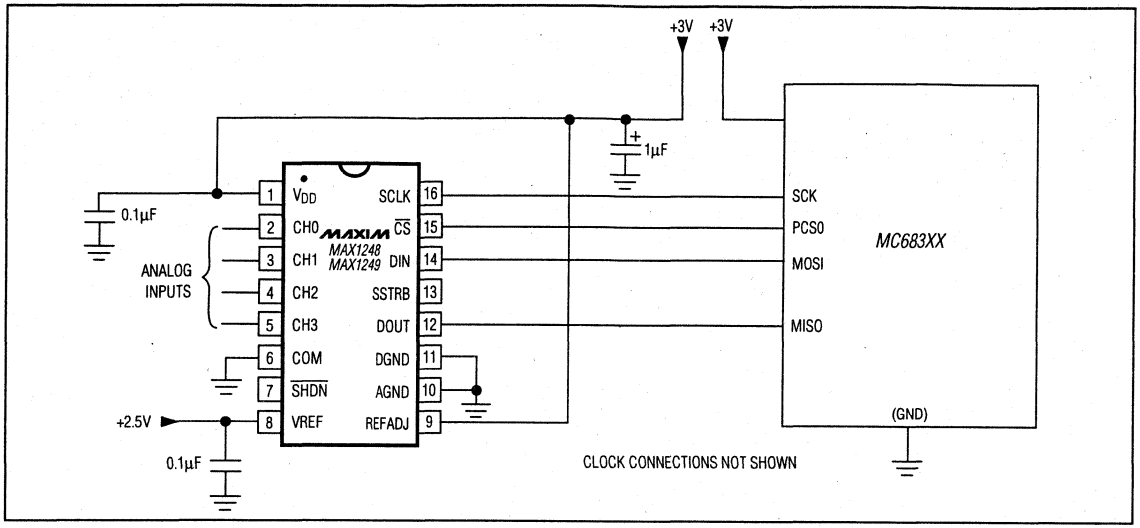


Figure 19. MAX1248/MAX1249 QSPI Connections External Reference

The MAX1248/MAX1249 are QSPI compatible up to their maximum external clock frequency of 2MHz.

TMS320LC3x Interface

Figure 20 shows an application circuit to interface the MAX1248/MAX1249 to the TMS320 in external clock mode. The timing diagram for this interface circuit is shown in Figure 21.

Use the following steps to initiate a conversion in the MAX1248/MAX1249 and to read the results:

1) The TMS320 should be configured with CLKX (transmit clock) as an active-high output clock and CLKR (TMS320 receive clock) as an active-high input clock. CLKX and CLKR on the TMS320 are tied together with the MAX1248/MAX1249's SCLK input.
2) The MAX1248/MAX1249's $\overline{CS}$ pin is driven low by the TMS320's XF_ I/O port, to enable data to be clocked into the MAX1248/MAX1249's DIN.
3) An 8-bit word (1XXXXX11) should be written to the MAX1248/MAX1249 to initiate a conversion and place the device into external clock mode. Refer to Table 1 to select the proper XXXXX bit values for your specific application.
4) The MAX1248/MAX1249's SSTRB output is monitored via the TMS320's FSR input. A falling edge on the SSTRB output indicates that the conversion is in progress and data is ready to be received from the MAX1248/MAX1249.
5) The TMS320 reads in one data bit on each of the next 16 rising edges of SCLK. These data bits represent the 10 + 2-bit conversion result followed by four trailing bits, which should be ignored.

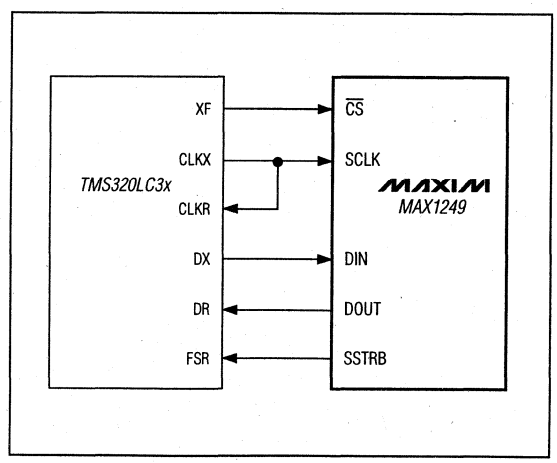


Figure 20. MAX1248/MAX1249-to-TMS320 Serial Interface

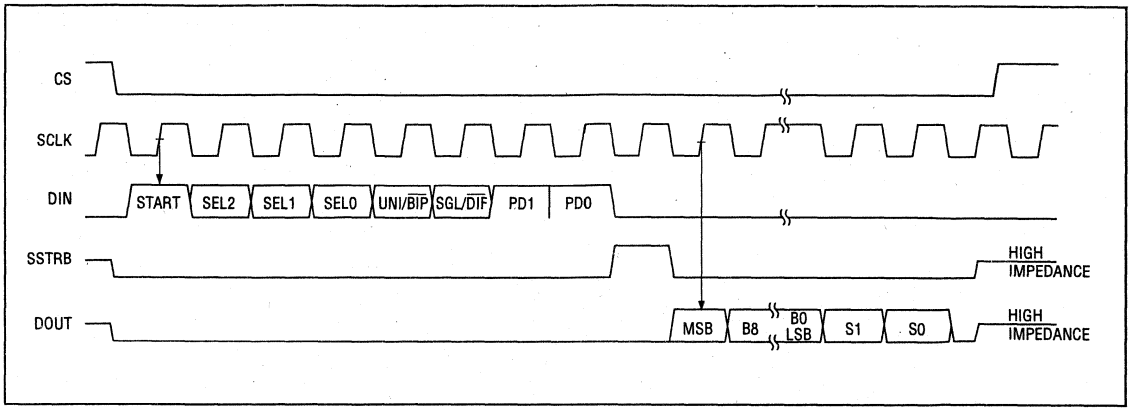


Figure 21. TMS320 Serial-Interface Timing Diagram

Ordering Information (continued)

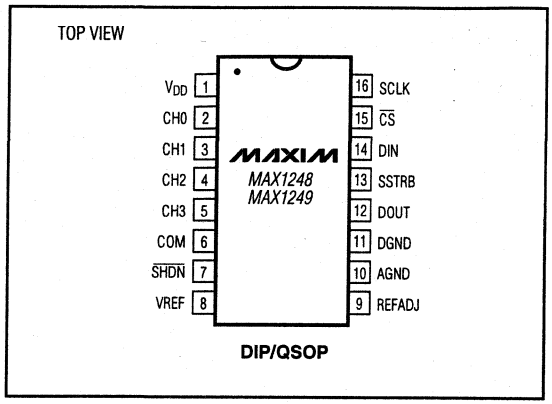
PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1248AEPE	-40°C to +85°C	16 Plastic DIP*	±1/2
MAX1248BEPE	-40°C to +85°C	16 Plastic DIP*	±1
MAX1248AEEE	-40°C to +85°C	16 QSOP*	±1/2
MAX1248BEEE	-40°C to +85°C	16 QSOP*	±1
MAX1248AMJE	-55°C to +125°C	16 CERDIP**	±1/2
MAX1248BMJE	-55°C to +125°C	16 CERDIP**	±1
MAX1249ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX1249BCPE	0°C to +70°C	16 Plastic DIP	±1

PART†	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX1249ACEE	0°C to +70°C	16 QSOP	±1/2
MAX1249BCEE	0°C to +70°C	16 QSOP	±1
MAX1249AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX1249BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX1249AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX1249BEEE	-40°C to +85°C	16 QSOP	±1
MAX1249AMJE	-55°C to +125°C	16 CERDIP**	±1/2
MAX1249BMJE	-55°C to +125°C	16 CERDIP**	±1

† *Contact factory for availability of alternate surface-mount packages.*
* *Contact factory for availability.*
** *Contact factory for availability of CERDIP package, and for processing to MIL-STD-883B.*

+2.7V to +5.25V, Low-Power, 4-Channel, Serial 10-Bit ADCs in QSOP-16

Pin Configuration



Chip Information

TRANSISTOR COUNT: 2554

MAXIM

Video Products/High-Speed Amplifiers

Video Products/High-Speed Amplifiers, Product Tables and Trees 8-3

MAX4012	Low-Cost, High-Speed, SOT23, Single-Supply Op Amp with Rail-to-Rail Outputs	8-9
MAX4014	Low-Cost, SOT23, High-Speed Buffer with Rail-to-Rail Outputs	8-25 *
MAX4016	Dual, Low-Cost, High-Speed, Single-Supply Op Amp with Rail-to-Rail Outputs	8-9
MAX4017	Dual, Low-Cost, High-Speed Buffer with Rail-to-Rail Outputs	8-25 *
MAX4018	Triple, Low-Cost, High-Speed, Single-Supply Op Amp with Rail-to-Rail Outputs	8-9
MAX4019	Triple, Low-Cost, High-Speed Buffer with Rail-to-Rail Outputs in QSOP Package	8-25 *
MAX4020	Quad, Low-Cost, High-Speed, Single-Supply Op Amp with Rail-to-Rail Outputs	8-9
MAX4022	Quad, Low-Cost, High-Speed Buffer with Rail-to-Rail Outputs in QSOP Package	8-25 *
MAX4108	400MHz, Unity-Gain-Stable, Ultra-Low-Distortion Op Amp	8-117
MAX4109	400MHz, Ultra-Low-Distortion Op Amp	8-117
MAX4142	High-Speed, Differential Line Driver	8-27 *
MAX4144	High-Speed, Differential Line Receiver with +2V/V Fixed Gain	8-29 *
MAX4145	High-Speed, Differential Line Receiver	8-29 *
MAX4146	High-Speed, Differential Line Receiver with Adjustable Gain	8-29 *
MAX4158	350MHz, 2-Channel Video Multiplexer/Amplifier	8-31
MAX4159	350MHz, 2-Channel Video Multiplexer/Amplifier	8-31
MAX4160	350MHz, 120mW, 4-Channel Video Multiplexer/Amplifier	8-47 *
MAX4161	350MHz, 310mW, 8-Channel Video Multiplexer/Amplifier	8-47 *
MAX4180	270MHz, 1mA, SOT23, Current-Feedback Amplifier with Shutdown (A_V = +2V/V)	8-49
MAX4181	270MHz, 1mA, SOT23, Current-Feedback Amplifier with Shutdown (A_V = +1V/V)	8-49
MAX4182	Dual, 270MHz, 1mA, Current-Feedback Amplifier (A_V = +2V/V)	8-49
MAX4183	Dual, 270MHz, 1mA, Current-Feedback Amplifier with Shutdown (A_V = +2V/V)	8-49
MAX4184	Dual, 270MHz, 1mA, Current-Feedback Amplifier (A_V = +1V/V)	8-49
MAX4185	Dual, 270MHz, 1mA, Current-Feedback Amplifier with Shutdown (A_V = +1V/V)	8-49
MAX4186	Quad, 270MHz, 1mA, Current-Feedback Amplifier (A_V = +2V/V)	8-49
MAX4187	Quad, 270MHz, 1mA, Current-Feedback Amplifier (A_V = +1V/V)	8-49
MAX4188	Triple, Low-Power, 250MHz, Current-Feedback Amplifier with High-Speed Disable ($A_V \geq$ +2V/V)	8-73 *
MAX4189	Triple, Low-Power, 260MHz, Current-Feedback Amplifier with High-Speed Disable ($A_V \geq$ +2V/V)	8-73 *
MAX4190	Low-Power, 250MHz, Current-Feedback Amplifier with High-Speed Disable	8-73 *
MAX4191	Low-Power, 260MHz, Current-Feedback Amplifier with High-Speed Disable ($A_V \geq$ +2V/V)	8-73 *
MAX4200	High-Speed, 500MHz, Open-Loop Buffer in 5-Pin SOT23	8-75 *
MAX4201	High-Speed, 500MHz, Open-Loop Buffer with 50Ω Output Termination	8-75 *
MAX4202	High-Speed, 500MHz, Open-Loop Buffer with 75Ω Output Termination	8-75 *
MAX4203	Dual, High-Speed, 500MHz, Open-Loop Buffer in 8-Pin µMAX	8-75 *
MAX4204	Dual, High-Speed, 500MHz, Open-Loop Buffer with 50Ω Output Termination	8-75 *
MAX4205	Dual, High-Speed, 500MHz, Open-Loop Buffer with 75Ω Output Termination	8-75 *
MAX4206	High-Speed, Low-Power, Open-Loop Buffer in 5-Pin SOT23	8-77 *
MAX4207	High-Speed, Low-Power, Open-Loop Buffer with 50Ω Output Termination	8-77 *
MAX4208	High-Speed, Low-Power, Open-Loop Buffer with 75Ω Output Termination	8-77 *
MAX4209	Dual, High-Speed, Low-Power, Open-Loop Buffer in 8-Pin µMAX	8-77 *

*Advance Information–first page of a data sheet in preparation.

_Video Products/High-Speed Amplifiers (continued)

MAX4210	Dual, High-Speed, 1GHz, Low-Power, Open-Loop Buffer with 50Ω Output Termination	8-77 *
MAX4211	Dual, High-Speed, 1GHz, Low-Power, Open-Loop Buffer with 75Ω Output Termination	8-77 *
MAX4212	SOT23, 300MHz, Single-Supply, Rail-to-Rail Op Amp	8-79
MAX4213	Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amp with Enable	8-79
MAX4214	SOT23, 300MHz, Gain of +2V/V, Closed-Loop, Rail-to-Rail Buffer	8-95 *
MAX4215	300MHz, Gain of +2V/V, Closed-Loop, Rail-to-Rail Buffer with Enable	8-95 *
MAX4216	Miniature, 200MHz, Single-Supply, Rail-to-Rail Dual Op Amp with Enable	8-79
MAX4217	Miniature, 200MHz, Single-Supply, Rail-to-Rail Dual Buffer	8-95 *
MAX4218	Miniature, 200MHz, Single-Supply, Rail-to-Rail Triple Op Amp with Enable	8-79
MAX4219	Miniature, 200MHz, Rail-to-Rail Triple Buffer with Enable	8-95 *
MAX4220	Miniature, 200MHz, Single-Supply, Rail-to-Rail Quad Op Amp with Enable	8-79
MAX4222	200MHz, Rail-to-Rail Quad Buffer in QSOP Package	8-95 *
MAX4223	1GHz, Low-Power, SOT23 Current-Feedback Amp with Shutdown	8-97
MAX4224	1GHz, Low-Power, SOT23 Current-Feedback Amp with Shutdown	8-97
MAX4225	1GHz, Low-Power, Dual Current-Feedback Amp	8-97
MAX4226	1GHz, Low-Power, Dual Current-Feedback Amp with Shutdown	8-97
MAX4227	1GHz, Low-Power, Dual Current-Feedback Amp	8-97
MAX4228	1GHz, Low-Power, Dual Current-Feedback Amp with Shutdown	8-97
MAX4258	250MHz, 2-Channel Video Multiplexer/Amplifier	8-31
MAX4259	250MHz, 2-Channel Video Multiplexer/Amplifier	8-31
MAX4260	250MHz, 120mW, 4-Channel Video Multiplexer/Amplifier	8-47 *
MAX4261	250MHz, 310mW, 8-Channel Video Multiplexer/Amplifier	8-47 *
MAX4308	220MHz, Ultra-Low-Distortion Op Amp	8-117
MAX4309	200MHz, Ultra-Low-Distortion Op Amp	8-117
MAX4310	High-Speed, 2-Channel, Low-Power, Unity-Gain-Stable Video Multiplexer/Amplifier	8-129 *
MAX4311	High-Speed, 4-Channel, Low-Power, Unity-Gain-Stable Video Multiplexer/Amplifier	8-129 *
MAX4312	High-Speed, 8-Channel, Low-Power, Unity-Gain-Stable Video Multiplexer/Amplifier	8-129 *
MAX4313	High-Speed, 2-Channel, Low-Power, Video Multiplexer/Amplifier with +2V/V Fixed Gain	8-129 *
MAX4314	High-Speed, 4-Channel, Low-Power, Video Multiplexer/Amplifier with +2V/V Fixed Gain	8-129 *
MAX4315	High-Speed, 8-Channel, Low-Power, Video Multiplexer/Amplifier with +2V/V Fixed Gain	8-129 *

*Advance Information–first page of a data sheet in preparation.

Video & High-Speed Products

Buffers

MAX405
(180MHz, A_{VCL} = +0.998V/V)

MAX460
(140MHz, JFET input)

MAX467/468
(triple/quad, 100MHz)

MAX469/470
(triple/quad, 90MHz, A_{VCL} = +2V/V)

☆ MAX496/MAX497
(quad, 375/275MHz, A_{VCL} = +1/+2V/V)

☆ MAX4005
(950MHz, JFET)

☆ MAX4178/4278
(330/310MHz, A_{VCL} = +1/+2V/V)

† MAX4014
(low cost, SOT23, single supply, 200MHz, A_{VCL} = +2V/V)

† MAX4017/19/22
(low cost, dual/triple/quad, single supply, 150MHz, A_{VCL} = +2V/V)

† MAX4200/01/02
(single, 500MHz, open-loop buffers)

† MAX4203/4205
(dual, 500MHz, open-loop buffers)

† MAX4206/07/08
(single, 1GHz, open-loop buffers)

† MAX4207–4211
(dual, 1GHz, open-loop buffers)

† MAX4214/4215
(SOT23, single supply, 300MHz, A_{VCL} = +2V/V)

→ cont.

RGB Switches

☆ MAX463/MAX464
(100MHz, output drivers)

☆ MAX465/466
(90MHz, A_{VCL} = +2V/V, output drivers)

☆ MAX498/499
(250MHz, A_{VCL} = +2V/V, output drivers)

Crosspoint Switches

MAX456 (8x8)

☆ MAX458
(100MHz 8x4, output drivers)

☆ MAX459
(90MHz 8x4, A_{VCL} = +2V/V, output drivers)

☆ MAX4111
(330MHz 1x1)

☆ MAX4121
(330MHz 2x1)

☆ MAX4141
(330MHz 4x1)

☆ MAX4221
(330MHz dual 2x1)

† MAX4217/19/22
(dual/triple/quad, single supply, 200MHz, A_{VCL} = +2V/V)

Multiplexers

MAX440
(160MHz, 8-ch mux + output amp)

MAX441
(160MHz, 4-ch mux + output amp)

MAX442
(160MHz, 2-ch mux + output amp)

MAX453
(50MHz, 2-ch mux + output amp)

MAX454
(50MHz, 4-ch mux + output amp)

MAX455
(50MHz, 8-ch mux + output amp)

☆ MAX4111
(330MHz 1x1)

☆ MAX4121
(330MHz 2x1)

☆ MAX4141
(330MHz 4x1)

★☆ MAX4158/4159
(350MHz, A_{VCL} = +1V/V, 2-ch mux + output amp)

† MAX4160/4161
(350MHz, A_{VCL} = +1V/V, 4/8-ch mux + output amp)

MAX4221
(330MHz dual 2x1)

★☆ MAX4258/4259
(225MHz, A_{VCL} = +2V/V, 2-ch mux + output amp)

† MAX4260/4261
(250MHz, A_{VCL} = +2V/V, 4/8-ch mux + output amp)

→ cont.

Amplifiers

MAX404
(40MHz, A_{VCL} = +2V/V)

MAX408
(33MHz, A_{VCL} = +3V/V)

MAX428
(dual MAX408)

MAX435
(275MHz, diff in/diff out)

MAX436
(200MHz, diff in/single out)

MAX448
(quad MAX408)

MAX452
(50MHz)

MAX457
(70MHz dual)

☆ MAX477
(300MHz, 1100V/µs)

☆ MAX4100/4101
(500MHz, low power)

☆ MAX4102/4103
(250MHz, lowest DP/DG)

☆ MAX4106/4107
(350MHz, 0.75nV/√Hz)

☆ MAX4108/4109
(400MHz,1200V/µs)

→ cont.

† MAX4310/11/12
(450MHz, A_{VCL} ≥ +1V/V, 2/4/8-ch single-supply mux + output amp)

† MAX4313/14/15
(450MHz, A_{VCL} ≥ +2V/V, 2/4/8-ch single-supply mux + output amp)

CRT Driver

MAX445
(200MHz, 2.5ns tr/tf, high-voltage output)

★ MAX4012
(low cost, single supply, 200MHz)

★ MAX4016/18/20
(low cost, dual/triple/quad, single supply, 150MHz)

☆ MAX4112/4113
(400MHz,1200V/µs)

☆ MAX4117/4118
(dual, 400MHz)

★ MAX4119/4120
(quad, 300MHz, 1200V/µs)

★☆ MAX4180/4181
(SOT23-6, 270MHz, 1mA)

† MAX4182–4185
(dual, 270MHz, 1mA)

† MAX4186/4187
(quad, 270MHz, 1mA)

†☆ MAX4188/4189
(triple, 200MHz, 1mA)

† MAX4190/4191
(single, 200MHz, 1mA)

★☆ MAX4212/4213
(SOT23-5, single supply, 300MHz)

★ MAX4216/18/20
(dual/triple/quad, single supply, 200MHz)

★☆ MAX4223/4224
(SOT23-6, 1GHz, shutdown)

★ MAX4225–4228
(dual, 1GHz, shutdown)

★ MAX4308/4309
(220MHz, -83dBc SFDR, A_{VCL} = +5V/V/+10V/V)

Distribution Amplifiers

☆ MAX4135
(185MHz, A_{VCL} = +2V/V, 1 input/6 outputs)

☆ MAX4136
(140MHz, A_{VCL} ≥ +2V/V, 1 input/6 outputs)

☆ MAX4137
(185MHz, A_{VCL} = +2V/V, 1 input/4 outputs)

☆ MAX4138
(140MHz, A_{VCL} ≥ +2V/V, 1 input/4 outputs)

Differential Line Drivers

☆ MAX4147
(300MHz, A_{VCL} = +2V/V, high output drive)

† MAX4142
(300MHz, A_{VCL} = +2V/V, shutdown)

High-Speed Line Receivers

☆ MAX4144
(130MHz, A_{VCL} = +2V/V)

†☆ MAX4146
(70MHz, A_{VCL} = +10V/V)

† MAX4145
(70MHz, A_{VCL} = +100V/V)

★ New product
† Future product
☆ Evaluation kit available

Part Number	-3dB BW (MHz)	Min. Stable Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO/RF AMPLIFIERS											
MAX404	40	+2	–	500	±8/50	0.01/0.05	50	±5	30	Broadcast-quality, low DP/DG, symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2.68
MAX408/428/448	33	+3	–	90	±2.7/51	N/A	50/ op amp	±5	7/7.5 7.5	Single/dual/quad, high output drive	3.02/4.06/ 6.74
MAX435/436	275/200	+1	–	800	±3.5/500	N/A	10	±5	35	Ultra-fast differential input/output transconductance amp, no feedback required	2.75
MAX445	200		–	2.5ns tr/tf	75V (max)	N/A	80	±10, +75	70 (V+)	CRT video display driver for ultra-high-resolution monitors, single IC preamp and high-voltage (+75V) output stage	6.83
MAX452	50	+1	–	300	±3/150	0.2/0.5	14	±5	25	Unity-gain stable, drives 75Ω coaxial cable	2.40
MAX457	70	+1	–	300	±2.5/150	0.2/0.5	15	±5	17.5	Dual, unity-gain stable, drives 75Ω coaxial cable	4.45
MAX477	300	+1	130	1100	±3/100	0.01/0.01	70	±5	8	Voltage feedback, 130MHz 0.1dB gain flatness, drives 100pF C_{LOADS}	2.40
MAX4100/4101	500/200	+1/+2	65/50	250	±3.5/100	0.04/0.06, 0.04/0.07	65	±5	5	Low power, low cost, voltage feedback	1.95
MAX4102/4103	250/180	+1/+2	130/80	350	±3.4/100	0.002/0.002, 0.003/0.008	65	±5	4.6	Ultra-low differential phase/gain, broadcast quality	1.95
MAX4106/4107	350/300	+5/+10	75/45	275/500	±3.5/100	0.02/0.04, 0.03/0.03	65	±5	15	0.75nV/√Hz, ultra-low noise, low distortion	3.88
MAX4108/4109	400/225	+1/+2	100/25	1200	+2.7 to -3.7/100	0.008/0.004	90	±5	20	Ultra-low distortion: -93/-90dBc at 20MHz (SFDR)	3.88
MAX4012	200	+1	30	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, SOT23, high-speed, single-supply amplifier	0.88
MAX4016	150	+1	30	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, dual, high-speed, single-supply amplifier	1.10
MAX4018	150	+1	30	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, triple, high-speed, single-supply amplifier	1.80
MAX4020	150	+1	30	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, quad, high-speed, single-supply amplifier	2.05
MAX4112/4113	400/270	+2/+8	100/115	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	80	±5	5	Low power, low cost, current feedback	1.95
MAX4117/4118	400/300	+2/+8	100/115	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	80	±5	5	Dual, low power, low cost, current feedback, 280/240MHz full-power bandwidth	2.65
MAX4119/4120	270/300	+2/+8	100/115	1200/ 1800	±3.5/100	0.03/0.02, 0.04/0.02	80	±5	5	Quad, low-power, low-cost current feedback	3.95
MAX4180/4181	240/270	+2/+1	90/60	400	±3.2/150	0.03/0.08	50	+5 or ±5	1	Single, 1mA, high-speed SOT23 amplifier with shutdown	1.80
MAX4182/4183	340	+2	80	400	±3.2/150	0.03/0.08	50	+5 or ±5	1	Dual, 1mA, high-speed amplifiers, shutdown (MAX4183)	2.80/2.90
MAX4184/4185	400	+1	60	400	±3.2/150	0.03/0.08	50	+5 or ±5	1	Dual, 1mA, high-speed amplifiers, shutdown (MAX4185)	2.80/2.90
MAX4186/4187	340/400	+2/+1	80/60	400	±3.2/150	0.03/0.08	50	+5 or ±5	1	Quad, 1mA, high-speed amplifiers	3.65
MAX4188/4189	200	+1/+2	60	400	±3.2/150	0.03/0.08	90	+5 or ±5	1	Triple, 1mA, high-speed, low-glitch amplifiers	††
MAX4190/4191	200	+1/+2	60	400	±3.2/150	0.03/0.08	90	+5 or ±5	1	Single, 1mA, high-speed, low-glitch amplifiers	††
MAX4212/4213	300	+1	50	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	SOT23, high-speed, single-supply amplifiers, shutdown (MAX4213)	1.55
MAX4216	200	+1	35	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Dual, high-speed, single-supply amplifier	2.25
MAX4218	200	+1	35	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Triple, high-speed, single-supply amplifier with enable	2.98
MAX4220	200	+1	35	600	0.5 to 4.5/150	0.02/0.02	100	+3.3/+5 or ±5	5.5	Quad, high-speed, single-supply amplifier	3.95
MAX4223/4224	1000/600	+1/+2	300/200	1100/ 1700	+2.5	0.02/0.02	80	±5	6	SOT23, ultra-high-speed, low-power amplifiers with shutdown	2.15
MAX4225/4226	1000/600	+1	300	1100	+2.5	0.02/0.02	80	±5	6	Dual, ultra-high-speed, low-power amplifiers, shutdown (MAX4226)	3.45
MAX4227/4228	600	+2	200	1700	±2.5	0.02/0.02	80	±5	6	Dual, ultra-high-speed, low-power amplifiers, shutdown (MAX4228)	3.45
MAX4308/4309	200/200	+5/+10	100/30	1200	+2.7 to -3.7/100	0.008/0.004	90	±5	20	Ultra-low distortion: -83dBc at 20MHz (SFDR)	3.88

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	V_{OUT} Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO/RF BUFFERS											
MAX405	180	+0.99	–	650	±3.4/50	0.01/0.03	60	±5	35	Closed loop, 0.99V gain guaranteed over temp	4.25
MAX460	140	+0.99	–	1500	±9.8/100	N/A	90	±15	19	FET input, EL2005/LH0033 upgrade	19.78
MAX467	100	+1	–	200	±2.4/75	0.03/0.01	20	±5	17	Triple (RGB) video buffer, low DP/DG	3.70
MAX468	100	+1	–	200	±2.4/75	0.03/0.01	20	±5	16	Quad, unity-gain video buffer, low DP/DG	4.20
MAX469	90	+2	–	300	±2.4/75	0.14/0.12	20	±5	17	Triple (RGB), gain of +2 video buffer, low DP/DG	3.70
MAX470	90	+2	–	300	±2.4/75	0.14/0.12	20	±5	16	Quad, gain of +2 (6dB) video buffer, low DP/DG	4.20
MAX496	375	+1	80	1600	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +1 (0dB) closed-loop buffer, low DP/DG	4.95
MAX497	275	+2	120	1500	±3.3/50	0.01/0.01	66	±5	8	Quad, gain of +2 (6dB) closed-loop buffer, low DP/DG	4.95
MAX4005	950	+1	60	1000	+0.8 to -0.65/75	0.03/0.11	75Ω output	±5	24	FET input buffer with 75Ω output to minimize reflections, low DP/DG, 60MHz 0.1dB gain flatness, 28dBm IP_3 (100MHz)	2.75
MAX4178	330	+1	150	1300	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +1 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
MAX4200/1/2	500	1	100	4000	±3.5/100	0.05/0.8	80	±5	7.5	Single, low power, 500MHz, open-loop buffers	††
MAX4203/4/5	500	1	100	4000	±3.5/100	0.05/0.8	80	±5	7.5	Dual, low power, 500MHz, open-loop buffers	††
MAX4206/7/8	1000	1	200	5000	±3.5/100	0.05/0.8	80	±5	12.5	Single, low power, 1GHz, open-loop buffers	††
MAX4209/10/11	1000	1	200	5000	±3.5/100	0.05/0.8	80	±5	12.5	Dual, low power, 1GHz, open-loop buffers	††
MAX4014	200	+2	30	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, SOT23, high-speed, single-supply buffer	††
MAX4017	150	+2	30	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, dual, high-speed, single-supply buffer	††
MAX4019	150	+2	30	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, triple, high-speed, single-supply buffer with enable	††
MAX4022	150	+2	30	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Low-cost, quad, high-speed, single-supply buffer	††
MAX4214/4215	300	+2	50	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	SOT23, high-speed, single-supply buffers, enable (MAX4215)	††
MAX4217	200	+2	50	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Dual, high-speed, single-supply buffer	††
MAX4219	200	+2	50	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Triple, high-speed, single-supply buffer with enable	††
MAX4222	200	+2	50	600	0.7 to 4.3/50	0.02/0.02	100	+3.3/+5 or ±5	5.5	Quad, high-speed, single-supply buffer	††
MAX4278	310	+2	150	1600	±2.5/50	0.01/0.04	70	±5	8	Closed loop, gain of +2 buffer, 150MHz 0.1dB gain flatness, low DP/DG	2.40
VIDEO MULTIPLEXERS/AMPLIFIERS											
MAX440	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 8-channel mux, low DP/DG, 15ns switch time, high-Z output state	8.95
MAX441	160	+1	–	370	±3/150	0.03/0.04	20	±5	40	Video amp with 4-channel mux, low DP/DG, 15ns switch time	5.90
MAX442	140	+1	–	250	±3/75	0.09/0.07	33	±5	40	Video amp with 2-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 2-channel video mux	3.94
MAX454	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 4-channel video mux	5.25
MAX455	50	+1	–	300	±3/150	1.2/0.5	14	±5	25	Video amp with 8-channel video mux	8.75
MAX4111	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	1x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	2.10
MAX4141	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	4	4x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	2.95
MAX4158	350	+1	100	700	±3.5/50	0.01/0.01	70	±5	11	2 inputs/1 output, current feedback, $A_{VCL} \geq 1V/V$	2.30
MAX4159	350	+1	100	700	±3.5/50	0.01/0.01	70	±5	11	2 inputs/1 output, current feedback, $A_{VCL} \geq 1V/V$, output enable	2.60
MAX4160/4260	350/250	+1/+2	100/130	700/1000	±3.5/50	0.01/0.01	100	±5	11	4-channel video mux amps	††
MAX4161/4261	350/250	+1/+2	100/130	700/1000	±3.5/50	0.01/0.01	100	±5	11	8-channel video mux amps	††
MAX4221	330	+0.99	150	700	±2.5/5k	0.01/0.01	500µA	±5	5	Dual 2x1 video crosspoint building block, 150MHz 0.1dB gain flatness, low DP/DG	4.50
MAX4258	250	+2	130	1000	±3.5/50	0.01/0.02	70	±5	11	2 inputs/1 output, current feedback, $A_{VCL} \geq 2V/V$	2.30

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Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA min)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
VIDEO MULTIPLEXERS/AMPLIFIERS (continued)											
MAX4259	250	+2	130	1000	±3.5/50	0.01/0.02	70	±5	11	2 inputs/1 output, current feedback, $A_{VCL} \geq 2V/V$, output enable	2.60
MAX4310/4313	400/450	+1/+2	50	700/900	0.05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6.5	2-channel, single-supply video mux amps with shutdown	††
MAX4311/4314	400/450	+1/+2	50	700/900	0.05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6.5	4-channel, single-supply video mux amps with shutdown	††
MAX4312/4315	400/450	+1/+2	50	700/900	0.05 to 4.5/150	0.04/0.02	100	4 to 10, ±2 to ±5	6.5	8-channel, single-supply video mux amps with shutdown	††

Part Number	-3dB BW (MHz)	Buffer Amp Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	Switching Time (ns)	Number of Inputs	Number of Outputs	Output Current (mA)	EV Kit	Features	Price† 1000-up ($)
RGB VIDEO SWITCHES												
MAX463/465	100/90	+1/+2	–	300	±2.4/75	20	6 (RGB_A, RGB_B)	3 (RGB)	20		RGB switch with 75Ω cable drivers	6.97
MAX464/466	100/90	+1/+2	–	300	±2.4/75	20	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	20	Yes	RGB + sync switch with 75Ω cable drivers	7.97
MAX498	250	+2	70	1250	±3/100	3	8 (RGB_A + Sync, RGB_B + Sync)	4 (RGB + Sync)	40		Drives back-terminated 75Ω cables	4.40
MAX499	250	+2	70	1250	±3/100	3	6 (RGB_A, RGB_B)	3 (RGB)	40		Drives back-terminated 75Ω cables	3.50

Part Number	-3dB BW (MHz)	Min. Gain Stable (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DISTRIBUTION AMPLIFIERS											
MAX4135	185	+2	40	1000	+2.6 to -2.4 /150	0.02/0.09	70	±5	45	1 input/6 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	5.90
MAX4136	140	+2	40	1000	+2.6 to -2.4 /150	0.03/0.12	70	±5	45	1 input/6 outputs, external gain set, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	5.90
MAX4137	185	+2	40	1000	+2.6 to -2.4 /150	0.02/0.10	70	±5	30	1 input/4 outputs, fixed gain of 2V/V, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	4.50
MAX4138	140	+2	40	1000	+2.6 to -2.4 /150	0.02/0.10	70	±5	30	1 input/4 outputs, external gain set, high-impedance outputs in shutdown. Outputs can be individually enabled/disabled.	4.50

Part Number	-3dB BW (MHz)	Gain (V/V)	0.1dB BW (MHz)	Slew Rate (V/µs)	VOUT Swing/ Load (V/Ω)	DP/DG (deg./%)	Output Current (mA)	Supply Voltage (V)	Supply Current per Ch. (mA)	Features	Price† 1000-up ($)
DIFFERENTIAL LINE DRIVERS											
MAX4142	300	+2	70	2000	±6/100	0.03/0.008	80	±5	12	Fixed gain of +2V/V, high output drive	††
MAX4147	300	+2	70	2000	±5.6/53	0.01/0.008	160	±5	10	Fixed gain of +2V/V, high output drive	2.50
HIGH-SPEED LINE RECEIVERS											
MAX4144	130	+2	30	1000	±2.6/150	0.03/0.03	50	±5	13	Fixed gain of +2V/V, differential input/single-ended output	3.35
MAX4145	70	+100	10	800	±2.6/150	0.07/0.12	50	±5	13	External gain set +10V/V to +100V/V, low noise 3.5nV/√Hz, differential input/single-ended output	††
MAX4146	70	+10	10	800	±2.6/150	0.07/0.12	50	±5	13	External gain set +1V/V to +10V/V, low noise 3.5nV/√Hz, differential input/single-ended output	††

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Part Number	Min. -3dB BW (MHz)	Stable Gain (V/V)	0.1dB BW (MHz)	V_{OUT} Slew Rate (V/µs)	Swing/ Load (V/Ω)	DP/DG (deg./%)	Off Isolation (dB)	Crosstalk (dB)	EV Kit	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCHES											
MAX456	35	+1	–	250	±1.3/0	1/0.5	80 (5MHz)	-70 (5MHz)		8x8 crosspoint switch array with eight output buffers, high-Z output capability	19.98
MAX458/459	100/90	+1/+2	–	200 /300	±3/150	0.05/0.01	60 (10MHz)	-55 (10MHz)	Yes	8x4 crosspoint switch array with four 75Ω cable drivers, high-Z output capability	21.85
MAX4111	330	+0.99	150	700	±2.5/5k	0.01/0.01	86 (30MHz)	N/A	Yes	1x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	1.70
MAX4121	330	+0.99	150	700	±2.5/5k	0.01/0.01	78 (30MHz)	-92 (30MHz)	Yes	2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.10
MAX4141	330	+0.99	150	700	±2.5/5k	0.01/0.01	74 (30MHz)	-66 (30MHz)	Yes	4x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.95
MAX4221	330	+0.99	150	700	±2.5/5k	0.01/0.01	84 (30MHz)	-70 (30MHz)	Yes	Dual 2x1 video crosspoint building block, 0.1dB gain flatness of 150MHz	2.95

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-1246; Rev 0; 7/97

MAXIM

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

General Description

The MAX4012 single, MAX4016 dual, MAX4018 triple, and MAX4020 quad op amps are unity-gain-stable devices that combine high-speed performance with Rail-to-Rail® outputs. The MAX4018 has a disable feature that reduces power-supply current to 400µA and places its outputs into a high-impedance state. These devices operate from a +3.3V to +10V single supply or from ±1.65V to ±5V dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

These devices require only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/µs slew rate. These parts are an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation. In addition, when disabled, their high output impedance makes them ideal for multiplexing applications.

The MAX4012 comes in a miniature 5-pin SOT23 package, while the MAX4016 comes in 8-pin µMAX and SO packages. The MAX4018/MAX4020 are available in a space-saving 16-pin QSOP, as well as a 14-pin SO.

Applications

Set-Top Boxes
Surveillance Video Systems
Battery-Powered Instruments
Video Line Driver
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems

Features

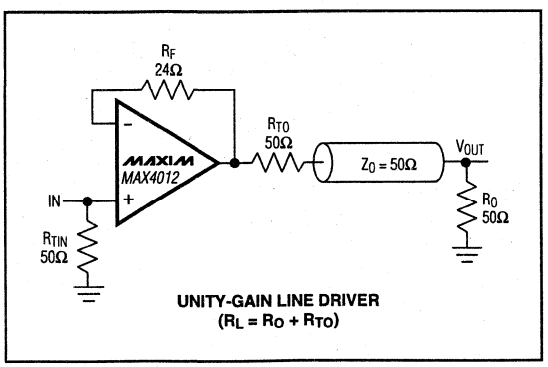
- **Low-Cost**
- **High Speed:**
  200MHz -3dB Bandwidth (MAX4012)
  150MHz -3dB Bandwidth (MAX4016/18/20)
  30MHz 0.1dB Gain Flatness
  600V/µs Slew Rate
- **Single 3.3V/5.0V Operation**
- **Rail-to-Rail Outputs**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase: 0.02%/0.02°**
- **Low Distortion at 5MHz:**
  -78dBc SFDR
  -75dB Total Harmonic Distortion
- **High Output Drive: ±120mA**
- **400µA Shutdown Capability (MAX4018)**
- **High Output Impedance in Off State (MAX4018)**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4012EUK	-40°C to +85°C	5 SOT23-5	ABZP
MAX4016ESA	-40°C to +85°C	8 SO	—
MAX4016EUA	-40°C to +85°C	8 µMAX	—

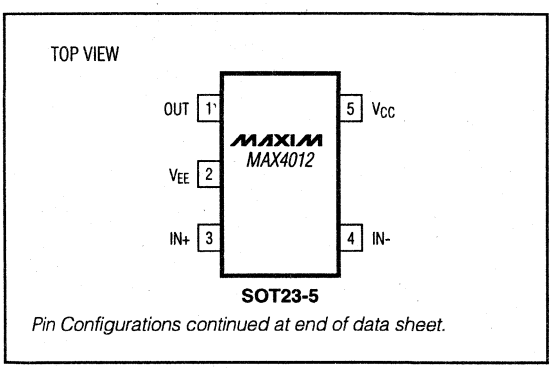
Ordering Information continued at end of data sheet.

Typical Operating Circuit



UNITY-GAIN LINE DRIVER
($R_L = R_O + R_{TO}$)

Pin Configurations



SOT23-5

Pin Configurations continued at end of data sheet.

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}).....+12V
IN_-, IN_+, OUT_, EN_.....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE}..... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C).....571mW
8-Pin SO (derate 5.9mW/°C above +70°C).....471mW
8-Pin µMAX (derate 4.1mW/°C above +70°C).....330mW
14-Pin SO (derate 8.3mW/°C above +70°C).....667mW
16-Pin QSOP (derate 8.3mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec).....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or at any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, EN_ = +5V, R_L = ∞ to V_{CC} / 2, V_{OUT} = V_{CC} / 2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test		V_{EE} - 0.20		V_{CC} - 2.25	V
Input Offset Voltage (Note 2)	V_{OS}				4	20	mV
Input Offset Voltage Temperature Coefficient	TC_{VOS}				8		µV/°C
Input Offset Voltage Matching		Any channels for MAX4016/MAX4018/ MAX4020			±1		mV
Input Bias Current	I_B	(Note 2)			5.4	20	µA
Input Offset Current	I_{OS}	(Note 2)			0.1	20	µA
Input Resistance	R_{IN}	Differential mode (-1V ≤ V_{IN} ≤ +1V)			70		kΩ
		Common mode (-0.2V ≤ V_{CM} ≤ +2.75V)			3		MΩ
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.2V) ≤ V_{CM} ≤ (V_{CC} - 2.25V)		70	100		dB
Open-Loop Gain (Note 2)	A_{VOL}	0.25V ≤ V_{OUT} ≤ 4.75V, R_L = 2kΩ			61		dB
		0.5V ≤ V_{OUT} ≤ 4.5V, R_L = 150Ω		52	59		
		1.0V ≤ V_{OUT} ≤ 4V, R_L = 50Ω			57		
Output Voltage Swing (Note 2)	V_{OUT}	R_L = 2kΩ	V_{CC} - V_{OH}		0.06		V
			V_{OL} - V_{EE}		0.06		
		R_L = 150Ω	V_{CC} - V_{OH}		0.30		
			V_{OL} - V_{EE}		0.30		
		R_L = 75Ω	V_{CC} - V_{OH}		0.6	1.5	
			V_{OL} - V_{EE}		0.6	1.5	
		R_L = 75Ω to ground	V_{CC} - V_{OH}		1.1	2.0	
			V_{OL} - V_{EE}		0.05	0.50	
Output Current	I_{OUT}	R_L = 20Ω to V_{CC} or V_{EE}		±100	±120		mA
Output Short-Circuit Current	I_{SC}	Sinking or sourcing			±150		mA
Open-Loop Output Resistance	R_{OUT}				8		Ω

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0V, EN_ = +5V, R_L = ∞ to V_{CC} / 2, V_{OUT} = V_{CC} / 2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 3)	PSRR	V_{CC} = 5V, V_{EE} = 0V, V_{CM} = +2.0V	46	57		dB
		V_{CC} = 5V, V_{EE} = -5V, V_{CM} = 0V	54	66		
		V_{CC} = 3.3V, V_{EE} = 0V, V_{CM} = +0.90V		45		
Operating Supply-Voltage Range	V_S	V_{CC} to V_{EE}	3.15		11.0	V
Disabled Output Resistance	$R_{OUT (OFF)}$	EN_ = 0V, 0V ≤ V_{OUT} ≤ 5V (Note 4)	28	35		kΩ
EN_ Logic-Low Threshold	V_{IL}				V_{CC} - 2.6	V
EN_ Logic-High Threshold	V_{IH}		V_{CC} - 1.6			V
EN_ Logic Input Low Current	I_{IL}	(V_{EE} + 0.2V) ≤ EN_ ≤ V_{CC}		0.5		µA
		EN_ = 0V		200	300	
EN_ Logic Input High Current	I_{IH}	EN_ = 5V		0.5	10	µA
Quiescent Supply Current (per Amplifier)	I_S	Enabled		5.5	7.0	mA
		MAX4018, disabled (EN_ = 0V)		0.40	0.55	

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = 2.5V, EN_ = +5V, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, V_{OUT} = V_{CC} / 2, A_{VCL} = +1, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 20mVp-p	MAX4012		200		MHz
			MAX4016/MAX4018/MAX4020		150		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p			140		MHz
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 20mVp-p (Note 5)		6	30		MHz
Slew Rate	SR	V_{OUT} = 2V step			600		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			45		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mVp-p			1		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p			-78		dBc
Harmonic Distortion	HD	f_C = 5MHz, V_{OUT} = 2Vp-p	2nd harmonic		-78		dBc
			3rd harmonic		-82		
			Total harmonic distortion		-75		dB
Two-Tone, Third-Order Intermodulation Distortion	IP3	f1 = 10.0MHz, f2 = 10.1MHz, V_{OUT} = 1Vp-p			35		dBc
Input 1dB Compression Point		f_C = 10MHz, A_{VCL} = +2			11		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω			0.02		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω			0.02		%
Input Noise-Voltage Density	e_n	f = 10kHz			10		$nV/\sqrt{Hz}$
Input Noise-Current Density	i_n	f = 10kHz			1.3		$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}				1		pF
Disabled Output Capacitance	$C_{OUT (OFF)}$	MAX4018, EN_ = 0V			2		pF
Output Impedance	Z_{OUT}	f = 10MHz			6		Ω
Amplifier Enable Time	t_{ON}	MAX4018			100		ns
Amplifier Disable Time	t_{OFF}	MAX4018			1		µs
Amplifier Gain Matching		MAX4016/MAX4018/MAX4020, f = 10MHz, V_{OUT} = 20mVp-p			0.1		dB
Amplifier Crosstalk	X_{TALK}	MAX4016/MAX4018/MAX4020, f = 10MHz, V_{OUT} = 2Vp-p, R_S = 50Ω to ground			-95		dB

Note 1: The MAX4012EUT is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 2: Tested with V_{CM} = +2.5V.

Note 3: PSR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; for dual ±5V supply with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V; and for single +3.3V supply with V_{EE} = 0V, V_{CC} = +3.15V to +3.45V.

Note 4: Does not include the external feedback network's impedance.

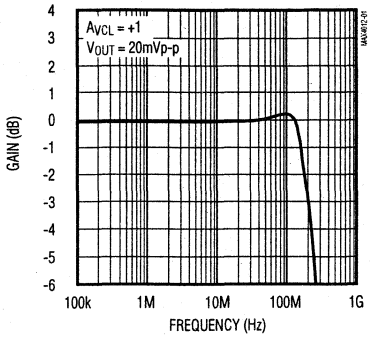
Note 5: Guaranteed by design.

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

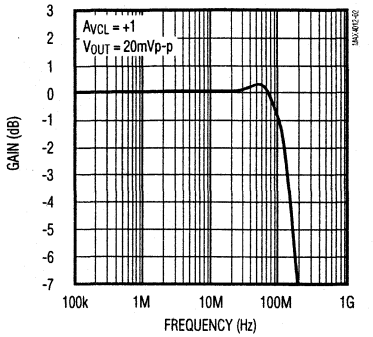
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

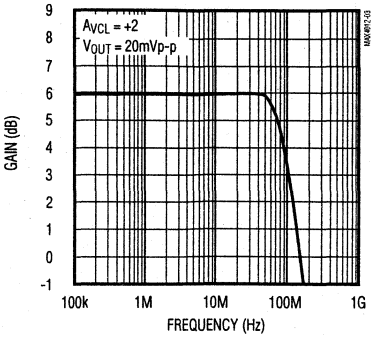
MAX4012
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



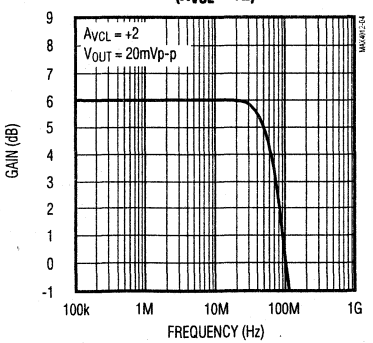
MAX4016/18/20
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



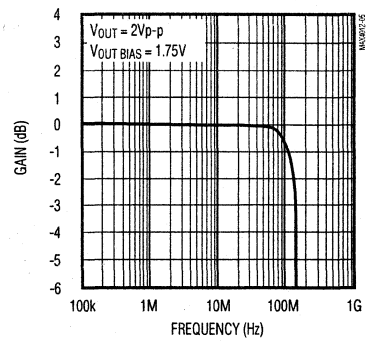
MAX4012
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



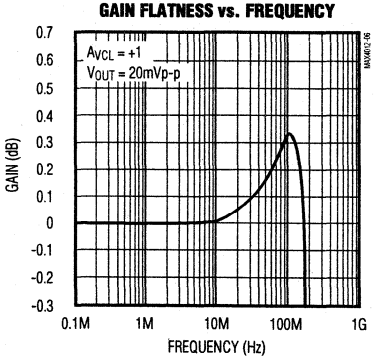
MAX4016/18/20
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



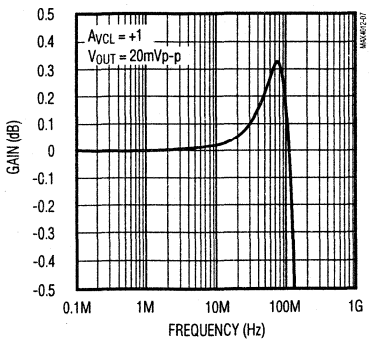
LARGE-SIGNAL GAIN vs. FREQUENCY



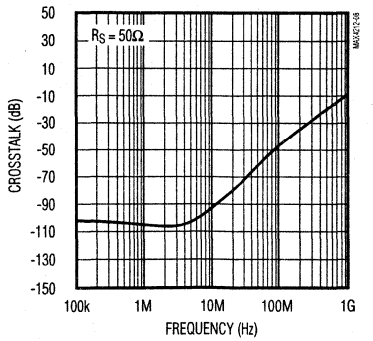
MAX4012
GAIN FLATNESS vs. FREQUENCY



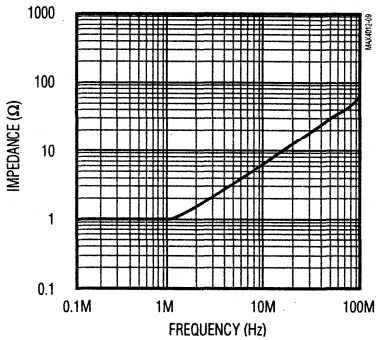
MAX4016/18/20
GAIN FLATNESS vs. FREQUENCY



MAX4016/18/20
CROSSTALK vs. FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE
vs. FREQUENCY

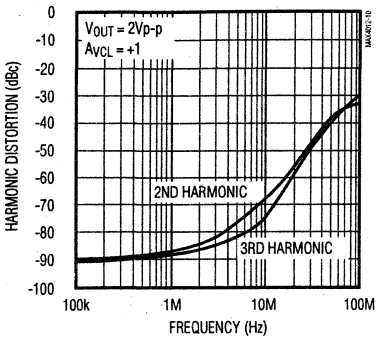


Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

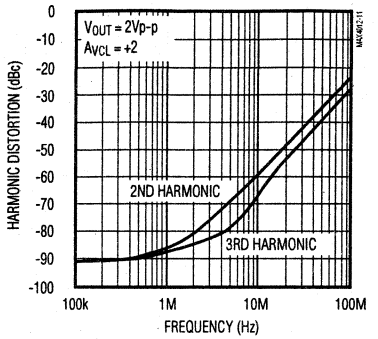
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

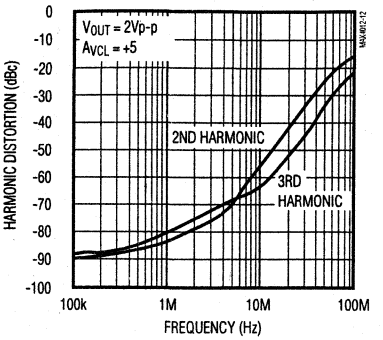
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +1)



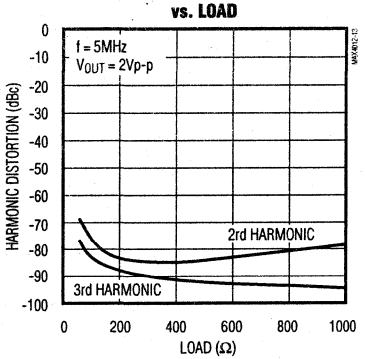
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +2)



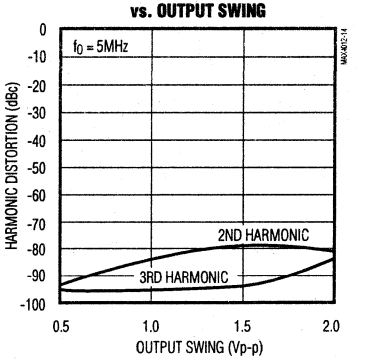
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +5)



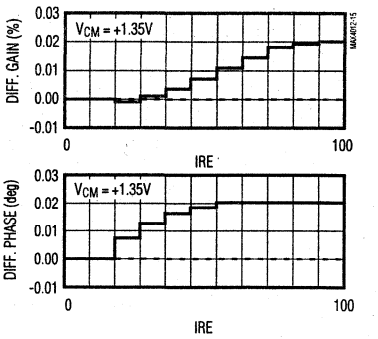
HARMONIC DISTORTION vs. LOAD



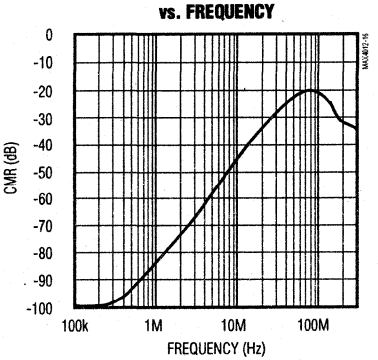
HARMONIC DISTORTION vs. OUTPUT SWING



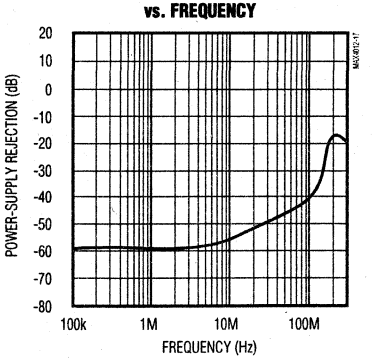
DIFFERENTIAL GAIN AND PHASE



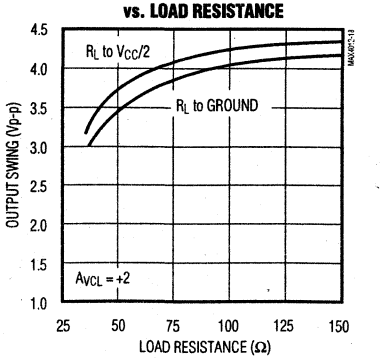
COMMON-MODE REJECTION vs. FREQUENCY



POWER-SUPPLY REJECTION vs. FREQUENCY



OUTPUT SWING vs. LOAD RESISTANCE

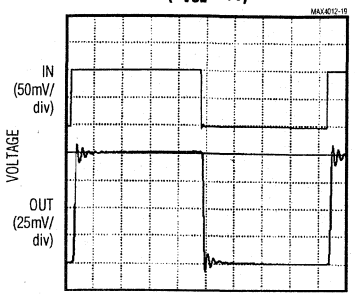


Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

Typical Operating Characteristics (continued)

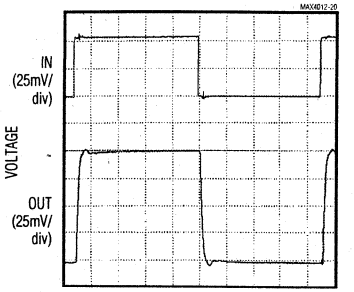
(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



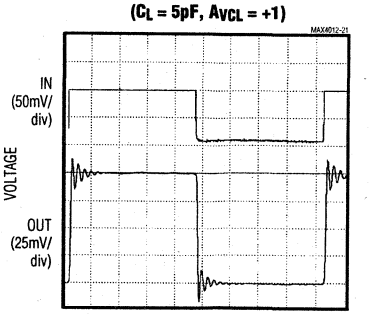
V_{CM} = +2.5V, R_L = 100Ω to GROUND

SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



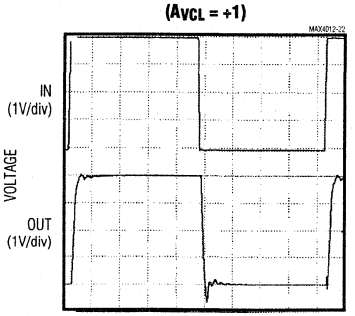
V_{CM} = +1.25V, R_L = 100Ω to GROUND

SMALL-SIGNAL PULSE RESPONSE (C_L = 5pF, A_{VCL} = +1)



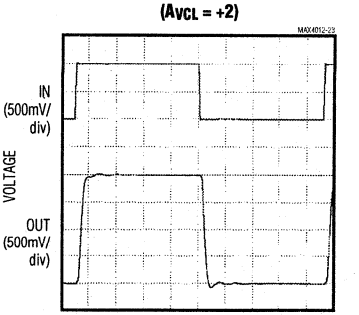
V_{CM} = +1.75V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



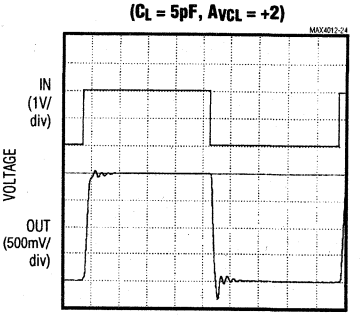
V_{CM} = +1.75V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



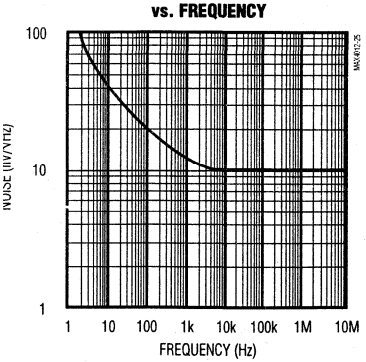
V_{CM} = 0.9V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (C_L = 5pF, A_{VCL} = +2)

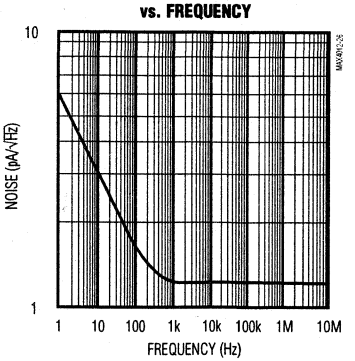


V_{CM} = +1.75V, R_L = 100Ω to GROUND

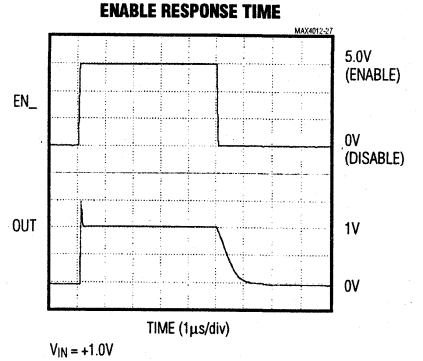
VOLTAGE-NOISE DENSITY vs. FREQUENCY



CURRENT-NOISE DENSITY vs. FREQUENCY



ENABLE RESPONSE TIME



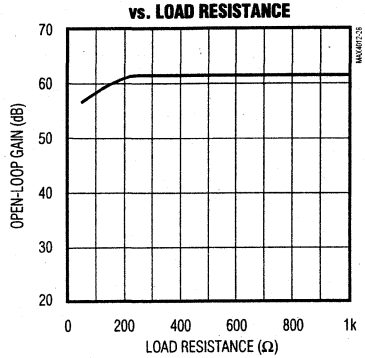
V_{IN} = +1.0V

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

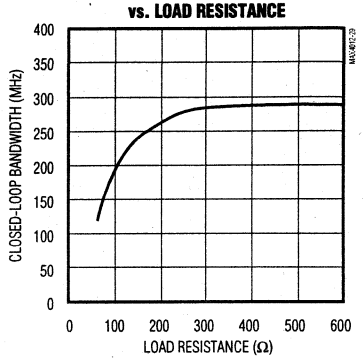
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

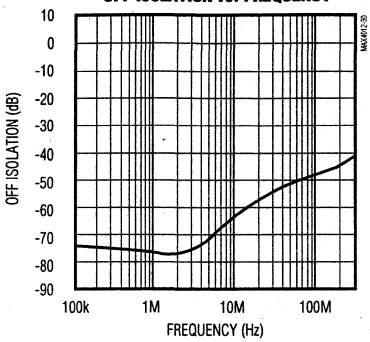
OPEN-LOOP GAIN vs. LOAD RESISTANCE



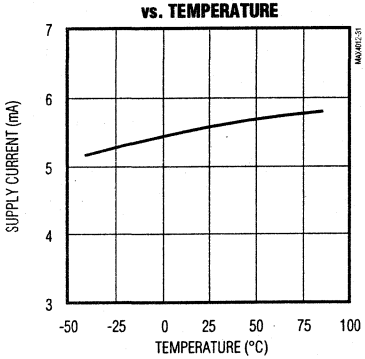
CLOSED-LOOP BANDWIDTH vs. LOAD RESISTANCE



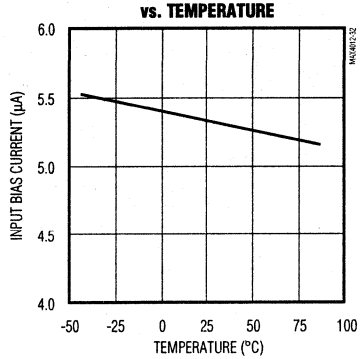
OFF ISOLATION vs. FREQUENCY



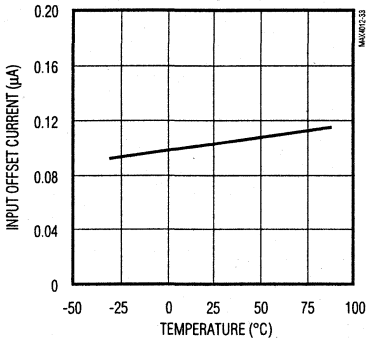
SUPPLY CURRENT vs. TEMPERATURE



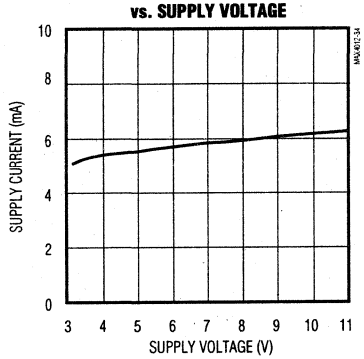
INPUT BIAS CURRENT vs. TEMPERATURE



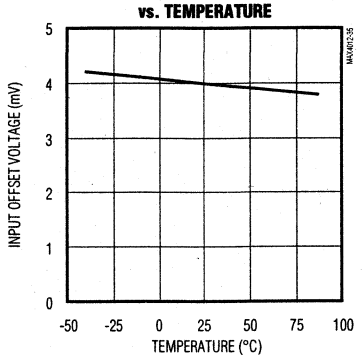
INPUT OFFSET CURRENT vs. TEMPERATURE



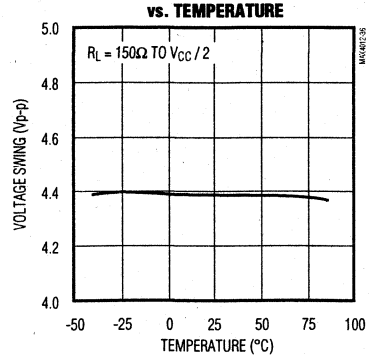
SUPPLY CURRENT vs. SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. TEMPERATURE



Pin Description

PIN						NAME	FUNCTION
MAX4012 SOT23-5	MAX4016 SO/µMAX	MAX4018		MAX4020			
		SO	QSOP	SO	QSOP		
—	—	—	8, 9	—	8, 9	N.C.	No Connect. Not internally connected. Tie to ground or leave open.
1	—	—	—	—	—	OUT	Amplifier Output
2	4	11	13	11	13	V_{EE}	Negative Power Supply or Ground (in single-supply operation)
3	—	—	—	—	—	IN+	Noninverting Input
4	—	—	—	—	—	IN-	Inverting Input
5	8	4	4	4	4	V_{CC}	Positive Power Supply
—	1	7	7	1	1	OUTA	Amplifier A Output
—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	7	8	10	7	7	OUTB	Amplifier B Output
—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	12	14	IND+	Amplifier D Noninverting Input
—	—	—	—	—	—	EN	Enable Amplifier
—	—	1	1	—	—	ENA	Enable Amplifier A
—	—	3	3	—	—	ENB	Enable Amplifier B
—	—	2	2	—	—	ENC	Enable Amplifier C

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

Detailed Description

The MAX4012/MAX4016/MAX4018/MAX4020 are single-supply, rail-to-rail, voltage-feedback amplifiers that employ current-feedback techniques to achieve 600V/µs slew rates and 200MHz bandwidths. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

The output voltage swing comes to within 50mV of each supply rail. Local feedback around the output stage assures low open-loop output impedance to reduce gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for ±120mA drive capability, while constraining total supply current to less than 7mA. The input stage permits common-mode voltages beyond the negative supply and to within 2.25V of the positive supply rail.

Applications Information

Choosing Resistor Values

Unity-Gain Configuration

The MAX4012/MAX4016/MAX4018/MAX4020 are internally compensated for unity gain. When configured for unity gain, the devices require a 24Ω resistor (R_F) in series with the feedback path. This resistor improves AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and inductance.

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration (R_F = R_G) using 1kΩ resistors, combined with 1pF of amplifier input capacitance and 1pF of PC board capacitance, causes a pole at 159MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 1kΩ resistors to 100Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load resistor. Table 1 shows suggested feedback, gain resistors, and bandwidth for several gain values in the configurations shown in Figures 1a and 1b.

Layout and Power-Supply Bypassing

These amplifiers operate from a single +3.3V to +11V power supply or from dual supplies to ±5.5V. For single-supply operation, bypass V_{CC} to ground with a 0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

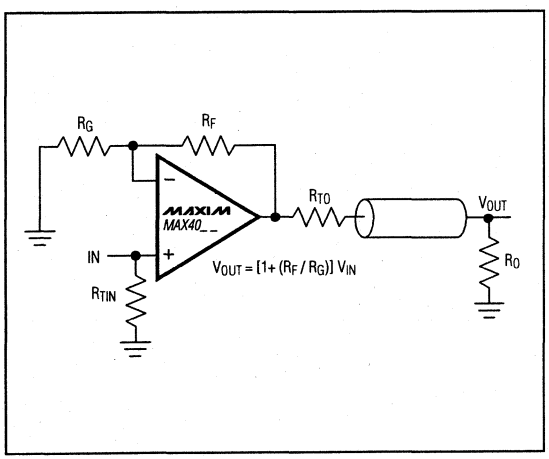


Figure 1a. Noninverting Gain Configuration

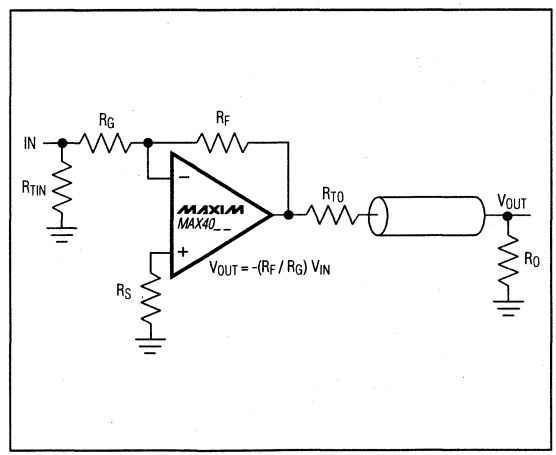


Figure 1b. Inverting Gain Configuration

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrap boards because they are too inductive.
- Don't use IC sockets because they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Rail-to-Rail Outputs, Ground-Sensing Input

The input common-mode range extends from (V_{EE} - 200mV) to (V_{CC} - 2.25V) with excellent common-mode rejection. Beyond this range, the amplifier output is a nonlinear function of the input, but does not undergo phase reversal or latchup.

The output swings to within 60mV of either power-supply rail with a 2kΩ load. The input ground-sensing and the rail-to-rail output substantially increase the dynamic range. With a symmetric input in a single +5V application, the input can swing 2.95Vp-p, and the output can swing 4.9Vp-p with minimal distortion.

Enable Input and Disabled Output

The enable feature (EN_) allows the amplifier to be placed in a low-power, high-output-impedance state. Typically, the EN_ logic low input current (I_{IL}) is small. However, as the EN voltage (V_{IL}) approaches the negative supply rail, I_{IL} increases (Figure 2). A single resistor connected as shown in Figure 3 prevents the rise in the logic-low input current. This resistor provides a feedback mechanism that increases V_{IL} as the logic input is brought to V_{EE}. Figure 4 shows the resulting input current (I_{IL}).

When the MAX4018 is disabled, the amplifier's output impedance is 35kΩ. This high resistance and the low 2pF output capacitance make this part ideal in RF/video multiplexer or switch applications. For larger arrays, pay careful attention to capacitive loading. See the *Output Capacitive Loading and Stability* section for more information.

Table 1. Recommended Component Values

COMPONENT	GAIN (V/V)									
	+1	-1	+2	-2	+5	-5	+10	-10	+25	-25
R_F (Ω)	24	500	500	500	500	500	500	500	500	1200
R_G (Ω)	∞	500	500	250	124	100	56	50	20	50
R_S (Ω)	—	0	—	0	—	0	—	0	—	0
R_{TIN} (Ω)	49.9	56	49.9	62	49.9	100	49.9	∞	49.9	∞
R_{TO} (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
Small-Signal -3dB Bandwidth (MHz)	200	90	105	60	25	33	11	25	6	10

Note: $R_L = R_O + R_{TO}$; R_{TIN} and R_{TO} are calculated for 50Ω applications. For 75Ω systems, R_{TO} = 75Ω; calculate R_{TIN} from the following equation:

$$R_{TIN} = \frac{75}{1-\frac{75}{R_G}}\Omega$$

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

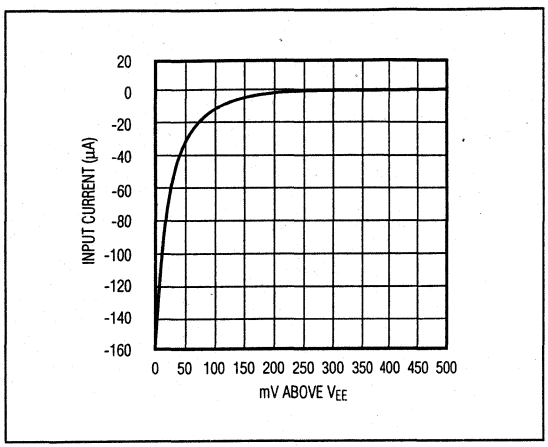


Figure 2. Enable Logic-Low Input Current vs. V_{IL}

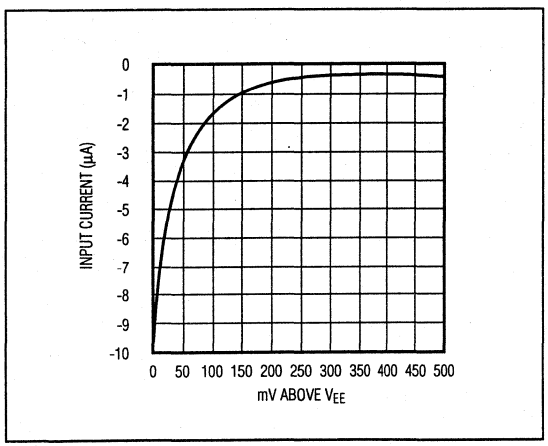


Figure 4. Enable Logic-Low Input Current vs. V_{IL} with 10kΩ Series Resistor

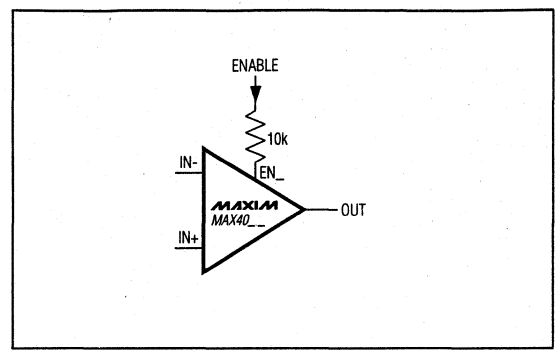


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

To implement the mux function, the outputs of multiple amplifiers can be tied together, and only the amplifier with the selected input will be enabled. All of the other amplifiers will be placed in the low-power shutdown mode, with their high output impedance presenting very little load to the active amplifier output. For gains of +2 or greater, the feedback network impedance of all the amplifiers used in a mux application must be considered when calculating the total load on the active amplifier output

Output Capacitive Loading and Stability

The MAX4012/MAX4016/MAX4018/MAX4020 are optimized for AC performance. They are not designed to drive highly reactive loads, which decreases phase margin and may produce excessive ringing and oscillation. Figure 5 shows a circuit that eliminates this problem. Figure 6 is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figure 7 shows how a capacitive load causes excessive peaking of the amplifier's frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 20Ω to 30Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Figure 8 shows the effect of a 27Ω isolation resistor on closed-loop response.

Coaxial cable and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the line's capacitance.

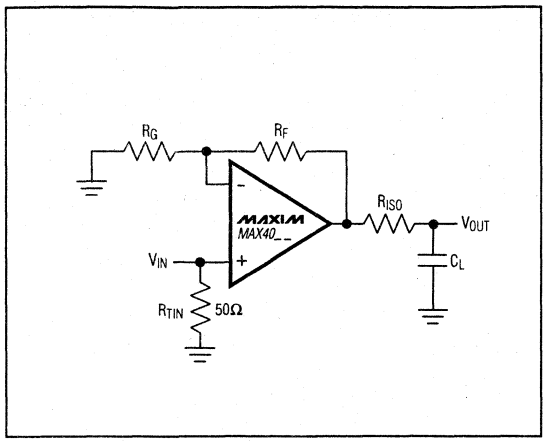


Figure 5. Driving a Capacitive Load through an Isolation Resistor

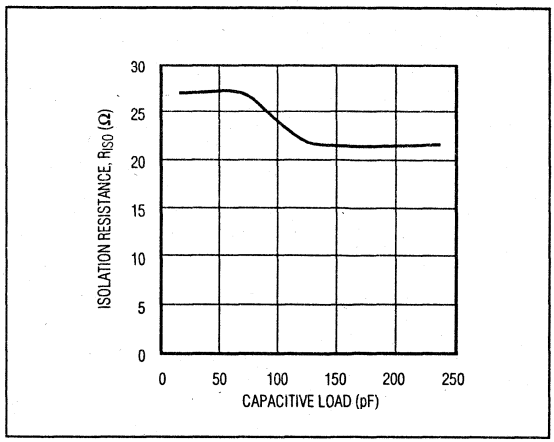


Figure 6. Capacitive Load vs. Isolation Resistance

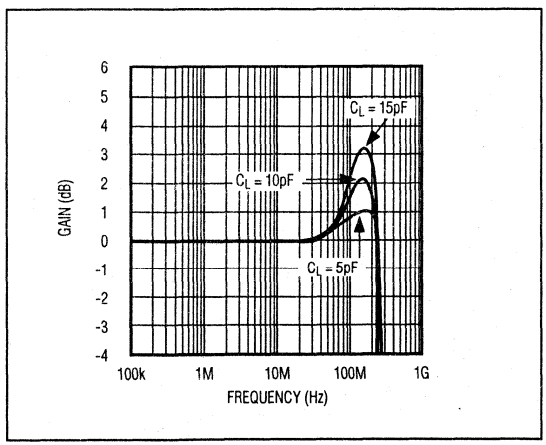


Figure 7. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

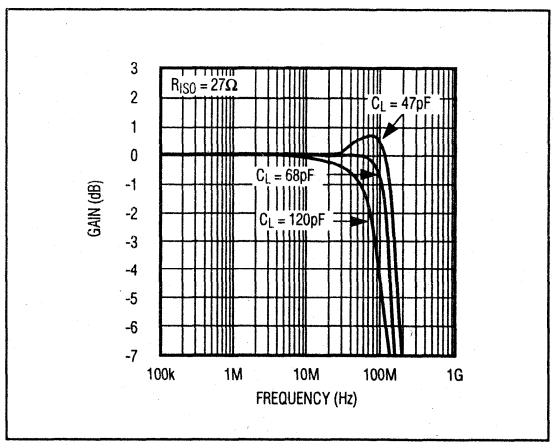
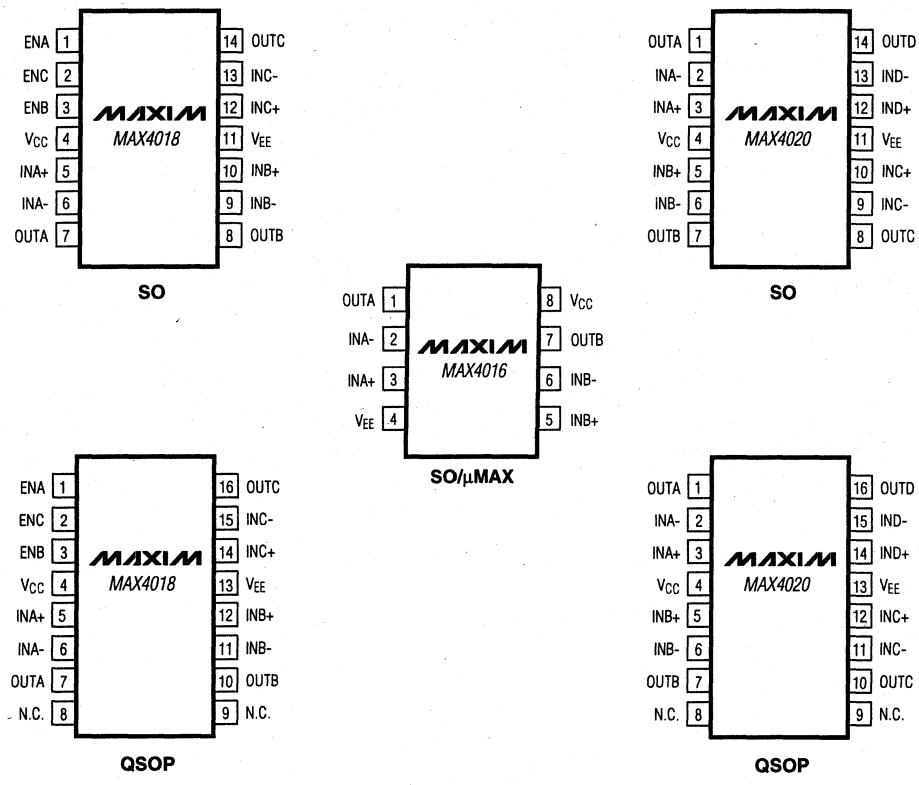


Figure 8. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Low-Cost, High-Speed, SOT23, Single-Supply Op Amps with Rail-to-Rail Outputs

Pin Configurations (continued)

TOP VIEW



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4018ESD	-40°C to +85°C	14 SO	—
MAX4018EEE	-40°C to +85°C	16 QSOP	—
MAX4020ESD	-40°C to +85°C	14 SO	—
MAX4020EEE	-40°C to +85°C	16 QSOP	—

Chip Information

PART	TRANSISTOR COUNT
MAX4012	95
MAX4016	190
MAX4018	299
MAX4020	362

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Cost, SOT23, High-Speed, Single-Supply Buffers with Rail-to-Rail Outputs

General Description

The MAX4014 family are precision, closed-loop, gain of +2, single-supply buffers featuring high slew rate, high output current drive, and low differential gain and phase errors. These devices operate from a +3.3V to +10V single supply or from ±1.65V to ±5V dual supplies. The input common-mode voltage range extends 200mV beyond the negative supply rail, and the output swings Rail-to-Rail®.

These devices require only 5.5mA of quiescent supply current while achieving a 200MHz -3dB bandwidth and a 600V/µs slew rate. Input voltage noise is only 10nV/√Hz, and input current noise is only 1.3pA/√Hz. These parts are ideal for low-power/low-voltage applications that require wide bandwidth, such as video, communications, and instrumentation systems. The MAX4019 has a disable feature that reduces power-supply current to 350µA and places the outputs into a high-impedance state. When disabled, these devices have a 1kΩ output impedance, making them well suited for multiplexing applications.

Applications

Battery-Powered Instruments
Video Line Driver
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems
Video Multiplexing Applications

Selector Guide

PART	No. OF AMPS	ENABLE	PIN-PACKAGE
MAX4014	1	No	5 SOT23
MAX4017	2	No	8 SO 8 µMAX
MAX4019	3	Yes	14 SO 16 QSOP
MAX4022	4	No	14 SO 16 QSOP

Rail-to-Rail is a trademark of Nippon Motorola Ltd.

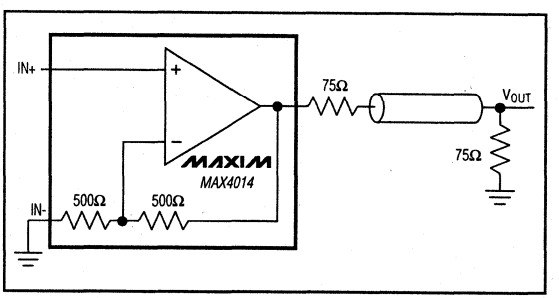
Features

- **High Speed:**
  200MHz -3dB Bandwidth (MAX4014)
  150MHz -3dB Bandwidth (MAX4017/19/22)
  30MHz 0.1dB Gain Flatness (MAX4014)
  600V/µs Slew Rate
- **+3.3V/+5V Single-Supply Operation**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase: 0.02%/0.02°**
- **Low Distortion at 5MHz:**
  -78dBc Spurious-Free Dynamic Range
  -75dB Total Harmonic Distortion
- **High Output Drive: ±120mA**
- **Low 5.5mA Supply Current**
- **Shutdown Capability: $I_S \leq 350\mu A$ (MAX4019)**
- **High Output Impedance in Off State (MAX4019)**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4014EUK-T	-40C to +85C	5 SOT23-5	ABZQ
MAX4017ESA	-40C to +85C	8 SO	—
MAX4017EUA	-40C to +85C	8 µMAX	—
MAX4019ESD	-40C to +85C	14 SO	—
MAX4019EEE	-40C to +85C	16 QSOP	—
MAX4022ESD	-40C to +85C	14 SO	—
MAX4022EEE	-40C to +85C	16 QSOP	—

Typical Operating Circuit



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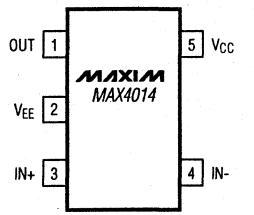
For small orders, phone 408-737-7600 ext. 3468.

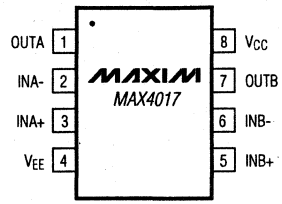
Low-Cost, SOT23, High-Speed, Single-Supply Buffers with Rail-to-Rail Outputs

Pin Configurations

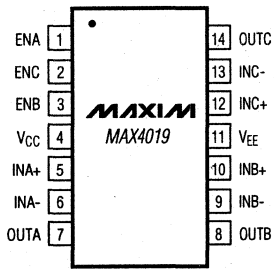
TOP VIEW



SOT23-5



SO/μMAX



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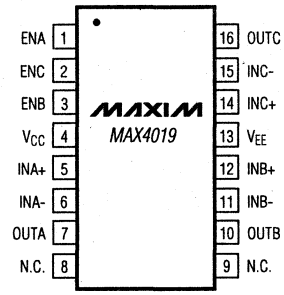
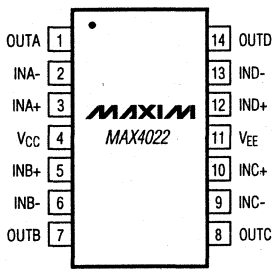
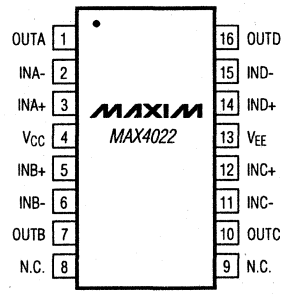


QSOP



SO



QSOP

N.C. = NOT INTERNALLY CONNECTED

MAXIM

High-Speed, Differential Line Driver

General Description

The MAX4142 differential line driver combines high-speed performance with fully symmetrical differential inputs and outputs. With an internally set +2V/V closed-loop gain, the MAX4142 is ideal for driving back-terminated cables and transmission lines.

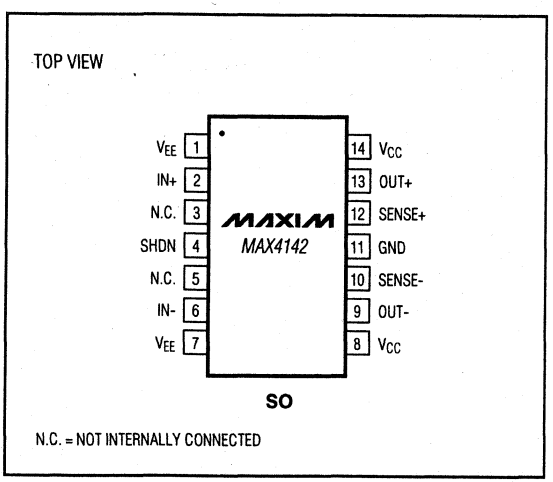
This device utilizes laser-trimmed, thin-film resistors and common-mode cancellation circuitry to deliver an outstanding 70dB at 10MHz common-mode rejection (CMR). Using current-feedback techniques, the MAX4142 achieves a 300MHz (A_V = +2V/V) bandwidth and a 2700 V/µs slew rate. Excellent differential gain/phase error and noise specifications make these amplifiers excellent choices for a wide variety of video and RF signal-processing applications.

The MAX4142 operates from ±5V power supplies and requires only 11mA of quiescent current. The output stage is capable of driving a 100Ω load to ±6V (differentially) or to ±3V (single-ended). The MAX4142 is available in a space saving 14-pin SO package.

Applications

Video Twisted-Pair Driver
Differential Pulse Amplifier
High-Speed Instrumentation Amplifier
Low-Noise Differential Receivers
Differential ADC Driver

Pin Configuration



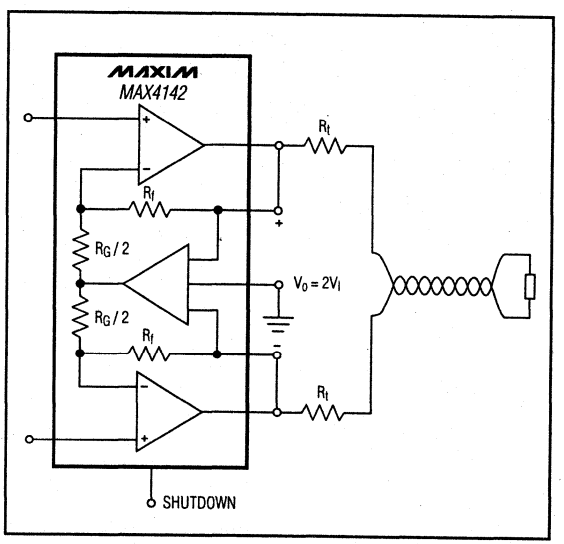
Features

- ♦ **300MHz Bandwidth (A_V = +2V/V)**
- ♦ **2700V/µs Slew Rate**
- ♦ **70dB at 10MHz CMR**
- ♦ **0.008%/0.03° Differential Gain/Phase**
- ♦ **±6V into 100Ω Output Drive**
- ♦ **800µA Shutdown Capability**
- ♦ **11mA Quiescent Supply Current**
- ♦ **Available in 14-pin, Narrow SO Package**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4142ESD	-40°C to +85°C	14 SO

Typical Application Circuit



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For small orders, phone 408-737-7600 ext. 3468.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

High-Speed, Differential Line Receivers

General Description

The MAX4144/MAX4145/MAX4146 differential line receivers offer unparalleled high-speed performance. Utilizing a three-op-amp instrumentation amplifier architecture, these devices have fully symmetrical differential inputs and a single-ended output. They operate from ±5V power supplies and are capable of driving a 150Ω load to ±3.5V. The MAX4144 has an internally set +2V/V closed-loop gain. The MAX4145 is optimized for gains from +1V/V to +10V/V, while the MAX4146 is optimized for gains from +10V/V to +100V/V. The MAX4145/MAX4146 require a single external resistor to set the closed-loop gain.

These amplifiers use laser-trimmed, matched thin-film resistors to deliver a 70dB at 10MHz common-mode rejection (CMR). Using current-feedback techniques, the MAX4144 achieves a 130MHz bandwidth and a 1000V/µs slew rate. The MAX4145 achieves a bandwidth of 150MHz and a slew rate of 600V/µs while operating with a closed-loop gain of +1V/V, and the MAX4146 features a bandwidth of 70MHz and a slew rate of 800V/µs with a gain of +10V/V. Excellent differential gain/phase and noise specifications make these amplifiers excellent choices for a wide variety of video and RF signal-processing applications.

For a complete differential transmission link, use the MAX4144/MAX4145/MAX4146 with the MAX4142/MAX4147 differential line drivers (see the MAX4147 data sheet for more information).

Applications

Differential-to-Single-Ended Conversion

Twisted-Pair-to-Coax Converter

High-Speed Instrumentation Amplifier

Data Acquisition

Medical Instrumentation

Features

MAX4144

- **2V/V Fixed Gain**
- **130MHz Bandwidth**
- **1000V/µs Slew Rate**
- **70dB CMR at 10MHz**
- **-90dBc SFDR (f_C = 10kHz)**
- **Low Differential Gain/Phase: 0.03%/0.03°**
- **800µA Shutdown**

MAX4145

- **External Gain Selection from +1V/V to +10V/V**
- **150MHz Bandwidth**
- **600V/µs Slew Rate**
- **70dB CMR at 10MHz**
- **-90dBc SFDR (f_C = 10kHz)**
- **Very Low Noise: 3.8nV/√Hz (G = 10V/V)**
- **800µA Shutdown**

MAX4146

- **External Gain Selection**
- **70MHz Bandwidth (A_V = 10V/V)**
- **800V/µs Slew Rate**
- **90dB CMR at 10MHz**
- **-82dBc SFDR (f_C = 10kHz)**
- **Very Low Noise: 3.5nV/√Hz (G = 100V/V)**
- **800µA Shutdown**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4144ESD	-40°C to +85°C	14 SO
MAX4145ESD	-40°C to +85°C	14 SO
MAX4146ESD	-40°C to +85°C	14 SO

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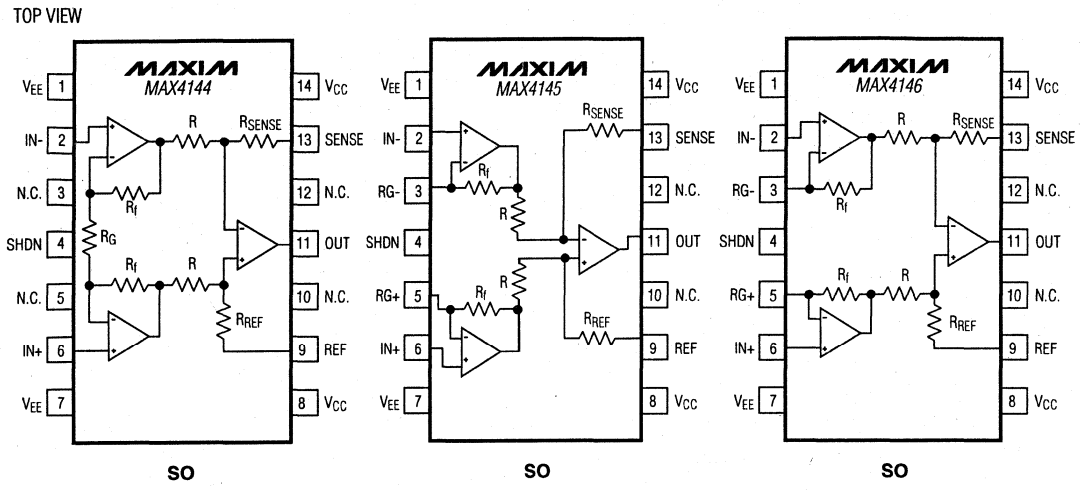
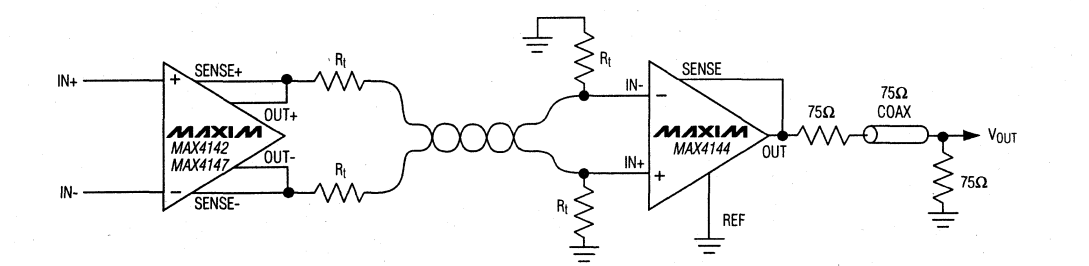
High-Speed, Differential Line Receivers

Pin Configurations/Functional Diagrams



Typical Application Circuit



TWISTED-PAIR-TO-COAX CABLE CONVERTER

19-1164; Rev 1; 3/97

EVALUATION KIT AVAILABLE

MAXIM

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

General Description

The MAX4158/MAX4159/MAX4258/MAX4259 are wideband, 2-channel, noninverting video amplifiers with input multiplexing, capable of driving ±2.5V signals into 50Ω or 75Ω loads. These devices are current-mode feedback amplifiers; gain is set by external feedback resistors. The MAX4158/MAX4159 are optimized for unity gain (0dB) with a -3dB bandwidth of 350MHz. The MAX4258/MAX4259 are optimized for gains of two (6dB) or more with a 250MHz -3dB bandwidth. These devices have low (0.01%/0.01°) differential gain and phase errors, and operate from ±5V supplies.

These devices are ideal for use in broadcast and graphics video systems because of their low, 2pF input capacitance, channel-to-channel switching time of only 20ns, and wide, 130MHz 0.1dB bandwidth. In addition, the combination of ultra-high speed and low power makes them suitable for use in general-purpose high-speed applications, such as medical imaging, industrial instrumentation, and communications systems.

The MAX4159/MAX4259 have address latching and high-impedance output disabling, allowing them to be incorporated into large switching arrays. They are available in 14-pin SO and 16-pin QSOP packages. The MAX4158/MAX4258 have no address latching or output disabling, but are available in space-saving 8-pin µMAX and SO packages.

Applications

Video-Signal Multiplexing
Video Crosspoint Switches
Pixel Switching
Coaxial Cable Drivers
Workstations
High-Definition TV (HDTV)
Broadcast Video
Multimedia Products
High-Speed Signal Processing

Features

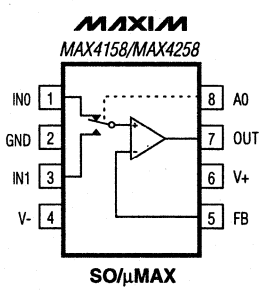
- **Excellent Video Specifications:**
  0.1dB Gain Flatness to 130MHz
  0.01%/0.01° Differential Gain/Phase Error
- **High Speed:**
  350MHz -3dB Bandwidth (MAX4158/4159)
  250MHz -3dB Bandwidth (MAX4258/4259)
  700V/µs Slew Rate (MAX4158/4159)
  1000V/µs Slew Rate (MAX4258/4259)
  20ns Settling Time to 0.1%
- **Fast Switching:**
  20ns Channel-Switching Time
  <70mV Switching Transient
- **Low Power: 100mW**
- **Directly Drive 75Ω or 50Ω Cables**
- **High Output Current Drive: >70mA**
- **Address Latch and High-Z Output Disable**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4158ESA	-40°C to +85°C	8 SO
MAX4158EUA	-40°C to +85°C	8 µMAX
MAX4159ESD	-40°C to +85°C	14 SO
MAX4159EEE	-40°C to +85°C	16 QSOP
MAX4258ESA	-40°C to +85°C	8 SO
MAX4258EUA	-40°C to +85°C	8 µMAX
MAX4259ESD	-40°C to +85°C	14 SO
MAX4259EEE	-40°C to +85°C	16 QSOP

Pin Configurations

TOP VIEW



SO/µMAX

MAX4158/MAX4258	
A0	**INPUT**
0	IN0
1	IN1

Pin Configurations continued at end of data sheet.

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For small orders, phone 408-737-7600 ext. 3468.

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V+ to GND) .....+6V
Negative Supply Voltage (V- to GND).....-6V
Amplifier Input Voltage (IN0 or IN1) .....(V- - 0.3V) to (V+ + 0.3V)
FB Current .....±20mA
Digital Input Voltage (A0, $\overline{EN}$, or LE).....-0.3V to (V+ + 0.3V)
Output Short Circuit to GND (Note 1).....Continuous
Output Short-Circuit Current to V+, V- (Note 1).....5sec

Continuous Power Dissipation (T_A = +70°C)
8-Pin SO (derate 5.88mW/°C above +70°C).....471mW
8-Pin µMAX (derate 4.10mW/°C above +70°C).....330mW
14-Pin SO (derate 8.33mW/°C above +70°C).....667mW
16-Pin QSOP (derate 8.33mW/°C above +70°C).....667mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Continuous power dissipation maximum rating must also be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V+ = +5V, V- = -5V, V_{IN} = 0V, V_{OUT} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply-Voltage Range	V+, V-	Inferred from the PSRR test		±4.5		±5.5	V
Input Voltage Range	V_{IN}	Inferred from the CMRR test		±2.5	±3.0		V
Input Offset Voltage (Either Channel)	V_{OS}				±1	±6	mV
Input Offset Voltage Temperature Coefficient (Either Channel)	TCV_{OS}				2		µV/°C
Input Bias Current (Channel On)	I_{IN}	T_A = +25°C			±2	±10	µA
		T_A = T_{MIN} to T_{MAX}				±18	
FB Pin Bias Current	I_{FB}	T_A = +25°C			±2	±12	µA
		T_A = T_{MIN} to T_{MAX}				±20	
Input Resistance	R_{IN}	V_{IN} = -2.5V to 2.5V	Channel on	100	550		kΩ
			Channel off	1	20		MΩ
FB Pin Input Resistance	$R_{IN(FB)}$				50		Ω
Output Resistance	R_{OUT}	f = 0Hz			40		mΩ
Disabled Output Resistance	$R_{OUT(d)}$	MAX4159/MAX4259 only, $\overline{EN}$ = 5V, V_{OUT} = -3.0V to 3.0V (Note 2)		1	10		MΩ
Open-Loop Transimpedance	Z_T	V_{OUT} = -2.5V to 2.5V, R_L = 100Ω		1.5	3.0		MΩ
DC Common-Mode Rejection Ratio	CMRR	V_{IN} = -2.5V to 2.5V		50	60		dB
DC Power-Supply Rejection Ratio	PSRR	Open loop, V+ = +4.5V to +5.5V, V- = -4.5V to -5.5V		60	78		dB
Output Voltage Swing	V_{OUT}	R_L = open circuit		±3.0	±4.0		V
		R_L = 50Ω		±2.5	±3.5		
Output Current	I_{OUT}	V_{OUT} = -2.5V to 2.5V		70	100		mA
Output Short-Circuit Current	I_{SC}	Sinking or sourcing to ground			120		mA
Positive Supply Current	I+	MAX4158/MAX4258			10.9	13.0	mA
		$\overline{EN}$ = GND, MAX4159/MAX4259			10.9	13.0	
		$\overline{EN}$ = V+, MAX4159/MAX4259			6.3	8.0	
Negative Supply Current	I-	MAX4158/MAX4258			9.9	12.0	mA
		$\overline{EN}$ = GND, MAX4159/MAX4259			9.9	12.0	
		$\overline{EN}$ = V+, MAX4159/MAX4259			5.0	7.0	

DC ELECTRICAL CHARACTERISTICS (continued)

(V+ = +5V, V- = -5V, V_{IN} = 0V, V_{OUT} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC CHARACTERISTICS (Note 3)						
Logic-Low Threshold	V_{IL}				0.8	V
Logic-High Threshold	V_{IH}		2.0			V
Logic-Low Input Current	I_{IL}	V_{IL} = 0V		-2	-20	µA
Logic-High Input Current	I_{IH}	V_{IH} = 5.5V, V+ = +5.5V		130	300	µA

AC ELECTRICAL CHARACTERISTICS—MAX4158/MAX4159

(V+ = +5V, V- = -5V, V_{IN} = 0V, V_{OUT} = 0V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS						
-3dB Bandwidth	BW	A_V = 0dB, V_{IN} = 20mVp-p (Note 4)		350		MHz
Bandwidth for ±0.1dB Gain Flatness	BW(0.1)	A_V = 0dB, V_{IN} = 20mVp-p (Note 4)		100		MHz
Full-Power Bandwidth	FPBW	A_V = 0dB, V_{OUT} = 2Vp-p (Note 4)		155		MHz
Slew Rate	SR	A_V = 0dB, V_{OUT} = 2Vp-p (Note 4)		700		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, A_V = 0dB (Note 4)		10		ns
Differential Gain Error	DG	A_V = 0dB (Notes 4, 5)		0.01		%
Differential Phase Error	DP	A_V = 0dB (Notes 4, 5)		0.01		degrees
Channel-to-Channel Crosstalk	Xtalk	f = 30MHz, R_S = 50Ω, A_V = 0dB, V_{IN} = ±2Vp-p (Note 4)		70		dB
Output Impedance	Z_{OUT}	f = 30MHz, A_V = 0dB (Note 4)		9		Ω
Total Harmonic Distortion	THD	f = 30MHz, V_{OUT} = 2Vp-p, A_V = 0dB (Note 4)		50		dBc
Off-Isolation (MAX4159 only)	A_{ISO}	f = 30MHz, A_V = 0dB, $\overline{EN}$ = 5V, V_{IN} = ±2Vp-p (Note 4)		105		dB
Output Capacitance	C_{OUT}			3		pF
Input Capacitance	C_{IN}	Channel on or off		2		pF
Input Voltage-Noise Density	e_n	f = 100kHz		2		nV/√Hz
Input Current-Noise Density	i_n	f = 100kHz		2		pA/√Hz
FB Current-Noise Density	i_n(FB)	f = 100kHz		22		pA/√Hz
SWITCHING CHARACTERISTICS						
Channel Switching Time	t_{SW}	(Notes 6, 7)		20		ns
Address Setup Time	t_S	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Address Hold Time	t_{TH}	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Latch Propagation Delay	t_{LPD}	(Note 6)		20		ns
Latch Pulse Width	t_{LPW}	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Enable Delay Time	t_{PDE}	(Notes 6, 9)		20		ns
Disable Delay Time	t_{PDD}	(Notes 6, 9)		20		ns
Switching Transient	V_{TRAN}	A_V = 0dB (Notes 4, 10)		±70		mV

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

AC ELECTRICAL CHARACTERISTICS—MAX4258/MAX4259

(V+ = +5V, V- = -5V, V_{IN} = 0V, V_{OUT} = 0V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

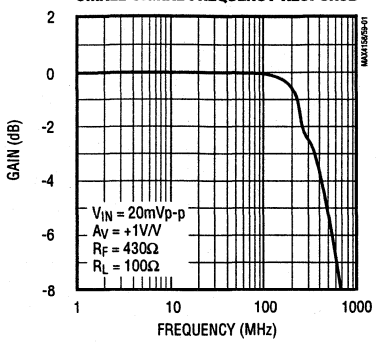
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AMPLIFIER CHARACTERISTICS						
-3dB Bandwidth	BW	A_V = 6dB, V_{IN} = 20mVp-p (Note 4)		250		MHz
Bandwidth for ±0.1dB Gain Flatness	BW(0.1)	A_V = 6dB, V_{IN} = 20mVp-p (Note 4)		130		MHz
Full-Power Bandwidth	FPBW	A_V = 6dB, V_{OUT} = 2Vp-p (Note 4)		200		MHz
Slew Rate	SR	A_V = 6dB, V_{OUT} = 2Vp-p (Note 4)		1000		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, A_V = 6dB (Note 4)		10		ns
Differential Gain Error	DG	A_V = 6dB (Notes 4, 5)		0.01		%
Differential Phase Error	DP	A_V = 6dB (Notes 4, 5)		0.02		degrees
Channel-to-Channel Crosstalk	Xtalk	f = 30MHz, R_S = 50Ω, A_V = 6dB, V_{IN} = ±1Vp-p (Note 4)		70		dB
Output Impedance	Z_{OUT}	f = 30MHz, A_V = 6dB (Note 4)		9		Ω
Total Harmonic Distortion	THD	f = 30MHz, V_{OUT} = 2Vp-p, A_V = 6dB (Note 4)		50		dBc
Off-Isolation (MAX4259)	A_{ISO}	f = 30MHz, A_V = 6dB, $\overline{EN}$ = 5V, V_{IN} = ±1Vp-p (Note 4)		110		dB
Output Capacitance	C_{OUT}			3		pF
Input Capacitance	C_{IN}	Channel on or off		2		pF
Input Voltage-Noise Density	e_n	f = 100kHz		2		nV/√Hz
Input Current-Noise Density	i_n	f = 100kHz		2		pA/√Hz
FB Current-Noise Density	i_n(FB)	f = 100kHz		22		pA/√Hz
SWITCHING CHARACTERISTICS						
Channel-Switching Time	t_{SW}	(Notes 6, 7)		20		ns
Address-Setup Time	t_S	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Address-Hold Time	t_{TH}	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Latch Propagation Delay	t_{LPD}	(Note 6)		20		ns
Latch Pulse Width	t_{LPW}	T_A = T_{MIN} to T_{MAX} (Notes 6, 8)	10			ns
Enable Delay Time	t_{PDE}	(Notes 6, 9)		20		ns
Disable Delay Time	t_{PDD}	(Notes 6, 9)		20		ns
Switching Transient	V_{TRAN}	A_V = 6dB (Notes 4, 10)		±90		mV

Note 2: Does not include external feedback network resistance.
Note 3: Applies to all digital input pins ($\overline{EN}$, LE, and A0).
Note 4: Specified with feedback network chosen for optimal AC performance. See Tables 1 and 2 for recommended component values.
Note 5: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE). IRE is a unit of video-signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.
Note 6: See timing diagram (Figure 5).
Note 7: Channel-switching time specified for switching between the two input channels; does not include signal rise/fall times for switching between channels with different input voltages.
Note 8: Guaranteed by design; not production tested.
Note 9: Output enable/disable delay times do not include amplifier output slewing times.
Note 10: Switching transient measured while switching between two grounded channels.

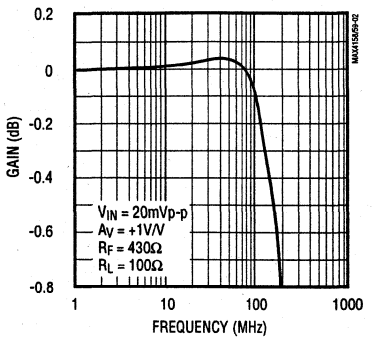
Typical Operating Characteristics

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

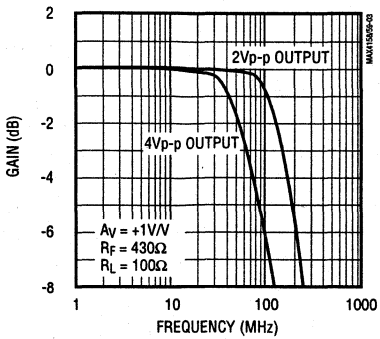
MAX4158/MAX4159
SMALL-SIGNAL FREQUENCY RESPONSE



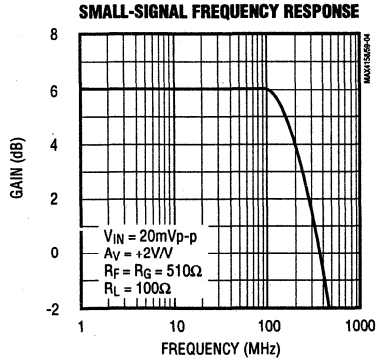
MAX4158/MAX4159
GAIN FLATNESS vs. FREQUENCY



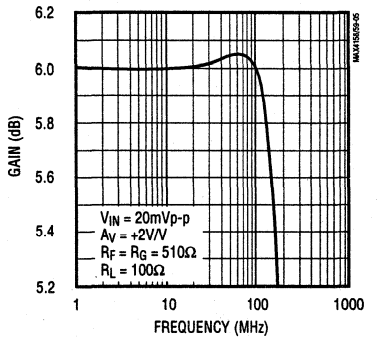
MAX4158/MAX4159
LARGE-SIGNAL FREQUENCY RESPONSE



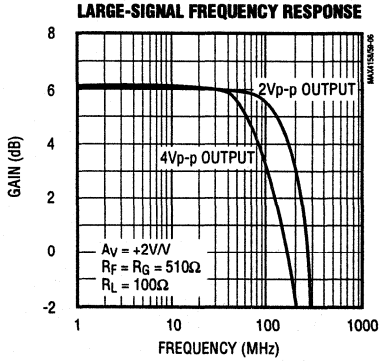
MAX4258/MAX4259
SMALL-SIGNAL FREQUENCY RESPONSE



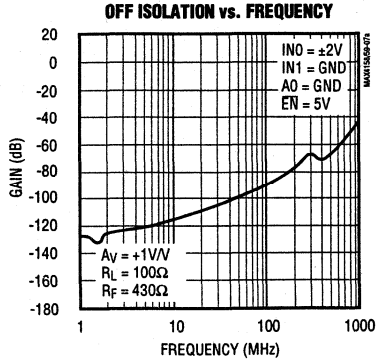
MAX4258/MAX4259
GAIN FLATNESS vs. FREQUENCY



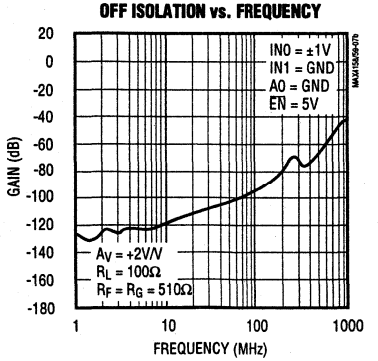
MAX4258/MAX4259
LARGE-SIGNAL FREQUENCY RESPONSE



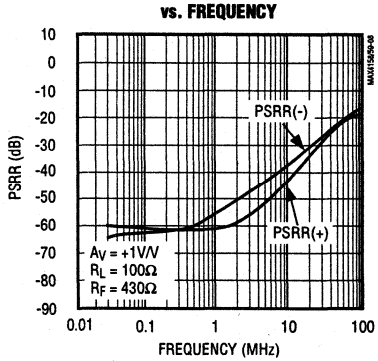
MAX4159
OFF ISOLATION vs. FREQUENCY



MAX4259
OFF ISOLATION vs. FREQUENCY



MAX4158/MAX4159
POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY

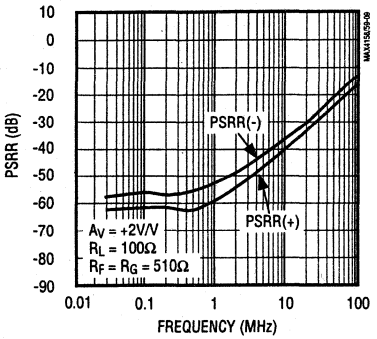


350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

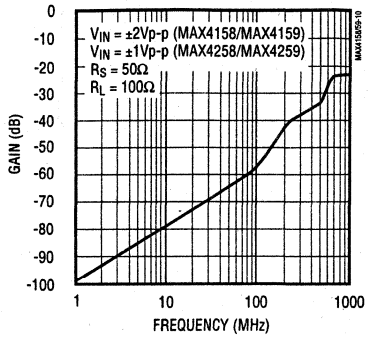
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

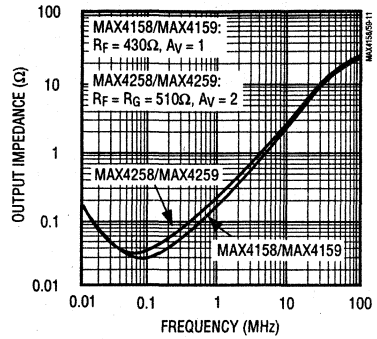
MAX4258/MAX4259 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



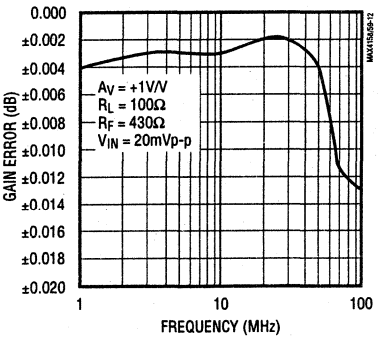
CROSSTALK vs. FREQUENCY



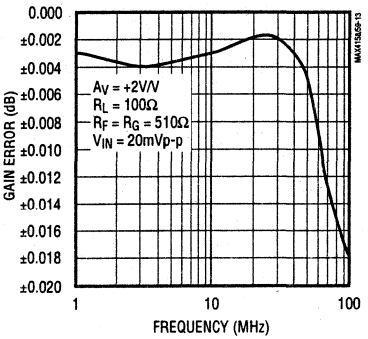
OUTPUT IMPEDANCE vs. FREQUENCY



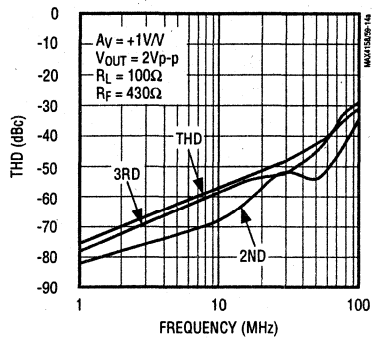
MAX4158/MAX4159 CHANNEL-TO-CHANNEL GAIN MATCHING vs. FREQUENCY



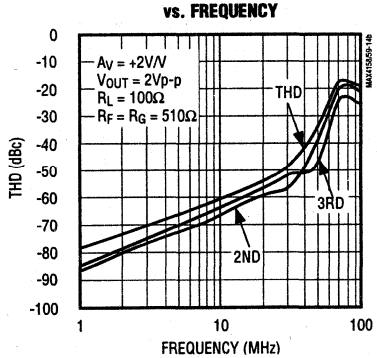
MAX4258/MAX4259 CHANNEL-TO-CHANNEL GAIN MATCHING vs. FREQUENCY



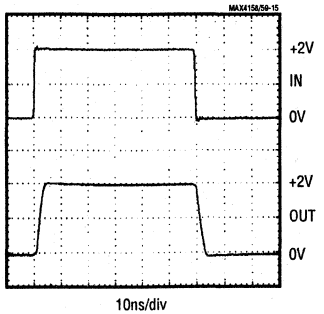
MAX4158/MAX4159 TOTAL HARMONIC DISTORTION vs. FREQUENCY



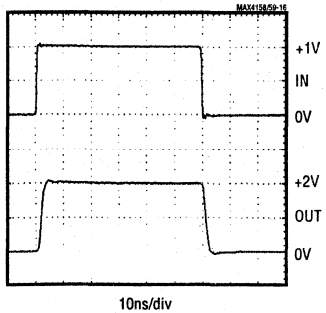
MAX4258/MAX4259 TOTAL HARMONIC DISTORTION vs. FREQUENCY



MAX4158/MAX4159 LARGE-SIGNAL PULSE RESPONSE



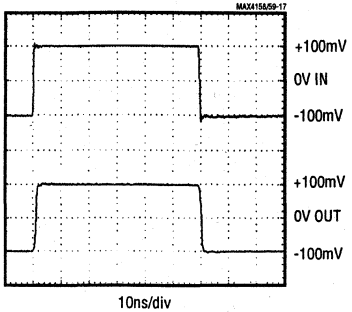
MAX4258/MAX4259 LARGE-SIGNAL PULSE RESPONSE



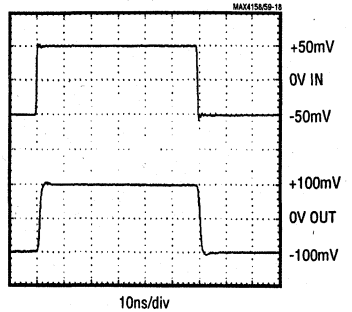
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

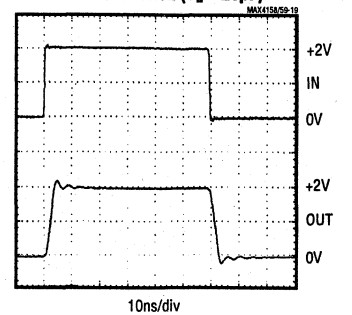
MAX4158/MAX4159 SMALL-SIGNAL PULSE RESPONSE



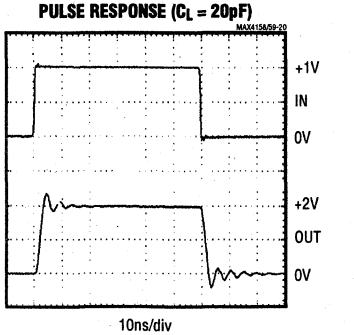
MAX4258/MAX4259 SMALL-SIGNAL PULSE RESPONSE



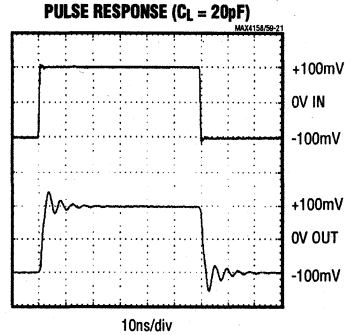
MAX4158/MAX4159 LARGE-SIGNAL PULSE RESPONSE (C_L = 20pF)



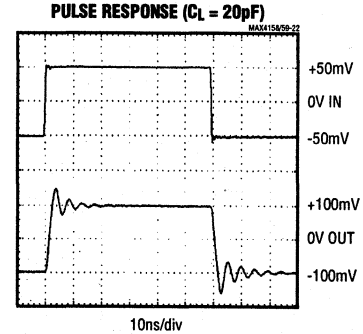
MAX4258/MAX4259 LARGE-SIGNAL PULSE RESPONSE (C_L = 20pF)



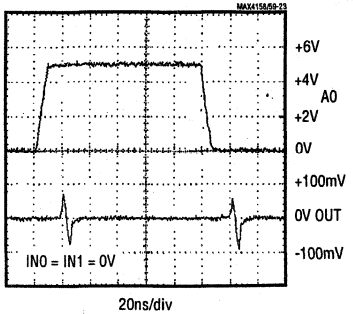
MAX4158/MAX4159 SMALL-SIGNAL PULSE RESPONSE (C_L = 20pF)



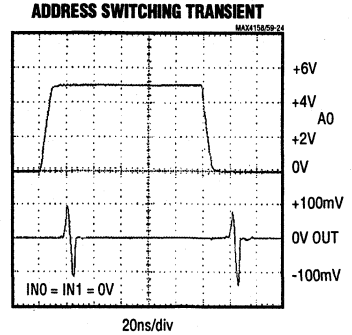
MAX4258/MAX4259 SMALL-SIGNAL PULSE RESPONSE (C_L = 20pF)



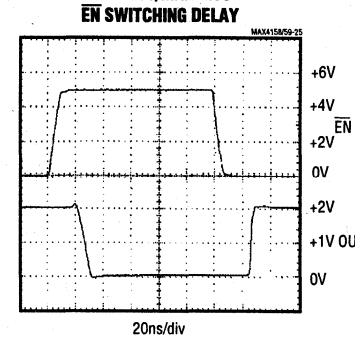
MAX4158/MAX4159 ADDRESS SWITCHING TRANSIENT



MAX4258/MAX4259 ADDRESS SWITCHING TRANSIENT



MAX4159/MAX4259 $\overline{EN}$ SWITCHING DELAY

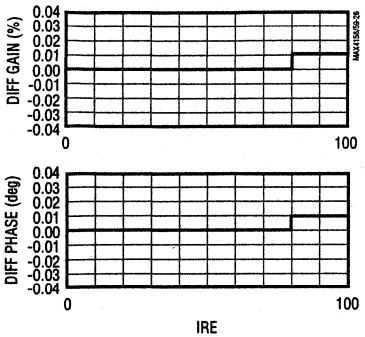


350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

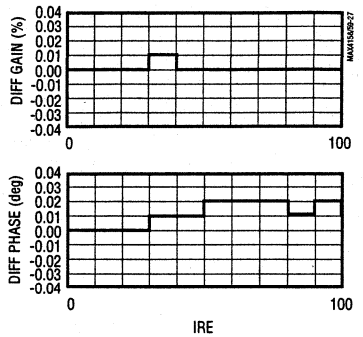
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

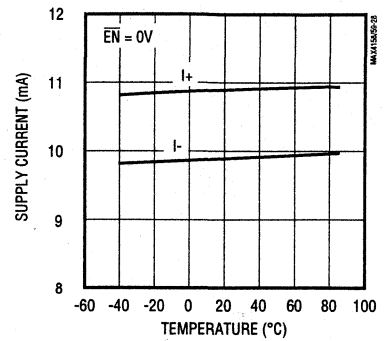
MAX4158/MAX4159 DIFFERENTIAL GAIN AND PHASE



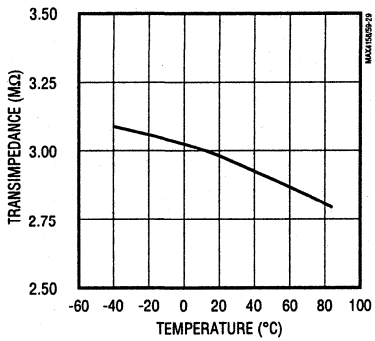
MAX4258/MAX4259 DIFFERENTIAL GAIN AND PHASE



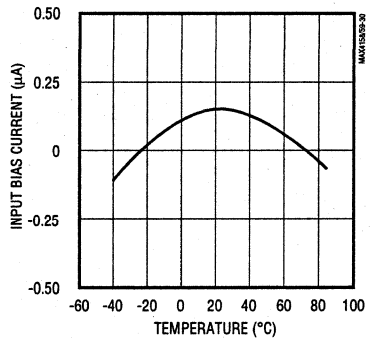
SUPPLY CURRENT vs. TEMPERATURE



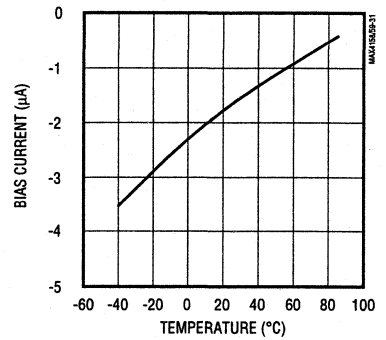
TRANSIMPEDANCE vs. TEMPERATURE



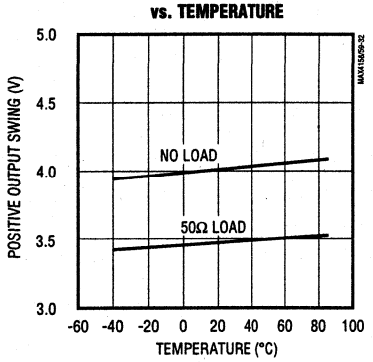
INPUT BIAS CURRENT vs. TEMPERATURE



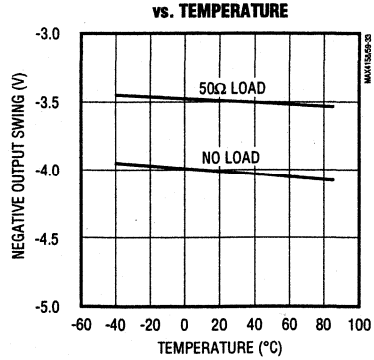
FB PIN BIAS CURRENT vs. TEMPERATURE



POSITIVE OUTPUT SWING vs. TEMPERATURE



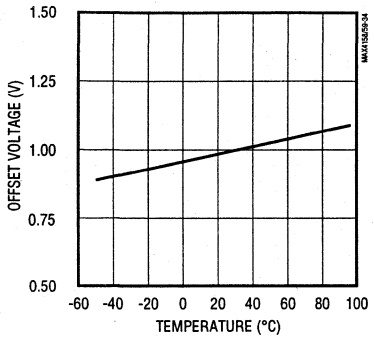
NEGATIVE OUTPUT SWING vs. TEMPERATURE



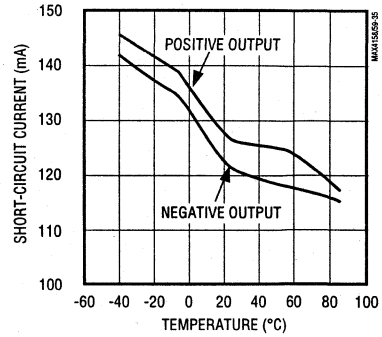
Typical Operating Characteristics (continued)

(V+ = +5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

INPUT OFFSET VOLTAGE vs. TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
MAX4158 MAX4258	MAX4159 MAX4259			
	SO	QSOP		
—	1	1	$\overline{EN}$	Output Enable Logic Input. Connect $\overline{EN}$ to logic low or leave open for normal operation. Connect to logic high to disconnect amplifier output (output is high impedance).
1	3	3	IN0	Amplifier Input, Channel 0
2	2, 4, 6, 8, 10	2, 4, 6, 9, 11	GND	Power Supply, Analog and Digital Ground. Connect GND to ground plane for best RF performance.
3	5	5	IN1	Amplifier Input, Channel 1
—	—	7, 15	N.C.	No Connect. Not internally connected. Connect to ground plane for best RF performance.
4	7	8	V-	Negative Power-Supply Voltage
5	9	10	FB	Amplifier Feedback Input
6	11	12	V+	Positive Power-Supply Voltage
7	12	13	OUT	Amplifier Output
8	13	14	A0	Channel-Address Logic Input (see *Truth Table*)
—	14	16	LE	Latch-Enable Logic Input (see *Truth Table*)

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

Detailed Description

The MAX4158/MAX4159 are optimized for closed-loop gains (A_{VCL}) of 1V/V (0dB) or greater; the MAX4258/MAX4259 are optimized for closed-loop gains of 2V/V (6dB) or greater. These low-power, high-speed, current-mode feedback amplifiers operate from ±5V supplies. They drive video loads (including 50Ω and 75Ω cables) with excellent distortion characteristics. Differential gain and phase errors are 0.01%/0.01° for MAX4158/MAX4159 and 0.01%/0.02° for MAX4258/MAX4259, respectively.

The input multiplexers feature very short switching times and small switching transients. They also have high input resistance and constant input capacitance, so overall input impedance can be set by external input terminating resistors. Each video input is isolated by an AC-ground pin, which reduces channel-to-channel capacitance and minimizes crosstalk.

The MAX4159/MAX4259 have address latching and an output enable function that places the output in a high-impedance state. These functions allow multiple mux/amps to be paralleled together to form larger switching arrays.

Truth Tables

Input Control Logic

LOGIC INPUTS		AMPLIFIER INPUT	FUNCTION
LE	A0		
0	0	IN0	Channel 0 selected
0	1	IN1	Channel 1 selected
1	X	[LAST]	Channel addresses latched; retains last input address.

X = Don't Care

MAX4159/MAX4259 Output Control Logic

LOGIC INPUT ($\overline{EN}$)	AMPLIFIER OUTPUT	FUNCTION
0	On	Output on
1	Off	Output off; high impedance

All logic levels ($\overline{EN}$, LE, and A0) default low (0) if left open circuit. Output disable is completely independent of input address and latch.

Applications Information

Theory of Operation

Since the MAX4158/MAX4159/MAX4258/MAX4259 are current-mode feedback amplifiers, their open-loop transfer function is expressed as a transimpedance, $\Delta V_{OUT}/\Delta I_{FB}$, or Z_T. The frequency behavior of this open-loop transimpedance is similar to the open-loop gain of a voltage-mode feedback amplifier. That is, it has a large DC value and decreases at approximately 6dB per octave at high frequency.

Analyzing the current-mode feedback amplifier in a gain configuration (Figure 1) yields the following transfer function:

$$V_{OUT} / V_{IN} = G \times Z_{T(S)} / (Z_{T(S)} + G \times R_{IN(FB)} + R_F)$$

where $G = A_{VCL} = 1 + R_F / R_G$.

At low gains, $G \times R_{IN(FB)} << R_F$. Therefore, unlike traditional voltage-mode feedback amplifiers, the closed-loop bandwidth is essentially independent of closed-loop gain. Note also that at low frequencies, $Z_T >> [G \times R_{IN(FB)} + R_F]$ so:

$$V_{OUT} / V_{IN} = G = 1 + R_F / R_G$$

Layout and Power-Supply Bypassing

The MAX4158/MAX4159/MAX4258/MAX4259 have extremely high bandwidth, and consequently require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

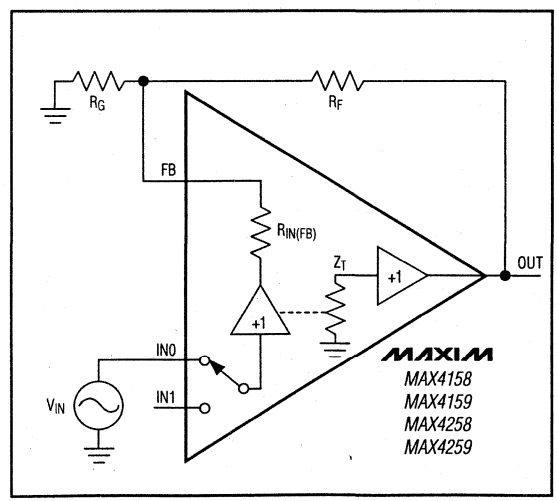


Figure 1. Current-Mode Feedback Amplifier

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible, with one exception: the feedback pin (FB) should have as low a capacitance to ground as possible. This means that there should be no ground plane under FB or under the components (R_F and R_G) connected to it. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Regardless of whether or not a constant-impedance board is used, it is best to observe the following guidelines when designing the board:

1) Do not use wire-wrap boards (they are much too inductive) or breadboards (they are much too capacitive).
2) Do not use IC sockets. IC sockets increase reactances.
3) Keep lines as short and as straight as possible. Do not make 90° turns; round all corners.
4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
5) Bear in mind that, in general, surface-mount components have shorter bodies and lower parasitic reactance, giving much better high-frequency performance than through-hole components.

The bypass capacitors should include a 10nF ceramic surface-mount capacitor between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10µF tantalum capacitor at the power-supply pins' points of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tantalum capacitor to the V+ and V- pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components.

Ground pins have been placed between input channels to minimize crosstalk between the two input channels. (The grounds extend inside the package all the way to the silicon.) These pins should be connected to a common ground plane on the PC board.

Input termination resistors and output back-termination resistors, if used, should be surface-mount types, and should be placed as close to the IC pins as possible.

Choosing Feedback and Gain Resistors

As with all current-mode feedback amplifiers, the frequency response of the MAX4158/MAX4159/MAX4258/MAX4259 is critically dependent on the value of the feedback resistor R_F. R_F, in conjunction with an internal compensation capacitor, forms the dominant pole in the feedback loop. Reducing R_F's value increases the pole frequency and the -3dB bandwidth, but also increases peaking due to interaction with other nondominant poles. Increasing R_F's value reduces peaking and bandwidth.

Tables 1 and 2 show optimal values for the feedback resistor (R_F) and gain-setting resistor (R_G) for all parts. Note that the MAX4258/MAX4259 offer superior AC performance for all gains except unity gain (0dB). These values provide optimal AC response using surface-mount resistors and good layout techniques. The MAX4159/MAX4259 evaluation kit provides a practical example of such layout techniques.

Stray capacitance at FB causes feedback resistor decoupling and produces peaking in the frequency-response curve. Keep the capacitance at FB as low as possible by using surface-mount resistors, and avoiding the use of a ground plane beneath or beside these resistors and the FB pin. Some capacitance is unavoidable; if necessary, its effects can be counteracted by adjusting R_F. 1% resistors are recommended to maintain consistency over a wide range of production lots.

Table 1. MAX4158/MAX4159 Bandwidth and Gain vs. Gain-Setting Resistors

GAIN		R_G (Ω)	R_F (Ω)	-3dB BW (MHz)	0.1dB BW (MHz)
(V/V)	(dB)				
1	0	∞	430	350	100
2	6	110	110	200	110
5	14	32.5	130	80	12
10	20	14.5	130	40	6

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

Table 2. MAX4258/MAX4259 Bandwidth and Gain vs. Gain-Setting Resistors

GAIN (V/V)	GAIN (dB)	R_G (Ω)	R_F (Ω)	-3dB BW (MHz)	0.1dB BW (MHz)
2	6	510	510	250	130
5	14	45	180	195	92
10	20	20	180	90	14

DC Errors and Noise

The MAX4158/MAX4159/MAX4258/MAX4259 output offset voltage, V_{OUT} (Figure 2) can be calculated with the following equation:

$$V_{OUT} = V_{OS} \times [1 + R_F / R_G] + I_B \times R_S \times [1 + R_F / R_G] + I_{FB} \times R_F$$

where:

V_{OS} = input offset voltage (in volts)

$1 + R_F / R_G$ = amplifier closed-loop gain (dimensionless)

I_B = input bias current (in amps)

I_{FB} = feedback input bias current (in amps)

R_G = gain-setting resistor (in ohms)

R_F = feedback resistor (in ohms)

R_S = source resistor (in ohms)

The following equation represents output noise density:

$$e_{n(OUT)} = (1+R_F/R_G) \times \sqrt{[i_n \times R_S]^2 + [i_{n(FB)} \times (R_F \parallel R_G)]^2 + [e_n]^2}$$

where:

i_n = input noise current density (in $A/\sqrt{Hz}$)

e_n = input noise voltage density (in $V/\sqrt{Hz}$)

The MAX4158/MAX4159/MAX4258/MAX4259 have a very low, $2nV/\sqrt{Hz}$ noise voltage. The current noise at the input (i_n) is $2pA/\sqrt{Hz}$, and the current noise at the feedback input ($i_{n(FB)}$) is $22pA/\sqrt{Hz}$.

An example of DC-error calculations, using the MAX4258 typical data and the typical operating circuit with $R_F = R_G = 510\Omega$ ($R_F \parallel R_G = 255\Omega$) and $R_S = 50\Omega$, gives:

$$V_{OUT} = [1 \times 10^{-3} \times (1 + 1)] + [2 \times 10^{-6} \times 50 \times (1 + 1)] + [2 \times 10^{-6} \times 510]$$

$$V_{OUT} = 3.22mV$$

Calculating total output noise in a similar manner yields the following:

$$e_{n(OUT)} = (1 + 1) \times \sqrt{\left[\left(2 \times 10^{-12}\right) \times 50\right]^2 + \left[\left(22 \times 10^{-12}\right) \times 255\right]^2 + \left(2 \times 10^{-9}\right)^2}$$

$$e_{n(OUT)} = 11.9nV/\sqrt{Hz}$$

With a 200MHz system bandwidth, this calculates to $168\mu V_{RMS}$ (approximately 1.01mVp-p, using the six-sigma calculation).

Video Line Driver

The MAX4158/MAX4159/MAX4258/MAX4259 are optimized to drive coaxial transmission lines when the cable is terminated at both ends (Figure 3). Cable frequency response may cause variations in the flatness of the signal.

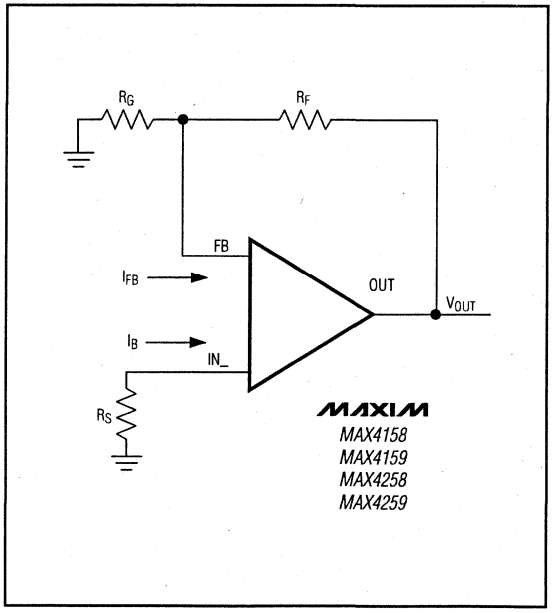


Figure 2. Output Offset Voltage

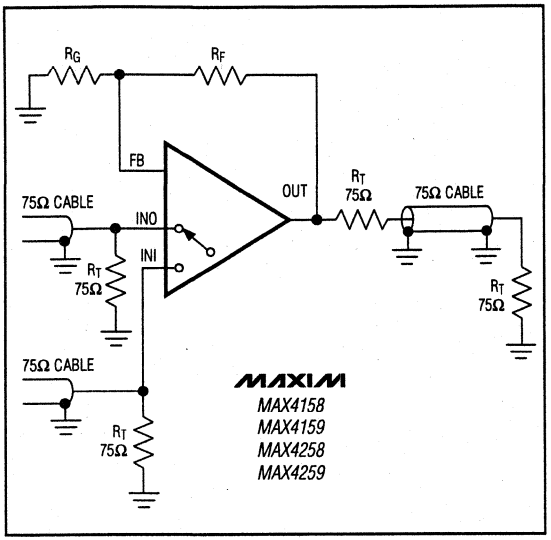


Figure 3. Video Line Driver

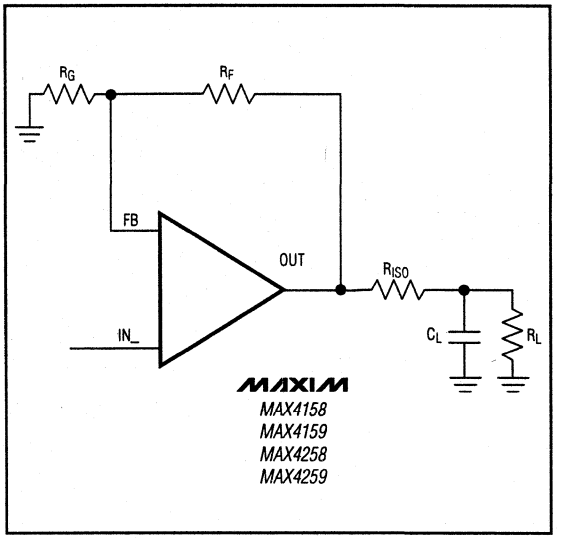


Figure 4. Using an Isolation Resistor (R_{ISO}) for High Capacitive Loads

Driving Capacitive Loads

A correctly terminated transmission line is purely resistive and presents no capacitive load to the amplifier. Consequently, the MAX4158/MAX4159/MAX4258/MAX4259 are optimized for AC performance and are not designed to drive highly capacitive loads. Reactive loads will decrease phase margin and may produce excessive ringing and oscillation (see *Typical Operating Characteristics*). The circuit of Figure 4 reduces this problem. The small (usually 5Ω to 20Ω) isolation resistor R_{ISO}, placed before the reactive load, prevents ringing and oscillation. At higher capacitive loads, AC performance is limited by the interaction of load capacitance with the isolation resistor.

350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

Input Voltage Range

The guaranteed input voltage range is ±2.5V. Exceeding this value can cause unpredictable results, including output clipping, excessive input current, and switching delays.

Multiplexer

The input multiplexer (mux) is controlled by TTL/CMOS-compatible address inputs (see *Truth Tables*.) There is no internal memory except the address latch (LE) on the MAX4159/MAX4259. If power is first applied with the latch enabled, IN0 is selected.

Input capacitance is a constant, low 2pF for either input channel, regardless of whether or not the channel is selected.

All logic levels ($\overline{EN}$, LE, and A0) default low if left open-circuit.

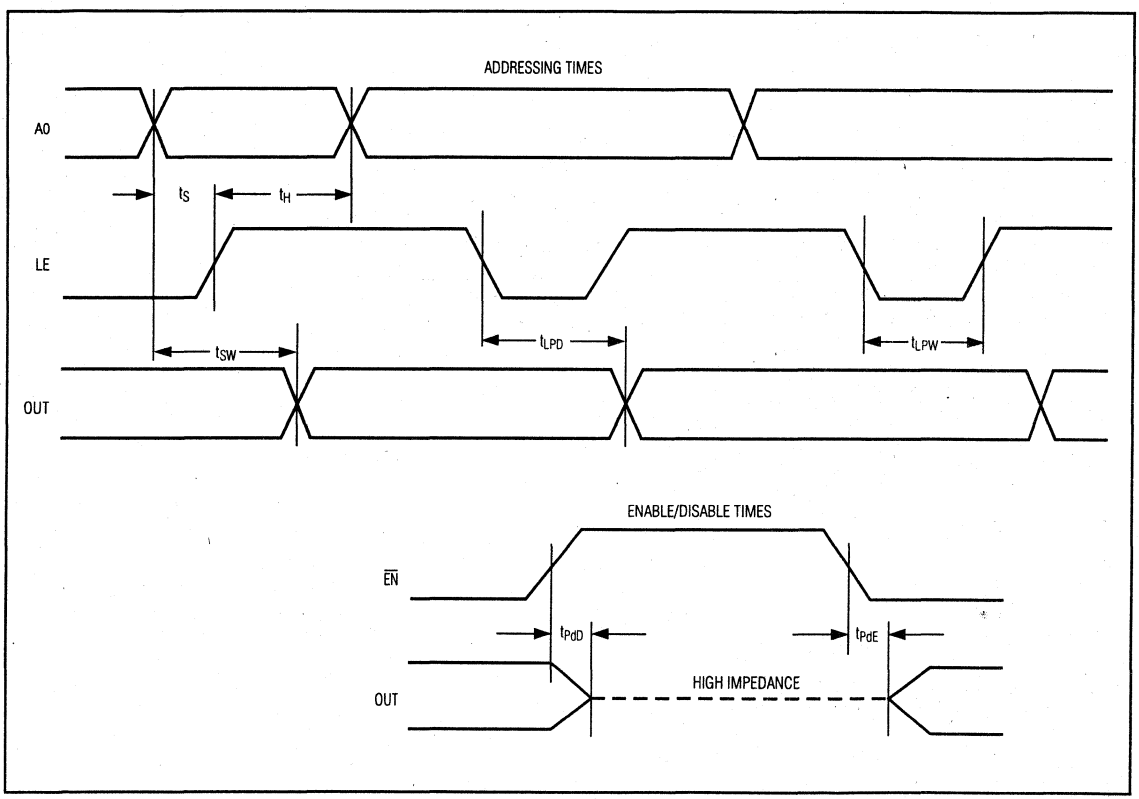
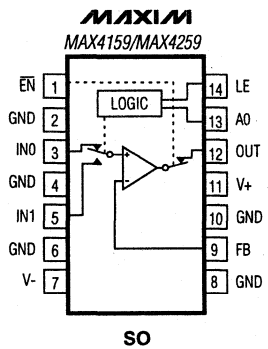


Figure 5. Switching Timing Diagram

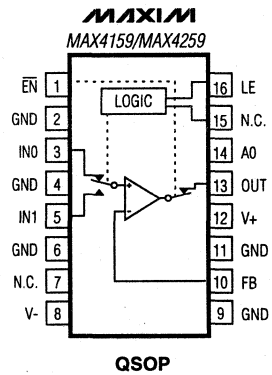
350MHz/250MHz, 2-Channel Video Multiplexer-Amplifiers

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



SO



QSOP

MAX4159/MAX4259		
LE	A0	INPUT
0	0	IN0
0	1	IN1
1	X	LAST

X = DON'T CARE

MAX4159/MAX4259	
$\overline{EN}$	OUTPUT
0	ON
1	OFF (HI-Z)

N.C. = NOT INTERNALLY CONNECTED

Chip Information

TRANSISTOR COUNT: 239

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

350MHz/250MHz, 4-Channel/8-Channel Video Multiplexer-Amplifiers

General Description

The MAX4160/MAX4161/MAX4260/MAX4261 are wideband 4-channel/8-channel noninverting video amplifiers with input multiplexing, capable of driving ±2.5V signals into 50Ω or 75Ω loads. These devices are current-feedback amplifiers; gain is set by external feedback resistors. The MAX4160/MAX4161 are optimized for unity gain (0dB) with a 350MHz -3dB bandwidth. The MAX4260/MAX4261 are optimized for gains of two (6dB) or more with a 250MHz -3dB bandwidth. These devices have low (0.01%/0.01°) differential gain and phase errors and operate from ±5V supplies.

These amplifiers are ideal for use in broadcast and graphics video systems because of their low 2pF input capacitance, channel-to-channel switching time of only 20ns, and wide 130MHz 0.1dB bandwidth. In addition, the combination of ultra-high speed and low power makes them suitable for use in general-purpose, high-speed applications such as medical imaging, industrial instrumentation, and communications systems.

These parts have address latching and high-impedance output disabling, allowing them to be incorporated into large arrays. The MAX4160/MAX4260 are available in 16-pin QSOP and narrow SO packages. The MAX4161/MAX4261 are available in 28-pin SSOP and wide SO packages.

Features

- **Excellent Video Specifications:**
  0.1dB Gain Flatness to 130MHz
  0.01%/0.01° Differential Gain/Phase Error
- **High Speed:**
  350MHz -3dB Bandwidth (MAX4160/MAX4161)
  250MHz -3dB Bandwidth (MAX4260/MAX4261)
  700V/µs Slew Rate (MAX4160/MAX4161)
  1000V/µs Slew Rate (MAX4260/MAX4261)
  20ns Settling Time to 0.1%
- **Fast Switching:**
  20ns Channel-Switching Time
  <70mV Switching Transient
- **Low Power:**
  120mW (MAX4160/MAX4260)
  310mW (MAX4161/MAX4261)
- **Directly Drives 75Ω or 50Ω Cables**
- **>70mA Output Current Drive**
- **Address Latch and High-Z Output Disable**

Applications

Video Signal Multiplexing
Video Crosspoint Switches
Pixel Switching
Coaxial Cable Drivers
Workstations
High Definition TV
Broadcast Video
Multimedia Products
High-Speed Signal Processing

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4160ESE	-40°C to +85°C	16 Narrow SO
MAX4160EEE	-40°C to +85°C	16 QSOP
MAX4161EWI	-40°C to +85°C	28 Wide SO
MAX4161EAI	-40°C to +85°C	28 SSOP
MAX4260ESE	-40°C to +85°C	16 Narrow SO
MAX4260EEE	-40°C to +85°C	16 QSOP
MAX4261EWI	-40°C to +85°C	28 Wide SO
MAX4261EAI	-40°C to +85°C	28 SSOP

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

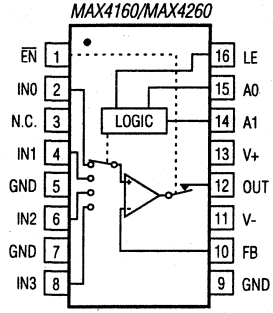
350MHz/250MHz, 4-Channel/8-Channel Video Multiplexer-Amplifiers

Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW

MAXIM

MAX4160/MAX4260



QSOP/SO

$\overline{EN}$	OUTPUT
0	ON
1	OFF (HI-Z)

MAX4160/MAX4260			
LE	A1	A0	INPUT
1	X	X	LAST
0	0	0	IN0
0	0	1	IN1
0	1	0	IN2
0	1	1	IN3

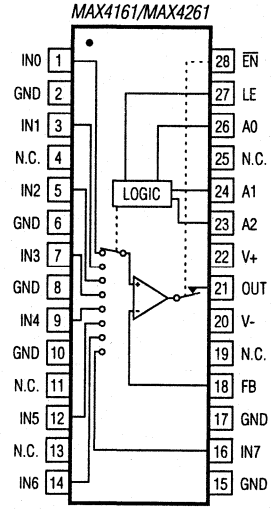
X = DON'T CARE

MAX4161/MAX4261				
LE	A2	A1	A0	INPUT
1	X	X	X	LAST
0	0	0	0	IN0
0	0	0	1	IN1
0	0	1	0	IN2
0	0	1	1	IN3
0	1	0	0	IN4
0	1	0	1	IN5
0	1	1	0	IN6
0	1	1	1	IN7

X = DON'T CARE

MAXIM

MAX4161/MAX4261



SSOP/SO

N.C. = NOT INTERNALLY CONNECTED

19-1221; Rev 1; 8/97

MAXIM

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

General Description

The MAX4180 family of current-feedback amplifiers combines high-speed performance, low distortion, and excellent video specifications with ultra-low-power operation in miniature packages. They operate from ±2.25V to ±5.5V dual supplies, or from a single +5V supply. They require only 1mA of supply current per amplifier while delivering up to ±60mA of output current drive. The MAX4180/MAX4182/MAX4183/MAX4186 are compensated for applications with a closed-loop gain of +2 (6dB) or greater, and provide a -3dB bandwidth of 240MHz and a 0.1dB bandwidth of 70MHz. The MAX4181/MAX4184/MAX4185/MAX4187 are compensated for applications with a +1 (0dB) or greater gain, and provide a -3dB bandwidth of 270MHz and a 0.1dB bandwidth of 60MHz.

The MAX4180–MAX4187 feature 0.08%/0.03° differential gain and phase errors, a 20ns settling time to 0.1%, and a 450V/µs slew rate, making them ideal for high-performance video applications. The MAX4180/MAX4181/MAX4183/MAX4185 have a low-power shutdown mode that reduces power-supply current to 135µA and places the outputs in a high-impedance state. This feature makes them ideal for multiplexing applications.

The single MAX4180/MAX4181 are offered in space-saving 6-pin SOT23 packages.

Applications

Portable/Battery-Powered Video/Multimedia Systems

Broadcast and High-Definition TV Systems

High-Speed A/D Buffers

CCD Imaging Systems

Medical Imaging

High-Definition Surveillance Video

Professional Cameras

Video Switching/ Multiplexing

Selector Guide

PART	No. OF AMPS	SHUTDOWN MODE	OPTIMIZED FOR
MAX4180	1	Yes	$A_V \geq 2$
MAX4181	1	Yes	$A_V \geq 1$
MAX4182	2	No	$A_V \geq 2$
MAX4183	2	Yes	$A_V \geq 2$
MAX4184	2	No	$A_V \geq 1$
MAX4185	2	Yes	$A_V \geq 1$
MAX4186	4	No	$A_V \geq 2$
MAX4187	4	No	$A_V \geq 1$

Features

- ♦ **Ultra-Low Supply Current: 1mA per Amplifier**
- ♦ **Shutdown Mode:**
  Outputs Placed in High-Z
  Supply Current Reduced to 135µA
- ♦ **Operate from a Single +5V Supply or Dual ±5V Supplies**
- ♦ **Wide Bandwidth:**
  270MHz -3dB Small-Signal Bandwidth (MAX4181/84/85/87)
- ♦ **450V/µs Slew Rate**
- ♦ **Fast, 20ns Settling Time to 0.1%**
- ♦ **Excellent Video Specifications:**
  Gain Flatness to 70MHz (MAX4180/82/83/86)
  0.08%/0.03° Differential Gain/Phase
- ♦ **Low Distortion:**
  -73dBc SFDR (f_C = 5MHz, V_{OUT} = 2Vp-p)
- ♦ **Available in Tiny Surface-Mount Packages:**
  6-Pin SOT23 (MAX4180/81)
  10-Pin µMAX (MAX4183/85)
  16-Pin QSOP (MAX4186/87)

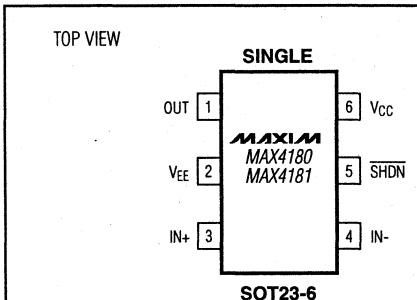
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4180EUT-T	-40°C to +85°C	6 SOT23-6	AAAB
MAX4180ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

8

Pin Configurations



Pin Configurations continued at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Analog Input Voltage ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Differential Input Voltage ..... ±2V
$\overline{SHDN}$ Input Voltage ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Short-Circuit Duration (OUT to GND, V_{CC} or V_{EE}) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin SOT23 (derate 7.10mW/°C above +70°C) 571mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
10-Pin µMAX (derate 5.60mW/°C above +70°C) 444mW
14-Pin SO (derate 8.33mW/°C above +70°C) 667mW
16-Pin QSOP (derate 8.30mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS—Dual Supplies

(V_{CC} = +5V, V_{EE} = -5V, V_{IN+} = 0V, $\overline{SHDN} \geq 3V$; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CM}	Guaranteed by CMRR test	±3.6	±3.9		V
Input Offset Voltage	V_{OS}	V_{CM} = 0V		±1.5	±7	mV
Input Offset-Voltage Drift	TC_{VOS}			±12		µV/°C
Input Offset-Voltage Matching		MAX4182–MAX4187		±1		mV
Input Bias Current (Positive Input)	I_{B+}			±1	±7	µA
Input Bias Current (Negative Input)	I_{B-}			±1	±12	µA
Input Resistance (Positive Input)	R_{IN+}	-3.6V ≤ V_{IN+} ≤ 3.6V, -1V ≤ (V_{IN+} - V_{IN-}) ≤ 1V	250	800		kΩ
Input Resistance (Negative Input)	R_{IN-}			160		Ω
Common-Mode Rejection Ratio	CMRR	-3.6V ≤ V_{CM} ≤ 3.6V	-50	-58		dB
Open-Loop Transresistance	T_R	R_L = 1kΩ, V_{OUT} = ±3.6V	0.8	3.0		MΩ
		R_L = 150Ω, V_{OUT} = ±2.5V	0.3	0.9		
Output Voltage Swing	V_{SW}	R_L = 1kΩ	±3.75	±4.0		V
		R_L = 150Ω	±3.0	±3.3		
		R_L = 100Ω		±3.0		
Output Current	I_{OUT}	R_L = 30Ω	±32	±60		mA
Output Short-Circuit Current	I_{SC}			±80		mA
Output Resistance	R_{OUT}			0.2		Ω
Disabled Output Leakage Current	$I_{OUT(OFF)}$	$\overline{SHDN} \leq V_{IL}$, V_{OUT} ≤ ±3V (Notes 2, 4)		±0.1	±6.0	µA
$\overline{SHDN}$ Logic Low Threshold	V_{IL}	(Notes 3, 4)			V_{CC} - 3.0	V
$\overline{SHDN}$ Logic High Threshold	V_{IH}	(Notes 3, 4)	V_{CC} - 2.0			V

DC ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{IN+} = 0V, $\overline{SHDN}$ ≥ 3V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Logic Input Bias Current	I_{IN}	$V_{EE} \le \overline{SHDN} \le V_{CC}$ (Note 4)			±0.1	±2.0	µA
Positive Power-Supply Rejection Ratio	PSRR+	V_{EE} = -5V, V_{CC} = 4.5V to 5.5V		60	71		dB
Negative Power-Supply Rejection Ratio	PSRR-	V_{CC} = 5V, V_{EE} = -4.5V to -5.5V		53	62		dB
Operating Supply Voltage	V_{CC}/V_{EE}			±2.25		±5.50	V
Quiescent Supply Current per Amplifier	I_S	R_L = ∞	MAX418_EUT		1.0	1.3	mA
			All other packages		1.0	1.2	
Shutdown Supply Current per Amplifier	$I_{S(OFF)}$	$\overline{SHDN}$ = 0V, R_L = ∞ (Note 4)			135	180	µA

DC ELECTRICAL CHARACTERISTICS—Single Supply

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, R_L to $V_{CC}/2$; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CM}		1.3 to 3.7	1.1 to 3.9		V
Input Offset Voltage	V_{OS}	V_{CM} = 2.5V		±1.5	±7	mV
Input Offset Voltage Drift	TC_{VOS}			±12		µV/°C
Input Offset Voltage Matching		MAX4182–MAX4187		±1		mV
Input Bias Current (Positive Input)	I_{B+}			±1	±7	µA
Input Bias Current (Negative Input)	I_{B-}			±1	±12	µA
Input Resistance (Positive Input)	R_{IN+}	1.3V ≤ V_{IN+} ≤ 3.7V, -1V ≤ (V_{IN+} - V_{IN-}) ≤ 1V	250	800		kΩ
Input Resistance (Negative Input)	R_{IN-}			160		Ω
Common-Mode Rejection Ratio	CMRR	1.3V ≤ V_{CM} ≤ 3.7V	-50	-58		dB
Open-Loop Transresistance	T_R	R_L = 1kΩ, V_{OUT} = 1.2V to 3.8V	0.8	2.5		MΩ
		R_L = 150Ω, V_{OUT} = 1.4V to 3.6V	0.275	0.9		
Output Voltage Swing	V_{SW}	R_L = 1kΩ	1.15 to 3.85	1.0 to 4.0		V
		R_L = 150Ω	1.35 to 3.65	1.2 to 3.8		
		R_L = 100Ω		1.3 to 3.7		

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

DC ELECTRICAL CHARACTERISTICS—Single Supply (continued)

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, R_L to $V_{CC}/2$; T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Current	I_{OUT}	R_L = 30Ω		±18	±30		mA
Output Short-Circuit Current	I_{SC}				±50		mA
Output Resistance	R_{OUT}				0.2		Ω
Disabled Output Leakage Current	$I_{OUT(OFF)}$	$\overline{SHDN}$ ≤ V_{IL}, 1.2V ≤ V_{OUT} ≤ 3.8V (Notes 2, 4)			±0.1	±4.0	µA
$\overline{SHDN}$ Logic-Low Threshold	V_{IL}	(Notes 3, 4)				V_{CC} - 3.0	V
$\overline{SHDN}$ Logic-High Threshold	V_{IH}	(Notes 3, 4)		V_{CC} - 2.0			V
$\overline{SHDN}$ Logic Input Bias Current	I_{IN}	0V ≤ $\overline{SHDN}$ ≤ V_{CC} (Note 4)			±0.1	±2.0	µA
Power-Supply Rejection Ratio	PSRR	V_{CC} = 4.5V to 5.5V		60	71		dB
Operating Supply Voltage	V_{CC}			4.5		5.5	V
Quiescent Supply Current per Amplifier	I_S	R_L = ∞	MAX418_EUT		1.0	1.25	mA
			All other packages		1.0	1.2	
Shutdown Supply Current per Amplifier	$I_{S(OFF)}$	$\overline{SHDN}$ = 0V, R_L = ∞ (Note 4)			135	180	µA

AC ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX4180/4182/4183/4186)

(V_{CC} = +5V, V_{EE} = -5V, V_{IN} = 0V, $\overline{SHDN}$ ≥ 3V, A_V = +2V/V; see Table 1 for R_F and R_G values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth (Note 5)	BW_{SS}	<0.5dB peaking	R_L=1kΩ	180	245		MHz
			R_L=150Ω		190		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p, R_L = 1kΩ			150		MHz
Bandwidth for 0.1dB Flatness (Note 5)	$BW_{0.1dB}$	R_L = 1kΩ		30	70		MHz
		R_L = 150Ω			70		
Slew Rate (Note 5)	SR	V_{OUT} = 2V step, R_L = 1kΩ	Rising edge	340	450		V/µs
			Falling edge	315	420		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, R_L = 1kΩ			20		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 2V step, R_L = 1kΩ			5		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		73		dBc
			R_L = 150Ω		57		
Second Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-83		dBc
			R_L = 150Ω		-68		
Third Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-73		dBc
			R_L = 150Ω		-57		

AC ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX4180/4182/4183/4186) (cont.)

(V_{CC} = +5V, V_{EE} = -5V, V_{IN} = 0V, $\overline{SHDN}$ ≥ 3V, A_V = +2V/V; see Table 1 for R_F and R_G values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Phase Error	DP	NTSC	R_L = 1kΩ		0.03		degrees
			R_L = 150Ω		0.30		
Differential Gain Error	DG	NTSC	R_L = 1kΩ		0.08		%
			R_L = 150Ω		0.01		
Input Noise Voltage Density	e_n	f = 10kHz			2		nV/√Hz
Input Noise Current Density	i_n	f = 10kHz	IN+		4		pA/√Hz
			IN-		5		
Input Capacitance (Negative Input)	C_{IN-}				1.5		pF
Output Impedance	Z_{OUT}	f = 10kHz			4.8		Ω
Disabled Output Capacitance	$C_{OUT(OFF)}$	$\overline{SHDN}$ ≤ V_{IL}, V_{OUT} ≤ ±3V (Notes 2, 4)			4		pF
Turn-On Time from $\overline{SHDN}$	t_{ON}	(Note 4)			40		ns
Turn-Off Time to $\overline{SHDN}$	t_{OFF}	(Note 4)			400		ns
Power-Up Time					200		µs
Off Isolation		$\overline{SHDN}$ ≤ 2V, R_L = 150Ω, f = 10MHz			-60		dB
Crosstalk		f = 10MHz, MAX4182/4183/4186			-60		dB
Gain Matching to 0.1dB		f = 10MHz, MAX4182/4183/4186			25		MHz

AC ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX4181/4184/4185/4187)

(V_{CC} = +5V, V_{EE} = -5V, V_{IN+} = 0V, $\overline{SHDN}$ ≥ 3V, A_V = 1V/V; see Table 1 for R_F values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth (Note 5)	BW_{SS}	<0.5dB peaking	R_L = 1kΩ	195	270		MHz
			R_L = 150Ω		205		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p, R_L = 1kΩ			90		MHz
Bandwidth for 0.1dB Flatness (Note 5)	$BW_{0.1dB}$	R_L = 1kΩ		20	60		MHz
		R_L = 150Ω			55		
Slew Rate (Note 5)	SR	V_{OUT} = 2V step, R_L = 1kΩ	Rising edge	250	320		V/µs
			Falling edge	200	265		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, R_L = 1kΩ			21		ns
Rise/Fall Time	t_R and t_F	V_{OUT} = 2V step, R_L = 1kΩ			5		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		57		dB
			R_L = 150Ω		66		
Second Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-70		dB
			R_L = 150Ω		-73		
Third Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-57		dB
			R_L = 150Ω		-66		
Differential Phase Error	DP	NTSC	R_L = 1kΩ		0.01		degrees
			R_L = 150Ω		0.48		

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Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

AC ELECTRICAL CHARACTERISTICS—Dual Supplies (MAX4181/4184/4185/4187) (cont.)

(V_{CC} = +5V, V_{EE} = -5V, V_{IN+} = 0V, $\overline{SHDN}$ ≥ 3V, A_V = +1V/V; see Table 1 for R_F values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Gain Error	DG	NTSC	R_L = 1kΩ		0.09		%
			R_L = 150Ω		0.16		
Input Noise Voltage Density	e_n	f = 10kHz			2		nV/√Hz
Input Noise Current Density	i_n	f = 10kHz	IN+		4		pA/√Hz
			IN-		5		
Input Capacitance (Negative Input)	C_{IN+}				1.5		pF
Output Impedance	Z_{OUT}	f = 10kHz			4.8		Ω
Disabled Output Capacitance	$C_{OUT(OFF)}$	$\overline{SHDN}$ ≤ V_{IL}, V_{OUT} ≤ ±3V (Notes 2, 4)			4		pF
Turn-On Time from $\overline{SHDN}$	t_{ON}	(Note 4)			50		ns
Turn-Off Time to $\overline{SHDN}$	t_{OFF}	(Note 4)			400		ns
Power-Up Time					200		µs
Off Isolation		$\overline{SHDN}$ ≤ 2V, R_L = 150Ω, f = 10MHz			-54		dB
Crosstalk		f = 10MHz, MAX4184/4185/4187			-60		dB
Gain Matching to 0.1dB		f = 10MHz, MAX4184/4185/4187			25		MHz

AC ELECTRICAL CHARACTERISTICS—Single Supply (MAX4180/4182/4183/4186)

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, A_V = +2V/V; see Table 1 for R_F and R_G values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth (Note 5)	BW_{SS}	<0.5dB peaking	R_L = 1kΩ	155	210		MHz
			R_L = 150Ω		165		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p, R_L = 1kΩ			110		MHz
Bandwidth for 0.1dB Flatness (Note 5)	$BW_{0.1dB}$	R_L = 1kΩ		20	50		MHz
		R_L = 150Ω			40		
Slew Rate (Note 5)	SR	V_{OUT} = 2V step, R_L = 1kΩ	Rising edge	260	340		V/µs
			Falling edge	220	300		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, R_L = 1kΩ			20		ns
Rise/Fall Time	t_R and t_F	V_{OUT} = 2V step, R_L = 1kΩ			6		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		72		dB
			R_L = 150Ω		57		
Second Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-80		dBc
			R_L = 150Ω		-76		
Third Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-72		dBc
			R_L = 150Ω		-57		
Differential Phase Error	DP	NTSC	R_L = 1kΩ		0.01		degrees
			R_L = 150Ω		0.35		

AC ELECTRICAL CHARACTERISTICS—Single Supply (MAX4180/4182/4183/4186) (cont.)

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, A_V = +2V/V; see Table 1 for R_F and R_G values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Gain Error	DG	NTSC	R_L = 1kΩ		0.10		%
			R_L = 150Ω		0.03		
Input Noise Voltage Density	e_n	f = 10kHz			2		nV/√Hz
Input Noise Current Density	i_n	f = 10kHz	IN+		4		pA/√Hz
			IN-		5		
Input Capacitance (Negative Input)	C_{IN-}				1.5		pF
Output Impedance	Z_{OUT}	f = 10kHz			4.8		Ω
Disabled Output Capacitance	$C_{OUT(OFF)}$	$\overline{SHDN}$ ≤ V_{IL}, 1.2V ≤ V_{OUT} ≤ 3.8V (Notes 2, 4)			4		pF
Turn-On Time from $\overline{SHDN}$	t_{ON}	(Note 4)			40		ns
Turn-Off Time to $\overline{SHDN}$	t_{OFF}	(Note 4)			400		ns
Power-Up Time					200		µs
Off Isolation		$\overline{SHDN}$ ≤ 2V, R_L = 150Ω, f = 10MHz			-60		dB
Crosstalk		f = 10MHz, MAX4182/4183/4186			-60		dB
Gain Matching to 0.1dB		f = 10MHz, MAX4182/4183/4186			25		MHz

AC ELECTRICAL CHARACTERISTICS—Single Supply (MAX4181/4184/4185/4187)

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, A_V = +1V/V; see Table 1 for R_F values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth (Note 5)	BW_{SS}	<0.5dB peaking	R_L = 1kΩ	175	220		MHz
			R_L = 150Ω		170		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p, R_L = 1kΩ			110		MHz
Bandwidth for 0.1dB Flatness (Note 5)	$BW_{0.1dB}$	R_L = 1kΩ		16	40		MHz
		R_L = 150Ω			30		
Slew Rate (Note 5)	SR	V_{OUT} = 2V step, R_L = 1kΩ	Rising edge	210	275		V/µs
			Falling edge	170	215		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step, R_L = 1kΩ			22		ns
Rise/ Fall Time	t_R and t_F	V_{OUT} = 2V step, R_L = 1kΩ			7		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		55		dB
			R_L = 150Ω		59		
Second Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-61		dBc
			R_L = 150Ω		-72		
Third Harmonic Distortion		f_C = 5MHz, V_{OUT} = 2Vp-p	R_L = 1kΩ		-55		dBc
			R_L = 150Ω		-59		
Differential Phase Error	DP	NTSC	R_L = 1kΩ		0.01		degrees
			R_L = 150Ω		0.35		

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

AC ELECTRICAL CHARACTERISTICS—Single Supply (MAX4181/4184/4185/4187) (cont.)

(V_{CC} = +5V, V_{EE} = 0V, V_{IN+} = 2.5V, $\overline{SHDN}$ ≥ 3V, A_V = +1V/V; see Table 1 for R_F values; T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Gain Error	DG	NTSC	R_L = 1kΩ		0.10		%
			R_L = 150Ω		0.03		
Input Noise Voltage Density	e_n	f = 10kHz			2		nV/√Hz
Input Noise Current Density	i_n	f = 10kHz	IN+		4		pA/√Hz
			IN-		5		
Input Capacitance (Negative Input)	C_{IN-}				1.5		pF
Output Impedance	Z_{OUT}	f = 10kHz			4.8		Ω
Disabled Output Capacitance	$C_{OUT(OFF)}$	$\overline{SHDN}$ ≤ V_{IL}, 1.2V ≤ V_{OUT} ≤ 3.8V (Notes 2, 4)			4		pF
Turn-On Time from $\overline{SHDN}$	t_{ON}	(Note 4)			40		ns
Turn-Off Time to $\overline{SHDN}$	t_{OFF}	(Note 4)			400		ns
Power-Up Time					200		µs
Off Isolation		$\overline{SHDN}$ ≤ 2V, R_L = 150Ω, f = 10MHz			-54		dB
Crosstalk		f = 10MHz, MAX4184/4185/4187			-60		dB
Gain Matching to 0.1dB		f = 10MHz, MAX4184/4185/4187			25		MHz

Note 1: The MAX418_EUT is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 2: Does not include current into the external-feedback network.

Note 3: Over operating supply-voltage range.

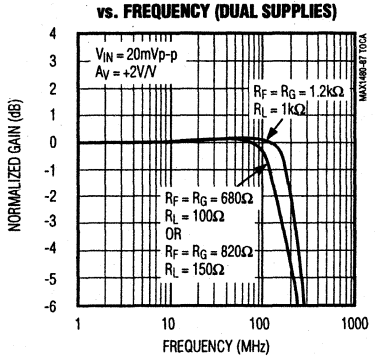
Note 4: Specification applies to MAX4180/MAX4181/MAX4183 and MAX4185.

Note 5: The AC specifications shown are not measured in a production test environment. The minimum AC specifications given are based on the combination of worst-case design simulations along with a sample characterization of units. These minimum specifications are for design guidance only and are not intended to guarantee AC performance (see AC *Testing/Performance*). For 100% testing of those parameters, contact the factory.

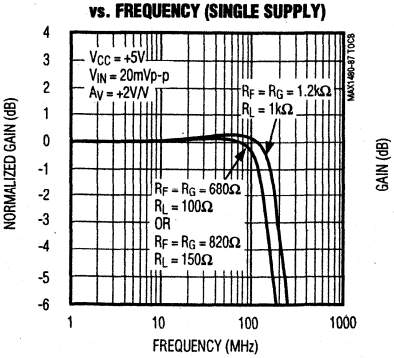
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

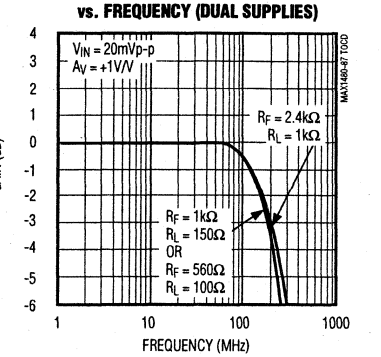
MAX4180 SMALL-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



MAX4180 SMALL-SIGNAL GAIN vs. FREQUENCY (SINGLE SUPPLY)



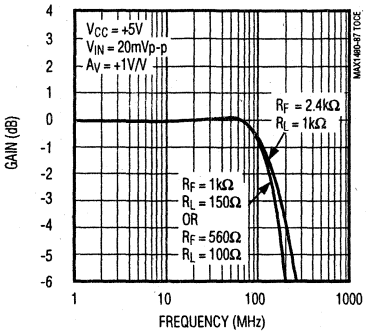
MAX4181 SMALL-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



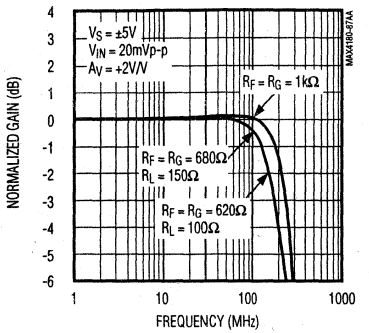
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

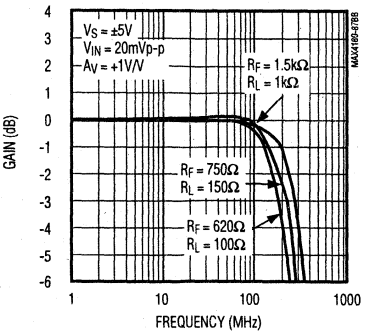
MAX4181 SMALL-SIGNAL GAIN vs. FREQUENCY (SINGLE SUPPLY)



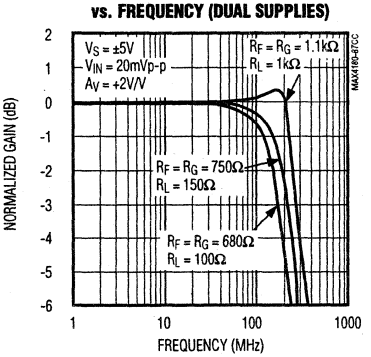
MAX4182/MAX4183 SMALL-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



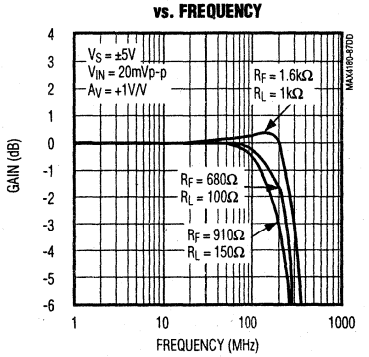
MAX4184/MAX4185 SMALL-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



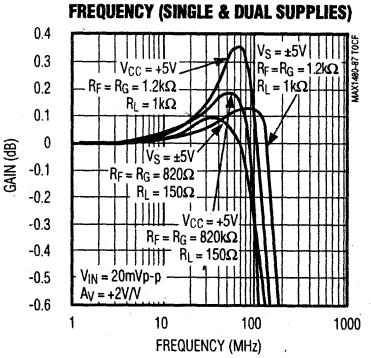
MAX4186 SMALL-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



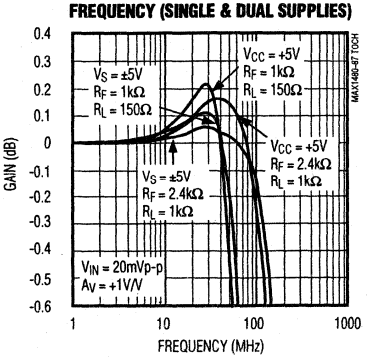
MAX4187 SMALL-SIGNAL GAIN vs. FREQUENCY



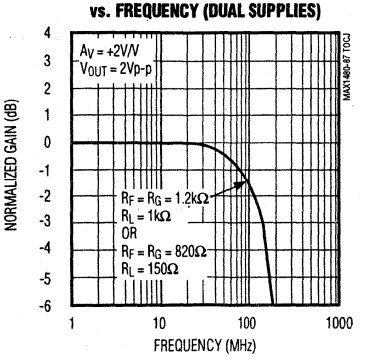
MAX4180 GAIN FLATNESS vs. FREQUENCY (SINGLE & DUAL SUPPLIES)



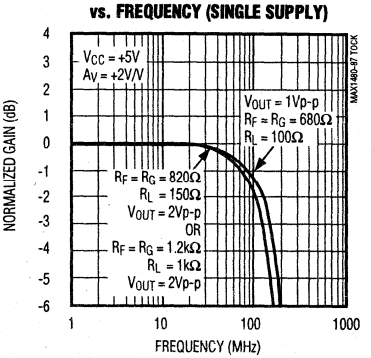
MAX4181 GAIN FLATNESS vs. FREQUENCY (SINGLE & DUAL SUPPLIES)



MAX4180 LARGE-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



MAX4180 LARGE-SIGNAL GAIN vs. FREQUENCY (SINGLE SUPPLY)



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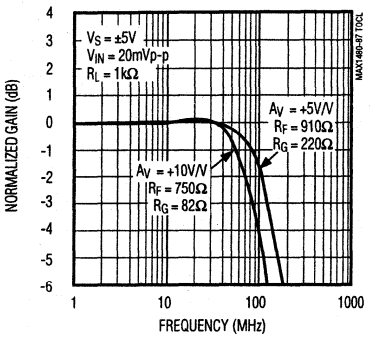
Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

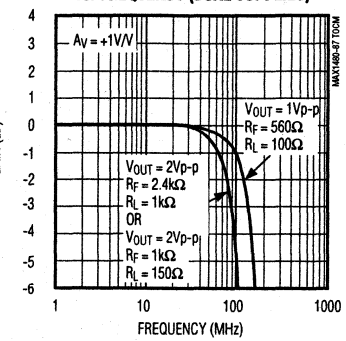
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

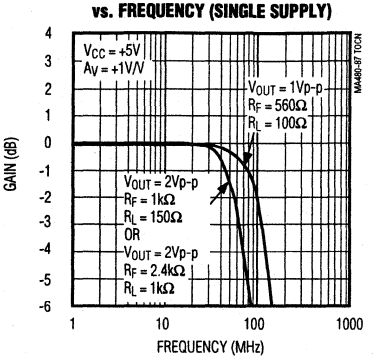
MAX4180 SMALL-SIGNAL GAIN vs. FREQUENCY



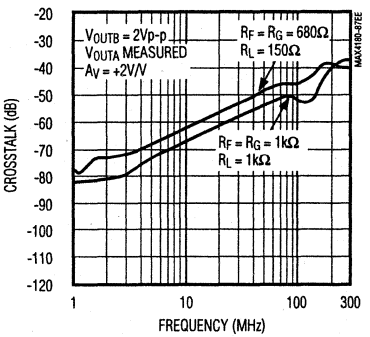
MAX4181 LARGE-SIGNAL GAIN vs. FREQUENCY (DUAL SUPPLIES)



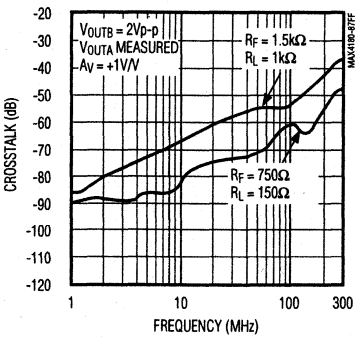
MAX4181 LARGE-SIGNAL GAIN vs. FREQUENCY (SINGLE SUPPLY)



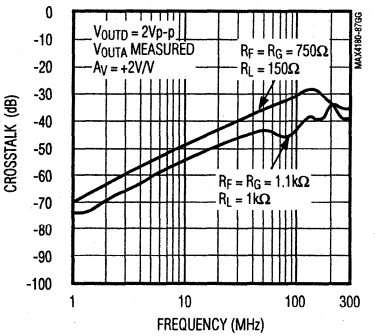
MAX4182 CROSSTALK vs. FREQUENCY



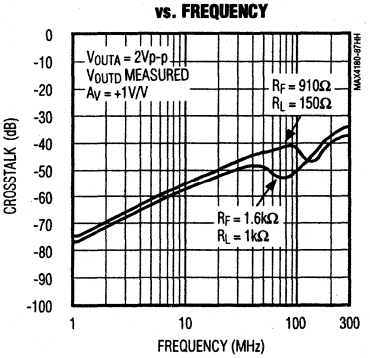
MAX4184 CROSSTALK vs. FREQUENCY



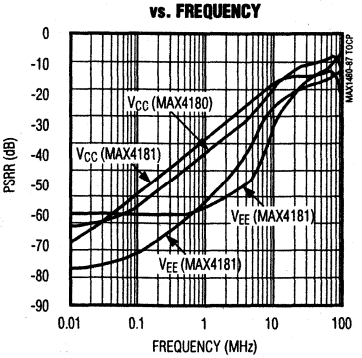
MAX4186 CROSSTALK vs. FREQUENCY



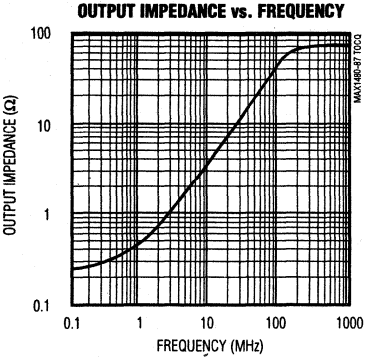
MAX4187 CROSSTALK vs. FREQUENCY



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



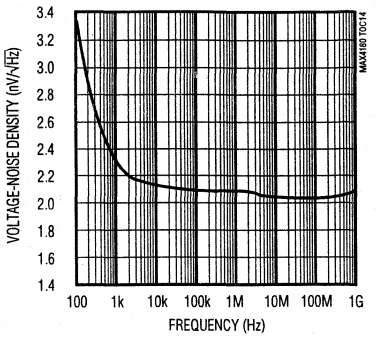
OUTPUT IMPEDANCE vs. FREQUENCY



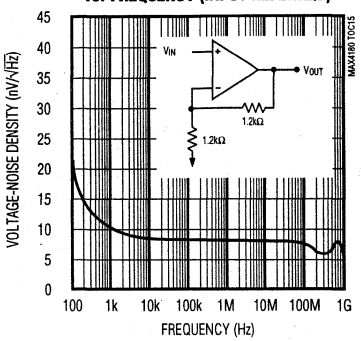
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

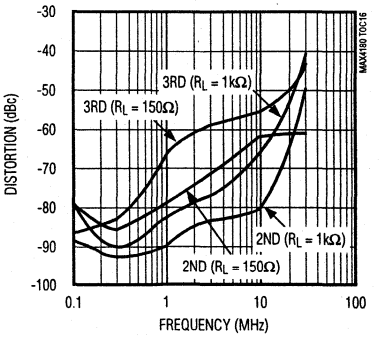
VOLTAGE-NOISE DENSITY vs. FREQUENCY (INPUT REFERRED)



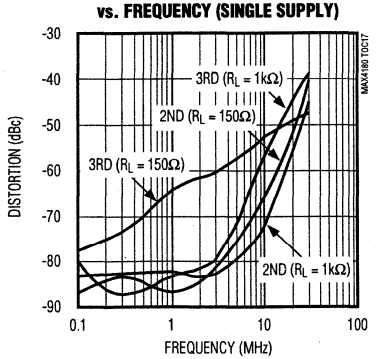
TOTAL VOLTAGE-NOISE DENSITY vs. FREQUENCY (INPUT REFERRED)



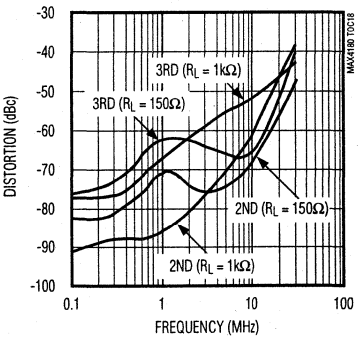
MAX4180 HARMONIC DISTORTION vs. FREQUENCY (DUAL SUPPLIES)



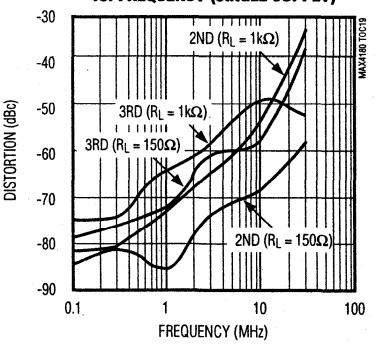
MAX4180 HARMONIC DISTORTION vs. FREQUENCY (SINGLE SUPPLY)



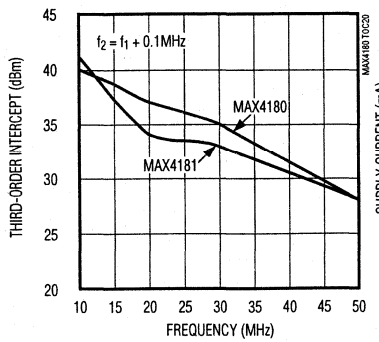
MAX4181 HARMONIC DISTORTION vs. FREQUENCY (DUAL SUPPLIES)



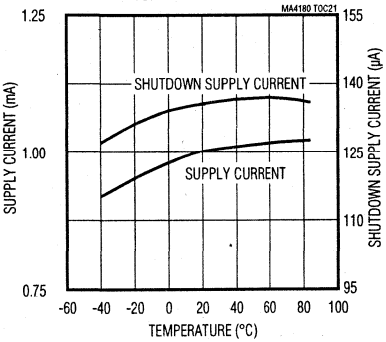
MAX4181 HARMONIC DISTORTION vs. FREQUENCY (SINGLE SUPPLY)



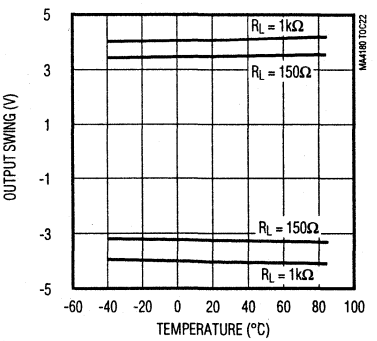
TWO-TONE THIRD-ORDER INTERCEPT vs. FREQUENCY



SUPPLY CURRENT (OPERATING & SHUTDOWN) vs. TEMPERATURE



OUTPUT VOLTAGE SWING vs. TEMPERATURE



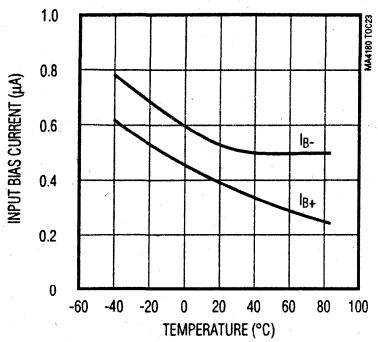
8

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

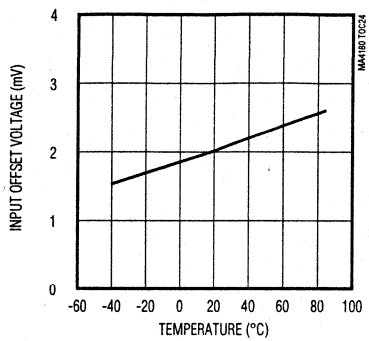
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

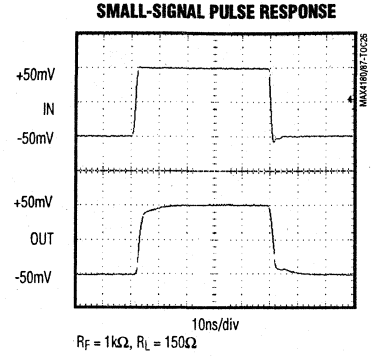
INPUT BIAS CURRENT vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE

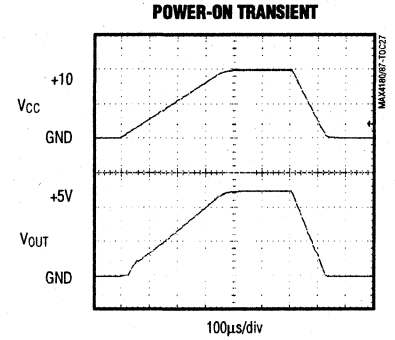


MAX4181 SMALL-SIGNAL PULSE RESPONSE



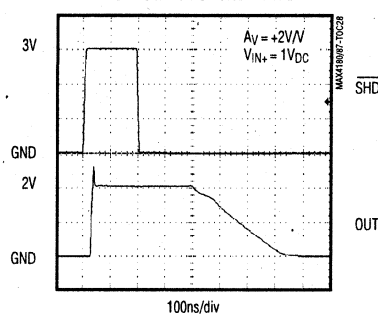
R_F = 1kΩ, R_L = 150Ω

POWER-ON TRANSIENT



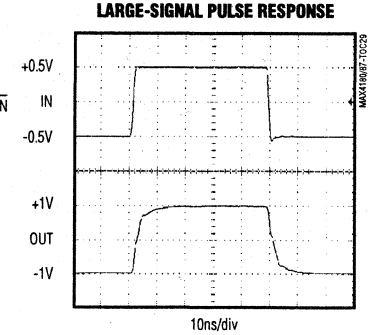
R_F = 1kΩ, V_{IN} = V_{CC}/2, R_L = ∞

SHUTDOWN RESPONSE TIME



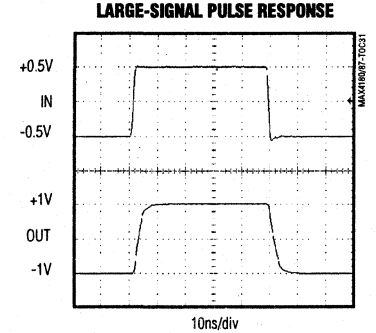
R_L = 150Ω, R_F = R_G = 820Ω

MAX4180 LARGE-SIGNAL PULSE RESPONSE



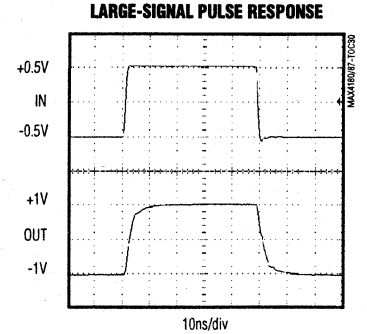
R_L = 1kΩ, R_F = R_G = 1.2kΩ

MAX4180 LARGE-SIGNAL PULSE RESPONSE



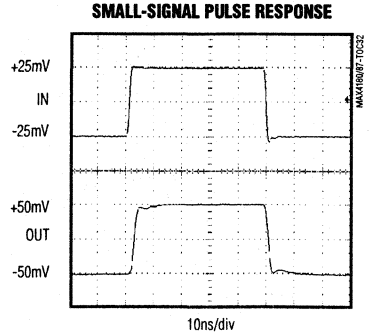
R_L = 100Ω, R_F = R_G = 680Ω

MAX4180 LARGE-SIGNAL PULSE RESPONSE



R_L = 150Ω, R_F = R_G = 820Ω

MAX4180 SMALL-SIGNAL PULSE RESPONSE



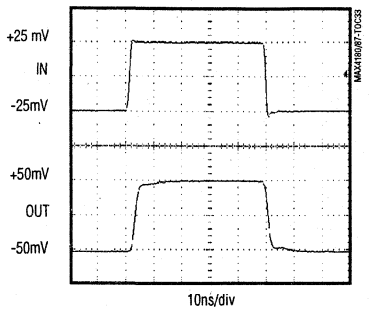
R_L = 1kΩ, R_F = R_G = 1.2kΩ

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

Typical Operating Characteristics (continued)

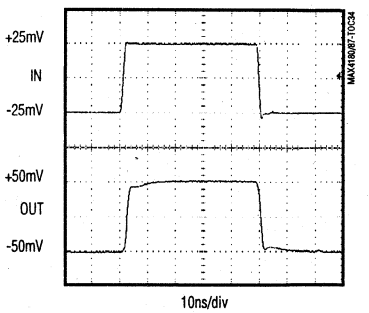
(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

MAX4180
SMALL-SIGNAL PULSE RESPONSE



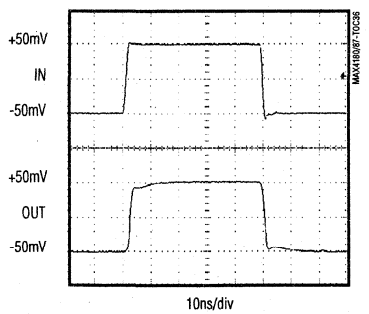
R_L = 150Ω, R_F = R_G = 820Ω

MAX4180
SMALL-SIGNAL PULSE RESPONSE



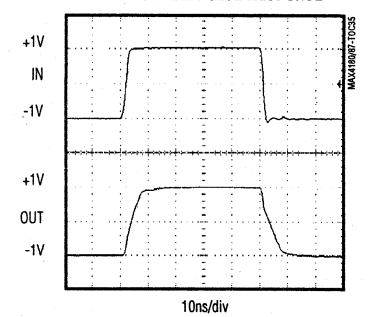
R_L = 100Ω, R_F = R_G = 680Ω

MAX4181
SMALL-SIGNAL PULSE RESPONSE



R_L = 1kΩ, R_F = 2.4kΩ

MAX4181
LARGE-SIGNAL PULSE RESPONSE



V_S = ±5V, R_L = 1kΩ, R_F = 2.4kΩ

Pin Description

8

MAX4180/MAX4181

PIN		NAME	FUNCTION
MAX4180/MAX4181			
SO	SOT23-6		
1, 5	—	N.C.	No Connect. Not internally connected.
2	4	IN-	Inverting Input
3	3	IN+	Noninverting Input
4	2	V_{EE}	Negative Power Supply. Connect V_{EE} to -5V or ground for single-supply operation.
6	1	OUT	Amplifier Output
7	6	V_{CC}	Positive Power Supply. Connect V_{CC} to +5V.
8	5	$\overline{SHDN}$	Shutdown Input. Device is enabled when $\overline{SHDN} \geq (V_{CC} - 2V)$ and disabled when $\overline{SHDN} \leq (V_{CC} - 3V)$.

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

Pin Description (continued)

MAX4182/MAX4183/MAX4184/MAX4185

PIN			NAME	FUNCTION
MAX4182 MAX4184	MAX4183 MAX4185	MAX4183 MAX4185		
SO	SO	µMAX		
1	1	1	OUTA	Amplifier A Output
2	2	2	INA-	Amplifier A Inverting Input
3	3	3	INA+	Amplifier A Noninverting Input
4	4	4	V_{EE}	Negative Power Supply. Connect V_{EE} to -5V or ground for single-supply operation.
—	5, 7, 8, 10	—	N.C.	No Connect. Not internally connected.
—	6	5	$\overline{SHDNA}$	Shutdown Control Input for Amplifier A. Amplifier A is enabled when $\overline{SHDNA} \geq (V_{CC} - 2V)$ and disabled when $\overline{SHDNA} \leq (V_{CC} - 3V)$.
—	9	6	$\overline{SHDNB}$	Shutdown Control Input for Amplifier B. Amplifier B is enabled when $\overline{SHDNB} \geq (V_{CC} - 2V)$ and disabled when $\overline{SHDNB} \leq (V_{CC} - 3V)$.
5	11	7	INB+	Amplifier B Noninverting Input
6	12	8	INB-	Amplifier B Inverting Input
7	13	9	OUTB	Amplifier B Output
8	14	10	V_{CC}	Positive Power Supply. Connect V_{CC} to +5V.

MAX4186/MAX4187

PIN		NAME	FUNCTION
MAX4186 MAX4187	MAX4186 MAX4187		
SO	QSOP		
1	1	OUTA	Amplifier A Output
2	2	INA-	Amplifier A Inverting Input
3	3	INA+	Amplifier A Noninverting Input
4	4	V_{CC}	Positive Power Supply. Connect V_{CC} to +5V.
5	5	INB+	Amplifier B Noninverting Input
6	6	INB-	Amplifier B Inverting Input
7	7	OUTB	Amplifier B Output
—	8, 9	N.C.	No Connect. Not internally connected.
8	10	OUTC	Amplifier C Output
9	11	INC-	Amplifier C Inverting Input
10	12	INC+	Amplifier C Noninverting Input
11	13	V_{EE}	Negative Power Supply. Connect V_{EE} to -5V or ground for single-supply operation.
12	14	IND+	Amplifier D Noninverting Input
13	15	IND-	Amplifier D Inverting Input
14	16	OUTD	Amplifier D Output

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

Detailed Description

The MAX4180–MAX4187 are ultra-low-power current-feedback amplifiers featuring bandwidths up to 270MHz, 0.1dB gain flatness to 90MHz, and low differential gain (0.08%) and phase (0.03°) errors. These amplifiers achieve ultra-high bandwidth-to-power ratios with low distortion, wide signal swing, and excellent load-driving capabilities. They are optimized for ±5V supplies but also operate from a single +5V supply while consuming only 1mA per amplifier. With ±60mA output current drive capability, the devices achieve low distortion even while driving 150Ω loads.

Wide bandwidth, low power, low differential phase and gain error, and excellent gain flatness make the MAX4180–MAX4187 ideal for use in portable video equipment such as cameras, video switchers, and other battery-powered applications. Their two-stage design provides higher gain and lower distortion than conventional single-stage, current-feedback topologies. This feature, combined with fast settling time, makes these devices suitable for buffering high-speed analog-to-digital converters (ADCs).

The MAX4180/MAX4181/MAX4183/MAX4185 have a low-power shutdown mode that is activated by driving the amplifiers' $\overline{SHDN}$ input low. Placing them in shutdown reduces quiescent supply current to 135µA (typ) and places amplifier outputs in a high-impedance state. These amplifiers can be used to implement a high-speed multiplexer by connecting together the outputs of multiple amplifiers and controlling the $\overline{SHDN}$ inputs to enable one amplifier and disable all the others. The disabled amplifiers present very little load (0.1µA leakage current and 4pF capacitance) to the active amplifiers' output. Note that the feedback network impedance of all the disabled amplifiers must be considered when calculating the total load on the active amplifier output.

Applications Information

Theory of Operation

The MAX4180–MAX4187 are current-feedback amplifiers, and their open-loop transfer function is expressed as a transimpedance, $\Delta V_{OUT}/\Delta I_{IN}$, or T_Z. The frequency behavior of the open-loop transimpedance is similar to the open-loop gain of a voltage-mode feedback amplifier. That is, it has a large DC value and decreases at approximately 6dB per octave.

Analyzing the follower with gain, as shown in Figure 1, yields the following transfer function:

$$V_{OUT} / V_{IN} = G \times [(T_Z(S) / T_Z(s) + G \times (R_{IN} + R_F)]$$

where $G = A_{VCL} = 1 + (R_F / R_G)$, and $R_{IN} = 1/g_M \cong 160\Omega$.

At low gains, $G \times R_{IN} < R_F$. Therefore, the closed-loop bandwidth is essentially independent of closed-loop gain. Similarly $T_Z > R_F$ at low frequencies, so that:

$$\frac{V_{OUT}}{V_{IN}} = G = 1 + (R_F / R_G)$$

Layout and Power-Supply Bypassing

The MAX4180–MAX4187 have an RF bandwidth and, consequently, require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side, and a large, low-impedance ground plane on the other side. The ground plane should be as free of voids as possible. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Regardless of whether a constant-impedance board is used, observe the following guidelines when designing the board:

- Do not use wire-wrap boards. They are too inductive.
- Do not use breadboards. They are too capacitive.
- Do not use IC sockets. They increase parasitic capacitance and inductance.
- Use surface-mount components rather than through-hole components. They give better high-frequency performance, have shorter leads, and have lower parasitic reactances.
- Keep lines as short and as straight as possible.

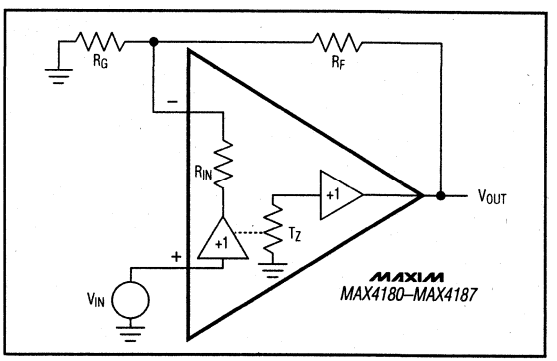


Figure 1. Current-Feedback Amplifier

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

- Do not make 90° turns; round all corners.
- Observe high-frequency bypassing techniques to maintain the amplifiers' accuracy. The bypass capacitors should include a 0.01µF to 0.1µF ceramic capacitor between each supply pin and the ground plane, located as close to the package as possible.
- Place a 1µF ceramic capacitor in parallel with each 0.01µF to 0.1µF capacitor, as close to them as possible.
- Place a 10µF to 15µF low-ESR tantalum at the point of entry to the power-supply pins' PC board. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins.
- Keep PC traces short and use surface-mount components to minimize parasitic inductance.

Maxim's High-Speed Evaluation Board

Figures 2 and 3 show layouts of Maxim's high-speed single SOT23 and SO evaluation boards. These boards were developed using the techniques described above. The smallest available surface-mount resistors were used for feedback and back-termination to minimize their distance from the part, reducing the capacitance associated with longer lead lengths.

SMA connectors were used for best high-frequency performance. Because distances are extremely short, performance is unaffected by the fact that inputs and outputs do not match a 50Ω line. However, in applications that require lead lengths greater than one-quarter of the wavelength of the highest frequency of interest, use constant-impedance traces.

Fully assembled evaluation boards are available for the MAX4180ESA.

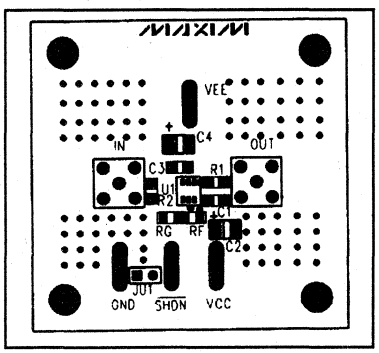


Figure 2a. SOT23 High-Speed EV Board Component Placement Guide—Component Side

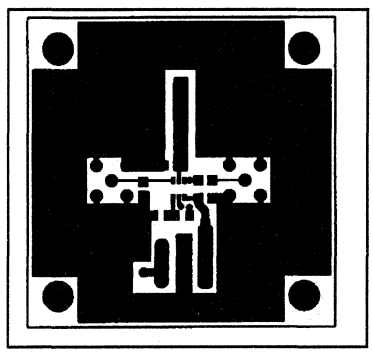


Figure 2b. SOT23 High-Speed EV Board Layout—Component Side

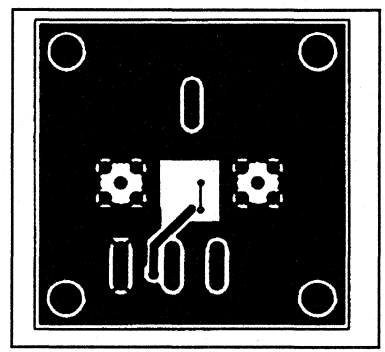


Figure 2c. High-Speed EV Board Layout—Solder Side

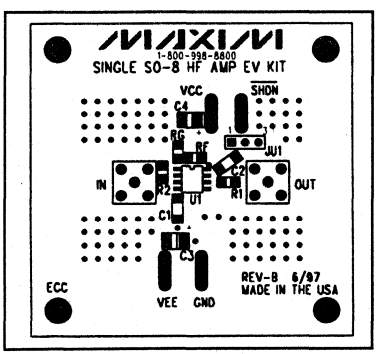


Figure 3a. SO-8 High-Speed EV Board Component Placement Guide—Component Side

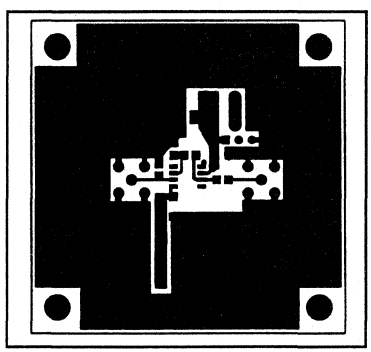


Figure 3b. SO-8 High-Speed EV Board Layout—Component Side

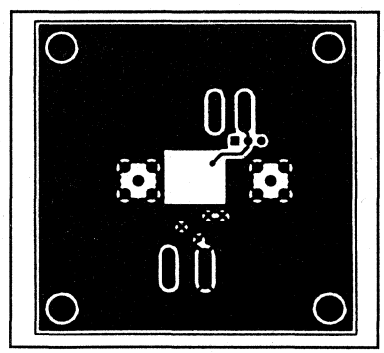


Figure 3c. SO-8 High-Speed EV Board Layout—Solder Side

Table 1. Recommended Component Values

COMPONENT/BW	MAX4180					MAX4181		
	AV = +2V/V			AV = +5V/V	AV = +10V/V	AV = +1V/V		
	RL = 1kΩ	RL = 150Ω	RL = 100Ω	RL = 1kΩ/150Ω	RL = 1kΩ/150Ω	RL = 1kΩ	RL = 150Ω	RL = 100Ω
RF (Ω)	1.2k	820	680	910	750	2.4k	1k	560
RG (Ω)	1.2k	820	680	220	180	—	—	—
-3dB BW (MHz)	245	190	190	120	105	270	205	200

COMPONENT/BW	MAX4182/MAX4183			MAX4184/MAX4185			MAX4186			MAX4187		
	AV = +2V/V			AV = +1V/V			AV = +2V/V			AV = +1V/V		
	RL = 1kΩ	RL = 150Ω	RL = 100Ω	RL = 1kΩ	RL = 150Ω	RL = 100Ω	RL = 1kΩ	RL = 150Ω	RL = 100Ω	RL = 1kΩ	RL = 150Ω	RL = 100Ω
RF (Ω)	1k	680	620	1.5k	750	620	1.1k	750	680	1.6k	910	680
RG (Ω)	1k	680	620	—	—	—	1.1k	750	680	—	—	—
-3dB BW (MHz)	245	190	160	270	205	180	245	190	175	270	205	200

Choosing Feedback and Gain Resistors

The optimum value of the external-feedback (R_F) and gain-setting (R_G) resistors used with the MAX4180–MAX4187 depends on the closed-loop gain and the application circuit's load. Table 1 lists the optimum resistor values for some specific gain configurations. One-percent resistor values are preferred to maintain consistency over a wide range of production lots. Figures 4a and 4b show the standard inverting and noninverting configurations. Note that the noninverting circuit gain (Figure 4) is 1 plus the magnitude of the inverting closed-loop gain. Otherwise, the two circuits are identical.

DC and Noise Errors

Several major error sources must be considered in any op amp. These apply equally to the MAX4180–MAX4187. Offset-error terms are given by the equation below. Voltage and current-noise errors are root-square summed and are therefore computed separately. In Figure 5, the total output offset voltage is determined by the following factors:

- The input offset voltage (V_{OS}) times the closed-loop gain ($1 = R_F / R_G$).
- The positive input bias current (I_{B+}) times the source resistor (R_S) (usually 50Ω or 75Ω), plus the negative input bias current (I_{B-}) times the parallel combination of R_G and R_F. In current-feedback amplifiers, the input bias currents at the IN+ and IN- terminals do not track each other and may have opposite polarity, so there is no benefit to matching the resistance at both inputs.

The equation for the total DC error at the output is:

$$V_{OUT} = \left[(I_{B+})R_S + (I_{B-})(R_F \,||\, R_G) + V_{OS}\right]\left(1+\frac{R_F}{R_G}\right)$$

The total output-referred noise voltage is:

$$e_{n(OUT)} = \left(1+\frac{R_F}{R_G}\right)\sqrt{\left[(i_{n+})R_S\right]^2 + \left[(i_{n-})R_F \,||\, R_G\right]^2 + (e_n)^2}$$

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

The MAX4180–MAX4187 have a very low, 2nV/√Hz noise voltage. The current noise at the positive input (i_{n+}) is 4pA/√Hz, and the current noise at the inverting input is 5pA/√Hz.

An example of the DC error calculations, using the MAX4180 typical data and typical operating circuit where $R_F = R_G = 1.2k\Omega$ ($R_F \parallel R_G = 600\Omega$) and $R_S = 37.5\Omega$, gives the following:

$$V_{OUT} = \left[\left(1x10^{-6}\right)x37.5 + \left(2x10^{-6}\right)x(600) + 1.5^{-3}\right]x(1+1)$$

$$V_{OUT} = 5.5mV$$

Calculating the total output noise in a similar manner yields:

$$e_{n(OUT)} = (1+1)\sqrt{\left(4x10^{-12}x37.5\right)^2 + \left(5x10^{-12}x600\right)^2 + \left(2x10^{-9}\right)^2}$$

$$e_{n(OUT)} = 7.2nV/\sqrt{Hz}$$

With a 200MHz system bandwidth, this calculates to 102μVRMS (approximately 612μVp-p, choosing the six-sigma value).

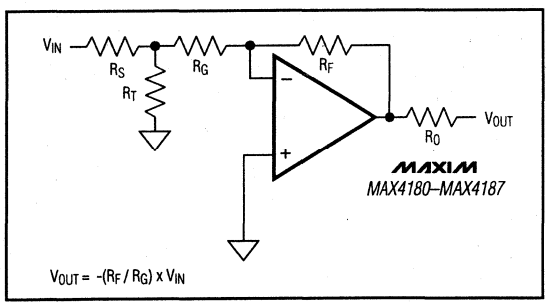


Figure 4a. Inverting Gain Configuration

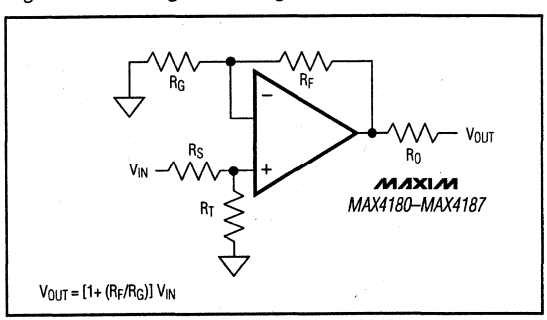


Figure 4b. Noninverting Gain Configuration

Video Line Driver

The MAX4180–MAX4187 are well suited to drive coaxial transmission lines when the cable is terminated at both ends, as shown in Figure 6. Cable frequency response can cause variations in the signal's flatness. See Table 1 for optimum R_F and R_G values.

Driving Capacitive Loads

The MAX4180–MAX4187 are optimized for AC performance. They are not designed to drive highly capacitive loads. Reactive loads decrease phase margin and may produce excessive ringing and oscillation. Figure 7a shows a circuit that eliminates this problem. Placing the small (usually 5Ω to 22Ω) isolation resistor, R_S, before the reactive load prevents ringing and oscillation. At higher capacitive loads, the interaction of the load capacitance and isolation resistor controls AC performance. Figures 7b and 7c show the MAX4180 and MAX4181 frequency response with a 47pF capaci-

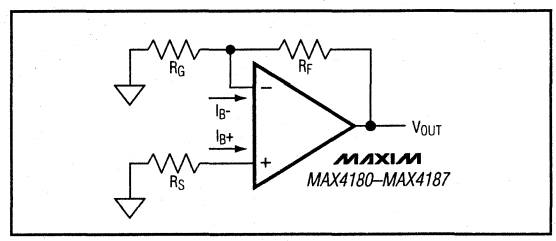


Figure 5. Output Offset Voltage

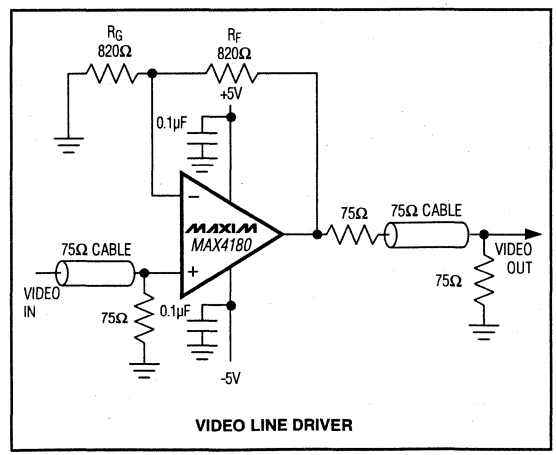


Figure 6. Video Line Driver

tive load. Note that in each case, gain peaking is substantially reduced when the 20Ω resistor is used to isolate the capacitive load from the amplifier output.

AC Testing/Performance

AC specifications on high-speed amplifiers are usually guaranteed without 100% production testing. Since these high-speed devices are sensitive to external parasitics introduced when automatic handling equipment is used, it is impractical to guarantee AC parameters through volume production testing. These parasitics are greatly reduced when using the recommended PC board layout (like the Maxim EV kit). Characterizing the part in this way more accurately represents the amplifier's true AC performance. Some manufacturers guarantee AC specifications without clearly stating how this guarantee is made. The AC specifications of the MAX4180–MAX4187 are derived through worst-case design simulations combined with a sample characterization of 100 units. The AC performance distributions along with the worst-case simulation results for MAX4180 and MAX4181 are shown in Figures 8–11. These distributions are repeatable provided that the proper board layout and power-supply bypassing are used (see *Layout and Power-Supply Bypassing* section).

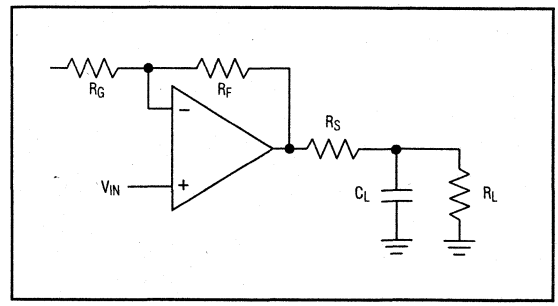


Figure 7a. Using an Isolation Resistor (R_S) for High Capacitive Loads

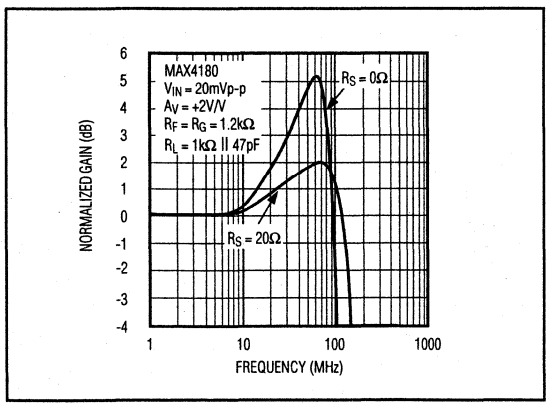


Figure 7b. Frequency Response with Capacitive Load (with and without Isolation Resistor)

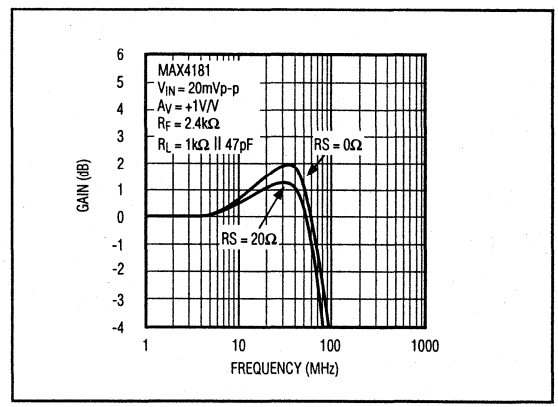


Figure 7c. Frequency Response with Capacitive Load (with and without Isolation Resistor)

8

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

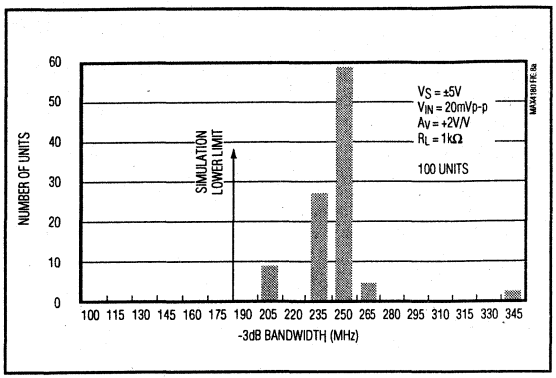


Figure 8a. MAX4180 -3dB Bandwidth Distribution (Dual Supplies)

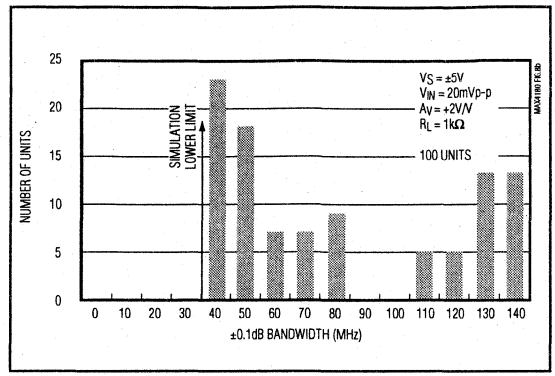


Figure 8b. MAX4180 ±0.1dB Bandwidth Distribution (Dual Supplies)

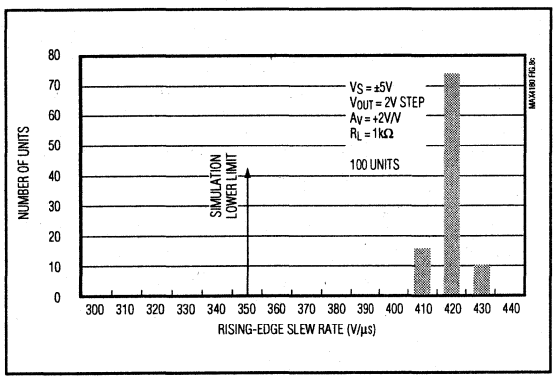


Figure 8c. MAX4180 Rising-Edge Slew-Rate Distribution (Dual Supplies)

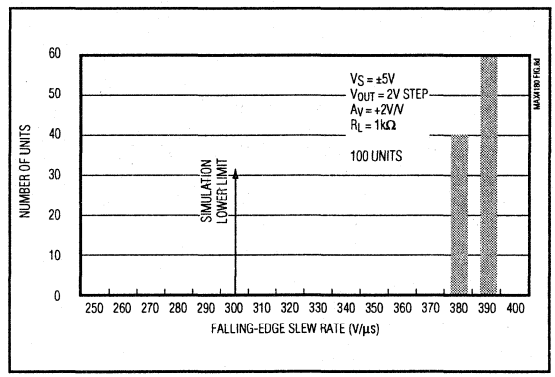


Figure 8d. MAX4180 Falling-Edge Slew-Rate Distribution (Dual Supplies)

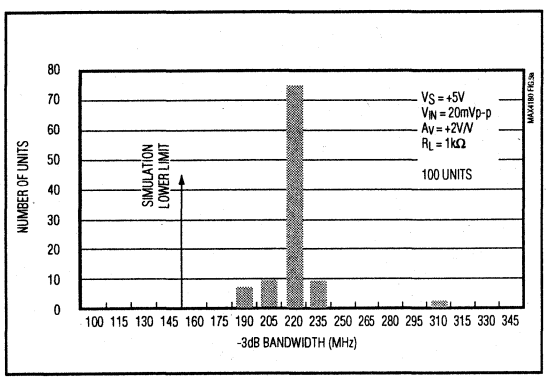


Figure 9a. MAX4180 -3dB Bandwidth Distribution (Single Supply)

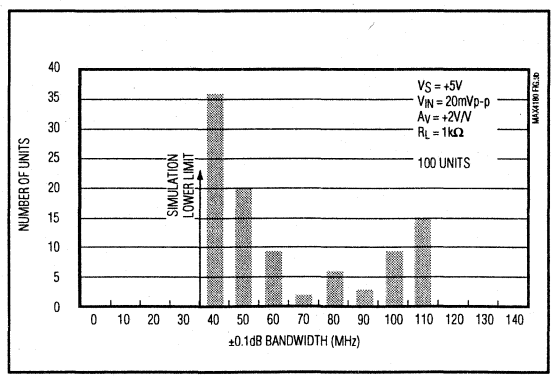


Figure 9b. MAX4180 ±0.1dB Bandwidth Distribution (Single Supply)

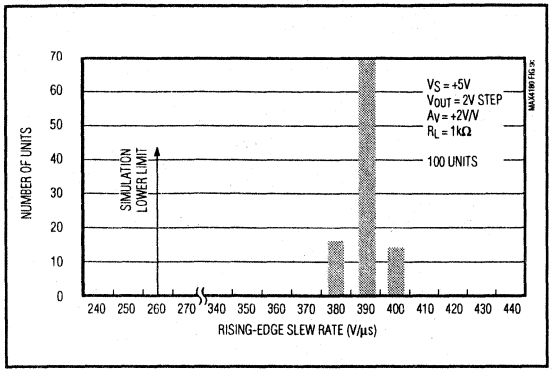


Figure 9c. MAX4180 Rising-Edge Slew-Rate Distribution (Single Supply)

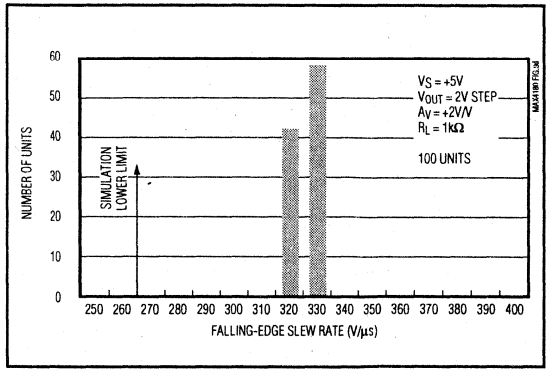


Figure 9d. MAX4180 Falling-Edge Slew-Rate Distribution (Single Supply)

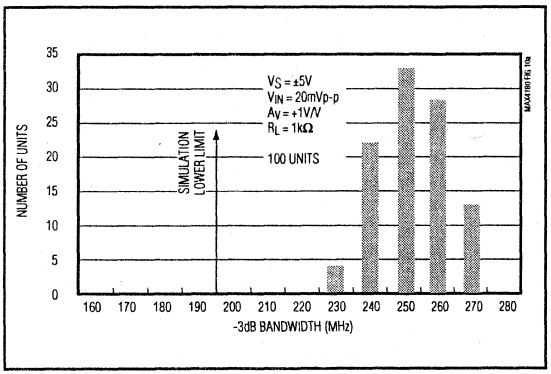


Figure 10a. MAX4181 -3dB Bandwidth Distribution (Dual Supplies)

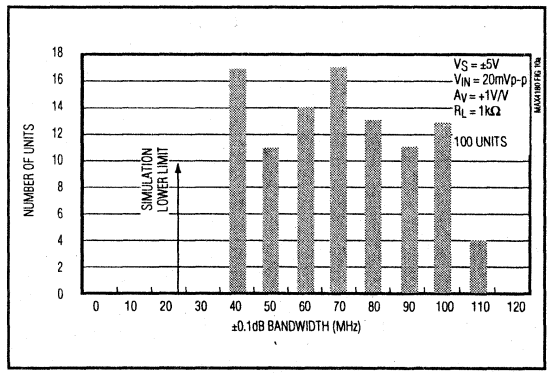


Figure 10b. MAX4181 ±0.1dB Bandwidth Distribution (Dual Supplies)

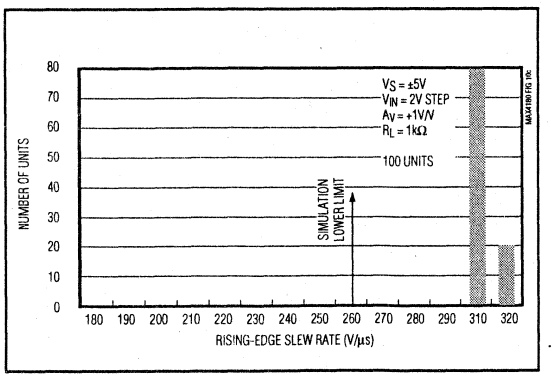


Figure 10c. MAX4181 Rising-Edge Slew-Rate Distribution (Dual Supplies)

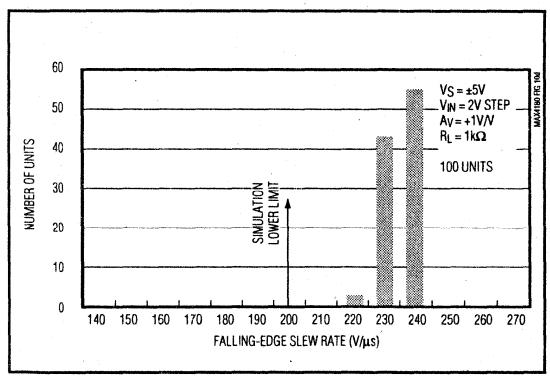


Figure 10d. MAX4181 Falling-Edge Slew-Rate Distribution (Dual Supplies)

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

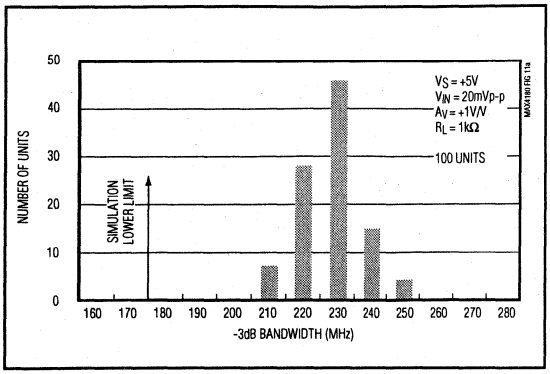


Figure 11a. MAX4181 -3dB Bandwidth Distribution (Single Supply)

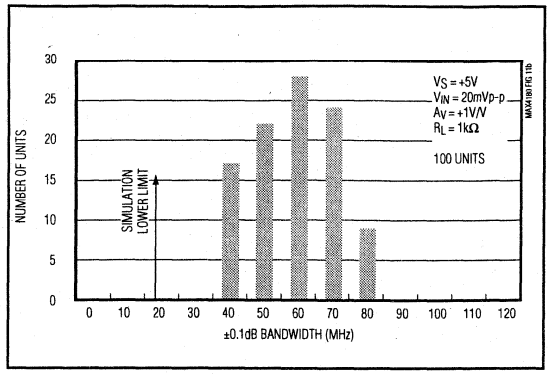


Figure 11b. MAX4181 ±0.1dB Bandwidth Distribution (Single Supply)

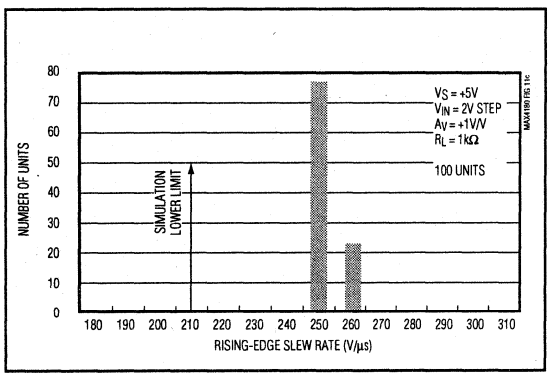


Figure 11c. MAX4181 Rising-Edge Slew-Rate Distribution (Single Supply)

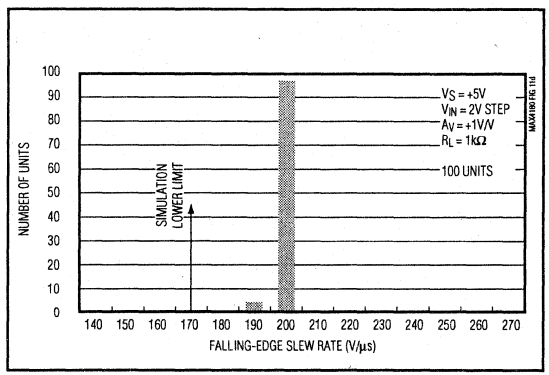


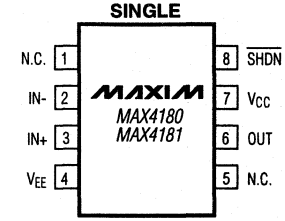
Figure 11d. MAX4181 Falling-Edge Slew-Rate Distribution (Single Supply)

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

Pin Configurations (continued)

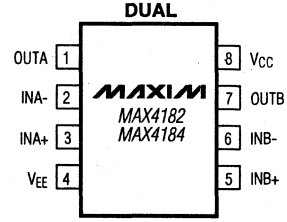
TOP VIEW

SINGLE



SO

DUAL



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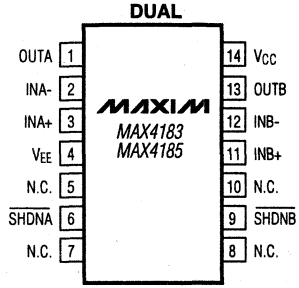
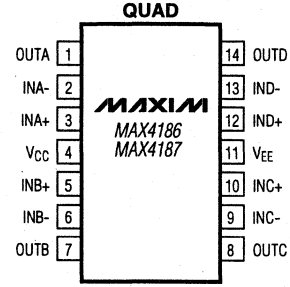
DUAL



SO

QUAD



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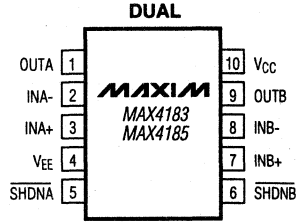
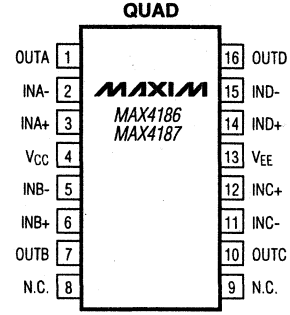
DUAL



µMAX

QUAD



QSOP

Single/Dual/Quad, 270MHz, 1mA, SOT23, Current-Feedback Amplifiers with Shutdown

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4181EUT	-40°C to +85°C	6 SOT23	AAAC
MAX4181ESA	-40°C to +85°C	8 SO	—
MAX4182ESA	-40°C to +85°C	8 SO	—
MAX4183EUB	-40°C to +85°C	10 µMAX*	—
MAX4183ESD	-40°C to +85°C	14 SO	—
MAX4184ESA	-40°C to +85°C	8 SO	—
MAX4185EUB	-40°C to +85°C	10 µMAX*	—
MAX4185ESD	-40°C to +85°C	14 SO	—
MAX4186ESD	-40°C to +85°C	14 SO	—
MAX4186EEE	-40°C to +85°C	16 QSOP	—
MAX4187ESD	-40°C to +85°C	14 SO	—
MAX4187EEE	-40°C to +85°C	16 QSOP	—

**Contact factory for availability.*

Chip Information

MAX4180/MAX4181
TRANSISTOR COUNT: 83
SUBSTRATE CONNECTED TO V_{EE}

MAX4182–MAX4185
TRANSISTOR COUNT: 166
SUBSTRATE CONNECTED TO V_{EE}

MAX4186/MAX4187
TRANSISTOR COUNT: 235
SUBSTRATE CONNECTED TO V_{EE}

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Single/Triple, Low-Power, 250MHz, Current-Feedback Amplifiers with High-Speed Disable

General Description

The MAX4188–MAX4191 current-feedback amplifiers with high-speed disable function combine high-speed performance, low distortion, and excellent video specifications with ultra-low-power operation in miniature packages. They operate from a ±2.25V to ±5.5V dual supply, or from a +5V single supply. These amplifiers consume only 1.6mA of supply current and are capable of delivering 30mA of output current. The MAX4188/MAX4190 are compensated for applications with a +2V/V (6dB) or greater closed-loop gain, and provide a -3dB 250MHz bandwidth. The MAX4189/MAX4191 are compensated for applications with a +1V/V (0dB) or greater closed-loop gain, and provide a 260MHz -3dB bandwidth.

The MAX4188–MAX4191 have a high-speed disable mode that isolates the inputs and places the outputs in a high-impedance state. Their high off-isolation, low switching transient, fast enable/disable times, and break-before-make switching allow them to be used in a wide range of multiplexing applications. Supply current is reduced to 450µA per amplifier in disable mode. In addition, these amplifiers feature 0.02%/0.04° differential gain/phase errors, a 20ns settling time to 0.1%, and a 720V/µs slew rate, making them ideal for high-performance video applications.

The single MAX4190/MAX4191 are offered in a tiny µMAX package, while the MAX4188/MAX4189 are available in a space-saving 16-pin QSOP package.

Applications

High-Definition Surveillance Video

Video Switching/Multiplexing

Portable/Battery-Powered Video/Multimedia Systems

High-Speed Analog-to-Digital Buffers

Medical Imaging

High-Speed Signal Processing

Professional Cameras

CCD Imaging Systems

Features

- **1.6mA/Amplifier Supply Current**
- **High Speed:**
  250MHz -3dB Small-Signal Bandwidth (MAX4188/MAX4190, $A_{VCL} \geq 2$)
  260MHz -3dB Small-Signal Bandwidth (MAX4189/MAX4191, $A_{VCL} \geq 1$)
- **Low-Power Disable Mode:**
  Inputs Disabled, Outputs Placed in High-Z, Supply Current Reduced to 450µA/Amplifier
- **65ns/35ns Enable/Disable Times**
- **100mVp-p Switching Transient**
- **720V/µS Slew Rate**
- **20ns to 0.1% Settling Time**
- **Excellent Video Specifications:**
  50MHz -0.1dB Gain Flatness (MAX4188/MAX4190)
  40MHz -0.1dB Gain Flatness (MAX4189/MAX4191)
  Differential Gain/Phase Errors: 0.08%/0.04°
- **Low Distortion:**
  75dB SFDR (f_C = 5MHz, V_O = 2Vp-p)
- **Available in Space-Saving Packages:**
  8-Pin µMax (MAX4190/MAX4191)
  16-Pin QSOP (MAX4188/MAX4189)

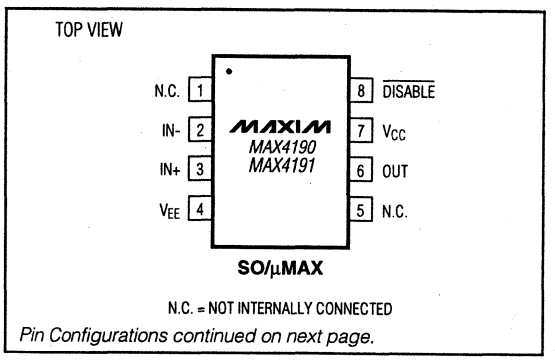
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4188ESD	-40°C to +85°C	14 SO
MAX4188EEE	-40°C to +85°C	16 QSOP
MAX4189ESD	-40°C to +85°C	14 SO
MAX4189EEE	-40°C to +85°C	16 QSOP

Ordering Information continued on next page.

8

Pin Configurations



Pin Configurations continued on next page.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

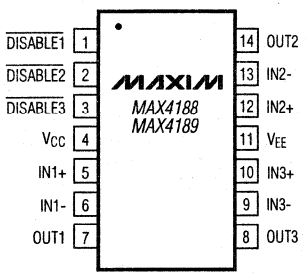
Single/Triple, Low-Power, 250MHz, Current-Feedback Amplifiers with High-Speed Disable

_Ordering Information (continued)

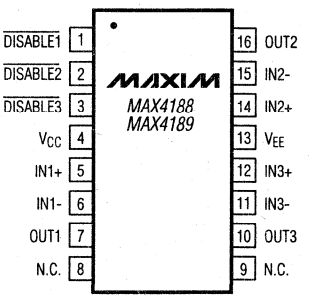
PART	TEMP. RANGE	PIN-PACKAGE
MAX4190ESA	-40°C to +85°C	8 SO
MAX4190EUA	-40°C to +85°C	8 µMAX
MAX4191ESA	-40°C to +85°C	8 SO
MAX4191EUA	-40°C to +85°C	8 µMAX

Pin Configurations (continued)

TOP VIEW



SO



QSOP

N.C. = NOT INTERNALLY CONNECTED

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

High-Speed, Low-Power, SOT23 Open-Loop Buffers

General Description

The MAX4200–MAX4205 are high-speed, open-loop buffers featuring high slew rate, high output current, and low noise. The MAX4200/MAX4201/MAX4202 are single buffers, while the MAX4203/MAX4204/MAX4205 are dual buffers. The MAX4201/MAX4204 have integrated 50Ω termination resistors, making them ideal for driving 50Ω transmission lines. The MAX4202/MAX4205 include on-chip, 75Ω back-termination resistors for driving 75Ω transmission lines. The MAX4200/MAX4203 have no internal termination resistors.

The MAX4200–MAX4205 use a proprietary architecture to achieve an 800MHz -3dB bandwidth, a 200MHz 0.1dB bandwidth, a slew rate of up to 4000V/µs, and a ±80mA output current drive. These buffers operate on ±5V supplies and draw only 2mA of quiescent current. These features, along with a -50dBc at 10MHz spurious-free dynamic range (SFDR), make these devices suitable for driving high-speed analog-to-digital converter (ADC) inputs or for data-communications applications.

Applications

High-Speed DAC Buffers

Wireless LANs

Digital Transmission Line Drivers

High-Speed ADC Input Buffers

Selector Guide

PART	No. OF AMPS	OUTPUT TERMINATION (Ω)	PIN-PACKAGE
MAX4200	1	—	8 SO 5 SOT23
MAX4201	1	50	8 SO 5 SOT23
MAX4202	1	75	8 SO 5 SOT23
MAX4203	2	—	8 SO/µMAX
MAX4204	2	50	8 SO/µMAX
MAX4205	2	75	8 SO/µMAX

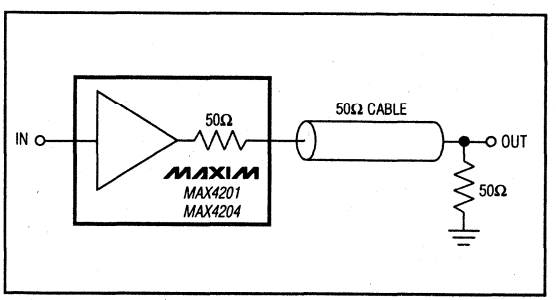
Features

- **2mA Supply Current**
- **High Speed:**
  500MHz -3dB Bandwidth (MAX4200/03)
  800MHz -3dB Bandwidth (MAX4201/02/04/05)
- **200MHz 0.1dB Gain Flatness (MAX4202/05)**
- **4000V/µs Slew Rate**
- **-50dBc SFDR at 10MHz**
- **±80mA High Output Drive (MAX4200/MAX4203)**
- **Available in Space-Saving SOT23 or µMAX Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4200ESA	-40°C to +85°C	8 SO	—
MAX4200EUK-T	-40°C to +85°C	5 SOT23-5	AABZ
MAX4201ESA	-40°C to +85°C	8 SO	—
MAX4201EUK-T	-40°C to +85°C	5 SOT23-5	ABAA
MAX4202ESA	-40°C to +85°C	8 SO	—
MAX4202EUK-T	-40°C to +85°C	5 SOT23-5	ABAB
MAX4203ESA	-40°C to +85°C	8 SO	—
MAX4203EUA	-40°C to +85°C	8 µMAX	—
MAX4204ESA	-40°C to +85°C	8 SO	—
MAX4204EUA	-40°C to +85°C	8 µMAX	—
MAX4205ESA	-40°C to +85°C	8 SO	—
MAX4205EUA	-40°C to +85°C	8 µMAX	—

Typical Operating Circuit

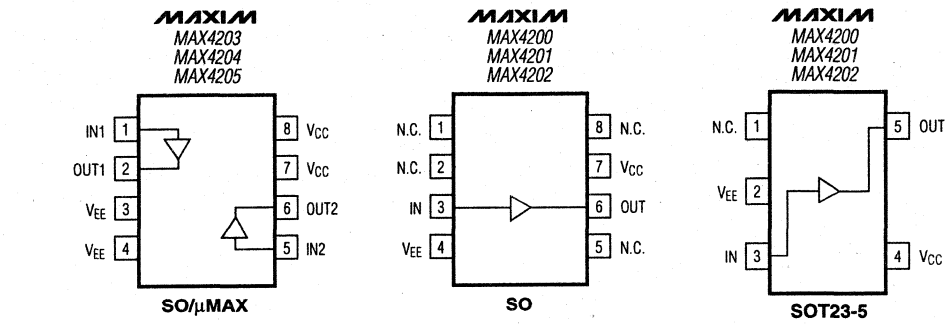


For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

High-Speed, Low-Power, SOT23 Open-Loop Buffers

Pin Configurations

TOP VIEW



N.C. = NOT INTERNALLY CONNECTED

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

High-Speed, Low-Power, SOT23 Open-Loop Buffers

General Description

The MAX4206–MAX4211 high-speed, open-loop buffers feature high slew rate, high output current drive, and low noise. The MAX4207/MAX4210 have integrated 50Ω termination resistors, making them ideal for driving 50Ω transmission lines. The MAX4208/MAX4211 include on-chip 75Ω back-termination resistors for driving 75Ω transmission lines. The MAX4206/MAX4209 have no internal termination resistors.

These devices use a proprietary architecture to achieve a 1.5GHz -3dB bandwidth, a 200MHz 0.1dB bandwidth, a slew rate of up to 5000V/µs, and an output current drive of ±80mA. These buffers operate on ±5V supplies and draw only 5mA of quiescent current. These features, along with a spurious-free dynamic range (SFDR) of -54dBc at 20MHz, make these devices suitable for driving high-speed analog-to-digital converter inputs or for data-communications applications.

Applications

High-Speed DAC Buffers

Wireless LANs

Digital Transmission Line Drivers

High-Speed ADC Input Buffers

Selector Guide

PART	NUMBER OF AMPLIFIERS	OUTPUT TERMINATION (Ω)	PIN-PACKAGE
MAX4206	1	—	8 SO 5 SOT23
MAX4207	1	50	8 SO 5 SOT23
MAX4208	1	75	8 SO 5 SOT23
MAX4209	2	—	8 SO/µMAX
MAX4210	2	50	8 SO/µMAX
MAX4211	2	75	8 SO/µMAX

Features

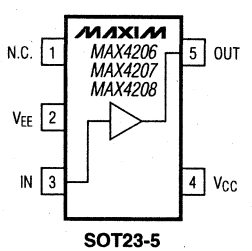
- **5mA Supply Current**
- **High Speed:**
  800MHz -3dB Bandwidth (MAX4206/09)
  1.5GHz -3dB Bandwidth (MAX4207/08/10/11)
- **200MHz 0.1dB Gain Flatness (MAX4206/07/09/10)**
- **5000V/µs Slew Rate**
- **-54dBc SFDR at 20MHz**
- **±80mA Output Drive (MAX4206/09)**
- **Available in Space-Saving SOT23 or µMAX Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4206ESA	-40°C to +85°C	8 SO	—
MAX4206EUK-T	-40°C to +85°C	5 SOT23-5	ABAC
MAX4207ESA	-40°C to +85°C	8 SO	—
MAX4207EUK-T	-40°C to +85°C	5 SOT23-5	ABAD
MAX4208ESA	-40°C to +85°C	8 SO	—
MAX4208EUK-T	-40°C to +85°C	5 SOT23-5	ABAE
MAX4209ESA	-40°C to +85°C	8 SO	—
MAX4209EUA	-40°C to +85°C	8 µMAX	—
MAX4210ESA	-40°C to +85°C	8 SO	—
MAX4210EUA	-40°C to +85°C	8 µMAX	—
MAX4211ESA	-40°C to +85°C	8 SO	—
MAX4211EUA	-40°C to +85°C	8 µMAX	—

Pin Configurations

TOP VIEW



SOT23-5

N.C. = NOT INTERNALLY CONNECTED

Pin Configurations continued on next page.

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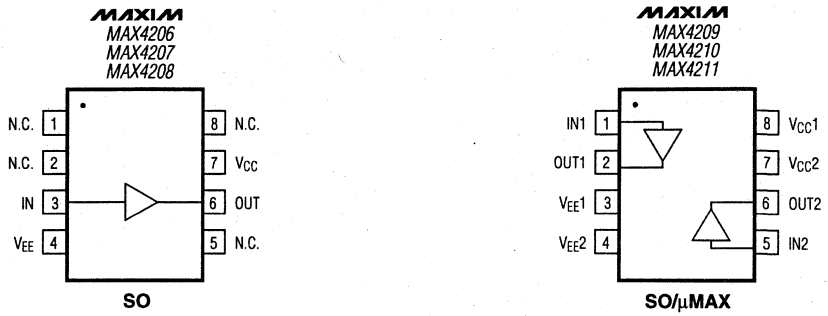
High-Speed, Low-Power, SOT23 Open-Loop Buffers

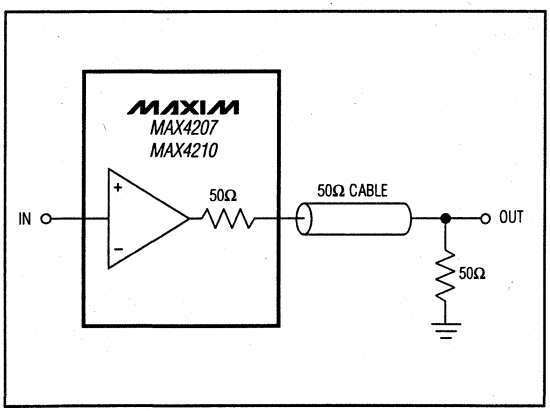
Pin Configurations (continued)

TOP VIEW



N.C. = NOT INTERNALLY CONNECTED

Typical Operating Circuit



19-1178; Rev 0; 12/96

MAXIM

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

General Description

The MAX4212/MAX4213 single, MAX4216 dual, MAX4218 triple, and MAX4220 quad op amps are unity-gain-stable devices that combine high-speed performance with rail-to-rail outputs. The MAX4213/MAX4218 have a disable feature that reduces power-supply current to 350µA max and places the outputs into a high-impedance state. These devices operate from a +3.3V to +10V single supply or from ±1.65V to ±5V dual supplies. The common-mode input voltage range extends beyond the negative power-supply rail (ground in single-supply applications).

These devices require only 5.5mA of quiescent supply current while achieving a 300MHz -3dB bandwidth and a 600V/µs slew rate. Input voltage noise is only 10nV/√Hz and input current noise is only 1.3pA/√Hz for either the inverting or noninverting input. These parts are an excellent solution in low-power/low-voltage systems that require wide bandwidth, such as video, communications, and instrumentation. In addition, when disabled, their high output impedance makes them ideal for multiplexing applications.

The MAX4212 comes in a miniature 5-pin SOT23 package, while the MAX4213/MAX4216 come in 8-pin µMAX and SO packages. The MAX4218/MAX4220 are available in a space-saving 16-pin QSOP, as well as a 14-pin SO.

Applications

Battery-Powered Instruments
Video Line Driver
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems

Features

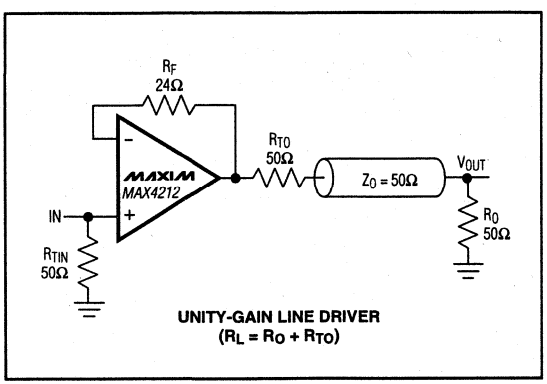
- **High Speed:**
  300MHz -3dB Bandwidth (MAX4212/13)
  200MHz -3dB Bandwidth (MAX4216/18/20)
  50MHz 0.1dB Gain Flatness (MAX4212/13)
  600V/µs Slew Rate
- **Single 3.3V/5.0V Operation**
- **Rail-to-Rail Outputs**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **Low Differential Gain/Phase: 0.02%/0.02°**
- **Low Distortion at 5MHz:**
  -78dBc SFDR
  -75dB Total Harmonic Distortion
- **High Output Drive: ±100mA**
- **Shutdown Capability: $I_S \leq 350\mu A$ (MAX4213/18)**
- **High Output Impedance in Off State (MAX4213/18)**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4212EUK	-40°C to +85°C	5 SOT23-5	ABAF
MAX4213ESA	-40°C to +85°C	8 SO	—
MAX4213EUA	-40°C to +85°C	8 µMAX	—

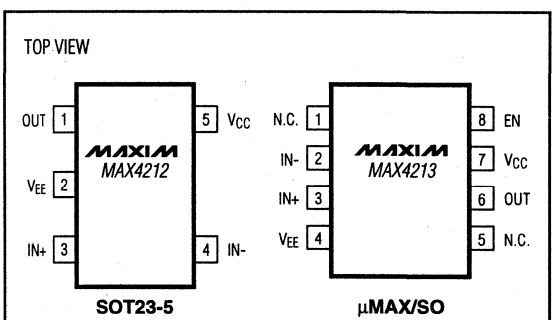
Ordering Information continued at end of data sheet.

Typical Operating Circuit



UNITY-GAIN LINE DRIVER
($R_L = R_O + R_{TO}$)

Pin Configurations



Pin Configurations continued at end of data sheet.

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Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) ..... +12V
IN_-, IN_+, OUT_, EN_ ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Output Short-Circuit Duration to V_{CC} or V_{EE} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
5-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
8-Pin µMAX (derate 4.5mW/°C above +70°C) 221mW
14-Pin SO (derate 8.3mW/°C above +70°C) 667mW
16-Pin QSOP (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or at any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, EN_ = +5V, R_L = 2kΩ to V_{CC} / 2, V_{OUT} = V_{CC} / 2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test		V_{EE} - 0.20		V_{CC} - 2.25	V
Input Offset Voltage (Note 1)	V_{OS}	MAX4212EUK, MAX421_EUA			4	12	mV
		MAX42_ _ES_, MAX42_ _EEE			4	9	
Input Offset Voltage Temperature Coefficient	TC_{VOS}				8		µV/°C
Input Offset Voltage Matching		Any channels for MAX4216/MAX4218/ MAX4220			±1		mV
Input Bias Current	I_B	(Note 1)			5.4	9.0	µA
Input Offset Current	I_{OS}	(Note 1)			0.1	1.0	µA
Input Resistance	R_{IN}	Differential mode (-1V ≤ V_{IN} ≤ +1V)			70		kΩ
		Common mode (-0.2V ≤ V_{CM} ≤ +2.75V)			3		MΩ
Common-Mode Rejection Ratio	CMRR	(V_{EE} - 0.2V) ≤ V_{CM} ≤ (V_{CC} - 2.25V)		70	100		dB
Open-Loop Gain (Note 1)	A_{VOL}	0.25V ≤ V_{OUT} ≤ 4.75V, R_L = 2kΩ		55	61		dB
		0.5V ≤ V_{OUT} ≤ 4.5V, R_L = 150Ω		52	59		
		1.0V ≤ V_{OUT} ≤ 4V, R_L = 50Ω			57		
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	V_{CC} - V_{OH}		0.05		V
			V_{OL} - V_{EE}		0.05		
		R_L = 2kΩ	V_{CC} - V_{OH}		0.06	0.20	
			V_{OL} - V_{EE}		0.06	0.20	
		R_L = 150Ω	V_{CC} - V_{OH}		0.30	0.50	
			V_{OL} - V_{EE}		0.30	0.50	
		R_L = 50Ω	V_{CC} - V_{OH}		0.70		
			V_{OL} - V_{EE}		0.60		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = 0V, EN_ = +5V, R_L = 2kΩ to V_{CC} / 2, V_{OUT} = V_{CC} / 2, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Current	I_{OUT}	R_L = 20Ω to V_{CC} or V_{EE}	±100	±120		mA
Output Short-Circuit Current	I_{SC}	Sinking or sourcing		±150		mA
Open-Loop Output Resistance	R_{OUT}			8		Ω
Power-Supply Rejection Ratio (Note 2)	PSRR	V_{CC} = 5V, V_{EE} = 0V, V_{CM} = +2.0V	52	57		dB
		V_{CC} = 5V, V_{EE} = -5V, V_{CM} = 0V	60	66		
		V_{CC} = 3.3V, V_{EE} = 0V, V_{CM} = +0.90V		45		
Operating Supply-Voltage Range	V_S	V_{CC} to V_{EE}	3.15		11.0	V
Disabled Output Resistance	$R_{OUT (OFF)}$	EN_ = 0V, 0V ≤ V_{OUT} ≤ 5V (Note 3)	28	35		kΩ
EN_ Logic-Low Threshold	V_{IL}				V_{CC} - 2.6	V
EN_ Logic-High Threshold	V_{IH}		V_{CC} - 1.6			V
EN_ Logic Input Low Current	I_{IL}	(V_{EE} + 0.2V) ≤ EN_ ≤ V_{CC}		0.5		µA
		EN_ = 0V		100	150	
EN_ Logic Input High Current	I_{IH}	EN_ = 5V		0.5	10	µA
Quiescent Supply Current (per Amplifier)	I_S	Enabled		5.5	7.0	mA
		Disabled (EN_ = 0V)		0.20	0.35	

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = 0V, V_{CM} = 2.5V, EN_ = +5V, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, V_{OUT} = V_{CC} / 2, A_{VCL} = +1, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Small-Signal -3dB Bandwidth	BW_{SS}	V_{OUT} = 20mVp-p	MAX4212/MAX4213		300		MHz
			MAX4216/MAX4218/MAX4220		200		
Large-Signal -3dB Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p			180		MHz
Bandwidth for 0.1dB Gain Flatness	$BW_{0.1dB}$	V_{OUT} = 20mVp-p	MAX4212/MAX4213		50		MHz
			MAX4216/MAX4218/MAX4220		35		
Slew Rate	SR	V_{OUT} = 2V step			600		V/µs
Settling Time to 0.1%	t_S	V_{OUT} = 2V step			45		ns
Rise/Fall Time	t_R, t_F	V_{OUT} = 100mVp-p			1		ns
Spurious-Free Dynamic Range	SFDR	f_C = 5MHz, V_{OUT} = 2Vp-p			-78		dBc
Harmonic Distortion	HD	f_C = 5MHz, V_{OUT} = 2Vp-p	2nd harmonic		-78		dBc
			3rd harmonic		-82		
			Total harmonic distortion		-75		dB
Two-Tone, Third-Order Intermodulation Distortion	IP3	f1 = 10.0MHz, f2 = 10.1MHz, V_{OUT} = 1Vp-p			35		dBc
Input 1dB Compression Point		f_C = 10MHz, A_{VCL} = +2			11		dBm
Differential Phase Error	DP	NTSC, R_L = 150Ω			0.02		degrees
Differential Gain Error	DG	NTSC, R_L = 150Ω			0.02		%
Input Noise-Voltage Density	e_n	f = 10kHz			10		$nV/\sqrt{Hz}$
Input Noise-Current Density	i_n	f = 10kHz			1.3		$pA/\sqrt{Hz}$
Input Capacitance	C_{IN}				1		pF
Disabled Output Capacitance	$C_{OUT (OFF)}$	EN_ = 0V			2		pF
Output Impedance	Z_{OUT}	f = 10MHz			6		Ω
Amplifier Enable Time	t_{ON}				100		ns
Amplifier Disable Time	t_{OFF}				1		µs
Amplifier Gain Matching		MAX4216/MAX4218/MAX4220, f = 10MHz, V_{OUT} = 20mVp-p			0.1		dB
Amplifier Crosstalk	X_{TALK}	MAX4216/MAX4218/MAX4220, f = 10MHz, V_{OUT} = 2Vp-p			-95		dB

Note 1: Tested with V_{CM} = +2.5V.

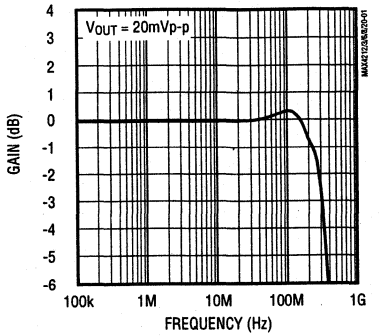
Note 2: PSR for single +5V supply tested with V_{EE} = 0V, V_{CC} = +4.5V to +5.5V; for dual ±5V supply with V_{EE} = -4.5V to -5.5V, V_{CC} = +4.5V to +5.5V; and for single +3.3V supply with V_{EE} = 0V, V_{CC} = +3.15V to +3.45V.

Note 3: Does not include the external feedback network's impedance.

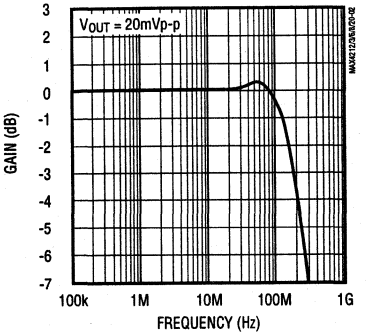
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

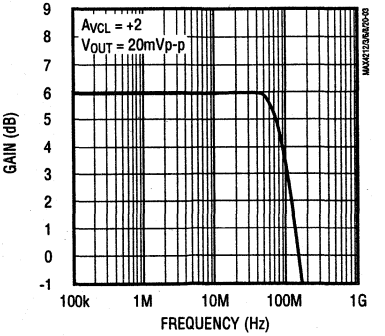
MAX4212/13
SMALL-SIGNAL GAIN vs. FREQUENCY



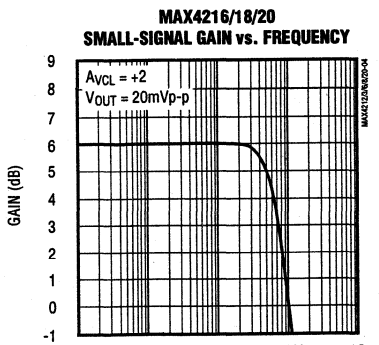
MAX4216/18/20
SMALL-SIGNAL GAIN vs. FREQUENCY



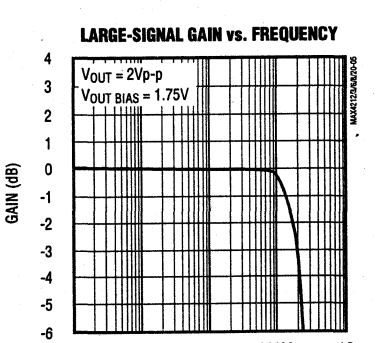
MAX4212/13
SMALL-SIGNAL GAIN vs. FREQUENCY



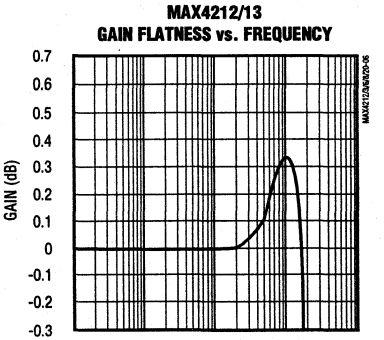
MAX4216/18/20
SMALL-SIGNAL GAIN vs. FREQUENCY



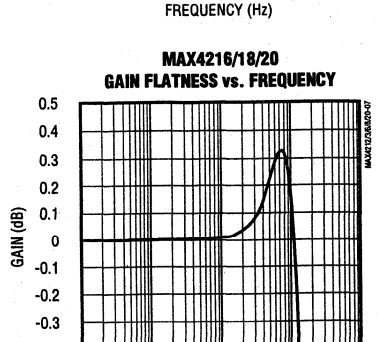
LARGE-SIGNAL GAIN vs. FREQUENCY



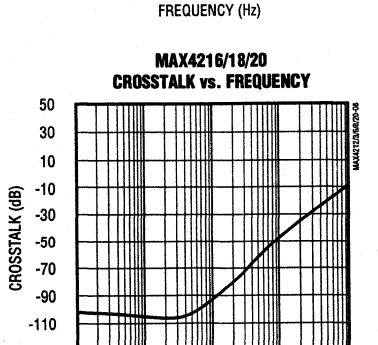
MAX4212/13
GAIN FLATNESS vs. FREQUENCY



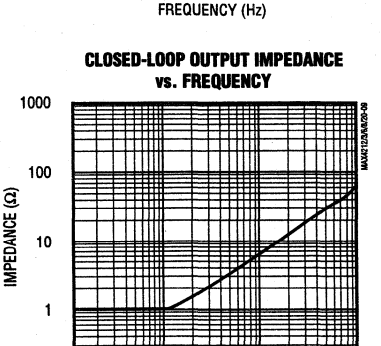
MAX4216/18/20
GAIN FLATNESS vs. FREQUENCY



MAX4216/18/20
CROSSTALK vs. FREQUENCY



CLOSED-LOOP OUTPUT IMPEDANCE
vs. FREQUENCY

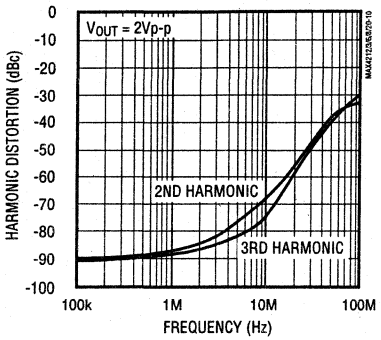


Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

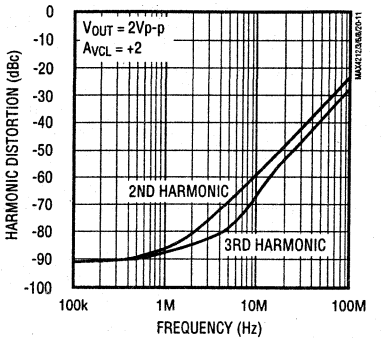
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

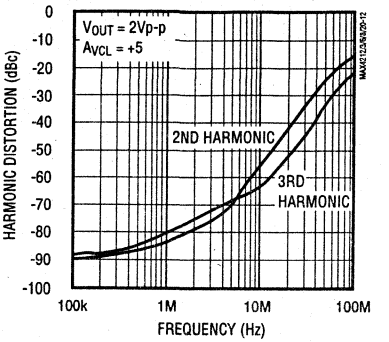
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +1)



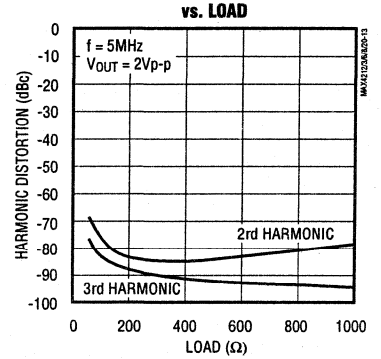
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +2)



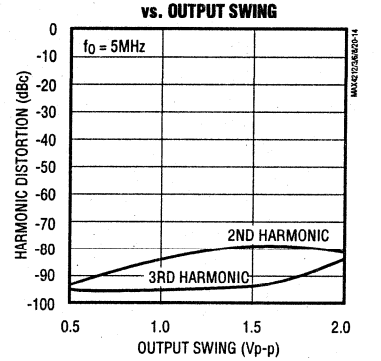
HARMONIC DISTORTION vs. FREQUENCY (A_{VCL} = +5)



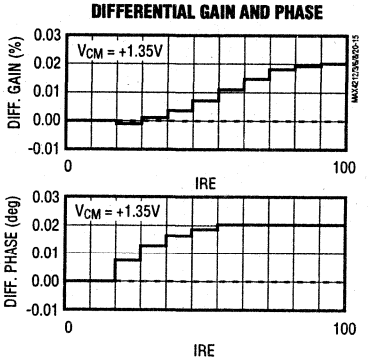
HARMONIC DISTORTION vs. LOAD



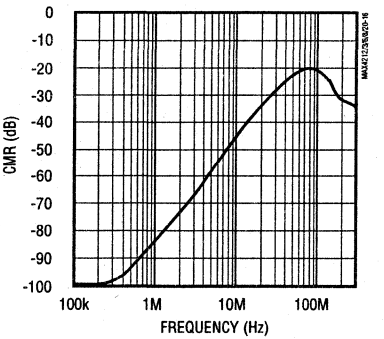
HARMONIC DISTORTION vs. OUTPUT SWING



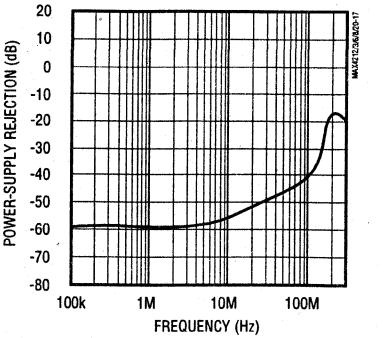
DIFFERENTIAL GAIN AND PHASE



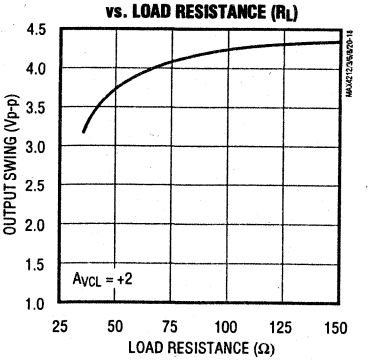
COMMON-MODE REJECTION vs. FREQUENCY



POWER-SUPPLY REJECTION vs. FREQUENCY



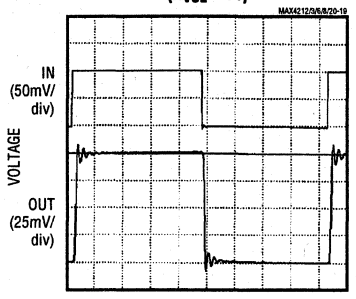
OUTPUT SWING vs. LOAD RESISTANCE (R_L)



Typical Operating Characteristics (continued)

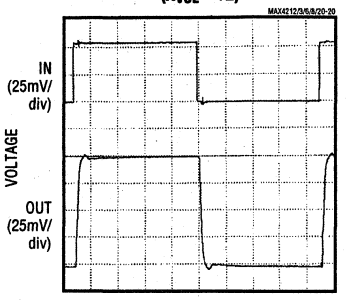
(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



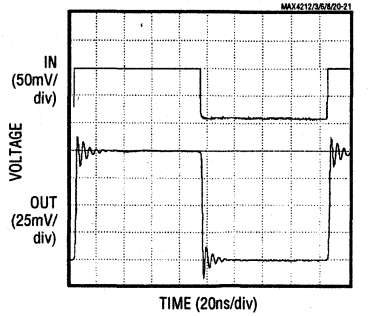
V_{CM} = +2.5V, R_L = 100Ω to GROUND

SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



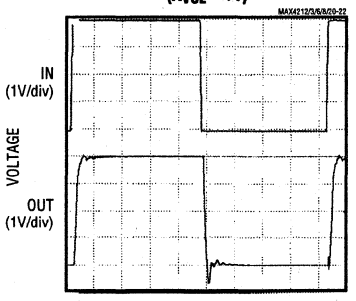
V_{CM} = +1.25V, R_L = 100Ω to GROUND

SMALL-SIGNAL PULSE RESPONSE (C_L = 5pF, A_{VCL} = +1)



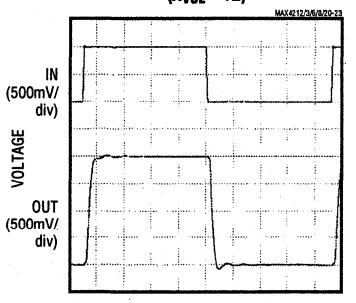
V_{CM} = +1.75V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



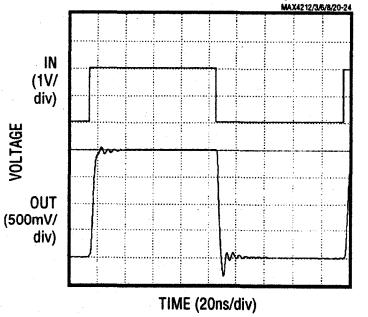
V_{CM} = +1.75V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



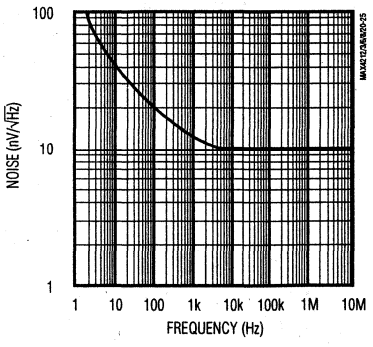
V_{CM} = 0.9V, R_L = 100Ω to GROUND

LARGE-SIGNAL PULSE RESPONSE (C_L = 5pF, A_{VCL} = +2)

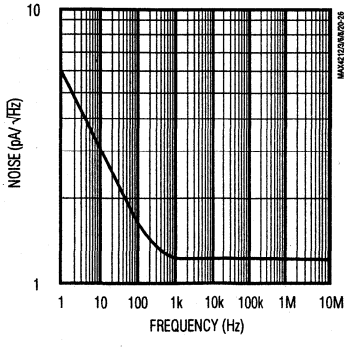


V_{CM} = +1.75V, R_L = 100Ω to GROUND

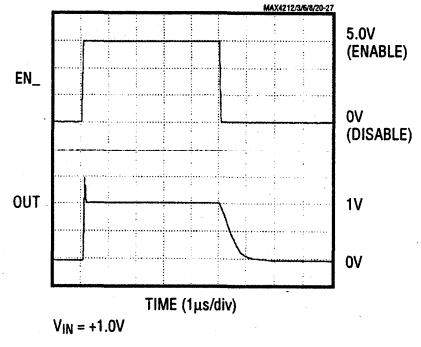
MAX4213 VOLTAGE NOISE DENSITY vs. FREQUENCY



MAX4218 CURRENT NOISE DENSITY vs. FREQUENCY



ENABLE RESPONSE TIME



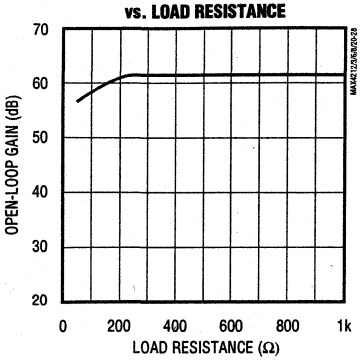
V_{IN} = +1.0V

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

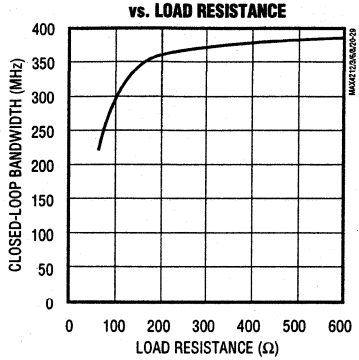
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = 0V, A_{VCL} = +1, R_F = 24Ω, R_L = 100Ω to V_{CC} / 2, T_A = +25°C, unless otherwise noted.)

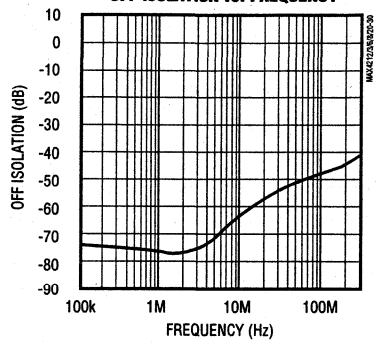
OPEN-LOOP GAIN vs. LOAD RESISTANCE



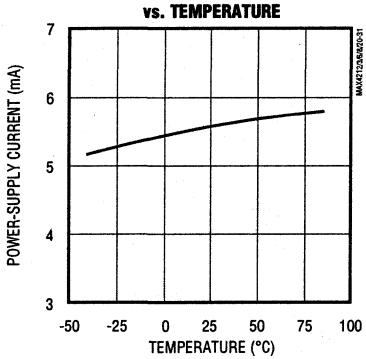
CLOSED-LOOP BANDWIDTH vs. LOAD RESISTANCE



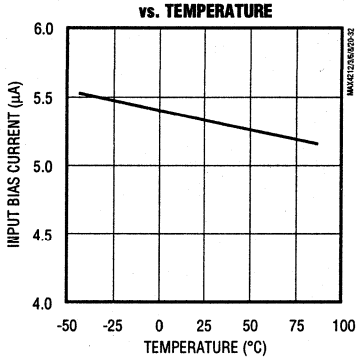
OFF ISOLATION vs. FREQUENCY



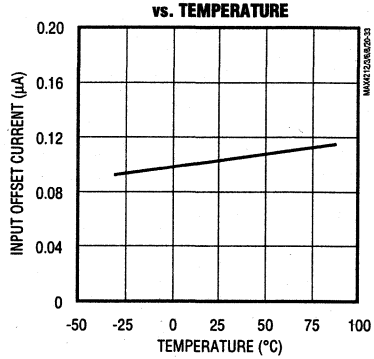
POWER-SUPPLY CURRENT vs. TEMPERATURE



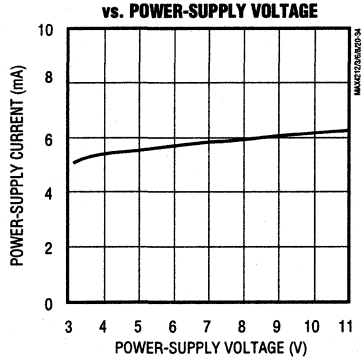
INPUT BIAS CURRENT vs. TEMPERATURE



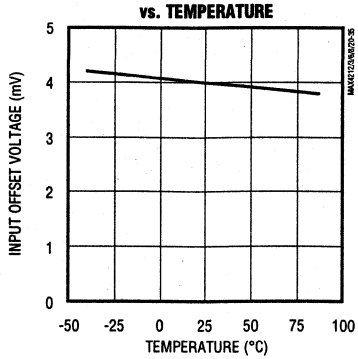
INPUT OFFSET CURRENT vs. TEMPERATURE



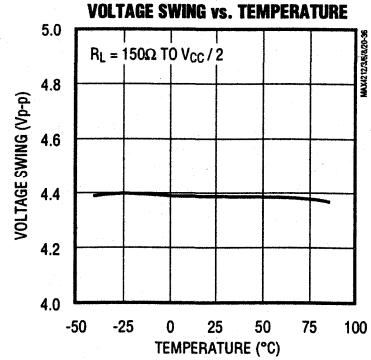
POWER-SUPPLY CURRENT vs. POWER-SUPPLY VOLTAGE



INPUT OFFSET VOLTAGE vs. TEMPERATURE



VOLTAGE SWING vs. TEMPERATURE



Pin Description

PIN							NAME	FUNCTION
MAX4212 SOT23-5	MAX4213 SO/µMAX	MAX4216 SO/µMAX	MAX4218		MAX4220			
			SO	QSOP	SO	QSOP		
—	1, 5	—	—	8, 9	—	8, 9	N.C.	No Connect. Not internally connected. Tie to ground or leave open.
1	6	—	—	—	—	—	OUT	Amplifier Output
2	4	4	11	13	11	13	V_{EE}	Negative Power Supply or Ground (in single-supply operation)
3	3	—	—	—	—	—	IN+	Noninverting Input
4	2	—	—	—	—	—	IN-	Inverting Input
5	7	8	4	4	4	4	V_{CC}	Positive Power Supply
—	—	1	7	7	1	1	OUTA	Amplifier A Output
—	—	2	6	6	2	2	INA-	Amplifier A Inverting Input
—	—	3	5	5	3	3	INA+	Amplifier A Noninverting Input
—	—	7	8	10	7	7	OUTB	Amplifier B Output
—	—	6	9	11	6	6	INB-	Amplifier B Inverting Input
—	—	5	10	12	5	5	INB+	Amplifier B Noninverting Input
—	—	—	14	16	8	10	OUTC	Amplifier C Output
—	—	—	13	15	9	11	INC-	Amplifier C Inverting Input
—	—	—	12	14	10	12	INC+	Amplifier C Noninverting Input
—	—	—	—	—	14	16	OUTD	Amplifier D Output
—	—	—	—	—	13	15	IND-	Amplifier D Inverting Input
—	—	—	—	—	12	14	IND+	Amplifier D Noninverting Input
—	8	—	—	—	—	—	EN	Enable Amplifier
—	—	—	1	1	—	—	ENA	Enable Amplifier A
—	—	—	3	3	—	—	ENB	Enable Amplifier B
—	—	—	2	2	—	—	ENC	Enable Amplifier C

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

Detailed Description

The MAX4212/MAX4213/MAX4216/MAX4218/MAX4220 are single-supply, rail-to-rail, voltage-feedback amplifiers that employ current-feedback techniques to achieve 600V/µs slew rates and 300MHz bandwidths. Excellent harmonic distortion and differential gain/phase performance make these amplifiers an ideal choice for a wide variety of video and RF signal-processing applications.

The output voltage swing comes to within 50mV of each supply rail. Local feedback around the output stage assures low open-loop output impedance to reduce gain sensitivity to load variations. This feedback also produces demand-driven current bias to the output transistors for ±100mA drive capability, while constraining total supply current to less than 7mA. The input stage permits common-mode voltages beyond the negative supply and to within 2.25V of the positive supply rail.

Applications Information

Choosing Resistor Values

Unity-Gain Configuration

The MAX4212/MAX4213/MAX4216/MAX4218/MAX4220 are internally compensated for unity gain. When configured for unity gain, the devices require a 24Ω resistor (R_F) in series with the feedback path. This resistor improves AC response by reducing the Q of the parallel LC circuit formed by the parasitic feedback capacitance and inductance.

Inverting and Noninverting Configurations

Select the gain-setting feedback (R_F) and input (R_G) resistor values to fit your application. Large resistor values increase voltage noise and interact with the amplifier's input and PC board capacitance. This can generate undesirable poles and zeros and decrease bandwidth or cause oscillations. For example, a noninverting gain-of-two configuration ($R_F = R_G$) using 1kΩ resistors, combined with 1pF of amplifier input capacitance and 1pF of PC board capacitance, causes a pole at 159MHz. Since this pole is within the amplifier bandwidth, it jeopardizes stability. Reducing the 1kΩ resistors to 100Ω extends the pole frequency to 1.59GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load resistor. Table 1 shows suggested feedback, gain resistors, and bandwidth for several gain values in the configurations shown in Figures 1a and 1b.

Layout and Power-Supply Bypassing

These amplifiers operate from a single +3.3V to +11V power supply or from dual supplies to ±5.5V. For single-supply operation, bypass V_{CC} to ground with a 0.1µF capacitor as close to the pin as possible. If operating with dual supplies, bypass each supply with a 0.1µF capacitor.

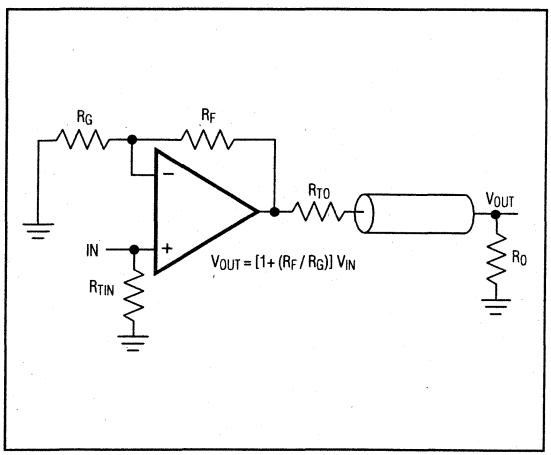


Figure 1a. Noninverting Gain Configuration

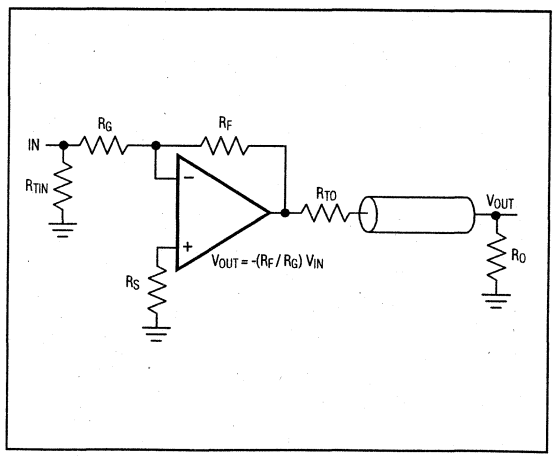


Figure 1b. Inverting Gain Configuration

Maxim recommends using microstrip and stripline techniques to obtain full bandwidth. To ensure that the PC board does not degrade the amplifier's performance, design it for a frequency greater than 1GHz. Pay careful attention to inputs and outputs to avoid large parasitic capacitance. Whether or not you use a constant-impedance board, observe the following guidelines when designing the board:

- Don't use wire-wrap boards because they are too inductive.
- Don't use IC sockets because they increase parasitic capacitance and inductance.
- Use surface-mount instead of through-hole components for better high-frequency performance.
- Use a PC board with at least two layers; it should be as free from voids as possible.
- Keep signal lines as short and as straight as possible. Do not make 90° turns; round all corners.

Rail-to-Rail Outputs, Ground-Sensing Input

The input common-mode range extends from (V_{EE} - 200mV) to (V_{CC} - 2.25V) with excellent common-mode rejection. Beyond this range, the amplifier output is a nonlinear function of the input, but does not undergo phase reversal or latchup.

The output swings to within 50mV of either power-supply rail with a 10kΩ load. The input ground-sensing and the rail-to-rail output substantially increase the dynamic range. With a symmetric input in a single +5V application, the input can swing 2.95Vp-p, and the output can swing 4.9Vp-p with minimal distortion.

Enable Input and Disabled Output

The enable feature (EN_) allows the amplifier to be placed in a low-power, high-output-impedance state. Typically, the EN_ logic low input current (I_{IL}) is small. However, as the EN voltage (V_{IL}) approaches the negative supply rail, I_{IL} increases (Figure 2). A single resistor connected as shown in Figure 3 prevents the rise in the logic-low input current. This resistor provides a feedback mechanism that increases V_{IL} as the logic input is brought to V_{EE}. Figure 4 shows the resulting input current (I_{IL}).

When the MAX4213/MAX4218 are disabled, the amplifier's output impedance is 35kΩ. This high resistance and the low 2pF output capacitance make these parts ideal in RF/video multiplexer or switch applications. For larger arrays, pay careful attention to capacitive loading. See the *Output Capacitive Loading and Stability* section for more information.

Table 1. Recommended Component Values

COMPONENT	GAIN (V/V)									
	+1	-1	+2	-2	+5	-5	+10	-10	+25	-25
R_F (Ω)	24	500	500	500	500	500	500	500	500	1200
R_G (Ω)	∞	500	500	250	124	100	56	50	20	50
R_S (Ω)	—	0	—	0	—	0	—	0	—	0
R_{TIN} (Ω)	49.9	56	49.9	62	49.9	100	49.9	∞	49.9	∞
R_{TO} (Ω)	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9	49.9
Small-Signal -3dB Bandwidth (MHz)	300	90	105	60	25	33	11	25	6	10

Note: $R_L = R_O + R_{TO}$; R_{TIN} and R_{TO} are calculated for 50Ω applications. For 75Ω systems, R_{TO} = 75Ω; calculate R_{TIN} from the following equation:

$$R_{TIN} = \frac{75}{1-\frac{75}{R_G}}\Omega$$

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

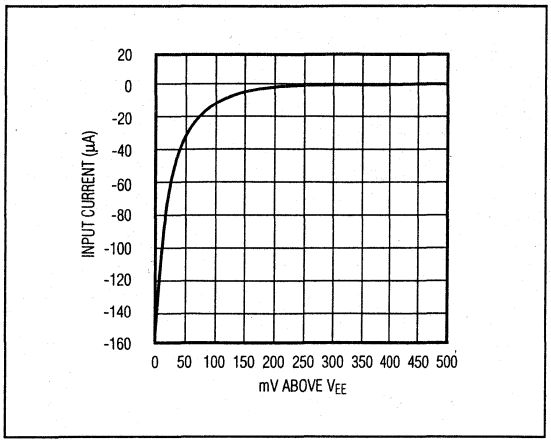


Figure 2. Enable Logic-Low Input Current vs. V_{IL}

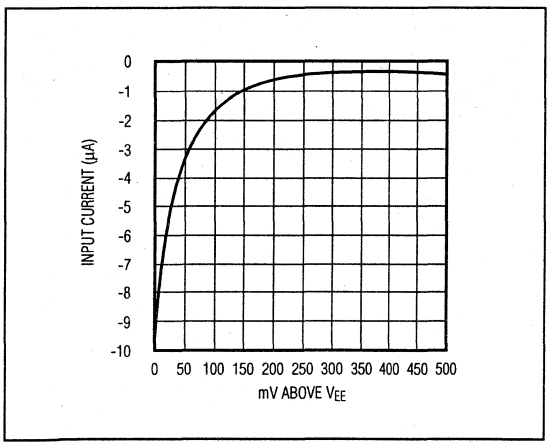


Figure 4. Enable Logic-Low Input Current vs. V_{IL} with 10kΩ Series Resistor

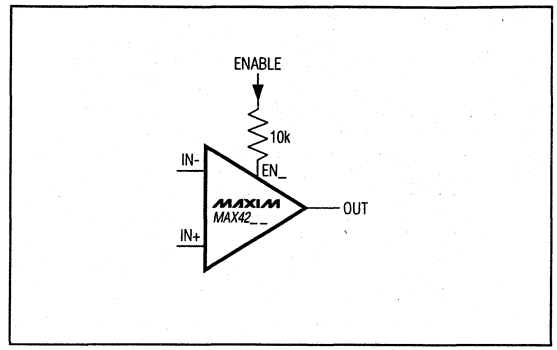


Figure 3. Circuit to Reduce Enable Logic-Low Input Current

Output Capacitive Loading and Stability

The MAX4212/MAX4213/MAX4216/MAX4218/MAX4220 are optimized for AC performance. They are not designed to drive highly reactive loads, which decreases phase margin and may produce excessive ringing and oscillation. Figure 5 shows a circuit that eliminates this problem. Figure 6 is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figure 7 shows how a capacitive load causes excessive peaking of the amplifier's frequency response if the capacitor is not isolated from the amplifier by a resistor. A small isolation resistor (usually 20Ω to 30Ω) placed before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance is controlled by the interaction of the load capacitance and the isolation resistor. Figure 8 shows the effect of a 27Ω isolation resistor on closed-loop response.

Coaxial cable and other transmission lines are easily driven when properly terminated at both ends with their characteristic impedance. Driving back-terminated transmission lines essentially eliminates the line's capacitance.

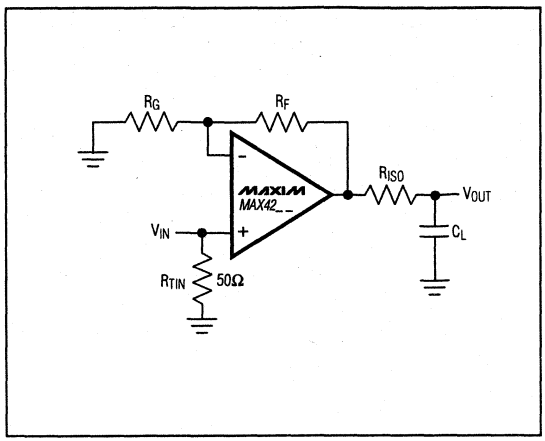


Figure 5. Driving a Capacitive Load through an Isolation Resistor

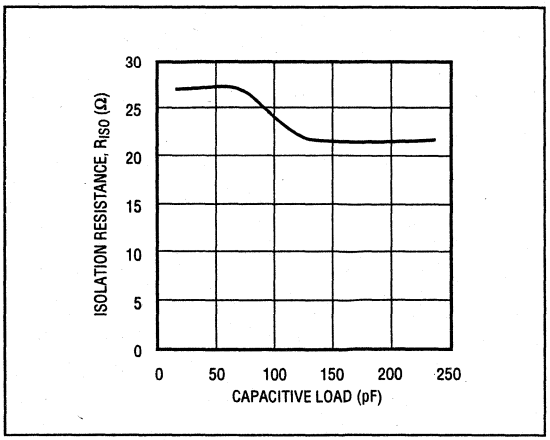


Figure 6. Capacitive Load vs. Isolation Resistance

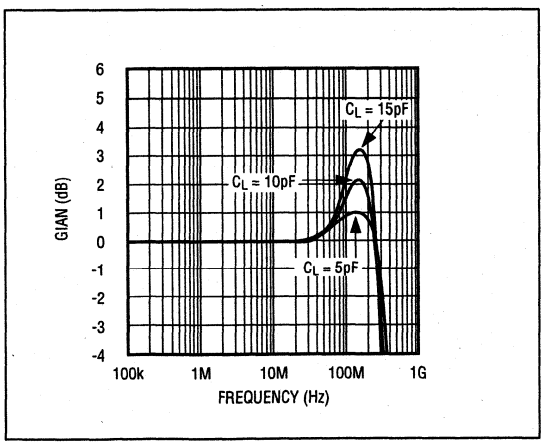


Figure 7. Small-Signal Gain vs. Frequency with Load Capacitance and No Isolation Resistor

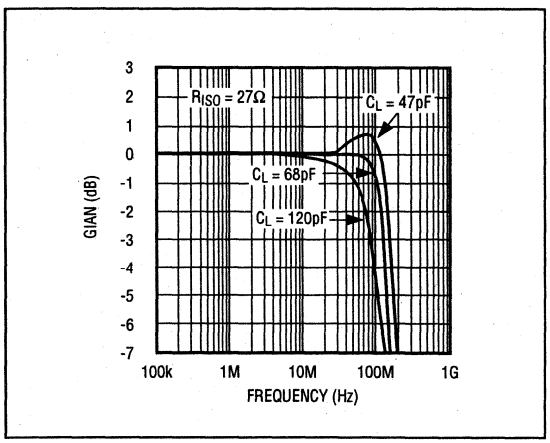
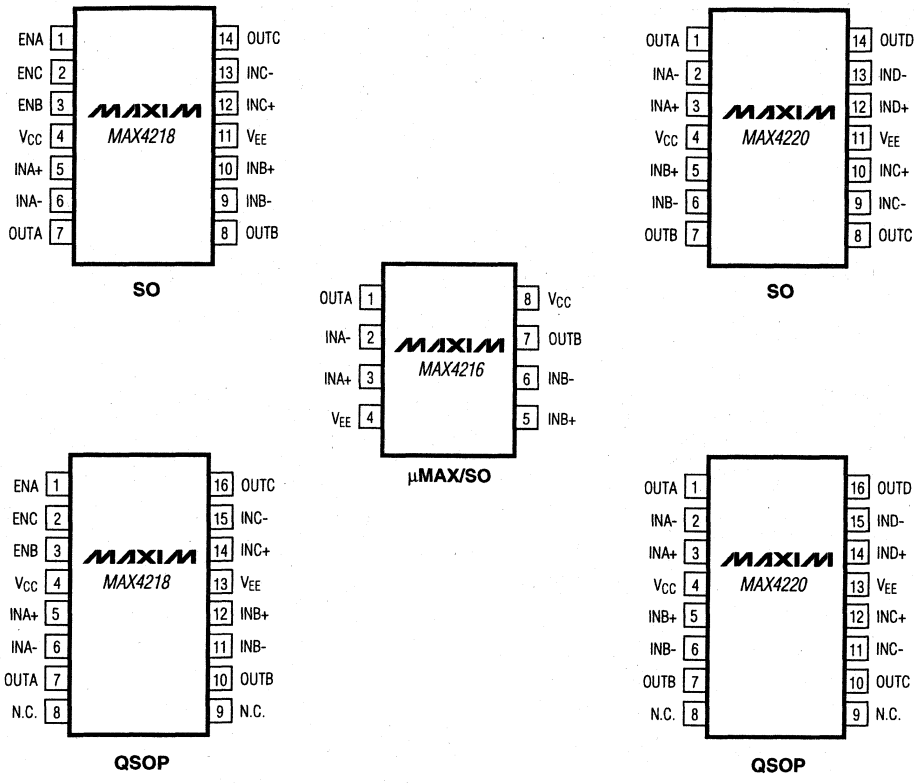


Figure 8. Small-Signal Gain vs. Frequency with Load Capacitance and 27Ω Isolation Resistor

Miniature, 300MHz, Single-Supply, Rail-to-Rail Op Amps with Enable

Pin Configurations (continued)

TOP VIEW



_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4216ESA	-40°C to +85°C	8 SO	—
MAX4216EUA	-40°C to +85°C	8 µMAX	—
MAX4218ESD	-40°C to +85°C	14 SO	—
MAX4218EEE	-40°C to +85°C	16 QSOP	—
MAX4220ESD	-40°C to +85°C	14 SO	—
MAX4220EEE	-40°C to +85°C	16 QSOP	—

Chip Information

PART	TRANSISTOR COUNT
MAX4212/MAX4213	95
MAX4216	190
MAX4218	299
MAX4220	362

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

SOT23, 300MHz, Single-Supply, Gain of +2V/V, Closed-Loop, Rail-to-Rail Buffers with Enable

General Description

The MAX4214/MAX4215 single, MAX4217 dual, MAX4219 triple, and MAX4222 quad precision, closed-loop, gain of +2V/V, single-supply buffers feature high slew rate, high output current drive, low noise, and low differential gain and phase errors. These devices operate from a +3.3V to +10V single supply or from ±1.65V to ±5V dual supplies. The input common-mode voltage range extends 200mV beyond the negative power-supply rail, and the output swings Rail-to-Rail®.

The MAX4214 family of buffers require only 5.5mA of quiescent supply current while achieving a 300MHz -3dB bandwidth and a 600V/µs slew rate. Input voltage noise is only 10nV/√Hz, and input current noise is only 1.3pA/√Hz. These devices are ideal for low-power/low-voltage applications that require wide bandwidth, such as video, communications, and instrumentation systems. The MAX4215/MAX4219 have a disable feature that reduces power-supply current to 350µA (max) and places the outputs into a high-impedance state. When disabled, these devices have a 1kΩ output impedance, making them well suited for multiplexing applications.

Features

- **High Speed:**
  300MHz -3dB Bandwidth (MAX4214/15)
  200MHz -3dB Bandwidth (MAX4217/19/22)
  50MHz 0.1dB Gain Flatness (MAX4214/15)
  600V/µs Slew Rate
- **+3.3V/+5V Single-Supply Operation**
- **Input Common-Mode Range Extends Beyond V_{EE}**
- **0.02%/0.02° Differential Gain/Phase**
- **Low Distortion at 5MHz:**
  -78dBc Spurious-Free Dynamic Range
  -75dB Total Harmonic Distortion
- **±100mA Output Drive**
- **5.5mA Supply Current**
- **Shutdown Capability: I_S < 350µA (MAX4215/19)**
- **High Output Impedance in Off State (MAX4215/19)**
- **Space-Saving SOT23-5, µMAX, or QSOP Packages**

Applications

Battery-Powered Instruments
Video Line Drivers
Analog-to-Digital Converter Interface
CCD Imaging Systems
Video Routing and Switching Systems
Video Multiplexing Applications

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4214EUK-T	-40°C to +85°C	5 SOT23-5	ABAH
MAX4215ESA	-40°C to +85°C	8 SO	—
MAX4217ESA	-40°C to +85°C	8 SO	—
MAX4217EUA	-40°C to +85°C	8 µMAX	—

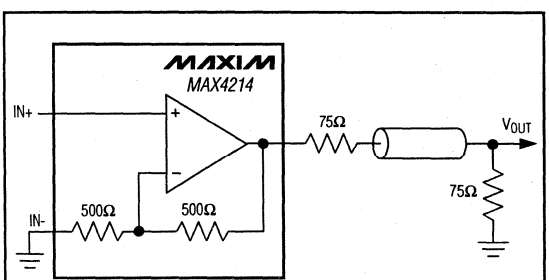
Ordering Information continued on next page.

Selector Guide

PART	NUMBER OF AMPLIFIERS	ENABLE	PIN-PACKAGE
MAX4214	1	No	5 SOT23
MAX4215	1	Yes	8 SO
MAX4217	2	No	8 SO/µMAX
MAX4219	3	Yes	14 SO 16 QSOP
MAX4222	4	No	14 SO 16 QSOP

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

Typical Operating Circuit



VIDEO/RF CABLE DRIVER

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For small orders, phone 408-737-7600 ext. 3468.

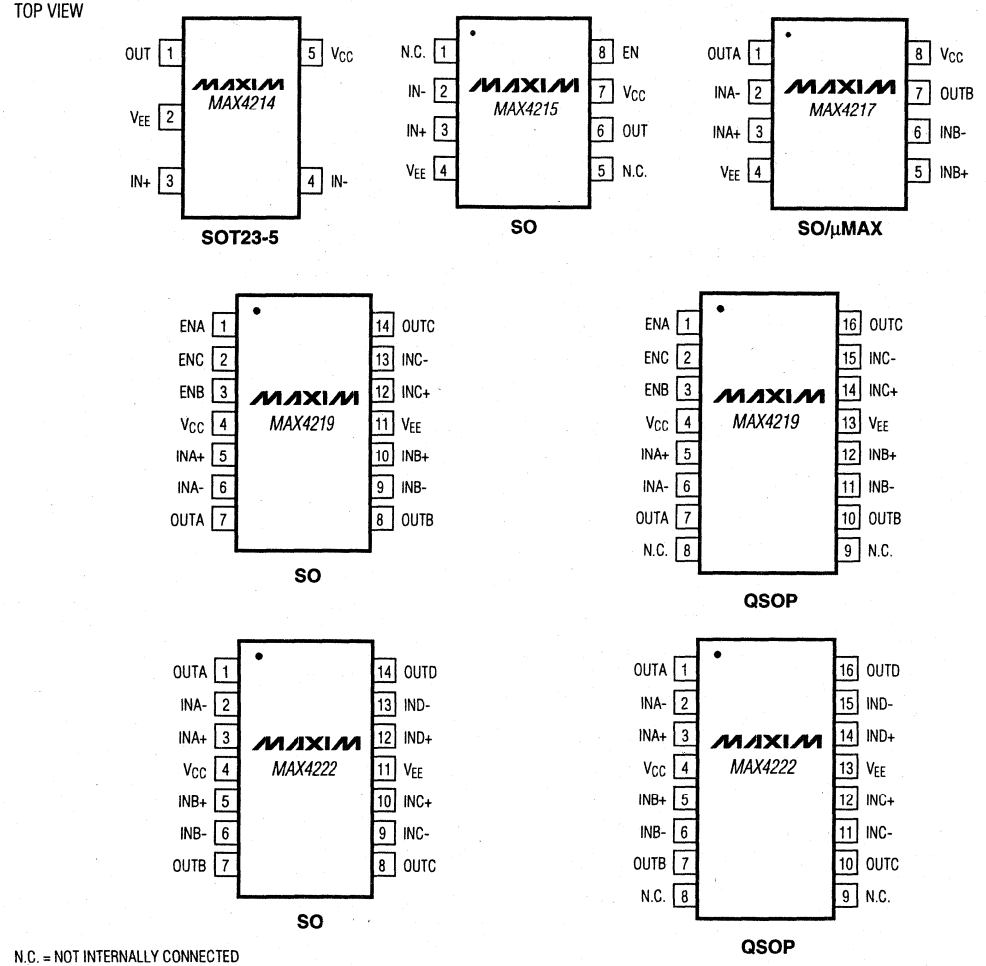
SOT23, 300MHz, Single-Supply, Gain of +2V/V, Closed-Loop, Rail-to-Rail Buffers with Enable

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4219ESD	-40°C to +85°C	14 SO	—
MAX4219EEE	-40°C to +85°C	16 QSOP	—
MAX4222ESD	-40°C to +85°C	14 SO	—
MAX4222EEE	-40°C to +85°C	16 QSOP	—

_Pin Configurations

TOP VIEW



N.C. = NOT INTERNALLY CONNECTED

19-1230; Rev 2; 6/97

EVALUATION KIT AVAILABLE

MAXIM

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

General Description

The MAX4223–MAX4228 current-feedback amplifiers combine ultra-high-speed performance, low distortion, and excellent video specifications with low-power operation. The MAX4223/MAX4224/MAX4226/MAX4228 have a shutdown feature that reduces power-supply current to 350µA and places the outputs into a high-impedance state. These devices operate with dual supplies ranging from ±2.85V to ±5.5V and provide a typical output drive current of 80mA. The MAX4223/MAX4225/MAX4226 are optimized for a closed-loop gain of +1 (0dB) or more and have a -3dB bandwidth of 1GHz, while the MAX4224/MAX4227/MAX4228 are compensated for a closed-loop gain of +2 (6dB) or more, and have a -3dB bandwidth of 600MHz (1.2GHz gain-bandwidth product).

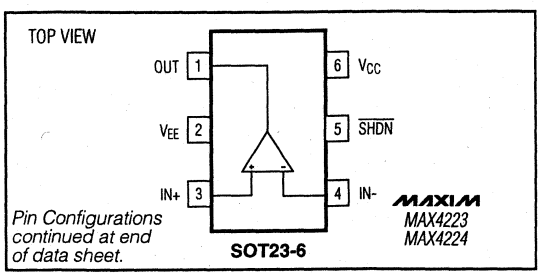
The MAX4223–MAX4228 are ideal for professional video applications, with differential gain and phase errors of 0.01% and 0.02°, 0.1dB gain flatness of 300MHz, and a 1100V/µs slew rate. Total harmonic distortion (THD) of -60dBc (10MHz) and an 8ns settling time to 0.1% suit these devices for driving high-speed analog-to-digital inputs or for data-communications applications. The low-power shutdown mode on the MAX4223/MAX4224/MAX4226/MAX4228 makes them suitable for portable and battery-powered applications. Their high output impedance in shutdown mode is excellent for multiplexing applications.

The single MAX4223/MAX4224 are available in space-saving 6-pin SOT23 packages. All devices are available in the extended -40°C to +85°C temperature range.

Applications

ADC Input Buffers	Data Communications
Video Cameras	Video Line Drivers
Video Switches	Video Multiplexing
Video Editors	XDSL Drivers
RF Receivers	Differential Line Drivers

Pin Configurations



Pin Configurations continued at end of data sheet.

Features

- **Ultra-High Speed and Fast Settling Time:**
  1GHz -3dB Bandwidth (MAX4223, Gain = +1)
  600MHz -3dB Bandwidth (MAX4224, Gain = +2)
  1700V/µs Slew Rate (MAX4224)
  5ns Settling Time to 0.1% (MAX4224)
- **Excellent Video Specifications (MAX4223):**
  Gain Flatness of 0.1dB to 300MHz
  0.01%/0.02° DG/DP Errors
- **Low Distortion:**
  -60dBc THD (f_C = 10MHz)
  42dBm Third-Order Intercept (f = 30MHz)
- **6.0mA Quiescent Supply Current (per amplifier)**
- **Shutdown Mode:**
  350µA Supply Current (per amplifier)
  100kΩ Output Impedance
- **High Output Drive Capability:**
  80mA Output Current
  Drives up to 4 Back-Terminated 75Ω Loads to ±2.5V while Maintaining Excellent Differential Gain/Phase Characteristics
- **Available in Tiny 6-Pin SOT23 and 10-Pin µMAX Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4223EUT-T	-40°C to +85°C	6 SOT23	AAAD
MAX4223ESA	-40°C to +85°C	8 SO	—

Ordering Information continued at end of data sheet.

8

Selector Guide

PART	MIN. GAIN	AMPS PER PKG.	SHUT-DOWN MODE	PIN-PACKAGE
MAX4223	1	1	Yes	6 SOT23, 8 SO
MAX4224	2	1	Yes	6 SOT23, 8 SO
MAX4225	1	2	No	8 SO
MAX4226	1	2	Yes	10 µMAX, 14 SO
MAX4227	2	2	No	8 SO
MAX4228	2	2	Yes	10 µMAX, 14 SO

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For small orders, phone 408-737-7600 ext. 3468.

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Analog Input Voltage ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Analog Input Current ..... ±25mA
$\overline{SHDN}$ Input Voltage ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Short-Circuit Duration
  OUT to GND ..... Continuous
  OUT to V_{CC} or V_{EE} 5sec

Continuous Power Dissipation (T_A = +70°C)
  6-Pin SOT23 (derate 7.1mW/°C above +70°C) 571mW
  8-Pin SO (derate 5.9mW/°C above +70°C) 471mW
  10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
  14-Pin SO (derate 8.3mW/°C above +70°C) 667mW
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $\overline{SHDN}$ = 5V, V_{CM} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	T_A = +25°C	MAX4223/MAX4224		±0.5	±4	mV
			MAX4225–MAX4228		±0.5	±5	
		T_A = T_{MIN} to T_{MAX}	MAX4223/MAX4224			±6	
			MAX4225–MAX4228			±7	
Input Offset Voltage Drift	TCV_{OS}				±2		µV/°C
Input Bias Current (Positive Input)	I_{B+}	T_A = +25°C			±2	±10	µA
		T_A = T_{MIN} to T_{MAX}				±15	
Input Bias Current (Negative Input)	I_{B-}	T_A = +25°C	MAX4223/MAX4224		±4	±20	µA
			MAX4225–MAX4228		±4	±25	
		T_A = T_{MIN} to T_{MAX}	MAX4223/MAX4224			±30	
			MAX4225–MAX4228			±35	
Input Resistance (Positive Input)	R_{IN+}				700		kΩ
Input Resistance (Negative Input)	R_{IN-}				45		Ω
Input Common-Mode Voltage Range	V_{CM}	Inferred from CMRR test		±2.5	±3.2		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±2.5V	T_A = +25°C	55	61		dB
			T_A = T_{MIN} to T_{MAX}	50			
Operating Supply Voltage Range	V_{CC}/V_{EE}	Inferred from PSRR test		±2.85		±5.5	V
Power-Supply Rejection Ratio	PSRR	V_{CC} = 2.85V to 5.5V, V_{EE} = -2.85V to -5.5V	T_A = +25°C	68	74		dB
			T_A = T_{MIN} to T_{MAX}	63			
Quiescent Supply Current (per Amplifier)	I_{SY}	Normal mode ($\overline{SHDN}$ = 5V)			6.0	9.0	mA
		Shutdown mode ($\overline{SHDN}$ = 0V)			0.35	0.55	
Open-Loop Transresistance	T_R	V_{OUT} = ±2.5V	R_L = ∞	0.7	1.5		MΩ
			R_L = 50Ω	0.3	0.8		
Output Voltage Swing	V_{OUT}	R_L = 50Ω		±2.5	±2.8		V
Output Current (Note 2)	I_{OUT}	V_{OUT} = ±2.5V		60	80		mA
Short-Circuit Output Current	I_{SC}	R_L = short to ground			140		mA
$\overline{SHDN}$ Logic Low	V_{IL}					0.8	V
$\overline{SHDN}$ Logic High	V_{IH}			2.0			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, $\overline{SHDN}$ = 5V, V_{CM} = 0V, R_L = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Input Current	I_{IL}/I_{IH}	$\overline{SHDN}$ = 0V or 5V		25	70	µA
Shutdown Mode Output Impedance		$\overline{SHDN}$ = 0V, V_{OUT} = -2.5V to +2.5V (Note 3)	10	100		kΩ

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, $\overline{SHDN}$ = 5V, V_{CM} = 0V, A_V = +1V/V for MAX4223/MAX4225/MAX4226, A_V = +2V/V for MAX4224/MAX4227/MAX4228, R_L = 100Ω, T_A = +25°C, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
-3dB Small-Signal Bandwidth (Note 5)	BW	V_{OUT} = 20mVp-p		MAX4223/5/6	750	1000		MHz
				MAX4224/7/8	325	600		
Bandwidth for ±0.1dB Gain Flatness (Note 5)	$BW_{0.1dB}$	V_{OUT} = 20mVp-p		MAX4223/5/6	100	300		MHz
				MAX4224/7/8	60	200		
Gain Peaking		MAX4223/5/6				1.5		dB
		MAX4224/7/8				0.1		
Large-Signal Bandwidth	BW_{LS}	V_{OUT} = 2Vp-p		MAX4223/5/6		250		MHz
				MAX4224/7/8		330		
Slew Rate (Note 5)	SR	V_{OUT} = 4V step	Rising edge	MAX4223/5/6	850	1100		V/µs
				MAX4224/7/8	1400	1700		
			Falling edge	MAX4223/5/6	625	800		
				MAX4224/7/8	1100	1400		
Settling Time to 0.1%	t_S	V_{OUT} = 2V step		MAX4223/5/6		8		ns
				MAX4224/7/8		5		
Rise and Fall Time	t_r, t_f	V_{OUT} = 2V step		MAX4223/5/6		1.5		ns
				MAX4224/7/8		1.0		
Off Isolation		$\overline{SHDN}$ = 0V, f = 10MHz, MAX4223/4/6/8				65		dB
Crosstalk	X_{TALK}	f = 30MHz, R_S = 50Ω		MAX4225/6		-68		dB
				MAX4227/8		-72		
Turn-On Time from Shutdown	t_{ON}	MAX4223/4/6/8				2		µs
Turn-Off Time to Shutdown	t_{OFF}	MAX4223/4/6/8				300		ns
Power-Up Time	t_{UP}	V_{CC}, V_{EE} = 0V to ±5V step				100		ns
Differential Gain Error	DG	R_L = 150Ω (Note 6)		MAX4223/5/6		0.01		%
				MAX4224/7/8		0.02		
Differential Phase Error	DP	R_L = 150Ω (Note 6)		MAX4223/5/6		0.02		degrees
				MAX4224/7/8		0.01		
Total Harmonic Distortion	THD	V_{OUT} = 2Vp-p, f_C = 10MHz	R_L = 100Ω	MAX4223/5/6		-60		dBc
				MAX4224/7/8		-61		
			R_L = 1kΩ	MAX4223/5/6		-65		
				MAX4224/7/8		-78		

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

AC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, $\overline{SHDN}$ = 5V, V_{CM} = 0V, A_V = +1V/V for MAX4223/MAX4225/MAX4226, A_V = +2V/V for MAX4224/MAX4227/MAX4228, R_L = 100Ω, T_A = +25°C, unless otherwise noted.) (Note 4)

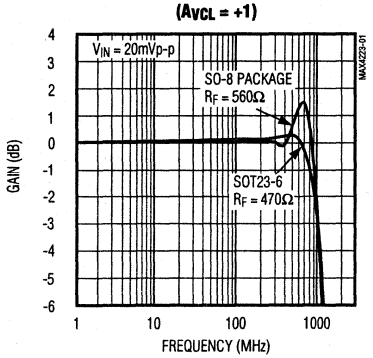
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Impedance	Z_{OUT}	f = 10kHz			2		Ω
Third-Order Intercept	IP3	f = 30kHz, f_Z = 30.1MHz	MAX4223/5/6		42		dBm
			MAX4224/7/8		36		
Spurious-Free Dynamic Range	SFDR	f = 10kHz	MAX4223/5/6		-61		dB
			MAX4224/7/8		-62		
1dB Gain Compression		f = 10kHz			20		dBm
Input Noise Voltage Density	e_n	f = 10kHz			2		nV/√Hz
Input Noise Current Density	i_n+, i_n-	f = 10kHz	IN+		3		pA/√Hz
			IN-		20		
Input Capacitance (Note 7)	C_{IN}	SO-8, SO-14 packages	Pin to pin		0.3		pF
			Pin to GND		1.0		
		SOT23-6, 10-pin μMAX packages	Pin to pin		0.3		
			Pin to GND		0.8		

Note 1: The MAX422_EUT is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 2: Absolute Maximum Power Dissipation must be observed.
Note 3: Does not include impedance of external feedback resistor network.
Note 4: AC specifications shown are with optimal values of R_F and R_G. These values vary for product and package type, and are tabulated in the *Applications Information* section of this data sheet.
Note 5: The AC specifications shown are not measured in a production test environment. The minimum AC specifications given are based on the combination of worst-case design simulations along with a sample characterization of units. These minimum specifications are for design guidance only and are not intended to guarantee AC performance (see *AC Testing/ Performance*). For 100% testing of these parameters, contact the factory.
Note 6: Input Test Signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE). IRE is a unit of video signal amplitude developed by the International Radio Engineers. 140IRE = 1V.
Note 7: Assumes printed circuit board layout similar to that of Maxim's evaluation kit.

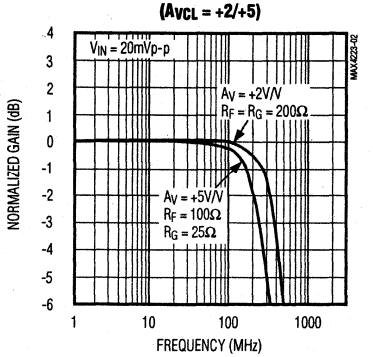
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

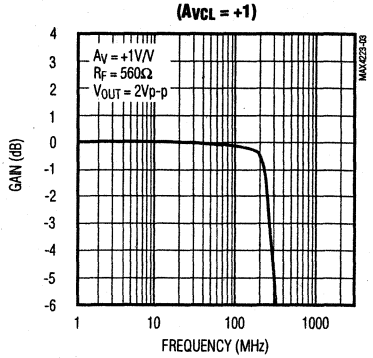
MAX4223
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



MAX4223
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2/+5)



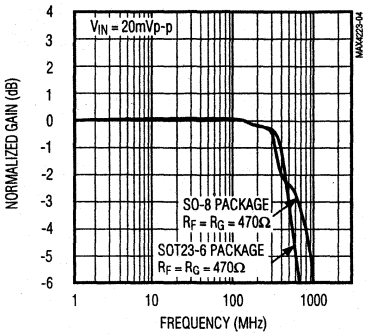
MAX4223/MAX4225/MAX4226
LARGE-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



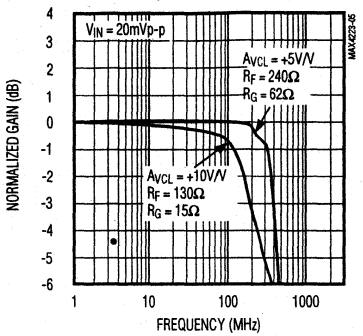
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

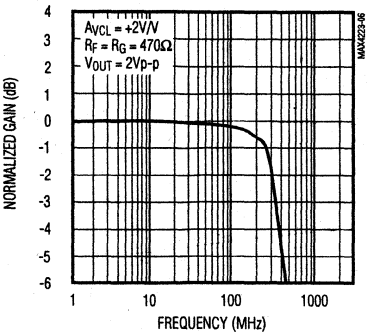
MAX4224
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



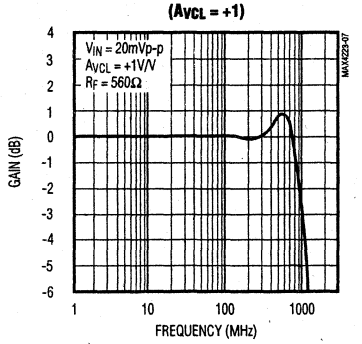
MAX4224
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +5/+10)



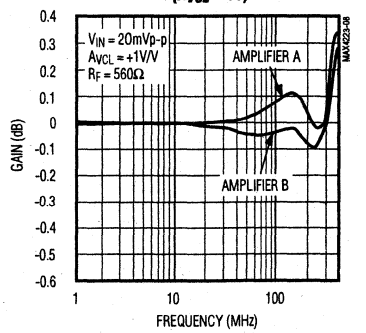
MAX4224/MAX4227/MAX4228
LARGE-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



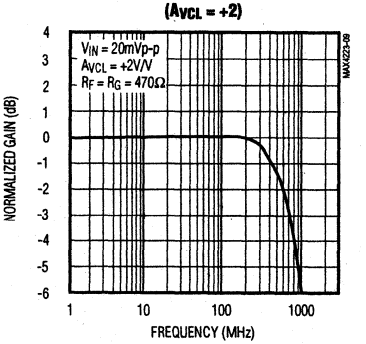
MAX4225/MAX4226
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +1)



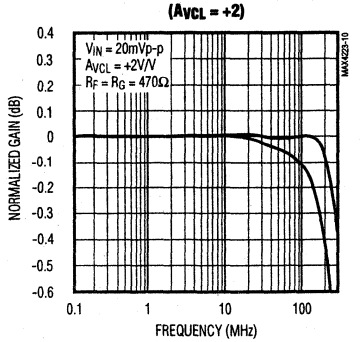
MAX4225/MAX4226
GAIN MATCHING vs. FREQUENCY
(A_{VCL} = +1)



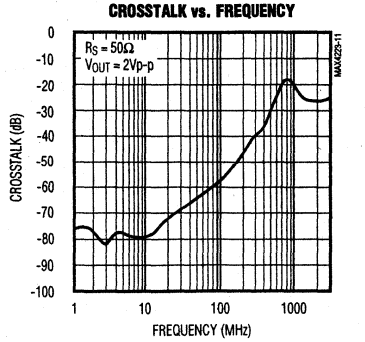
MAX4227/MAX4228
SMALL-SIGNAL GAIN vs. FREQUENCY
(A_{VCL} = +2)



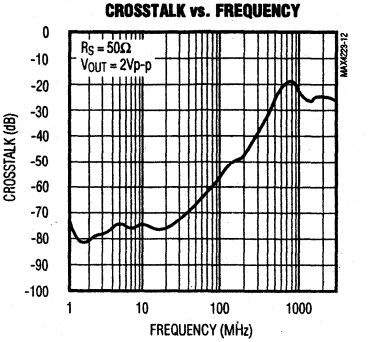
MAX4227/MAX4228
GAIN MATCHING vs. FREQUENCY
(A_{VCL} = +2)



MAX4225/MAX4226
CROSSTALK vs. FREQUENCY



MAX4227/MAX4228
CROSSTALK vs. FREQUENCY

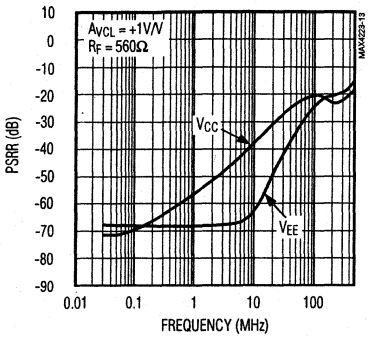


1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

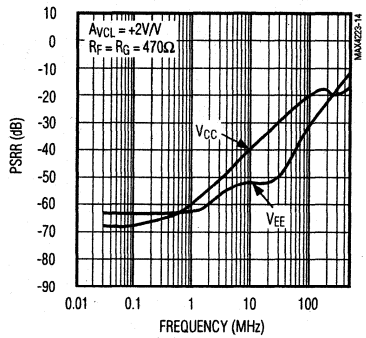
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

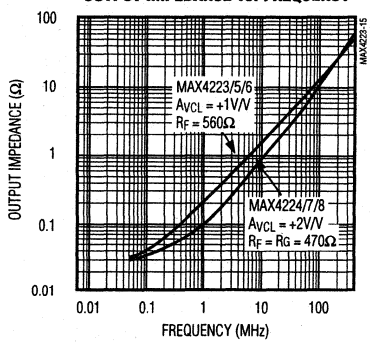
MAX4223/MAX4225/MAX4226 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (A_{VCL} = +1)



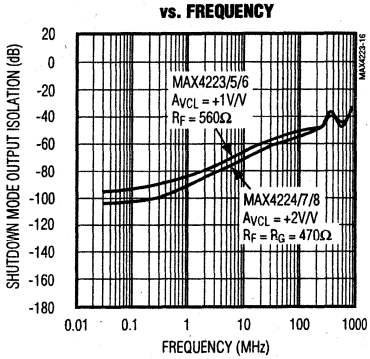
MAX4224/MAX4227/MAX4228 POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (A_{VCL} = +2)



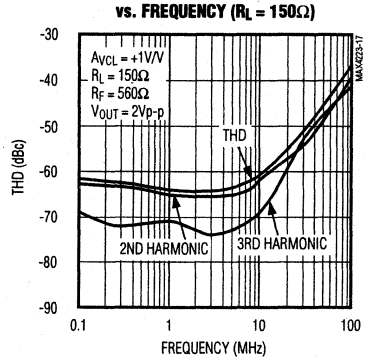
OUTPUT IMPEDANCE vs. FREQUENCY



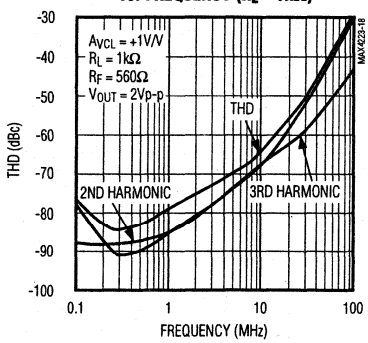
SHUTDOWN MODE OUTPUT ISOLATION vs. FREQUENCY



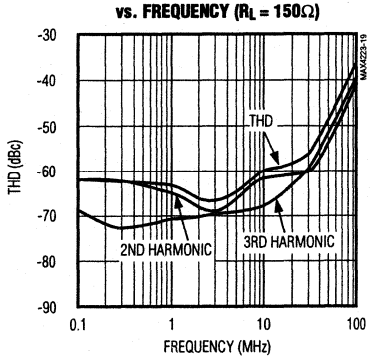
MAX4223/MAX4225/MAX4226 TOTAL HARMONIC DISTORTION vs. FREQUENCY (R_L = 150Ω)



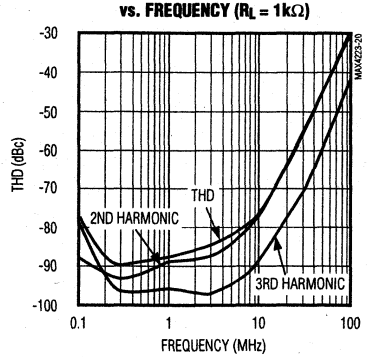
MAX4223/MAX4225/MAX4226 TOTAL HARMONIC DISTORTION vs. FREQUENCY (R_L = 1kΩ)



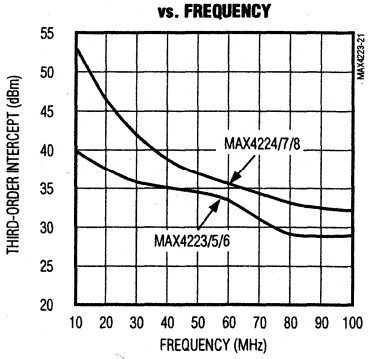
MAX4224/MAX4227/MAX4228 TOTAL HARMONIC DISTORTION vs. FREQUENCY (R_L = 150Ω)



MAX4224/MAX4227/MAX4228 TOTAL HARMONIC DISTORTION vs. FREQUENCY (R_L = 1kΩ)



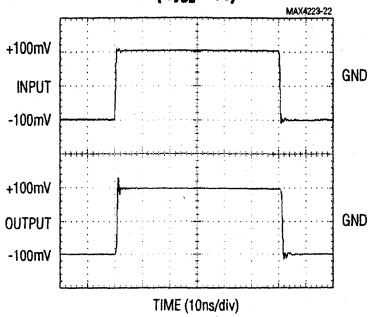
TWO-TONE THIRD-ORDER INTERCEPT vs. FREQUENCY



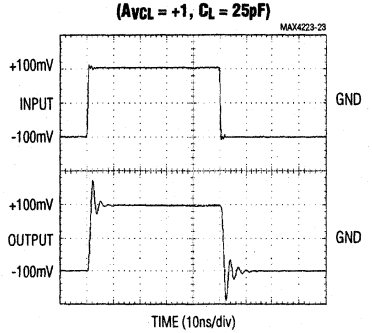
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

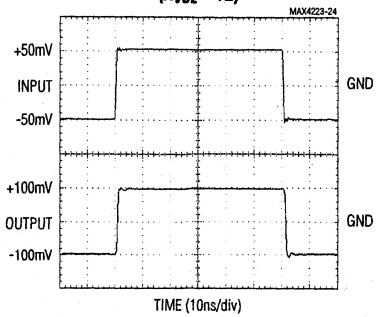
MAX4223/MAX4225/MAX4226 SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



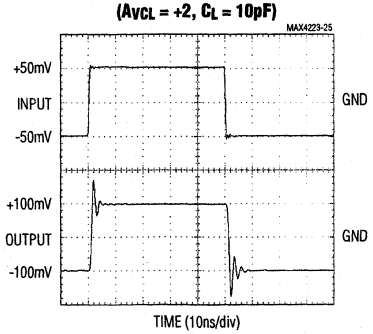
MAX4223/MAX4225/MAX4226 SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +1, C_L = 25pF)



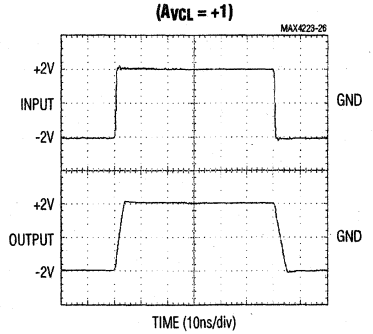
MAX4224/MAX4227/MAX4228 SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



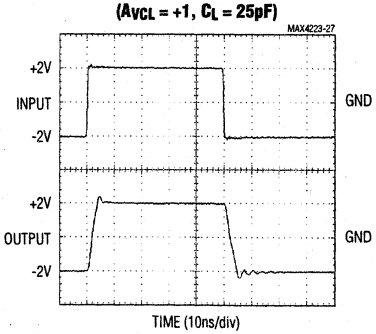
MAX4224/MAX4227/MAX4228 SMALL-SIGNAL PULSE RESPONSE (A_{VCL} = +2, C_L = 10pF)



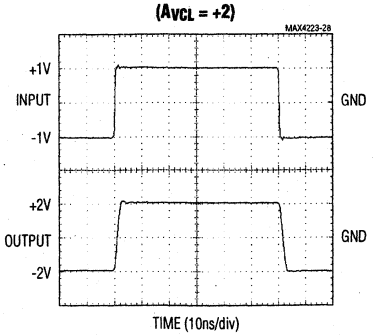
MAX4223/MAX4225/MAX4226 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1)



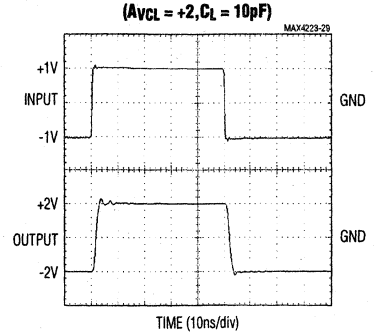
MAX4223/MAX4225/MAX4226 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +1, C_L = 25pF)



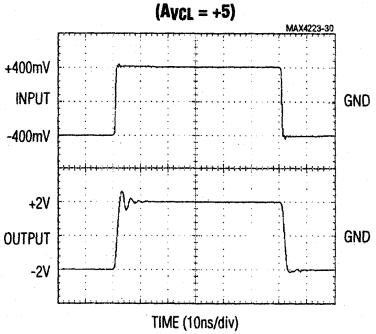
MAX4224/MAX4227/MAX4228 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2)



MAX4224/MAX4227/MAX4228 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +2, C_L = 10pF)



MAX4224/MAX4227/MAX4228 LARGE-SIGNAL PULSE RESPONSE (A_{VCL} = +5)



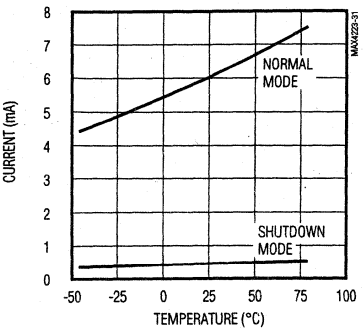
8

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

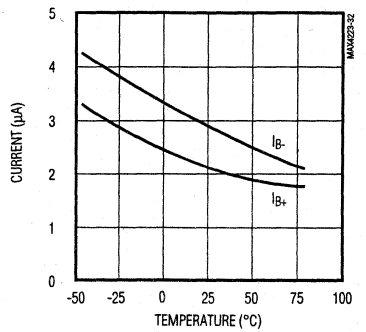
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

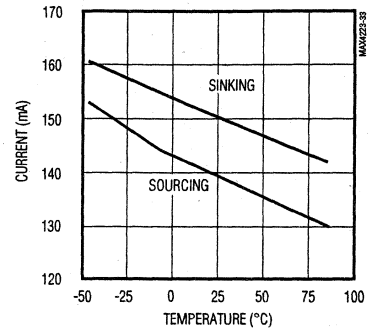
POWER-SUPPLY CURRENT PER AMPLIFIER vs. TEMPERATURE



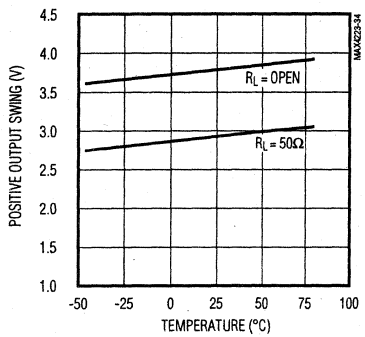
INPUT BIAS CURRENT vs. TEMPERATURE



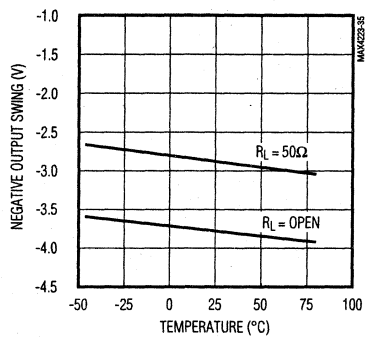
SHORT-CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



POSITIVE OUTPUT SWING vs. TEMPERATURE



NEGATIVE OUTPUT SWING vs. TEMPERATURE



1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

Pin Description

PIN					NAME	FUNCTION
MAX4223/MAX4224		MAX4225 MAX4227	MAX4226/MAX4228			
SOT23	SO	SO	µMAX	SO		
—	1, 5	—	—	5, 7, 8, 10	N.C.	No Connect. Not internally connected. Tie to GND for optimum AC performance.
1	6	—	—	—	OUT	Amplifier Output
2	4	4	4	4	V_{EE}	Negative Power-Supply Voltage. Connect to -5V.
3	3	—	—	—	IN+	Amplifier Noninverting Input
4	2	—	—	—	IN-	Amplifier Inverting Input
5	8	—	—	—	$\overline{SHDN}$	Amplifier Shutdown. Connect to +5V for normal operation. Connect to GND for low-power shutdown.
6	7	8	10	14	V_{CC}	Positive Power-Supply Voltage. Connect to +5V.
—	—	1	1	1	OUTA	Amplifier A Output
—	—	2	2	2	INA-	Amplifier A Inverting Input
—	—	3	3	3	INA+	Amplifier A Noninverting Input
—	—	5	7	11	INB+	Amplifier B Noninverting Input
—	—	6	8	12	INB-	Amplifier B Inverting Input
—	—	7	9	13	OUTB	Amplifier B Output
—	—	—	5	6	$\overline{SHDNA}$	Amplifier A Shutdown Input. Connect to +5V for normal operation. Connect to GND for low-power shutdown mode.
—	—	—	6	9	$\overline{SHDNB}$	Amplifier B Shutdown Input. Connect to +5V for normal operation. Connect to GND for low-power shutdown mode.

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

Detailed Description

The MAX4223–MAX4228 are ultra-high-speed, low-power, current-feedback amplifiers featuring -3dB bandwidths up to 1GHz, 0.1dB gain flatness up to 300MHz, and very low differential gain and phase errors of 0.01% and 0.02°, respectively. These devices operate on dual ±5V or ±3V power supplies and require only 6mA of supply current per amplifier. The MAX4223/MAX4225/MAX4226 are optimized for closed-loop gains of +1 (0dB) or more and have -3dB bandwidths of 1GHz. The MAX4224/MAX4227/MAX4228 are optimized for closed-loop gains of +2 (6dB) or more, and have -3dB bandwidths of 600MHz (1.2GHz gain-bandwidth product).

The current-mode feedback topology of these amplifiers allows them to achieve slew rates of up to 1700V/µs with corresponding large signal bandwidths up to 330MHz. Each device in this family has an output that is capable of driving a minimum of 60mA of output current to ±2.5V.

Theory of Operation

Since the MAX4223–MAX4228 are current-feedback amplifiers, their open-loop transfer function is expressed as a transimpedance:

$$\frac{\Delta V_{OUT}}{\Delta I_{IN-}} \text{ or } T_Z$$

The frequency behavior of this open-loop transimpedance is similar to the open-loop gain of a voltage-feedback amplifier. That is, it has a large DC value and decreases at approximately 6dB per octave.

Analyzing the current-feedback amplifier in a gain configuration (Figure 1) yields the following transfer function:

$$\frac{V_{OUT}}{V_{IN}} = G \times \frac{T_Z(S)}{T_Z(S) + G \times R_{IN-} + R_F}$$

where $G = A_V = 1 + \frac{R_F}{R_G}$.

At low gains, $(G \times R_{IN-}) << R_F$. Therefore, unlike traditional voltage-feedback amplifiers, the closed-loop bandwidth is essentially independent of the closed-loop gain. Note also that at low frequencies, $T_Z >> [(G \times R_{IN-}) + R_F]$, so that:

$$\frac{V_{OUT}}{V_{IN}} = G = 1 + \frac{R_F}{R_G}$$

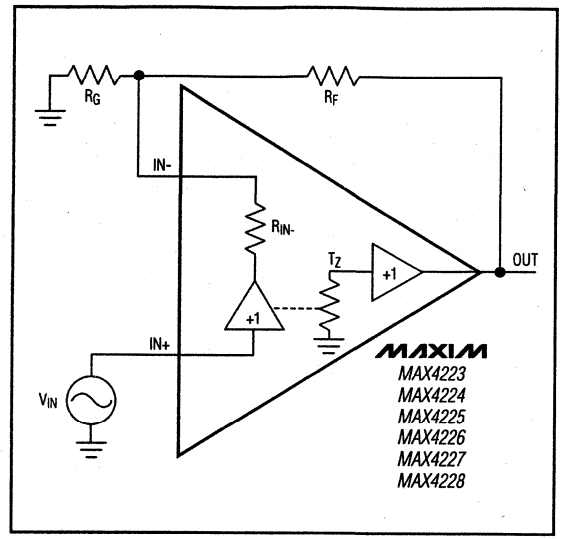


Figure 1. Current-Feedback Amplifier

Low-Power Shutdown Mode

The MAX4223/MAX4224/MAX4226/MAX4228 have a shutdown mode that is activated by driving the $\overline{SHDN}$ input low. When powered from ±5V supplies, the $\overline{SHDN}$ input is compatible with TTL logic. Placing the amplifier in shutdown mode reduces quiescent supply current to 350µA typical, and puts the amplifier output into a high-impedance state (100kΩ typical). This feature allows these devices to be used as multiplexers in wideband systems. To implement the mux function, the outputs of multiple amplifiers can be tied together, and only the amplifier with the selected input will be enabled. All of the other amplifiers will be placed in the low-power shutdown mode, with their high output impedance presenting very little load to the active amplifier output. For gains of +2 or greater, the feedback network impedance of all the amplifiers used in a mux application must be considered when calculating the total load on the active amplifier output.

Applications Information

Layout and Power-Supply Bypassing

The MAX4223–MAX4228 have an extremely high bandwidth, and consequently require careful board layout, including the possible use of constant-impedance microstrip or stripline techniques.

To realize the full AC performance of these high-speed amplifiers, pay careful attention to power-supply bypassing and board layout. The PC board should have at least two layers: a signal and power layer on one side and a large, low-impedance ground plane on the other. The ground plane should be as free of voids as possible, with one exception: the inverting input pin (IN-) should have as low a capacitance to ground as possible. This means that there should be no ground plane under IN- or under the components (R_F and R_G) connected to it. With multilayer boards, locate the ground plane on a layer that incorporates no signal or power traces.

Whether or not a constant-impedance board is used, it is best to observe the following guidelines when designing the board:

1) Do not use wire-wrapped boards (they are too inductive) or breadboards (they are too capacitive).
2) Do not use IC sockets. IC sockets increase reactance.
3) Keep signal lines as short and straight as possible. Do not make 90° turns; round all corners.
4) Observe high-frequency bypassing techniques to maintain the amplifier's accuracy and stability.
5) In general, surface-mount components have shorter bodies and lower parasitic reactance, giving better high-frequency performance than through-hole components.

The bypass capacitors should include a 10nF ceramic, surface-mount capacitor between each supply pin and the ground plane, located as close to the package as possible. Optionally, place a 10µF tantalum capacitor at the power-supply pins' point of entry to the PC board to ensure the integrity of incoming supplies. The power-supply trace should lead directly from the tantalum capacitor to the V_{CC} and V_{EE} pins. To minimize parasitic inductance, keep PC traces short and use surface-mount components. The N.C. pins should be connected to a common ground plane on the PC board to minimize parasitic coupling.

If input termination resistors and output back-termination resistors are used, they should be surface-mount types, and should be placed as close to the IC pins as possible. Tie all N.C. pins to the ground plane to minimize parasitic coupling.

Choosing Feedback and Gain Resistors

As with all current-feedback amplifiers, the frequency response of these devices depends critically on the value of the feedback resistor R_F. R_F combines with an internal compensation capacitor to form the dominant pole in the feedback loop. Reducing R_F's value increases the pole frequency and the -3dB bandwidth, but also increases peaking due to interaction with other nondominant poles. Increasing R_F's value reduces peaking and bandwidth.

Table 1 shows optimal values for the feedback resistor (R_F) and gain-setting resistor (R_G) for the MAX4223–MAX4228. Note that the MAX4224/MAX4227/MAX4228 offer superior AC performance for all gains except unity gain (0dB). These values provide optimal AC response using surface-mount resistors and good layout techniques. Maxim's high-speed amplifier evaluation kits provide practical examples of such layout techniques.

Stray capacitance at IN- causes feedback resistor decoupling and produces peaking in the frequency-response curve. Keep the capacitance at IN- as low as possible by using surface-mount resistors and by avoiding the use of a ground plane beneath or beside these resistors and the IN- pin. Some capacitance is unavoidable; if necessary, its effects can be counteracted by adjusting R_F. Use 1% resistors to maintain consistency over a wide range of production lots.

Table 1. Optimal Feedback Resistor Networks

GAIN (V/V)	GAIN (dB)	R_F (Ω)	R_G (Ω)	-3dB BW (MHz)	0.1dB BW (MHz)
MAX4223/MAX4225/MAX4226					
1	0	560*	Open	1000	300
2	6	200	200	380	115
5	14	100	25	235	65
MAX4224/MAX4227/MAX4228					
2	6	470	470	600	200
5	14	240	62	400	90
10	20	130	15	195	35

**For the MAX4223EUT, this optimal value is 470Ω.*

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

DC and Noise Errors

The MAX4223–MAX4228 output offset voltage, V_{OUT} (Figure 2), can be calculated with the following equation:

$$V_{OUT} = V_{OS} \times (1 + R_F/R_G) + I_{B+} \times R_S \times \left(1 + \frac{R_F}{R_G}\right) + I_{B-} \times R_F$$

where:

V_{OS} = input offset voltage (in volts)

$1 + R_F / R_G$ = amplifier closed-loop gain (dimensionless)

I_{B+} = input bias current (in amps)

I_{B-} = inverting input bias current (in amps)

R_G = gain-setting resistor (in Ω)

R_F = feedback resistor (in Ω)

R_S = source resistor (in Ω)

The following equation represents output noise density:

$$e_{n(OUT)} = \left(1 + \frac{R_F}{R_G}\right) \times \sqrt{(i_{n+} \times R_S)^2 + \left[i_{n-} \times (R_F \parallel R_G)\right]^2 + (e_n)^2}$$

where:

i_n = input noise current density (in pA/√Hz)

e_n = input noise voltage density (in nV/√Hz)

The MAX4223–MAX4228 have a very low, 2nV/√Hz noise voltage. The current noise at the noninverting input (i_{n+}) is 3pA/√Hz, and the current noise at the inverting input (i_{n-}) is 20pA/√Hz.

An example of DC-error calculations, using the MAX4224 typical data and the typical operating circuit with $R_F = R_G = 470\Omega$ ($R_F \parallel R_G = 235\Omega$) and $R_S = 50\Omega$, gives:

$$V_{OUT} = [5 \times 10^{-4} \times (1 + 1)] + [2 \times 10^{-6} \times 50 \times (1 + 1)] + [4 \times 10^{-6} \times 470]$$

$$V_{OUT} = 3.1mV$$

Calculating total output noise in a similar manner yields the following:

$$e_{n(OUT)} = (1 + 1) \times \sqrt{\left[\left(3 \times 10^{-12}\right) \times 50\right]^2 + \left[\left(20 \times 10^{-12}\right) \times 235\right]^2 + \left(2 \times 10^{-9}\right)^2}$$

$$e_{n(OUT)} = 10.2nV/\sqrt{Hz}$$

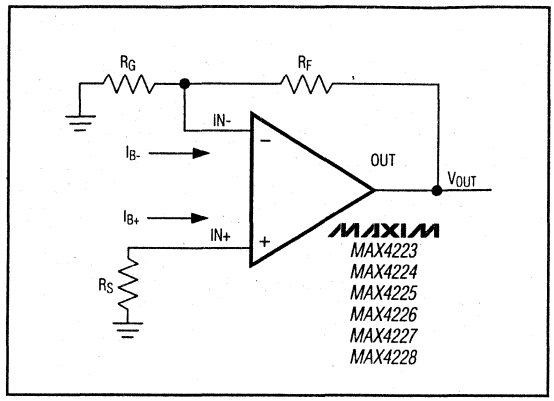


Figure 2. Output Offset Voltage

With a 600MHz system bandwidth, this calculates to 250μV_{RMS} (approximately 1.5mVp-p, using the six-sigma calculation).

Communication Systems

Nonlinearities of components used in a communication system produce distortion of the desired output signal. Intermodulation distortion (IMD) is the distortion that results from the mixing of two input signals of different frequencies in a nonlinear system. In addition to the input signal frequencies, the resulting output signal contains new frequency components that represent the sum and difference products of the two input frequencies. If the two input signals are relatively close in frequency, the third-order sum and difference products will fall close to the frequency of the desired output and will therefore be very difficult to filter. The third-order intercept (IP3) is defined as the power level at which the amplitude of the largest third-order product is equal to the power level of the desired output signal. Higher third-order intercept points correspond to better linearity of the amplifier. The MAX4223–MAX4228 have a typical IP3 value of 42dBm, making them excellent choices for use in communications systems.

ADC Input Buffers

Input buffer amplifiers can be a source of significant errors in high-speed ADC applications. The input buffer is usually required to rapidly charge and discharge the ADC's input, which is often capacitive (see the section *Driving Capacitive Loads*). In addition, a high-speed ADC's input impedance often changes very rapidly during the conversion cycle, requiring an amplifier with

very low output impedance at high frequencies to maintain measurement accuracy. The combination of high speed, fast slew rate, low noise, and low distortion makes the MAX4223–MAX4228 ideally suited for use as buffer amplifiers in high-speed ADC applications.

Video Line Driver

The MAX4223–MAX4228 are optimized to drive coaxial transmission lines when the cable is terminated at both ends, as shown in Figure 3. Note that cable frequency response may cause variations in the signal's flatness.

Driving Capacitive Loads

A correctly terminated transmission line is purely resistive and presents no capacitive load to the amplifier. Although the MAX4223–MAX4228 are optimized for AC performance and are not designed to drive highly capacitive loads, they are capable of driving up to 25pF without excessive ringing. Reactive loads decrease phase margin and may produce excessive ringing and oscillation (see *Typical Operating Characteristics*). Figure 4's circuit reduces the effect of large capacitive loads. The small (usually 5Ω to 20Ω) isolation resistor R_{ISO}, placed before the reactive load, prevents ringing and oscillation at the expense of a small gain error. At higher capacitive loads, AC performance is limited by the interaction of load capacitance with the isolation resistor.

Maxim's High-Speed Evaluation Board Layout

Figures 7 and 8 show a suggested layout for Maxim's high-speed, single-amplifier evaluation boards. These boards were developed using the techniques described above. The smallest available surface-mount resistors were used for the feedback and back-termination resistors to minimize the distance from the IC to these resistors, thus reducing the capacitance associated with longer lead lengths.

SMA connectors were used for best high-frequency performance. Because distances are extremely short, performance is unaffected by the fact that inputs and outputs do not match a 50Ω line. However, in applications that require lead lengths greater than 1/4 of the wavelength of the highest frequency of interest, constant-impedance traces should be used.

Fully assembled evaluation boards are available for the MAX4223 in an SO-8 package.

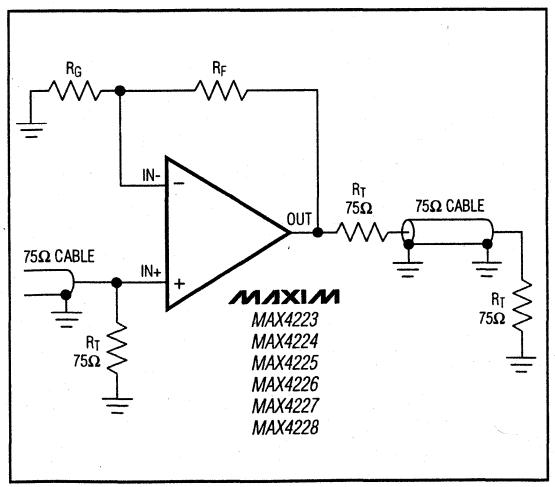


Figure 3. Video Line Driver

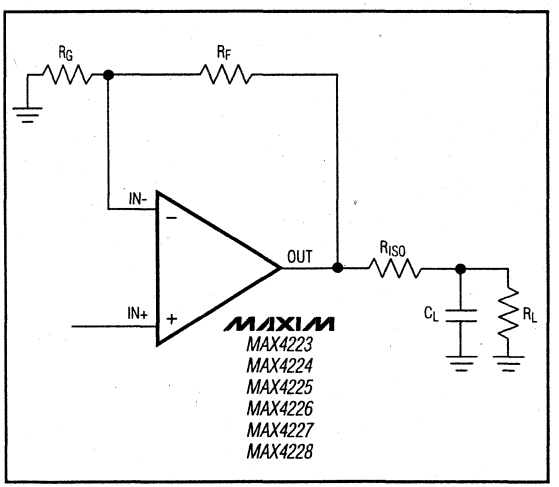


Figure 4. Using an Isolation Resistor (R_{ISO}) for High Capacitive Loads

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

AC Testing/Performance

AC specifications on high-speed amplifiers are usually guaranteed without 100% production testing. Since these high-speed devices are sensitive to external parasitics introduced when automatic handling equipment is used, it is impractical to guarantee AC parameters through volume production testing. These parasitics are greatly reduced when using the recommended PC board layout (like the Maxim evaluation kit). Characterizing the part in this way more accurately represents the amplifier's true AC performance. Some manufacturers guarantee AC specifications without clearly stating how this guarantee is made. The MAX4223–MAX4228 AC specifications are derived from worst-case design simulations combined with a sample characterization of 100 units. The AC performance distributions along with the worst-case simulation limits are shown in Figures 5 and 6. These distributions are repeatable provided that proper board layout and power-supply bypassing are used (see *Layout and Power-Supply Bypassing* section).

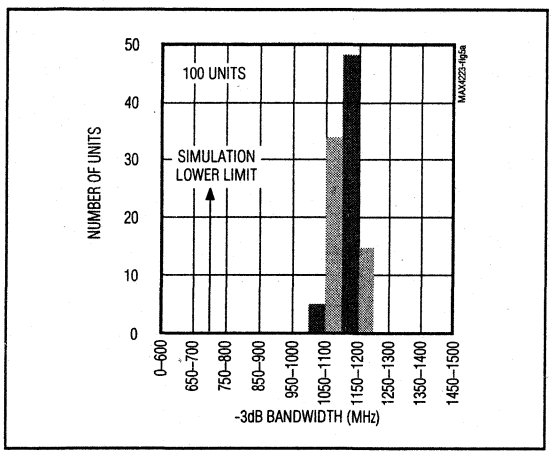


Figure 5a. MAX4223 -3dB Bandwidth Distribution

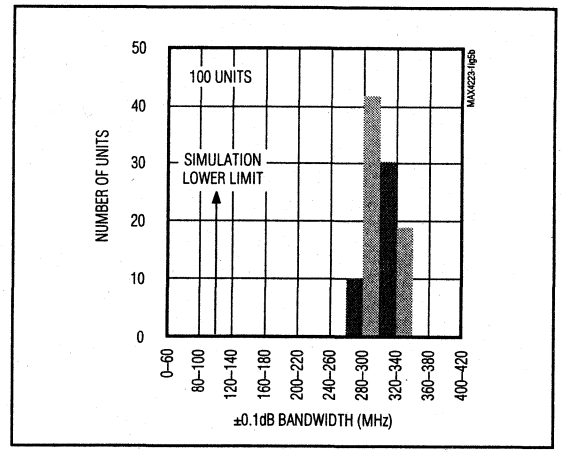


Figure 5b. MAX4223 ±0.1dB Bandwidth Distribution

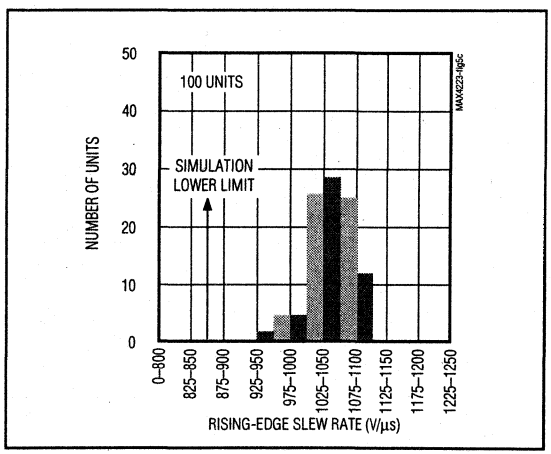


Figure 5c. MAX4223 Rising-Edge Slew-Rate Distribution

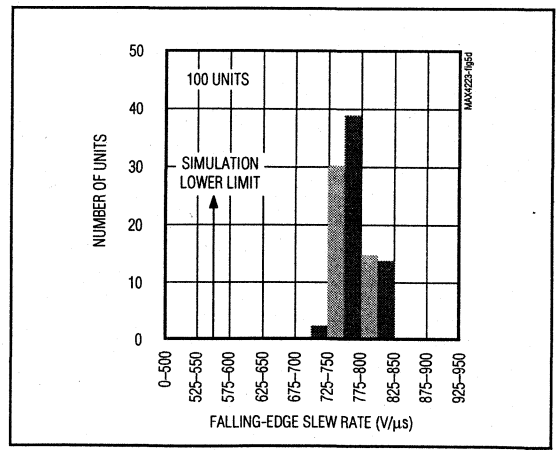


Figure 5d. MAX4223 Falling-Edge Slew-Rate Distribution

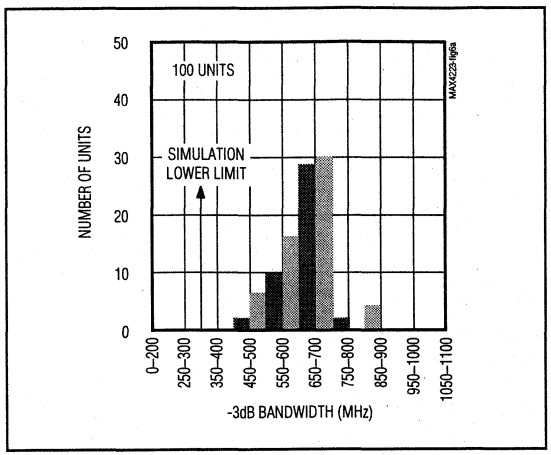


Figure 6a. MAX4224 -3dB Bandwidth Distribution

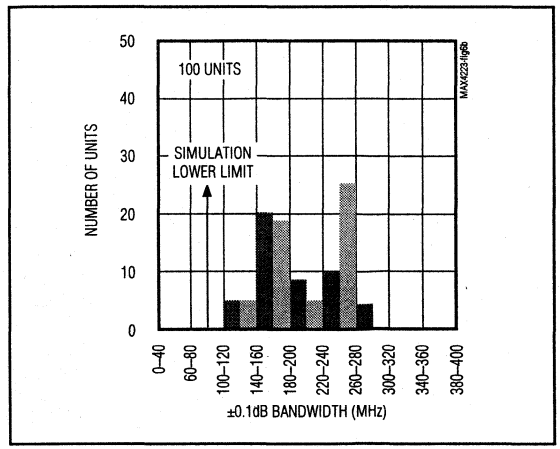


Figure 6b. MAX4224 ±0.1dB Bandwidth Distribution

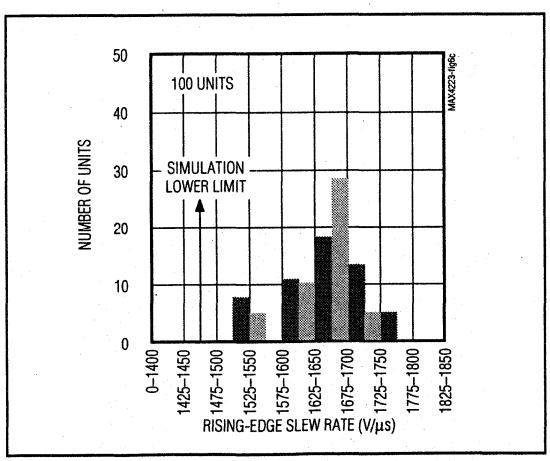


Figure 6c. MAX4224 Rising-Edge Slew-Rate Distribution

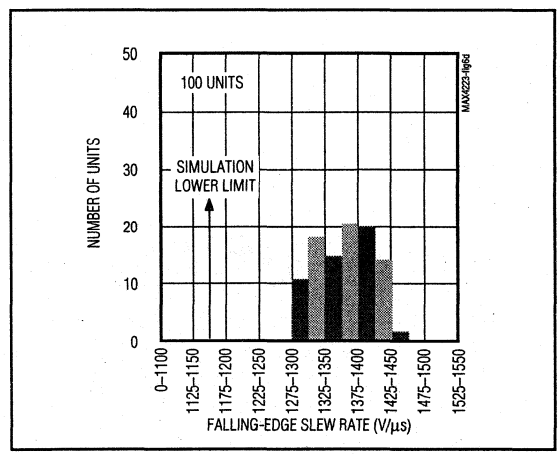


Figure 6d. MAX4224 Falling-Edge Slew-Rate Distribution

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

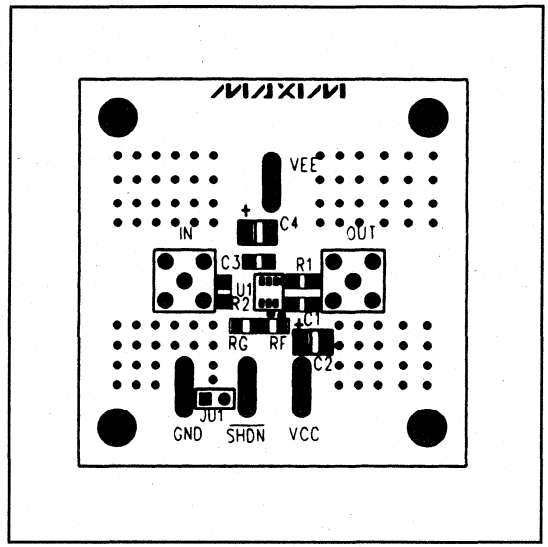


Figure 7a. Maxim SOT23 High-Speed Evaluation Board Component Placement Guide—Component Side

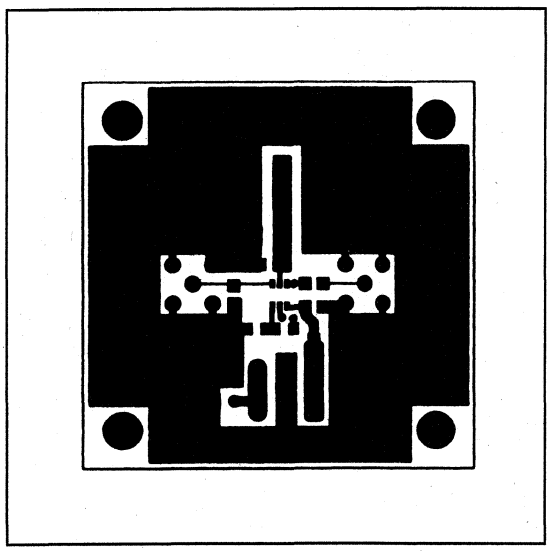


Figure 7b. Maxim SOT23 High-Speed Evaluation Board PC Board Layout—Component Side

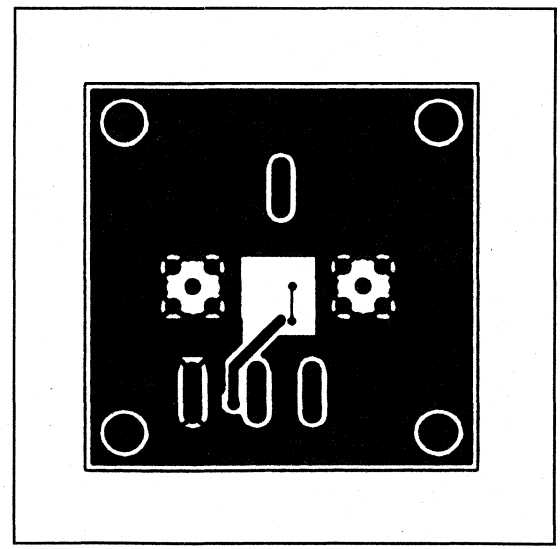


Figure 7c. Maxim SOT23 High-Speed Evaluation Board PC Board Layout—Back Side

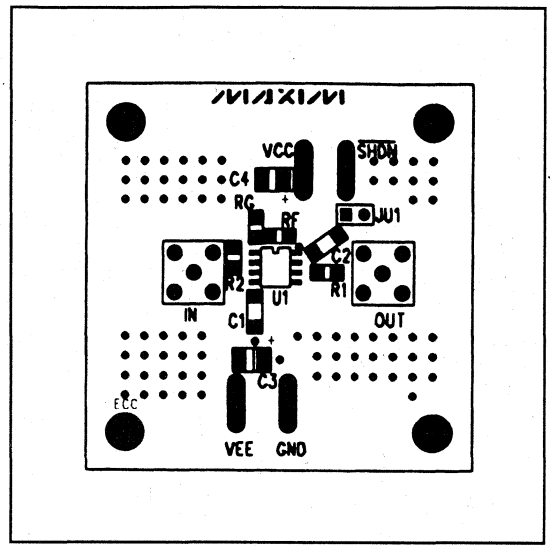


Figure 8a. Maxim SO-8 High-Speed Evaluation Board Component Placement Guide—Component Side

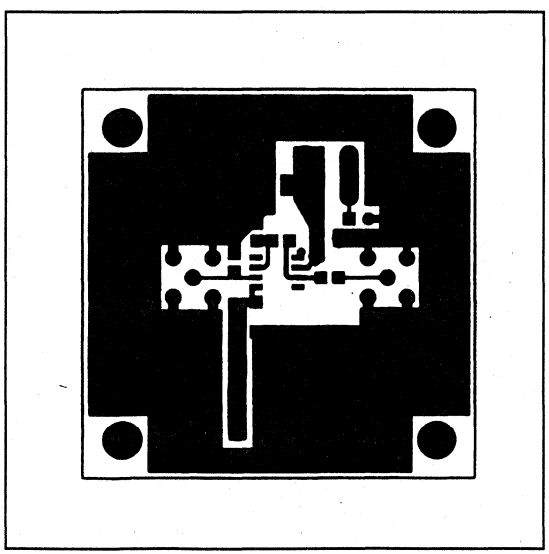


Figure 8b. Maxim SO-8 High-Speed Evaluation Board PC Board Layout—Component Side

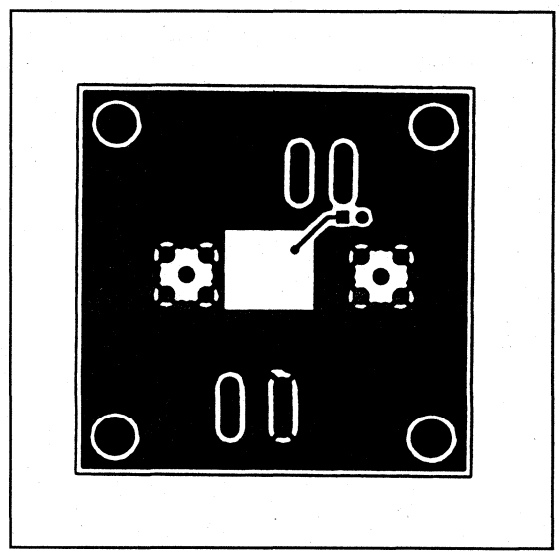


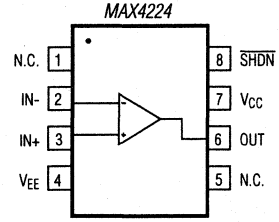
Figure 8c. Maxim SO-8 High-Speed Evaluation Board PC Board Layout—Back Side

1GHz, Low-Power, SOT23, Current-Feedback Amplifiers with Shutdown

Pin Configurations (continued)

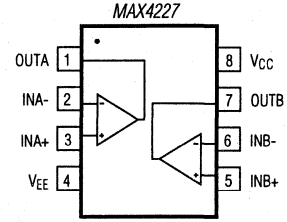
TOP VIEW

MAXIM
MAX4223
MAX4224



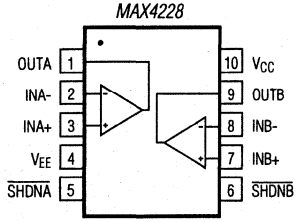
SO

MAXIM
MAX4225
MAX4227



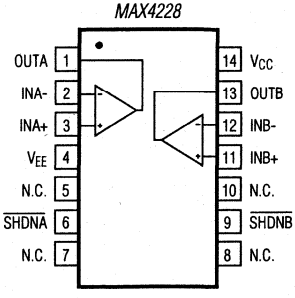
SO

MAXIM
MAX4226
MAX4228



µMAX

MAXIM
MAX4226
MAX4228



SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK
MAX4224EUT-T	-40°C to +85°C	6 SOT23	AAAE
MAX4224ESA	-40°C to +85°C	8 SO	—
MAX4225ESA	-40°C to +85°C	8 SO	—
MAX4226EUB	-40°C to +85°C	10 µMAX	—
MAX4226ESD	-40°C to +85°C	14 SO	—
MAX4227ESA	-40°C to +85°C	8 SO	—
MAX4228EUB	-40°C to +85°C	10 µMAX	—
MAX4228ESD	-40°C to +85°C	14 SO	—

Chip Information

MAX4223/MAX4224 TRANSISTOR COUNT: 87

MAX4225–MAX4228 TRANSISTOR COUNT: 171

SUBSTRATE CONNECTED TO V_{EE}

19-0461; Rev 2; 4/97

EVALUATION KIT AVAILABLE

MAXIM

400MHz, Ultra-Low-Distortion Op Amps

General Description

The MAX4108/MAX4109/MAX4308/MAX4309 op amps combine ultra-high-speed performance with ultra-low-distortion operation. The MAX4108 is compensated for unity-gain stability; the MAX4109, MAX4308, and MAX4309 are compensated for minimum closed-loop gains (A_{VCL}) of 2V/V, 5V/V, and 10V/V, respectively.

The MAX4108 delivers a 400MHz unity-gain bandwidth with a 1200V/µs slew rate. An ultra-low-distortion design provides an unprecedented spurious-free dynamic range of -93dBc (MAX4108) at 5MHz (V_{OUT} = 2Vp-p, R_L = 100Ω), making these amplifiers ideal for high-performance RF signal processing.

These high-speed op amps feature a wide output voltage swing and a high-current output-drive capability of 90mA.

Applications

High-Speed ADC/DAC Preamp

RGB and Composite Video

High-Performance Receivers

Pulse/RF Amplifier

Active Filters

Ultrasound

Broadcast and High-Definition TV

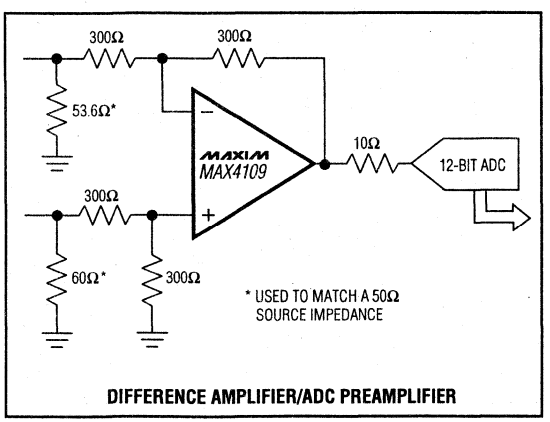
Features

- **High Speed:**
  400MHz Unity-Gain Bandwidth (MAX4108)
  225MHz -3dB Bandwidth (A_{VCL} = +2, MAX4109)
  220MHz -3dB Bandwidth (A_{VCL} = +5, MAX4308)
  200MHz -3dB Bandwidth (A_{VCL} = +10, MAX4309)
- **1200V/µs Slew Rate**
- **Excellent Spurious-Free Dynamic Range:**
  -93dBc at f_C = 5MHz (MAX4108)
  -90dBc at f_C = 5MHz (MAX4109)
- **100MHz 0.1dB Gain Flatness (MAX4108)**
- **High Full-Power Bandwidth: 300MHz (MAX4108, V_O = 2Vp-p)**
- **High Output Drive: 90mA**
- **Output Short-Circuit Protected**
- **Low Differential Gain/Phase: 0.004%/0.008°**

Ordering Information

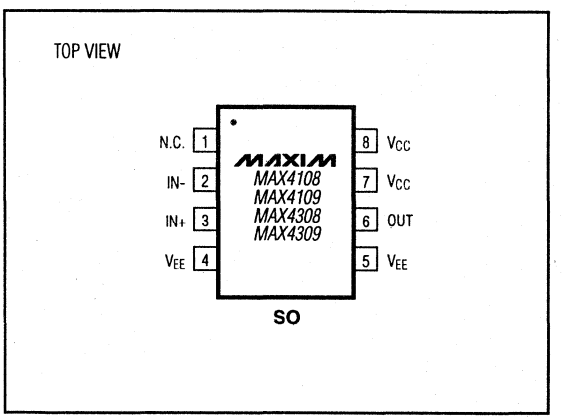
PART	TEMP. RANGE	PIN-PACKAGE
MAX4108ESA	-40°C to +85°C	8 SO
MAX4109ESA	-40°C to +85°C	8 SO
MAX4308ESA	-40°C to +85°C	8 SO
MAX4309ESA	-40°C to +85°C	8 SO

Typical Application Circuit



DIFFERENCE AMPLIFIER/ADC PREAMPLIFIER

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

400MHz, Ultra-Low-Distortion Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE}) 12V
Voltage on Any Pin to Ground or
Any Other Pin ..... (V_{EE} - 0.3V) to (V_{CC} + 0.3V)
Short-Circuit Duration (OUT to GND) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC SPECIFICATIONS (R_L = ∞)							
Input Offset Voltage	V_{OS}	V_{OUT} = 0V			1	8	mV
Input Offset Voltage Drift	TCV_{OS}	V_{OUT} = 0V			13		µV/°C
Input Bias Current	I_B	V_{OUT} = 0V, V_{IN} = -V_{OS}			12	34	µA
Input Offset Current	I_{OS}	V_{OUT} = 0V, V_{IN} = -V_{OS}			0.05	2.5	µA
Common-Mode Input Resistance	R_{INCM}	Either input			1.5		MΩ
Common-Mode Input Capacitance	C_{INCM}	Either input			1		pF
Input Voltage Noise	e_n	f = 10kHz			6		nV/√Hz
Integrated Voltage Noise	E_{nRMS}	f_B = 1MHz to 100MHz			75		$µV_{RMS}$
Input Current Noise	i_n	f = 10kHz			2		pA/√Hz
Integrated Current Noise	I_n	f_B = 1MHz to 100MHz			25		nA_{RMS}
Common-Mode Input Voltage	V_{CM}			-2.5		2.5	V
Common-Mode Rejection	CMR	V_{CM} = ±2.5V		70	100		dB
Power-Supply Rejection	PSR	V_S = ±4.5V to ±5.5V		70	90		dB
Open-Loop Voltage Gain	A_{OL}	V_{OUT} = ±2.0V, V_{CM} = 0V, R_L = 100Ω		70	100		dB
Quiescent Supply Current	I_S	V_{IN} = 0V			20	27	mA
Output Voltage Swing	V_{OUT}	R_L = ∞		2.5 to -3.1	2.9 to -3.8		V
		R_L = 100Ω		2.5 to -3.1	2.7 to -3.7		
Output Current Drive	I_{OUT}	R_L = 33Ω, T_A = 0°C to +85°C		65	90		mA
Short-Circuit Output Current	I_{SC}	Short to ground			100		mA
AC SPECIFICATIONS (R_L = 100Ω)							
-3dB Bandwidth	BW_{-3dB}	V_{OUT} ≤ 0.1V_{RMS}	MAX4108		400		MHz
			MAX4109		225		
			MAX4308		220		
			MAX4309		200		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

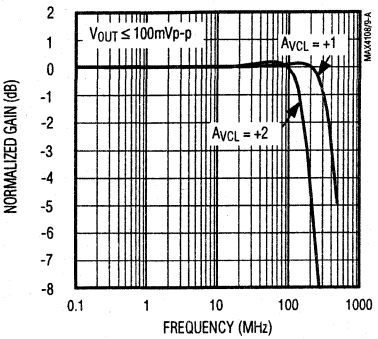
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC SPECIFICATIONS (R_L = 100Ω) (continued)							
Full-Power Bandwidth	FPBW	V_{OUT} = 2Vp-p	MAX4108		300		MHz
			MAX4109		200		
			MAX4308		190		
			MAX4309		130		
0.1dB Gain Flatness	$BW_{0.1dB}$	MAX4108, A_{VCL} = +1			100		MHz
		MAX4109, A_{VCL} = +2			25		
		MAX4308, A_{VCL} = +5			100		
		MAX4309, A_{VCL} = +10			30		
Slew Rate	SR	-2V ≤ V_{OUT} ≤ 2V			1200		V/µs
Settling Time	t_S	-1V ≤ V_{OUT} ≤ 1V	To 0.1%		8		ns
			To 0.01%		12		
Rise/Fall Times	t_R, t_F	10% to 90%	-2V ≤ V_{OUT} ≤ 2V		3		ns
			-50mV ≤ V_{OUT} ≤ 50mV		2		
Differential Gain	DG	f = 3.58MHz, R_L = 150Ω			0.004		%
Differential Phase	DP	f = 3.58MHz, R_L = 150Ω			0.008		degrees
Input Capacitance	C_{IN}				2		pF
Output Resistance	R_{OUT}	f = 10MHz			1		Ω
Spurious-Free Dynamic Range	SFDR	MAX4108, V_{OUT} = 2Vp-p, A_{VCL} = +1	f_C = 5MHz, R_L = 100Ω		-93		dBc
			f_C = 20MHz, R_L = 100Ω		-81		
		MAX4109, V_{OUT} = 2Vp-p, A_{VCL} = +2	f_C = 5MHz, R_L = 100Ω		-90		
			f_C = 20MHz, R_L = 100Ω		-80		
		MAX4308, V_{OUT} = 2Vp-p, A_{VCL} = +5	f_C = 5MHz, R_L = 100Ω		-83		
			f_C = 20MHz, R_L = 100Ω		-80		
		MAX4309, V_{OUT} = 2Vp-p, A_{VCL} = +10	f_C = 5MHz, R_L = 100Ω		-83		
			f_C = 20MHz, R_L = 100Ω		-80		
Third-Order Intercept	IP3	f_C = 10MHz	MAX4108		39		dBm
			MAX4109		36		
			MAX4308		46		
			MAX4309		43		

400MHz, Ultra-Low-Distortion Op Amps

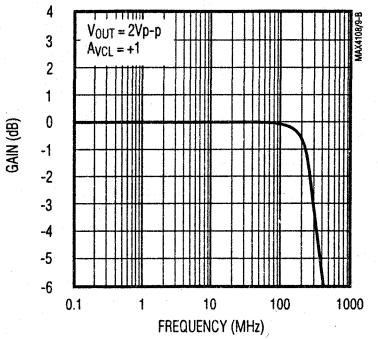
Typical Operating Characteristics

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless noted.)

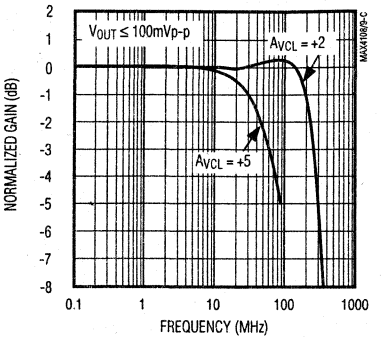
MAX4108
SMALL-SIGNAL GAIN vs. FREQUENCY



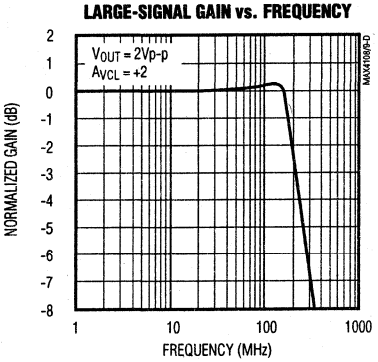
MAX4108
LARGE-SIGNAL GAIN vs. FREQUENCY



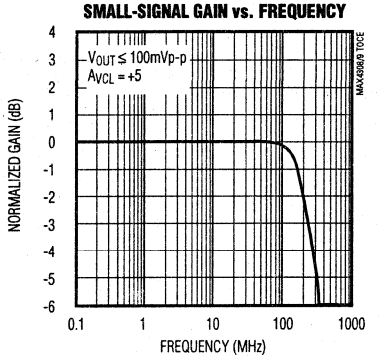
MAX4109
SMALL-SIGNAL GAIN vs. FREQUENCY



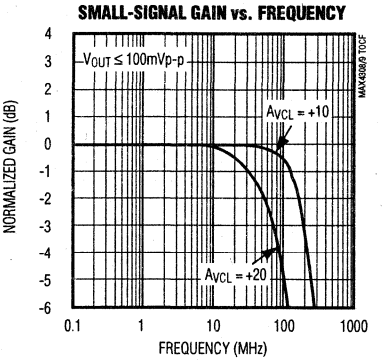
MAX4109
LARGE-SIGNAL GAIN vs. FREQUENCY



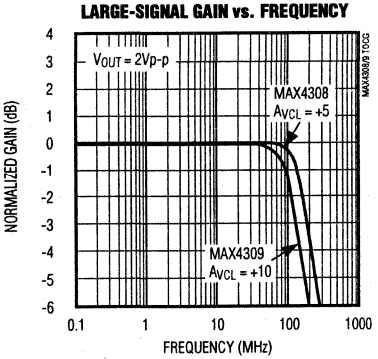
MAX4308
SMALL-SIGNAL GAIN vs. FREQUENCY



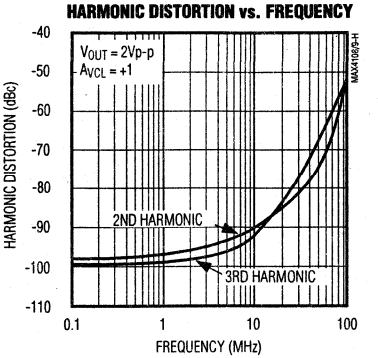
MAX4309
SMALL-SIGNAL GAIN vs. FREQUENCY



MAX4308/MAX4309
LARGE-SIGNAL GAIN vs. FREQUENCY



MAX4108
HARMONIC DISTORTION vs. FREQUENCY



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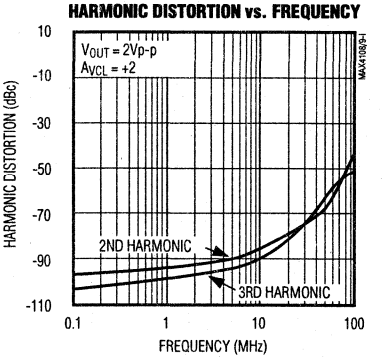
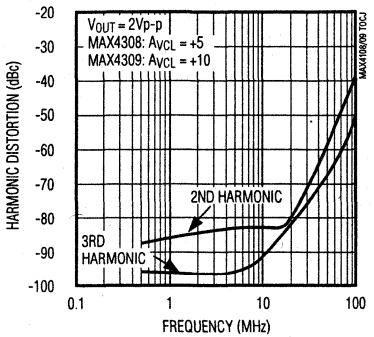
HARMONIC DISTORTION vs. FREQUENCY



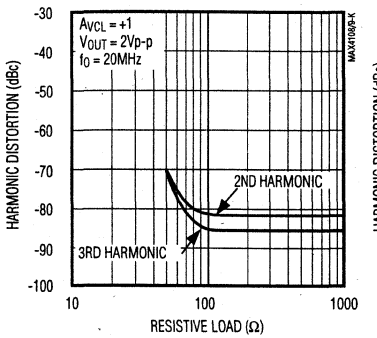
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

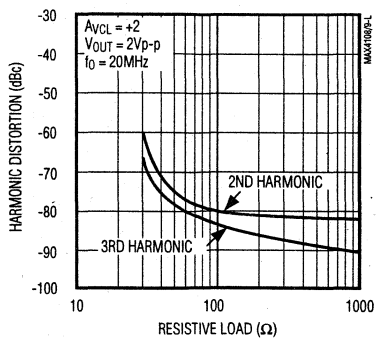
MAX4308/MAX4309
HARMONIC DISTORTION vs. FREQUENCY



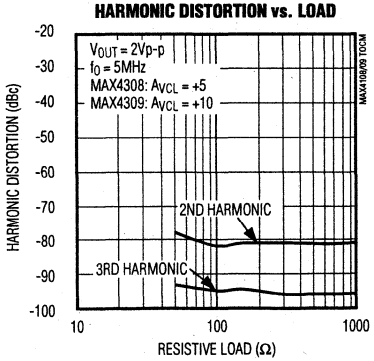
MAX4108
HARMONIC DISTORTION vs. LOAD



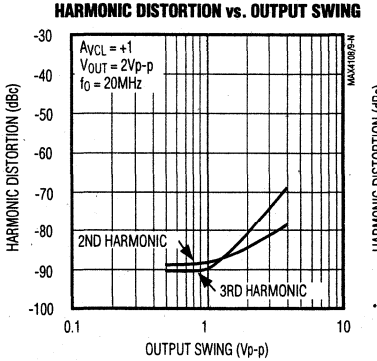
MAX4109
HARMONIC DISTORTION vs. LOAD



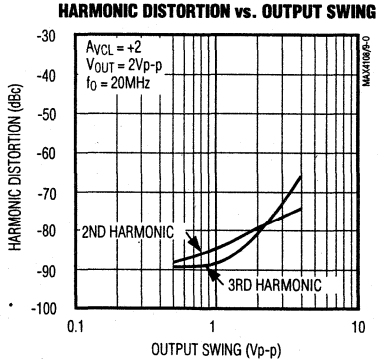
MAX4308/MAX4309
HARMONIC DISTORTION vs. LOAD



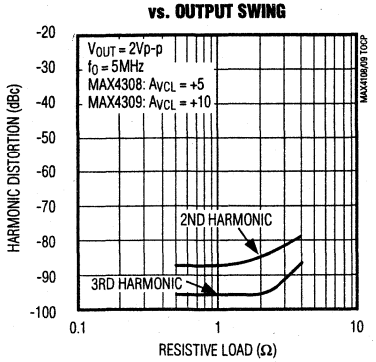
MAX4108
HARMONIC DISTORTION vs. OUTPUT SWING



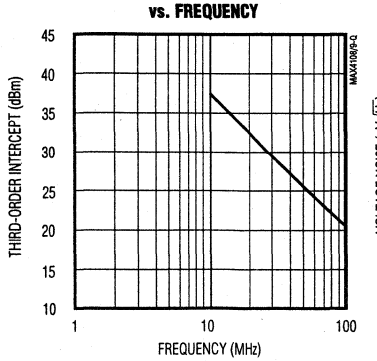
MAX4109
HARMONIC DISTORTION vs. OUTPUT SWING



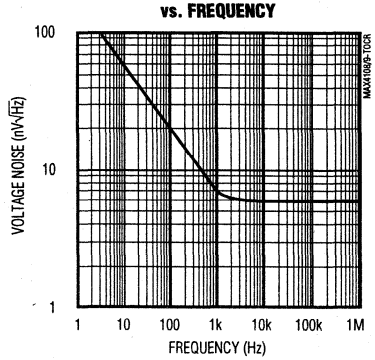
MAX4308/MAX4309
HARMONIC DISTORTION
vs. OUTPUT SWING



MAX4109
TWO-TONE THIRD-ORDER INTERCEPT
vs. FREQUENCY



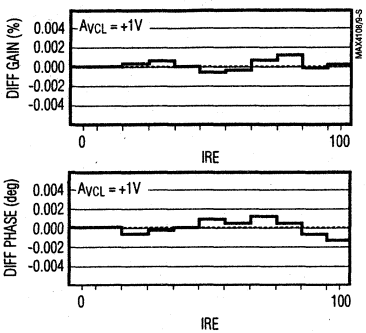
INPUT VOLTAGE NOISE
vs. FREQUENCY



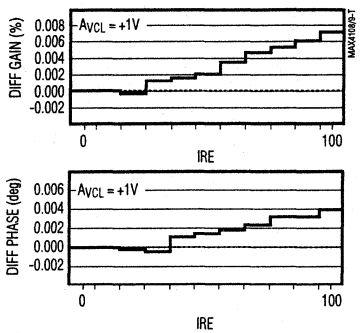
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

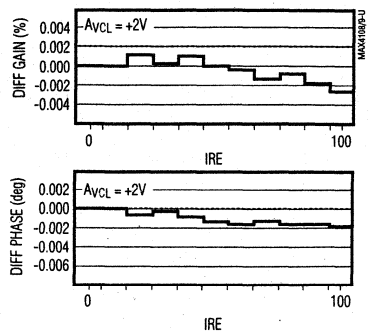
MAX4108
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



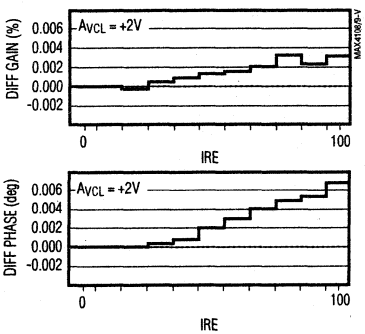
MAX4108
DIFFERENTIAL GAIN AND PHASE
(R_L = 75Ω)



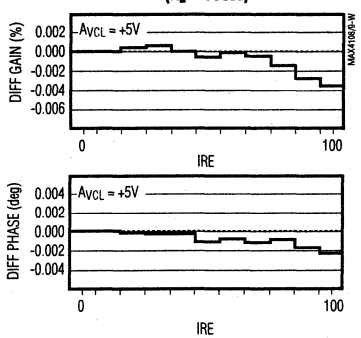
MAX4109
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



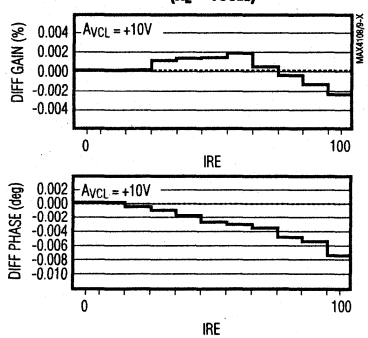
MAX4109
DIFFERENTIAL GAIN AND PHASE
(R_L = 75Ω)



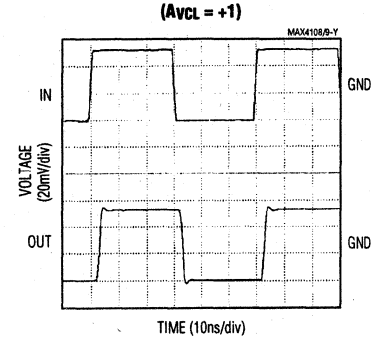
MAX4308
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



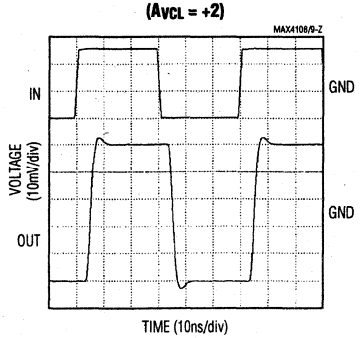
MAX4309
DIFFERENTIAL GAIN AND PHASE
(R_L = 150Ω)



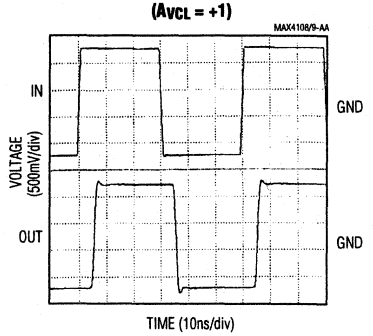
MAX4108
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +1)



MAX4108
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



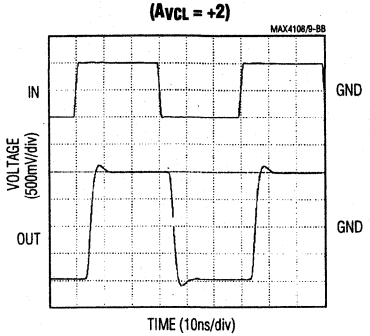
MAX4108
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +1)



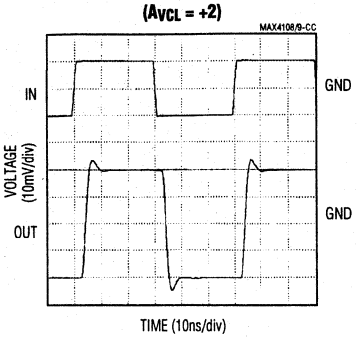
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

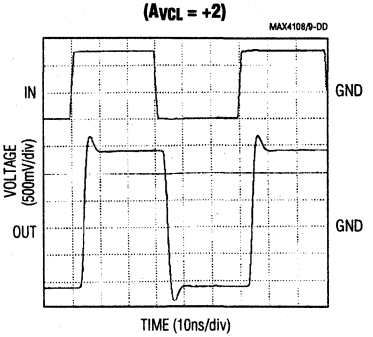
MAX4108
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



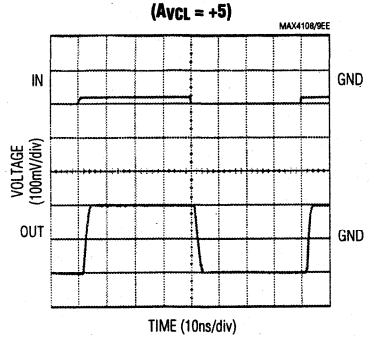
MAX4109
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



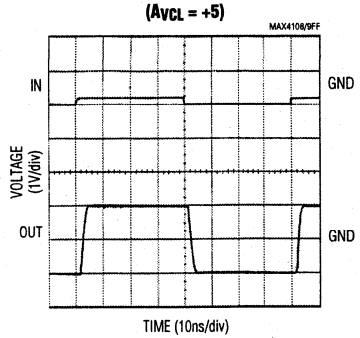
MAX4109
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +2)



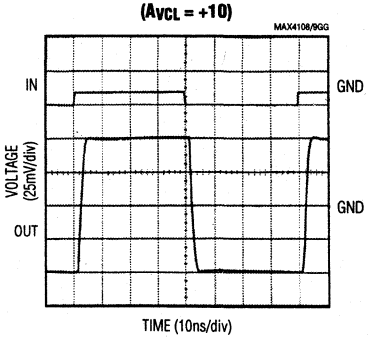
MAX4308
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



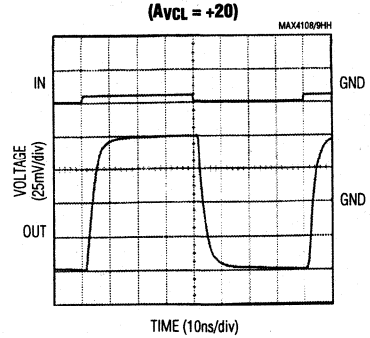
MAX4308
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +5)



MAX4309
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



MAX4309
SMALL-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)



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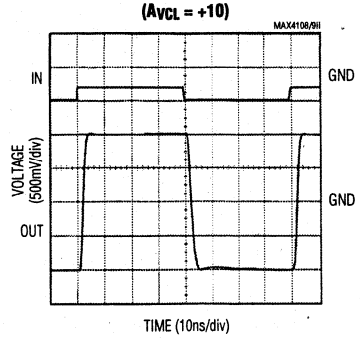
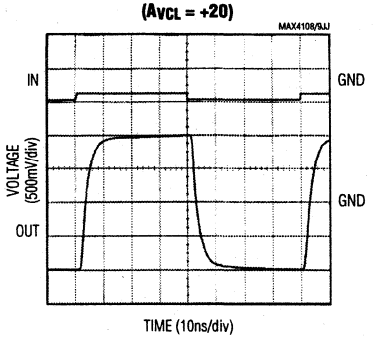
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +10)



MAX4309
LARGE-SIGNAL PULSE RESPONSE
(A_{VCL} = +20)

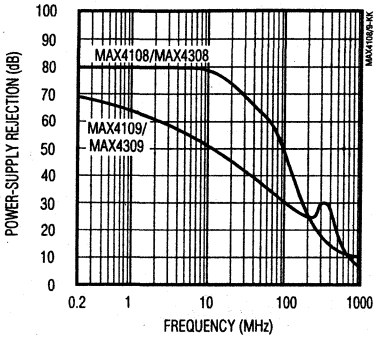


400MHz, Ultra-Low-Distortion Op Amps

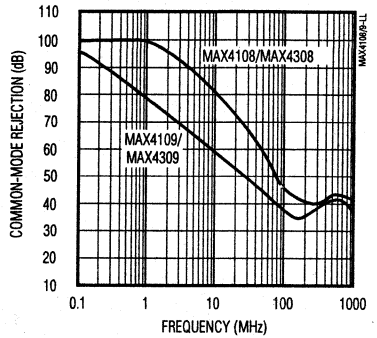
Typical Operating Characteristics (continued)

(V_{CC} = +5V, V_{EE} = -5V, R_L = 100Ω, T_A = +25°C, unless otherwise noted.)

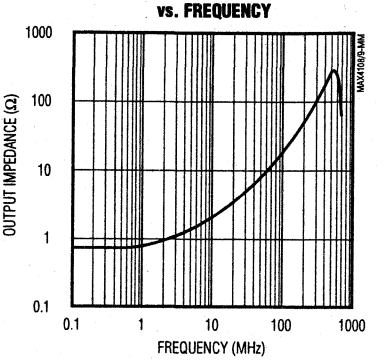
POWER-SUPPLY REJECTION vs. FREQUENCY



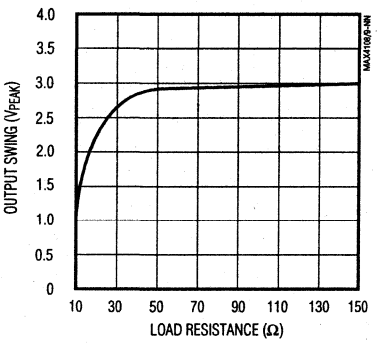
COMMON-MODE REJECTION vs. FREQUENCY



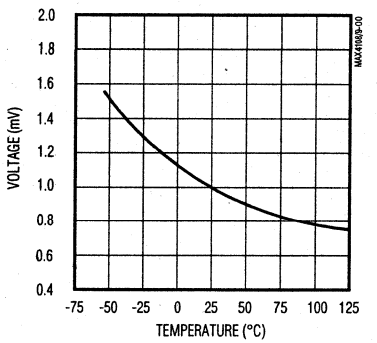
CLOSED-LOOP OUTPUT IMPEDANCE vs. FREQUENCY



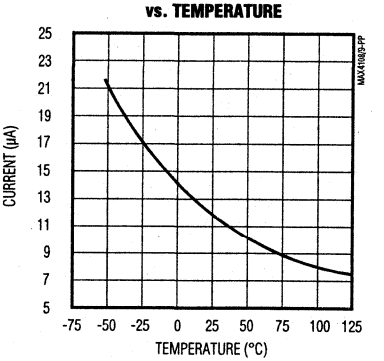
OUTPUT SWING vs. LOAD RESISTANCE



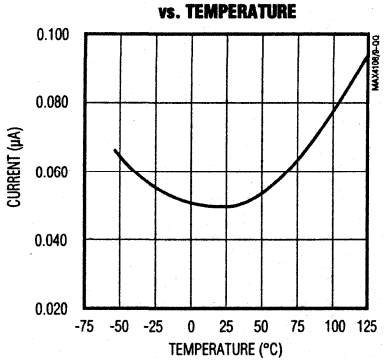
INPUT OFFSET VOLTAGE vs. TEMPERATURE



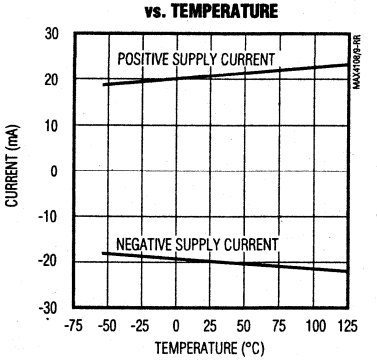
INPUT BIAS CURRENT vs. TEMPERATURE



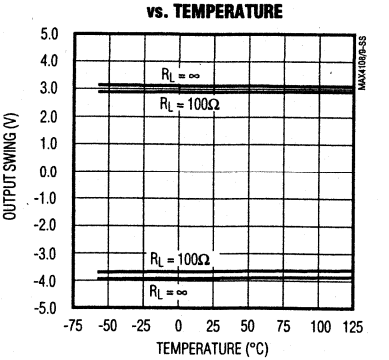
INPUT OFFSET CURRENT vs. TEMPERATURE



POWER-SUPPLY CURRENT vs. TEMPERATURE



OUTPUT SWING vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	N.C.	No Connection. Not internally connected.
2	IN-	Inverting Input
3	IN+	Noninverting Input
4, 5	V_{EE}	Negative Power Supply, connect to -5V_{DC}.
6	OUT	Amplifier Output
7, 8	V_{CC}	Positive Power Supply, connect to +5V_{DC}.

Detailed Description

Choosing Resistor Values

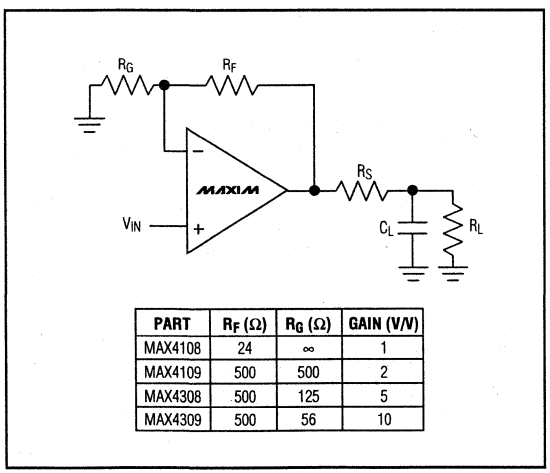
Unity-Gain Configuration

The MAX4108 is internally compensated for unity gain. When configured for unity gain, the device requires a small resistor in series with the feedback path. This resistor improves the AC response by reducing the Q of the tank circuit, which is formed by parasitic feedback inductance and capacitance.

Inverting and Noninverting Configurations

The values of the gain-setting feedback and input resistors are important design considerations. Large resistor values will increase voltage noise, and will interact with the amplifier's input and PC board capacitance to generate undesirable poles and zeros, which can decrease bandwidth or cause oscillations. For example, a noninverting gain of +2, using 1kΩ resistors combined with 2pF of input capacitance and 0.5pF of board capacitance, will cause a feedback pole at 128MHz. If this pole is within the anticipated amplifier bandwidth, it will jeopardize stability. Reducing these 1kΩ resistors to 100Ω will extend the pole frequency to 1.28GHz, but could limit output swing by adding 200Ω in parallel with the amplifier's load. Clearly, the selection of resistor values must be tailored to the specific application.

The MAX4108/MAX4109/MAX4308/MAX4309 are ultra-low-distortion, high-bandwidth op amps. The output distortion will be degraded as the total load resistance seen by the amplifier decreases. To minimize distortion products, keep the input and gain-setting resistors relatively large. A 500Ω feedback resistor combined with an appropriate input resistor to set the gain will provide excellent AC performance without significantly increasing distortion.



PART	R_F (Ω)	R_G (Ω)	GAIN (V/V)
MAX4108	24	∞	1
MAX4109	500	500	2
MAX4308	500	125	5
MAX4309	500	56	10

Figure 1a. Using an Isolation Resistor for High Capacitive Loads

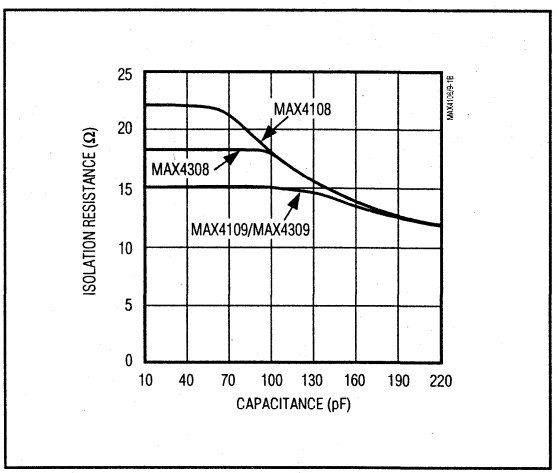


Figure 1b. Optimal Isolation Resistor (R_S) vs. Capacitive Load

Driving Capacitive Loads

The MAX4108/MAX4109/MAX4308/MAX4309 are optimized for AC performance. They are not designed to drive highly reactive loads. Reactive loads will decrease phase margin and may produce excessive ringing and oscillation. Figure 1a shows a circuit that eliminates this problem, and Figure 1b is a graph of the optimal isolation resistor (R_S) vs. capacitive load. Figures 2a–2d show how a capacitive load causes excessive peaking of the amplifier's bandwidth if the capacitive load is not isolated (R_S) from the amplifier. A small isolation resistor (usually 15Ω to 22Ω) placed

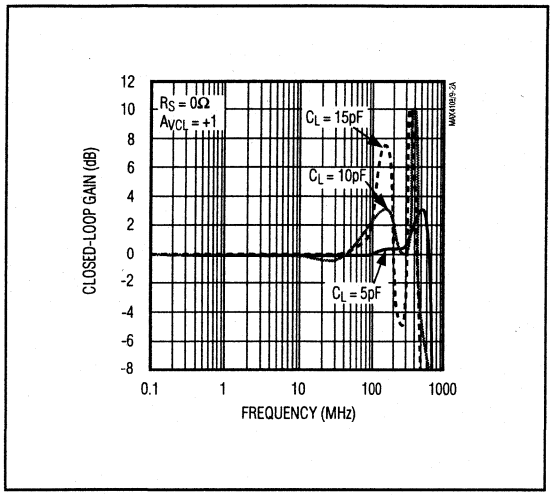


Figure 2a. MAX4108 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1a)

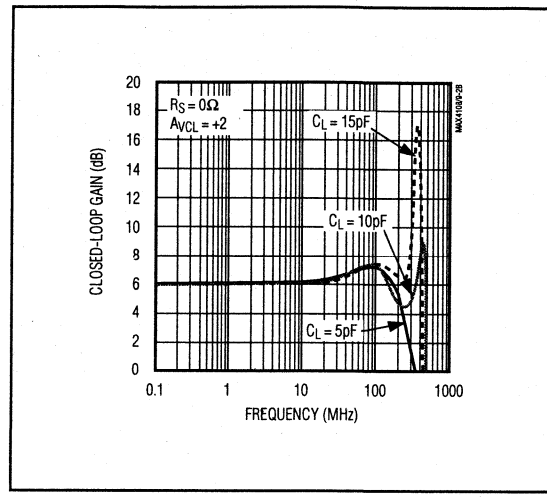


Figure 2b. MAX4109 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1a)

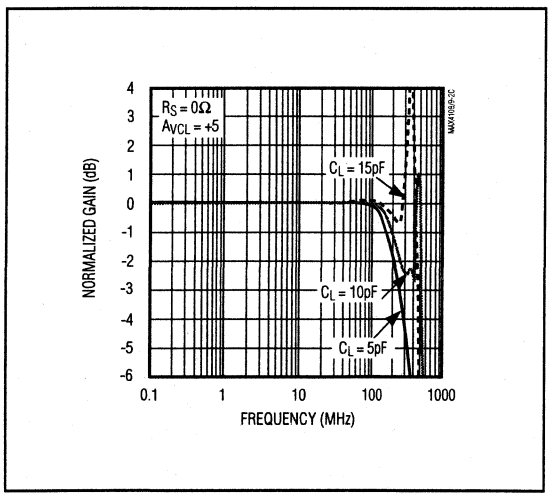


Figure 2c. MAX4308 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1a)

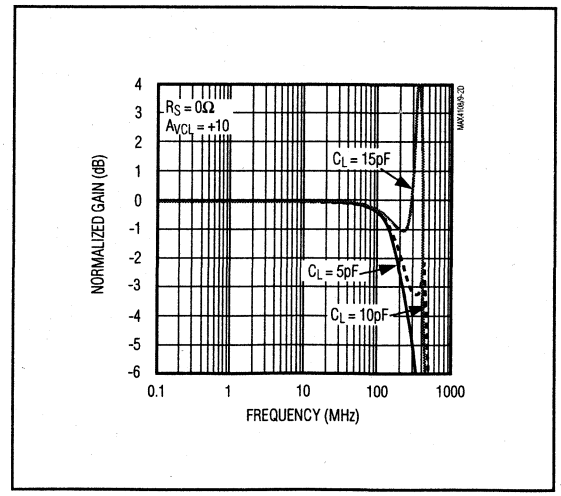


Figure 2d. MAX4309 Response vs. Capacitive Load—No Resistive (R_S) Isolation (circuit shown in Figure 1a)

before the reactive load prevents ringing and oscillation. At higher capacitive loads, AC performance will be controlled by the interaction of the load capacitance and isolation resistor. Figures 3a–3c show the effect of an isolation resistor on the MAX4108/MAX4109/MAX4308/MAX4309 closed-loop response.

Coaxial cable and other transmission lines are easily driven when terminated at both ends with their characteristic impedance. When driving back-terminated transmission lines, the capacitance of the transmission line is essentially eliminated.

ADC Input Buffers

Input buffer amplifiers can be a source of significant errors in high-speed ADC applications. The input buffer is usually required to rapidly charge and discharge the ADC's input, which is often capacitive (see the section *Driving Capacitive Loads*). In addition, a high-speed ADC's input impedance often changes very rapidly during the conversion cycle, requiring an amplifier with very low output impedance at high frequencies to maintain measurement accuracy. The combination of high speed, fast slew rate, low noise, and a low and stable distortion over load makes the MAX4108/MAX4109/MAX4308/MAX4309 ideally suited for use as buffer amplifiers in high-speed ADC applications.

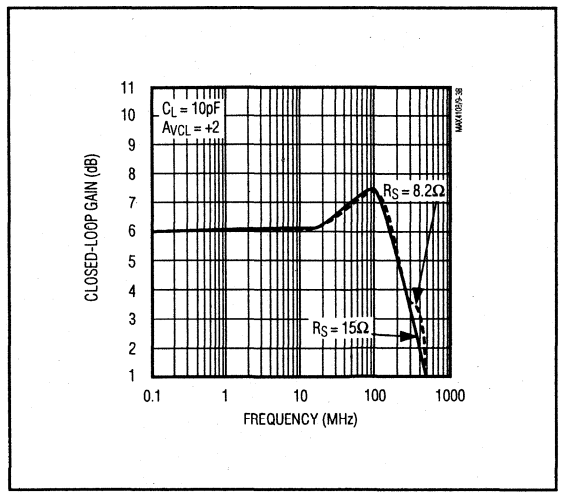


Figure 3b. MAX4308 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1a)

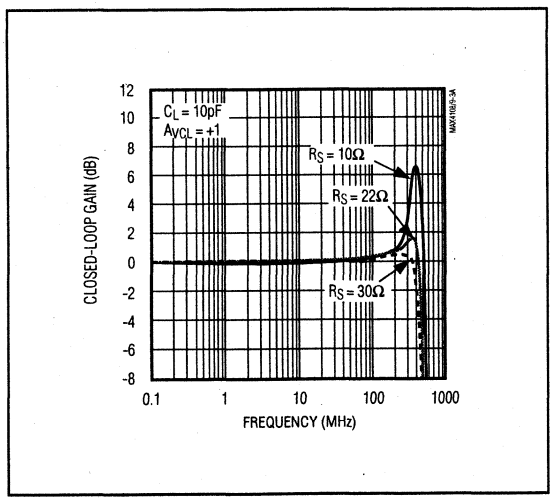


Figure 3a. MAX4108 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1a)

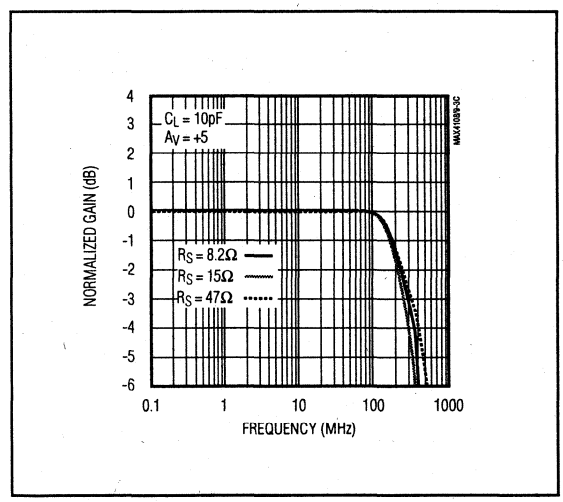


Figure 3c. MAX4108/MAX4309 Response vs. Capacitive Load with Resistive (R_S) Isolation (circuit shown in Figure 1a)

Chip Information

TRANSISTOR COUNT: 57

SUBSTRATE CONNECTED TO V_{EE}

MAXIM

High-Speed, Low-Power, Single-Supply Video Multiplexer/Amplifiers

General Description

The MAX4310 family of single-supply multiplexer (mux) amps combines high-speed operation with excellent video specifications. The MAX4310/MAX4311/MAX4312 integrate a 2-/4-/8-channel mux with a unity-gain-stable amplifier. The MAX4313/MAX4314/MAX4315 integrate a 2-/4-/8-channel mux with a fixed gain of +2V/V amplifier.

These devices operate from a single +3V to +10V supply. Their outputs swing Rail-to-Rail®, and they have an input common-mode voltage range that includes ground. The 2-/4-/8-channel MAX4310/MAX4311/MAX4312 have a 150MHz bandwidth and a 300V/µs slew rate, while the 2-/4-/8-channel MAX4313/MAX4314/MAX4315 have a 110MHz bandwidth and a 300V/µs slew rate, making them ideal for driving back-terminated cables. Supply current is less than 5.6mA. In addition, a low-power shutdown mode reduces supply current to 600µA and places the output in a high-impedance state.

The MAX4310–MAX4315 maintain an open-loop output impedance of only 8Ω over the full output range, minimizing the gain error and bandwidth changes under load that are typical of most rail-to-rail amplifiers. These devices are ideal for broadcast-video applications, with differential gain and phase errors of 0.06% and 0.04°, respectively.

Applications

Video-Signal Multiplexing

Video-Crosspoint Switching

Flash ADC Input Buffers

75Ω Cable Drivers

Medical Imaging

Features

- ♦ **+3V Single-Supply Operation**
- ♦ **150MHz Bandwidth (MAX4310/MAX4311/MAX4312; gain = +1V/V)**
  110MHz Bandwidth (MAX4313/MAX4314/MAX4315; gain = +2V/V)
- ♦ **300V/µs Slew Rate**
- ♦ **30ns Channel-Switching Time**
- ♦ **0.06%/0.04° Differential Phase/Gain Errors**
- ♦ **Outputs Swing Rail-to-Rail**
- ♦ **Input Common-Mode Range Includes GND**
- ♦ **300µA Low-Power Shutdown Mode**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX4310ESA	-40°C to +85°C	8 SO
MAX4310EUA	-40°C to +85°C	8 µMAX
MAX4311ESD	-40°C to +85°C	14 Narrow SO
MAX4311EEE	-40°C to +85°C	16 QSOP
MAX4312ESE	-40°C to +85°C	16 Narrow SO
MAX4312EEE	-40°C to +85°C	16 QSOP
MAX4313ESA	-40°C to +85°C	8 SO
MAX4313EUA	-40°C to +85°C	8 µMAX
MAX4314ESD	-40°C to +85°C	14 Narrow SO
MAX4314EEE	-40°C to +85°C	16 QSOP
MAX4315ESE	-40°C to +85°C	16 Narrow SO
MAX4315EEE	-40°C to +85°C	16 QSOP

8

Selector Guide

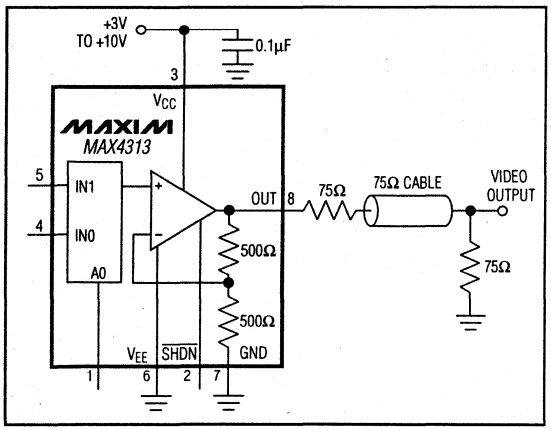
PART	INPUT CHANNELS	AMPLIFIER GAIN (V/V)	PIN-PACKAGE	SHUTDOWN
MAX4310	2	+1/adjustable	8 SO/µMAX	Yes
MAX4311	4	+1/adjustable	14 Narrow SO, 16 QSOP	Yes
MAX4312	8	+1/adjustable	16 Narrow SO/QSOP	Yes
MAX4313	2	+2	8 SO/µMAX	Yes
MAX4314	4	+2	14 Narrow SO, 16 QSOP	Yes
MAX4315	8	+2	16 Narrow SO/QSOP	Yes

Rail-to-Rail is a registered trademark of Nippon Motorola Ltd.

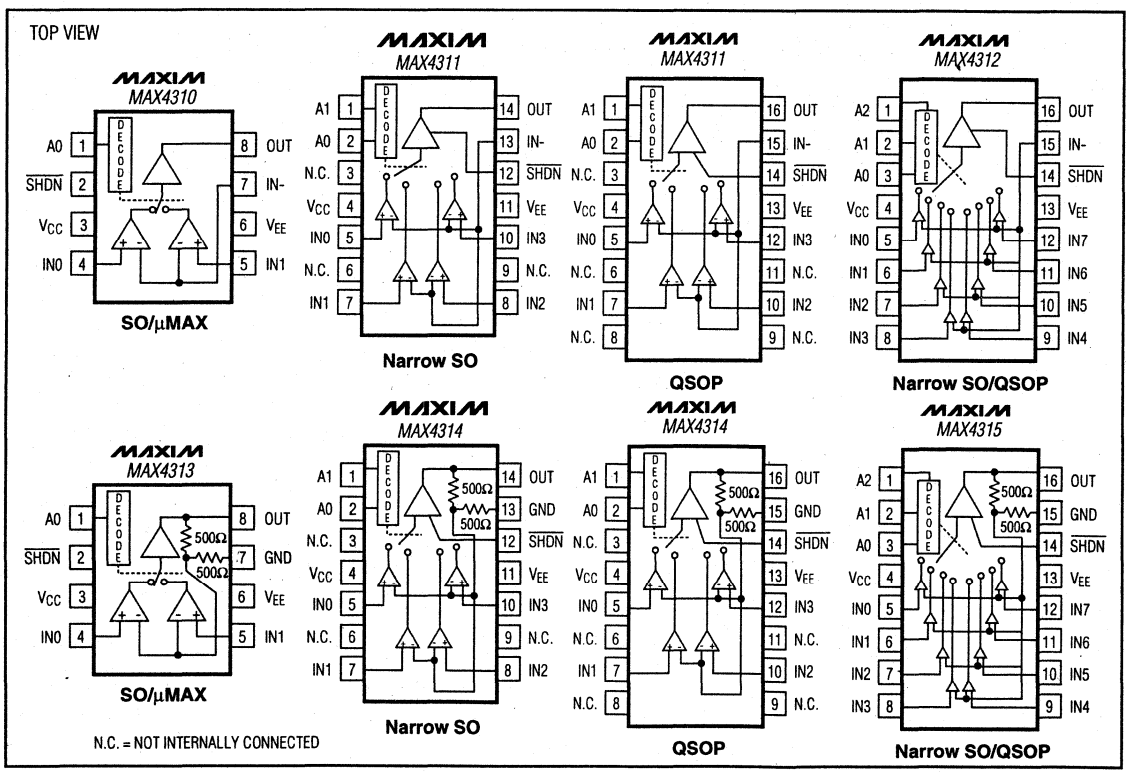
For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

High-Speed, Low-Power, Single-Supply Video Multiplexer/Amplifiers

Typical Operating Circuit



Pin Configurations



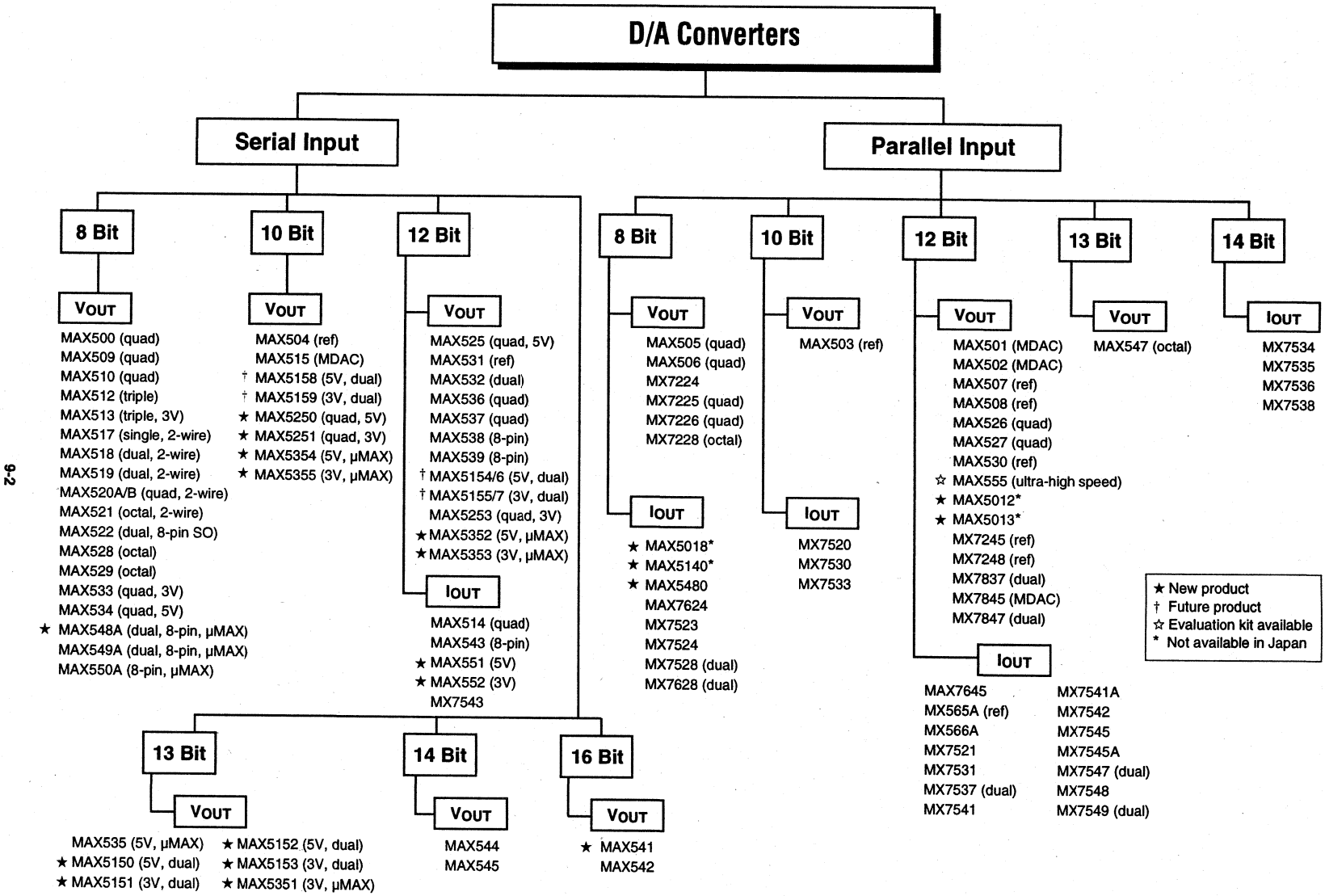
MAXIM

D/A Converters

D/A Converters, Product Tables and Trees 9-2

MAX535	+5V, Single-Supply, 13-Bit Voltage-Output DAC with Serial Interface	9-7
MAX548A	+2.5V to +5.5V, Low-Power, Dual, 8-Bit Voltage-Output DAC in µMAX Package	9-23
MAX549A	+2.5V to +5.5V, Low-Power, Dual, 8-Bit Voltage-Output DAC in µMAX Package	9-23
MAX550A	+2.5V to +5.5V, Low-Power, 8-Bit Voltage-Output DAC in µMAX Package	9-23
MAX551	+5V, 12-Bit, Serial, Multiplying DAC in µMAX Package	9-37
MAX552	+3V, 12-Bit, Serial, Multiplying DAC in µMAX Package	9-37
MAX5012	12-Bit, 100Msps ECL DAC	9-49
MAX5013	12-Bit, 100Msps TTL DAC	9-55
MAX5018	275Msps 8-Bit, High-Speed DAC	9-61
MAX5140	400Msps 8-Bit, Ultra-High-Speed DAC	9-73
MAX5150	+5V, Dual, 13-Bit Voltage-Output DAC with Serial Interface	9-85
MAX5151	+3V, Dual, 13-Bit Voltage-Output DAC with Serial Interface	9-85
MAX5152	+5V, Dual, 13-Bit Serial, Voltage-Output DAC with Configurable Output	9-101*
MAX5153	+3V, Dual, 13-Bit Serial, Voltage-Output DAC with Configurable Output	9-101*
MAX5154	+5V, Dual, 12-Bit Voltage-Output DAC with Serial Interface	9-103*
MAX5155	+3V, Dual, 12-Bit Voltage-Output DAC with Serial Interface	9-103*
MAX5156	+5V, Dual, 12-Bit Serial, Voltage-Output DAC with Configurable Output	9-105*
MAX5157	+3V, Dual, 12-Bit Serial, Voltage-Output DAC with Configurable Output	9-105*
MAX5158	+5V, Dual, 10-Bit Voltage-Output DAC with Serial Interface	9-107*
MAX5159	+3V, Dual, 10-Bit Voltage-Output DAC with Serial Interface	9-107*
MAX5250	Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface	9-109
MAX5251	+3V, Quad,10-Bit Voltage-Output DAC with Serial Interface	9-125
MAX5351	+3.3V, Single-Supply, 13-Bit Voltage-Output DAC with Serial Interface	9-7
MAX5352	+5V, Single-Supply, 12-Bit Voltage-Output DAC with Serial Interface	9-141
MAX5353	+3.3V, Single-Supply, 12-Bit Voltage-Output DAC with Serial Interface	9-141
MAX5354	+5V, Single-Supply, 10-Bit Voltage-Output DAC	9-157
MAX5355	+3.3V, Single-Supply, 10-Bit Voltage-Output DAC	9-157

*Advance Information–first page of a data sheet in preparation.


D/A Converters
Serial Input
Parallel Input
8 Bit
VOUT
MAX500 (quad)
MAX509 (quad)
MAX510 (quad)
MAX512 (triple)
MAX513 (triple, 3V)
MAX517 (single, 2-wire)
MAX518 (dual, 2-wire)
MAX519 (dual, 2-wire)
MAX520A/B (quad, 2-wire)
MAX521 (octal, 2-wire)
MAX522 (dual, 8-pin SO)
MAX528 (octal)
MAX529 (octal)
MAX533 (quad, 3V)
MAX534 (quad, 5V)
★ MAX548A (dual, 8-pin, µMAX)
MAX549A (dual, 8-pin, µMAX)
MAX550A (8-pin, µMAX)
10 Bit
VOUT
MAX504 (ref)
MAX515 (MDAC)
† MAX5158 (5V, dual)
† MAX5159 (3V, dual)
★ MAX5250 (quad, 5V)
★ MAX5251 (quad, 3V)
★ MAX5354 (5V, µMAX)
★ MAX5355 (3V, µMAX)
12 Bit
VOUT
MAX525 (quad, 5V)
MAX531 (ref)
MAX532 (dual)
MAX536 (quad)
MAX537 (quad)
MAX538 (8-pin)
MAX539 (8-pin)
† MAX5154/6 (5V, dual)
† MAX5155/7 (3V, dual)
MAX5253 (quad, 3V)
★ MAX5352 (5V, µMAX)
★ MAX5353 (3V, µMAX)
IOUT
MAX514 (quad)
MAX543 (8-pin)
★ MAX551 (5V)
★ MAX552 (3V)
MX7543
13 Bit
VOUT
MAX535 (5V, µMAX)
★ MAX5150 (5V, dual)
★ MAX5151 (3V, dual)
★ MAX5152 (5V, dual)
★ MAX5153 (3V, dual)
★ MAX5351 (3V, µMAX)
14 Bit
VOUT
MAX544
MAX545
16 Bit
VOUT
★ MAX541
MAX542
8 Bit
VOUT
MAX505 (quad)
MAX506 (quad)
MX7224
MX7225 (quad)
MX7226 (quad)
MX7228 (octal)
IOUT
★ MAX5018*
★ MAX5140*
★ MAX5480
MAX7624
MX7523
MX7524
MX7528 (dual)
MX7628 (dual)
10 Bit
VOUT
MAX503 (ref)
IOUT
MX7520
MX7530
MX7533
12 Bit
VOUT
MAX501 (MDAC)
MAX502 (MDAC)
MAX507 (ref)
MAX508 (ref)
MAX526 (quad)
MAX527 (quad)
MAX530 (ref)
☆ MAX555 (ultra-high speed)
★ MAX5012*
★ MAX5013*
MX7245 (ref)
MX7248 (ref)
MX7837 (dual)
MX7845 (MDAC)
MX7847 (dual)
IOUT
MAX7645
MX565A (ref)
MX566A
MX7521
MX7531
MX7537 (dual)
MX7541
MX7541A
MX7542
MX7545
MX7545A
MX7547 (dual)
MX7548
MX7549 (dual)
13 Bit
VOUT
MAX547 (octal)
14 Bit
IOUT
MX7534
MX7535
MX7536
MX7538
★ New product
† Future product
☆ Evaluation kit available
* Not available in Japan

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MX7224	8	V	5	Ext	µP/8	+12 to +15 & -5	Single or dual supplies	2.95
MAX517	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface	2.10
MAX550A	8	V	***	Ext	Serial	+2.5 to +5.5	8-pin µMAX, 2.5V, <0.7mW (upgrade to MAX550B)	1.45
MX7523	8	I	0.15	MDAC	Logic	+15	Low-cost 8-bit DAC	2.60
MAX7624	8	I	0.25	MDAC	µP/8	+12 to +15	Improved MX7524	2.26
MX7524	8	I	0.4	MDAC	µP/8	+5 to +15	Low-cost 8-bit DAC	1.95
MAX5480	8	I	0.4	MDAC	µP/8	+5	Low-cost MDAC in 16-pin QSOP package	1.35
MAX5354	10	V	10	Ext	Serial	+5	+5V, 10-bit, 8-pin µMAX	2.70
MAX5355	10	V	10	Ext	Serial	+3.3	+3.3V, 10-bit, 8-pin µMAX	2.90
MAX503	10	V	25	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, complete DAC	2.95
MAX504	10	V	25	Int/MDAC	Serial	+5 or ±5	Serial version of MAX503	2.80
MAX515	10	V	25	Ext	Serial	+5	Ultra-low power, 8-pin DIP/SO	2.50
MX7520	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	0.5	MDAC	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	0.6	MDAC	Logic	+15	Low-cost 10-bit DAC	2.84
MAX501	12	V	5	MDAC	µP/8	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	5	MDAC	µP/12	±12 to ±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	5	Int	µP/12	±12 to ±15	Complete 12-bit DAC with reference	7.65
MAX508	12	V	5	Int	µP/8	±12 to ±15	Complete 12-bit DAC with reference	7.65
MX7845	12	V	5	MDAC	µP/12	±15	4-range, 4-quadrant multiplying DAC	6.26
MX7245	12	V	10	Int	µP/12	±15 or +12 to +15	Single or dual supplies with reference	8.33
MX7248	12	V	10	Int	µP/8	±15 or +12 to +15	8-bit interface MX7245	8.33
MAX5352	12	V	14	Ext	Serial	+5	+5V, 12-bit, 8-pin µMAX, 1.5mW	4.20
MAX5353	12	V	14	Ext	Serial	+3.3	+3.3V, 12-bit, 8-pin µMAX, 0.9mW	4.20
MAX530	12	V	25	Int/MDAC	µP/8	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX531	12	V	25	Int/MDAC	Serial	+5 or ±5	Serial version of MAX530	5.45
MAX538	12	V	25	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	25	Ext	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MX565A	12	I	0.25	Int	Logic	±15	10V buried-zener reference	9.68
MX566A	12	I	0.35	Ext	Logic	-15	No internal reference	9.04
MX7521	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	0.5	MDAC	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541A	12	I	0.6	MDAC	Logic	+15	12-bit data bus	4.05
MAX543	12	I	1	MDAC	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX551	12	I	1	MDAC	Serial	+5	Smallest current-output DAC, reset pin	3.95
MAX552	12	I	1	MDAC	Serial	+2.7 to +3.6	Smallest current-output DAC, reset pin	3.95
MAX7645	12	I	1	MDAC	µP/12	+15	Improved MX7545	5.60
MX7541	12	I	1	MDAC	Logic	+15	12-bit data bus	5.07
MX7545A	12	I	1	MDAC	µP/12	+5 to +15	Improved MX7545	6.03
MX7548	12	I	1	MDAC	µP/8	+5 to +15	8-bit data bus with latches	6.06
MX7542	12	I	2	MDAC	µP/4	+5	4-bit data bus with latches	7.52
MX7543	12	I	2	MDAC	Serial	+5	12-bit multiplying DAC	4.35
MX7545	12	I	2	MDAC	µP/12	+5 to +15	12-bit data bus with latches	5.00
MAX535	13	V	20	Ext	Serial	+5	+5V, 13-bit, 8-pin µMAX, 1.5mW	4.95
MAX5351	13	V	20	Ext	Serial	+3.3	+3.3V, 13-bit, 8-pin µMAX, 0.9mW	5.50
MAX544	14	V	***	Ext	Serial	+5	5V, 14-bit, low power, 8-pin SOIC	7.90
MAX545	14	V	***	Ext	Serial	+5	5V, unipolar or bipolar, low power, 14-pin DIP/SO	7.90
MX7534	14	I	1.5	MDAC	µP/8	+12 to +15	Double-buffered inputs	13.37
MX7535	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	Double-buffered inputs	15.00
MX7536	14	I	1.5	MDAC	µP/8 or 14	+12 to +15	No external resistors needed	14.66
MX7538	14	I	1.5	MDAC	µP/14	+12 to +15	Low-cost 14-bit DAC	8.88
MAX541	16	V	***	Ext	Serial	+5	5V, 16-bit, low power, 8-pin DIP/SO	9.95
MAX542	16	V	***	Ext	Serial	+5	5V, 16-bit, unipolar or bipolar, low power, 14-pin DIP/SO	9.95

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

† Prices provided are for design guidance and are for the lowest grade commercial temperature parts (FOB USA). International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Resolution (Bits)	Output Type*	Settling Time (µs)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
DUAL								
MAX518	8	V	6	Int (V_{DD})	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	2.35
MAX522	8	V	70	MDAC	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX548A	8	V	***	Int (V_{DD})	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	1.65
MAX549A	8	V	***	Ext	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power (upgrade to MAX549B)	1.65
MX7528	8	I	0.18	MDAC	µP/8	+5 to +15	Data latches for both DACs	2.11
MX7628	8	I	0.35	MDAC	µP/8	+12 to +15	Data latches for both DACs	3.80
MAX5158	10	V	8	Ext	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5159	10	V	8	Ext	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX532	12	V	4	MDAC	Serial	±12 to ±15	16-pin DIP/SO	8.45
MX7837	12	V	4	Ext	µP/8	±12 to ±15	Dual V_{OUT} DAC with 8-bit data bus	12.18
MX7847	12	V	4	Ext	µP/12	±12 to ±15	Dual V_{OUT} DAC with 12-bit data bus	12.18
MAX5154	12	V	12	Ext	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5155	12	V	15	Ext	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5156	12	V	15	Ext	Serial	+5	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX5157	12	V	18	Ext	Serial	+2.7 to +3.6	Low-power, dual, force/sense, QSOP-16 pkg.	††
MX7537	12	I	1.5	MDAC	µP/8	+12 to +15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	1.5	MDAC	µP/12	+12 to +15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	1.5	MDAC	µP/4	+15	Dual DAC with 4-bit data bus	12.97
MAX5150	13	V	16	Ext	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	7.95
MAX5151	13	V	20	Ext	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	7.95
MAX5152	13	V	18	Ext	Serial	+5	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX5153	13	V	22	Ext	Serial	+2.7 to +3.6	Low-power, dual, force/sense, QSOP-16 pkg.	††
TRIPLE								
MAX512	8	V	60	MDAC	Serial	+5 or ±5	Low power with shutdown, 14-pin narrow SO	2.85
MAX513	8	V	70	MDAC	Serial	+2.7 to ±3.6	For 3V systems	2.85
QUAD								
MAX500	8	V	4	Ext	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MX7225	8	V	4	Ext	µP/8	+12 to +15 & -5	Double buffered, separate reference inputs	9.26
MX7226	8	V	4	Ext	µP/8	+12 to +15 & -5	Single buffered, single reference input	6.50
MAX505	8	V	6	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, separate reference inputs	5.95
MAX506	8	V	6	MDAC	µP/8	+5 or ±5	Rail-to-rail outputs, single reference input	6.10
MAX509	8	V	6	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	6	MDAC	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX533	8	V	6	Ext	Serial	+2.7 to +3.6	2.7V, low power (1.9mW), serial, 16-pin QSOP	2.80
MAX534	8	V	6	Ext	Serial	+5	Low-power, +5V, quad DAC in 16-pin QSOP	2.80
MAX520	8	V	***	Ext	Serial, 2-wire	+5	2-wire interface, separate reference inputs	3.50
MAX5250	10	V	10	Ext	Serial	+5	5V, 1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	4.95
MAX5251	10	V	10	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	4.95
MAX526	12	V	3	Ext	µP/8	+12 to +15 & -5	Quad voltage-output DAC, available in DIP/SO	19.44
MAX527	12	V	3	Ext	µP/8	±5	±5V version of MAX526	16.56
MAX536	12	V	3	Ext	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	3	Ext	Serial	±5	Serial version of MAX527	15.95
MAX5253	12	V	16	Ext	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	11.35
MAX525	12	V	20	Ext	Serial	+5	1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	11.95
MAX514	12	I	1	MDAC	Serial	+5	Quad current-output DAC, available in DIP/SO	14.25
OCTAL								
MAX528	8	V	5	Ext	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	5	Ext	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MX7228	8	V	5	Ext	µP/8	+5 to +15 & -5 or +15	Single or dual supplies	11.95
MAX521	8	V	6	Ext	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX547	13	V	5	Ext	µP/13	±5	Unipolar or bipolar, four reference inputs	29.60

* V = voltage, I = current

† Prices provided are for design guidance and are for the lowest grade commercial temperature

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX517	8	V	1	Ext	6	Serial, 2-wire	+5	2-wire interface	2.10
MAX550	8	V	1	Ext	***	Serial	+2.5 to +5.5	8-pin µMAX, 2.5V, <0.7mW	1.45
MAX518	8	V	2	Int (V_{DD})	6	Serial, 2-wire	+5	2-wire interface, 8-pin SO	2.25
MAX519	8	V	2	Ext	6	Serial, 2-wire	+5	2-wire interface, two reference inputs	2.35
MAX522	8	V	2	MDAC	6	Serial	+2.7 to +5.5	Low-power dual in 8-pin SO	2.25
MAX548A	8	V	2	Int (V_{DD})	***	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power	1.65
MAX549A	8	V	2	Ext	***	Serial	+2.5 to +5.5	2.5V, 8-pin µMAX, low power (upgrade to MAX549B)	1.65
MAX512	8	V	3	MDAC	60	Serial	+5 or ±5	Low-power with shutdown, 14-pin narrow SO	2.85
MAX513	8	V	3	MDAC	70	Serial	+2.7 to ±3.6	MAX512 for 3V systems	2.85
MAX500	8	V	4	Ext	4	Serial	+12 to +15 & -5	16-pin DIP/SO, three reference inputs	5.70
MAX509	8	V	4	MDAC	6	Serial	+5 or ±5	Rail-to-rail outputs, four reference inputs	5.35
MAX510	8	V	4	MDAC	6	Serial	+5 or ±5	Rail-to-rail outputs, one reference input	5.19
MAX520	8	V	4	Ext	***	Serial, 2-wire	+5	2-wire interface, four reference inputs	3.50
MAX533	8	V	4	Ext	6	Serial	+2.7 to +3.6	2.7V, low-power (1.9mW), 16-pin QSOP	2.80
MAX534	8	V	4	Ext	6	Serial	+5	Low-power, +5V, quad DAC in 16-pin QSOP	2.80
MAX521	8	V	8	Ext	6	Serial, 2-wire	+5	2-wire interface, five reference inputs	4.95
MAX528	8	V	8	Ext	5	Serial	+5 to +15, +15 & -5 or +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5	Serial	+5 or ±5	Single +5V supply MAX528	5.65
MAX504	10	V	1	Int/MDAC	25	Serial	+5 or ±5	Ultra-low power, rail to rail	2.80
MAX515	10	V	1	Ext	25	Serial	+5	Ultra-low power, 8-pin SO/DIP	2.50
MAX5354	10	V	1	Ext	10	Serial	+5	+5V, 10-bit, 8-pin µMAX	2.70
MAX5355	10	V	1	Ext	10	Serial	+3.3	+3.3V, 10-bit, 8-pin µMAX	2.90
MAX5158	10	V	2	Ext	10	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5159	10	V	2	Ext	10	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5250	10	V	4	Ext	10	Serial	+5	5V, 1mW/DAC, serial, 20µA power-down, 20-pin DIP/SSOP	4.95
MAX5251	10	V	4	Ext	10	Serial	+3 to +3.6	3V, 0.6mW/DAC, serial, 20µA power-down	4.95
MAX531	12	V	1	Int/MDAC	25	Serial	+5 or ±5	Ultra-low power, flexible output range	5.45
MAX538	12	V	1	Ext	25	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 2V output	4.85
MAX539	12	V	1	Ext	25	Serial	+5	8-pin DIP/SO, ultra-low power, 0V to 5V output	4.85
MAX5352	12	V	1	Ext	20	Serial	+5	+5V, 12-bit, 8-pin µMAX, 1.5mW	4.20
MAX5353	12	V	1	Ext	20	Serial	+3.3	+3.3V, 12-bit, 8-pin µMAX, 0.9mW	4.20
MAX532	12	V	2	Ext	4	Serial	±12 to ±15	16-pin DIP/SO	8.45
MAX5154	12	V	2	Ext	12	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5155	12	V	2	Ext	15	Serial	+2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	††
MAX5156	12	V	2	Ext	15	Serial	+5	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX5157	12	V	2	Ext	18	Serial	+2.7 to +3.6	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX525	12	V	4	Ext	20	Serial	+5	<1mW/DAC, 20µA power-down, 20-pin DIP/SSOP	11.95
MAX536	12	V	4	Ext	3	Serial	+12 to +15 & -5	Serial version of MAX526	15.95
MAX537	12	V	4	Ext	3	Serial	±5	Serial version of MAX527	15.95
MAX5253	12	V	4	Ext	16	Serial	+3 to +3.6	3V, 0.6mW/DAC, 20µA power-down	11.35
MAX543	12	I	1	MDAC	1	Serial	+5 to +15	12-bit multiplying DAC in 8-pin DIP/SO	4.80
MAX551	12	I	1	MDAC	1	Serial	+5	Smallest current-output DAC, reset input	3.95
MAX552	12	I	1	MDAC	1	Serial	+2.7 to +3.6	Smallest current-output DAC, reset input	3.95
MX7543	12	I	1	MDAC	2	Serial	+5	12-bit multiplying DAC	7.52
MAX514	12	I	4	MDAC	1	Serial	+5	Quad current-output DACs, available in DIP/SO	14.25

* V = voltage, I = current

** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference

*** Settling time depends on internal resistive ladder and external load impedance.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Serial D/A Converters (continued)

Part Number	Resolution (Bits)	Output Type*	DACs in Package	Reference**	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX535	13	V	1	Ext	20	Serial	+5	13-bit, 8-pin µMAX, 1.5mW	4.95
MAX5351	13	V	1	Ext	20	Serial	+3.3	+3.3V, 13-bit, 8-pin µMAX, 0.9mW	5.50
MAX5150	13	V	2	Ext	16	Serial	+5	Low-power, dual DAC in QSOP-16 pkg.	7.95
MAX5151	13	V	2	Ext	20	Serial	2.7 to +3.6	Low-power, dual DAC in QSOP-16 pkg.	7.95
MAX5152	13	V	2	Ext	18	Serial	+5	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX5153	13	V	2	Ext	22	Serial	2.7 to +3.6	Low-power, dual, force/sense, QSOP-16 pkg.	††
MAX544	14	V	1	Ext	***	Serial	+5	5V, 14-bit, low power, 8-pin DIP/SO	7.90
MAX545	14	V	1	Ext	***	Serial	+5	5V, unipolar or bipolar, low power, 14-pin DIP SO	7.90
MAX541	16	V	1	Ext	***	Serial	+5	5V, 16-bit, low power, 8-pin DIP/SO	9.95
MAX542	16	V	1	Ext	***	Serial	+5	5V, 16-bit, unipolar or bipolar, low power, 14-pin DIP/SO	9.95

High-Speed D/A Converters

Part Number	Resolution (Bits)	Output Type*	Settling Time (ns)	Reference**	Data-Bus Interface (Bits)	Supply Voltage (V)	Features	Price† 1000-up ($)
MAX5140(1)	8	I	3	Ext	Parallel	-5.2	400Msps high-resolution video DAC with controls	‡
MAX5018(1)	8	I	4.5	Ext	Parallel	-5.2	165/275Msps video DAC with controls	‡
MAX555	12	V	0.5	Ext/MDAC	Parallel	-5.2	300Msps update rate, 72dB SFDR	‡
MAX5012(1)	12	V	13	Ext	Parallel	-5.2	High-speed, 12-bit, 100MHz DAC with ECL inputs	‡
MAX5013(1)	12	V	13	Ext	Parallel	+5, -5.2	High-speed, 12-bit, 100MHz DAC with TTL inputs	‡

* V = voltage, I = current
** MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
*** Settling time depends on internal resistive ladder and external load impedance.
(1) Not available in Japan.
‡ Contact factory for pricing.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product—contact factory for pricing and availability. Specifications are preliminary.

19-1124; Rev 1; 12/96

MAXIM

Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX535/MAX5351 combine a low-power, voltage-output, 13-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX535 operates from a single +5V supply and the MAX5351 operates from a single +3.3V supply. Both devices draw only 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX535/MAX5351 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with either SPI™/QSPI™ or Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- **13-Bit DAC with Configurable Output Amplifier**
- **+5V Single-Supply Operation (MAX535)**
  +3.3V Single-Supply Operation (MAX5351)
- **Low Supply Current: 0.24mA Normal Operation**
  2µA Shutdown Mode
- **Available in 8-Pin µMAX**
- **Power-On Reset Clears DAC Output to 0V**
- **SPI/QSPI and Microwire Compatible**
- **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**

Ordering Information

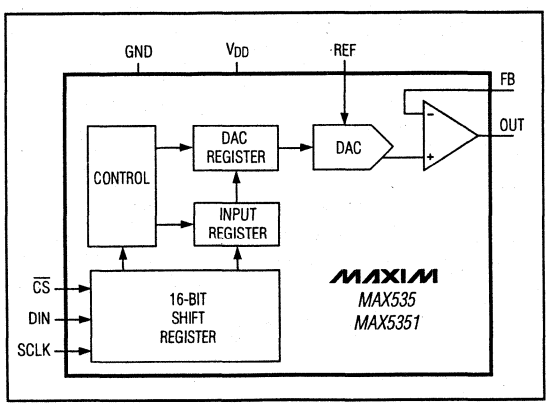
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX535ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX535BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX535ACUA	0°C to +70°C	8 µMAX†	±1/2
MAX535BCUA	0°C to +70°C	8 µMAX	±1
MAX535BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

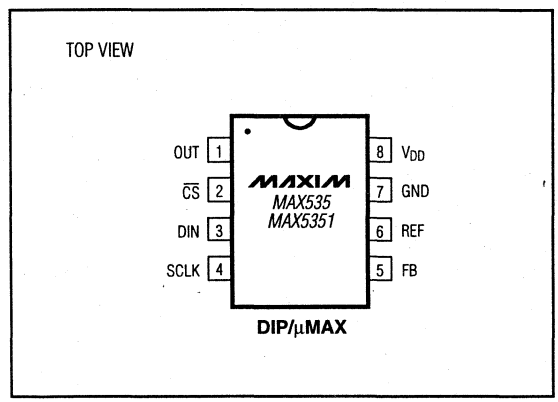
†Contact factory for availability.

**Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram



Pin Configuration



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Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +6V
REF, OUT, FB to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 6.90mW/°C above +70°C).....552mW
µMAX (derate 4.00mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX535_C_A/MAX5351_C_A.....0°C to +70°C
MAX535_E_A/MAX5351_E_A .....-40°C to +85°C
MAX535BMJA/MAX5351BMJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX535

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		13			Bits
Integral Nonlinearity (Note 1)	INL	MAX535A			±0.5	LSB
		MAX535B			±1.0	
		MAX535MJA			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 1)	GE			-0.5	±6	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1555 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		77		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS: MAX535 (continued)

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		16		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Time to Valid Operation on Start-Up				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.28	0.4	mA
Supply Current in Shutdown		(Note 3)		4	20	µA
Reference Current in Shutdown				0.001	±0.5	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 22 to code 8191 in unity-gain configuration.

Note 2: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 100mV, guaranteed by a power-supply rejection test at the end points.

Note 3: R_L = ∞, digital inputs at GND or V_{DD}.

Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS: MAX5351

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		13			Bits
Integral Nonlinearity (Note 4)	INL	MAX5351A			±1	LSB
		MAX5351B			±2	
		MAX5351MJA			±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 4)	GE			-0.5	±6	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR				600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1555 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE (V_{DD} = +3.3V)						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.9Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		16		µs
Output Voltage Swing		Rail-to-rail (Note 5)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Time to Valid Operation on Start-Up				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		3.15		3.6	V
Supply Current	I_{DD}	(Note 6)		0.24	0.4	mA
Supply Current in Shutdown		(Note 6)		1.6	10	µA
Reference Current in Shutdown				0.001	±0.5	µA

ELECTRICAL CHARACTERISTICS: MAX5351 (continued)

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: Guaranteed from code 44 to code 8191 in unity-gain configuration.

Note 5: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 150mV, guaranteed by a power-supply rejection test at the end points.

Note 6: R_L = ∞, digital inputs at GND or V_{DD}.

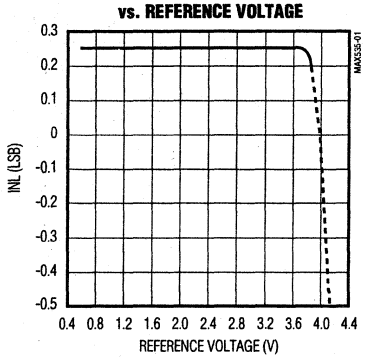
Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

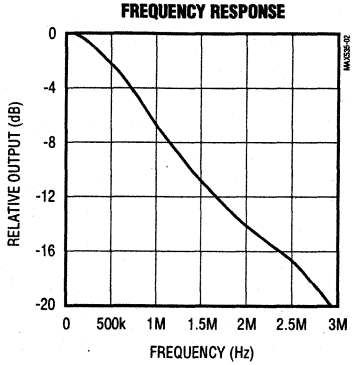
(MAX535 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX535

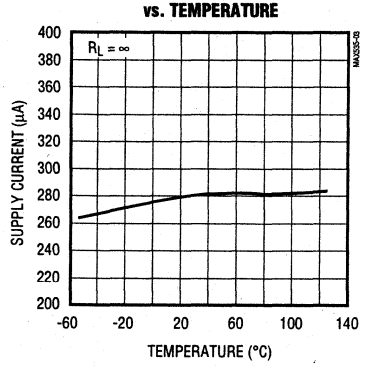
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



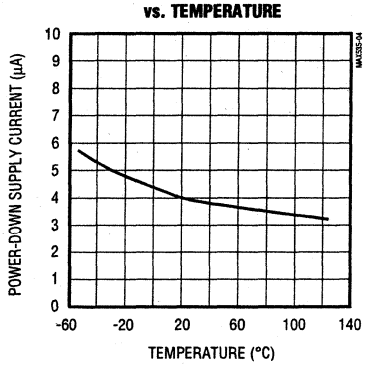
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



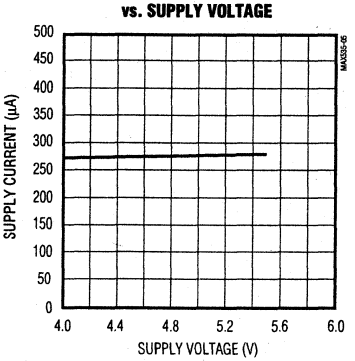
SUPPLY CURRENT vs. TEMPERATURE



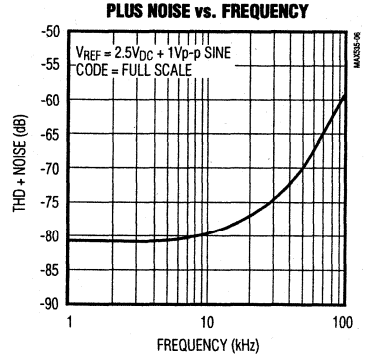
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



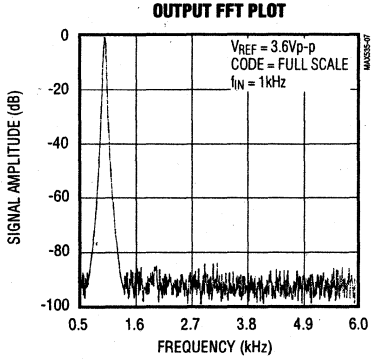
SUPPLY CURRENT vs. SUPPLY VOLTAGE



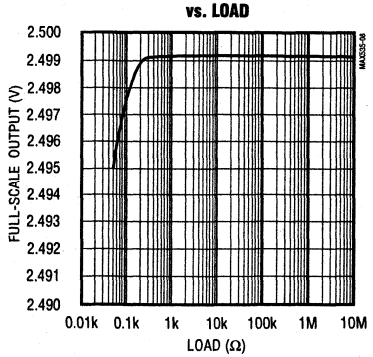
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



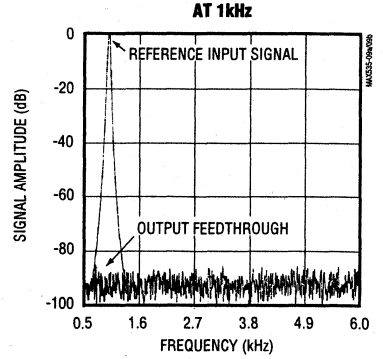
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

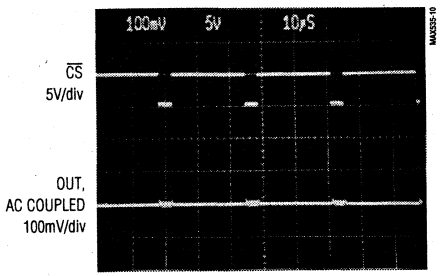


Typical Operating Characteristics (continued)

(MAX535 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

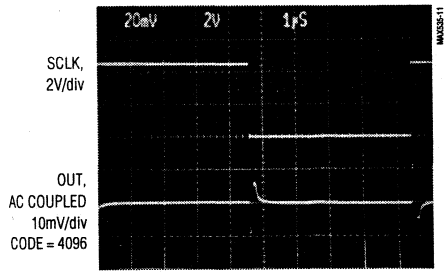
MAX535 (continued)

MAJOR-CARRY TRANSITION



10µs/div

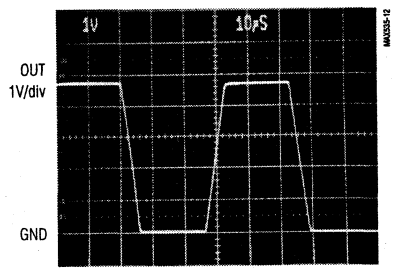
DIGITAL FEEDTHROUGH (f_{SCLK} = 100kHz)



2µs/div

CS = 5V

DYNAMIC RESPONSE



10µs/div

GAIN = 2, SWITCHING FROM CODE 0 TO 8040

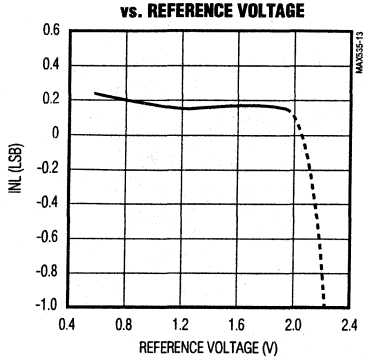
Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

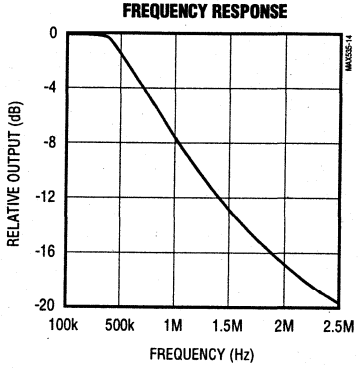
(MAX5351 only, V_{DD} = +3.3V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5351

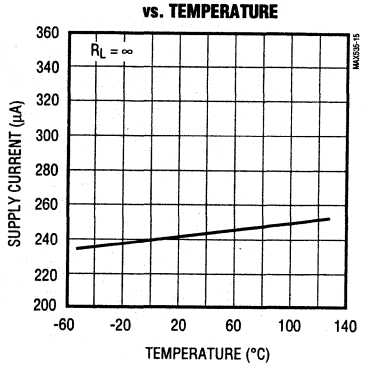
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



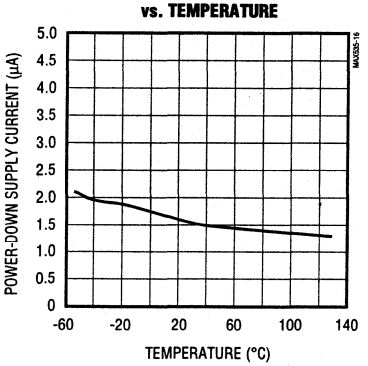
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



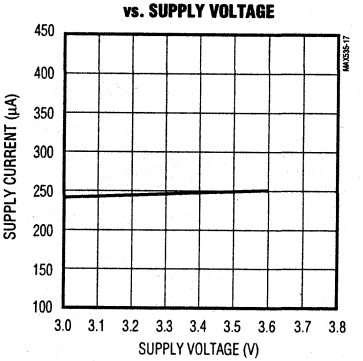
SUPPLY CURRENT vs. TEMPERATURE



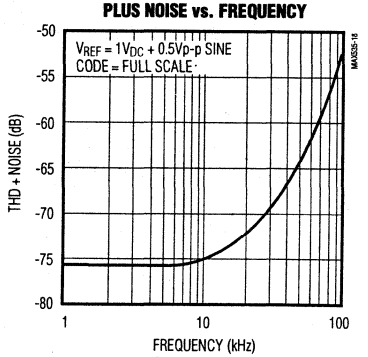
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



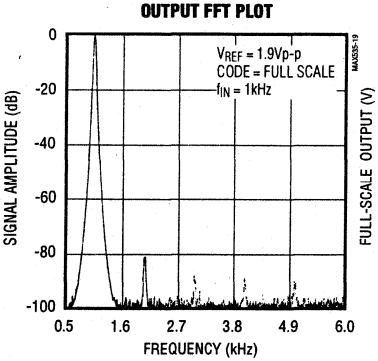
SUPPLY CURRENT vs. SUPPLY VOLTAGE



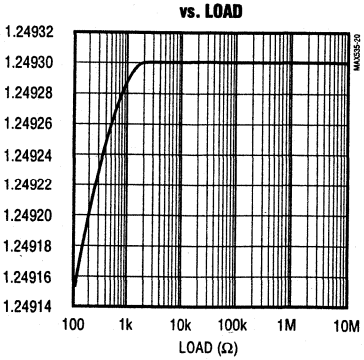
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



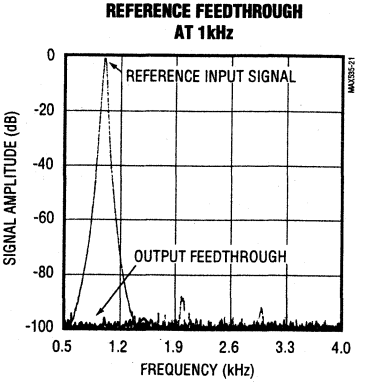
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz



Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{CS}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V_{DD}	Positive Power Supply

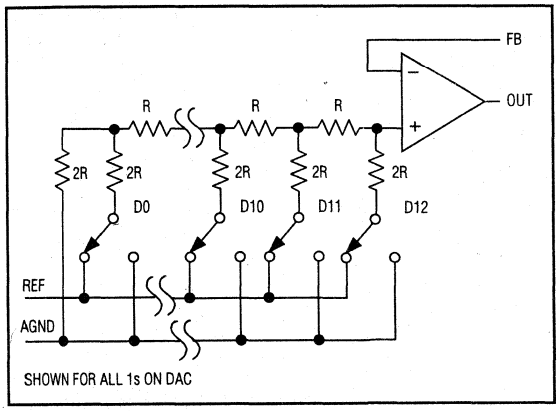


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX535/MAX5351 contain a 13-bit, voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. It includes a 16-bit shift register, and has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a 13-bit digital input into an equivalent analog output voltage in proportion to the applied reference voltage input. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source as:

$$V_{OUT} = (V_{REF} \times NB / 8192) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 8191), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 14kΩ when the DAC has an input code of 1555 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

The REF reference input has a 14kΩ guaranteed minimum input impedance. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.0062LSB (0.009LSB worst case) when driving the MAX535 reference input at 2.5V.

In shutdown mode, the MAX535/MAX5351's REF input enters a high-impedance state with a typical input leakage current of 0.001µA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (with an input code of all 1s).

Output Amplifier

The MAX535/MAX5351's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX535/MAX5351 output, the typical settling time to ±1/2LSB is 16µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX535 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

Shutdown Mode

The MAX535/MAX5351 feature a software-programmable shutdown that reduces supply current to a typical value of 4µA. Writing 111XXXXXXXXXXXX as the input-control word puts the MAX535/MAX5351 in shutdown mode (Table 1).

In shutdown mode, the MAX535/MAX5351 output amplifier and the reference input enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX535/MAX5351 to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the output to stabilize.

Serial-Interface Configurations

The MAX535/MAX5351's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 13 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX535/MAX5351's response outlined in Table 1.

The MAX535/MAX5351's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

Serial-Interface Description

The MAX535/MAX5351 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 13 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 13 data bits D12...D0 (Figure 4). The 3-bit control code determines:

- The register to be updated
- The configuration when exiting shutdown

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX535/MAX5351 input/DAC register on $\overline{CS}$'s rising edge.

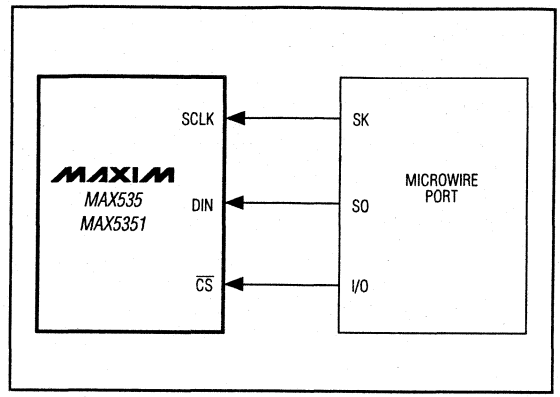


Figure 2. Connections for Microwire

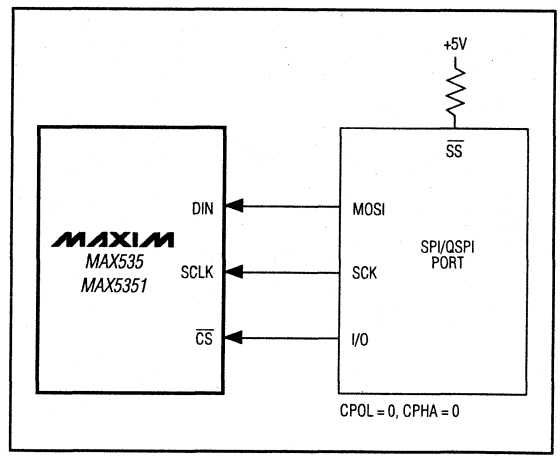


Figure 3. Connections for SPI/QSPI

MSB ..... LSB			
← 16 Bits of Serial Data →			
Control Bits			Data Bits MSB ..... LSB
C2	C1	C0	D12 ..... D0
← 3 Control Bits →			← 13 Data Bits →

Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD				FUNCTION
C2	C1	C0	D12.....D0 MSB LSB	
X	0	0	13 bits of data	Load input register; DAC register immediately updated (also exit shutdown).
X	0	1	13 bits of data	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXXXXX	Update DAC register from input register (also exit shutdown; recall previous state).
1	1	1	XXXXXXXXXXXXX	Shutdown
0	1	1	XXXXXXXXXXXXX	No operation (NOP)

"X" = Don't care

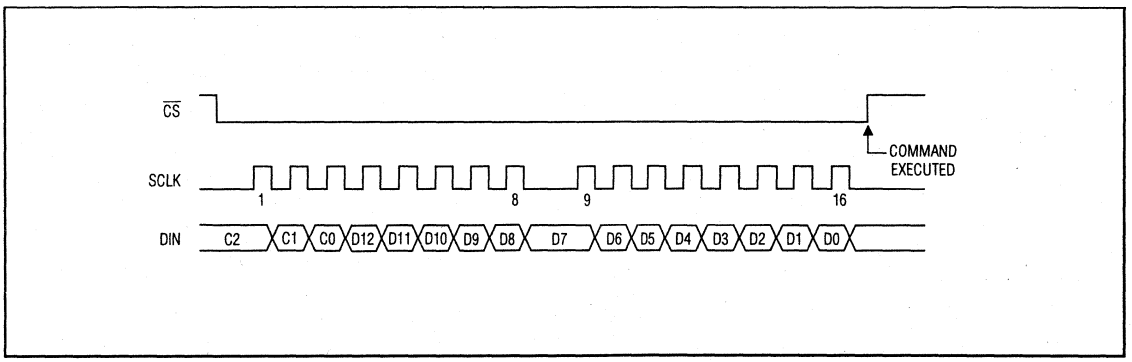


Figure 5. Serial-Interface Timing Diagram

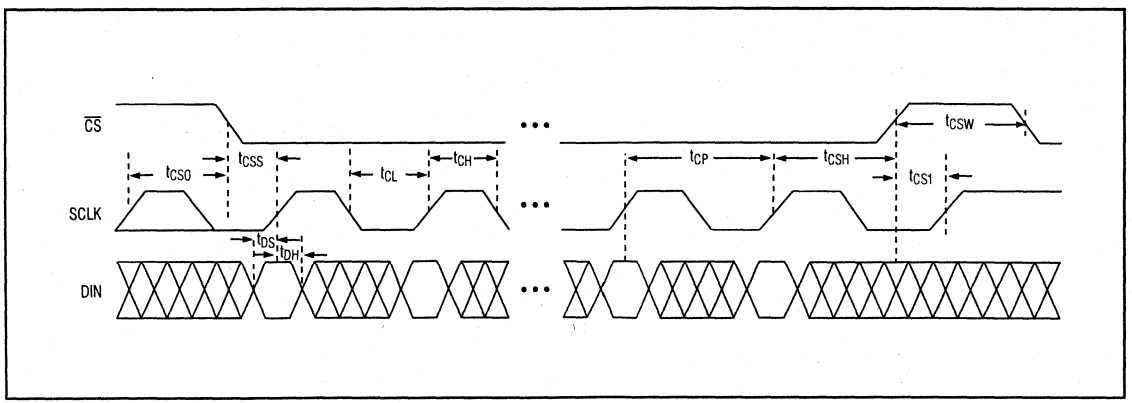


Figure 6. Detailed Serial-Interface Timing Diagram

Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

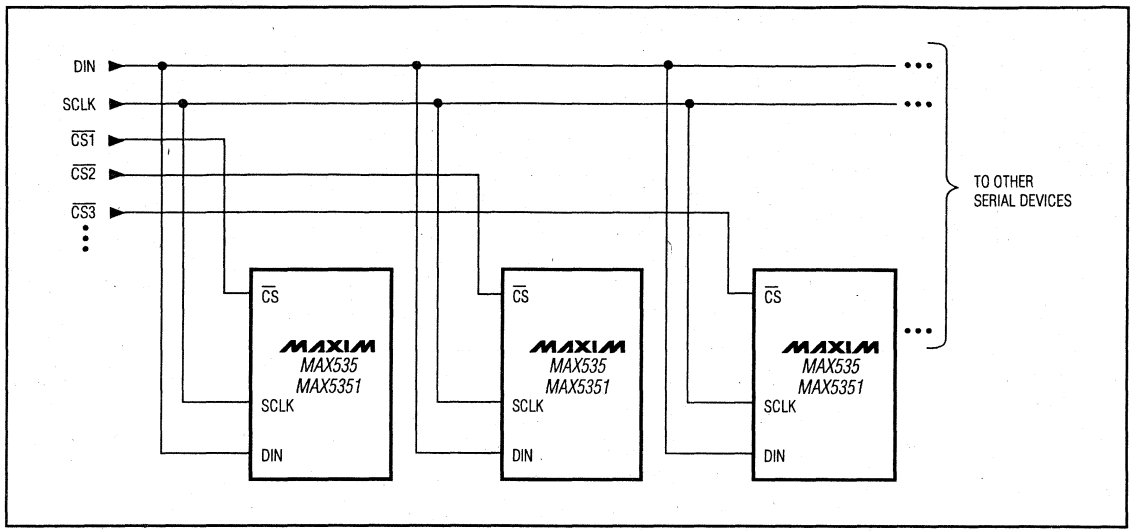


Figure 7. Multiple MAX535/MAX5351s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX535/MAX5351s. In this configuration, the clock and the data bus are common to all devices and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX535/MAX5351 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail output, see Figure 9. This circuit shows the MAX535/MAX5351 with the output amplifier configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used. When using the MAX5351 with a 1.25V reference, this circuit provides a 0V to 2.5V full-scale range.

Bipolar Output

The MAX535/MAX5351 output can be configured for bipolar operation using Figure 10's circuit.

$$V_{OUT} = V_{REF}\,[(2NB / 8192) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and the corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
11111	1111	1111	$+V_{REF}\left(\frac{8191}{8192}\right)$
10000	0000	0001	$+V_{REF}\left(\frac{4097}{8192}\right)$
10000	0000	0000	$+V_{REF}\left(\frac{4096}{8192}\right) = \frac{+V_{REF}}{2}$
01111	1111	1111	$+V_{REF}\left(\frac{4095}{8192}\right)$
00000	0000	0001	$+V_{REF}\left(\frac{1}{8192}\right)$
00000	0000	0000	0V

Using an AC Reference

In applications where the reference has AC-signal components, the MAX535/MAX5351 have multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
11111	1111	1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
10000	0000	0001	$+V_{REF}\left(\frac{1}{4096}\right)$
10000	0000	0000	0V
01111	1111	1111	$-V_{REF}\left(\frac{1}{4096}\right)$
00000	0000	0001	$-V_{REF}\left(\frac{4095}{4096}\right)$
00000	0000	0000	$-V_{REF}\left(\frac{4096}{4096}\right) = -V_{REF}$

The MAX535's total harmonic distortion plus noise (THD + N) is typically less than -77dB (full-scale code), and the MAX5351's THD + N is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz for both devices, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4–20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 8192)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

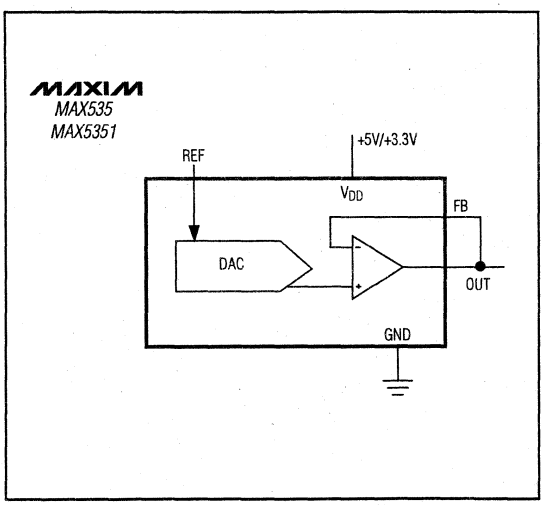


Figure 8. Unipolar Output Circuit

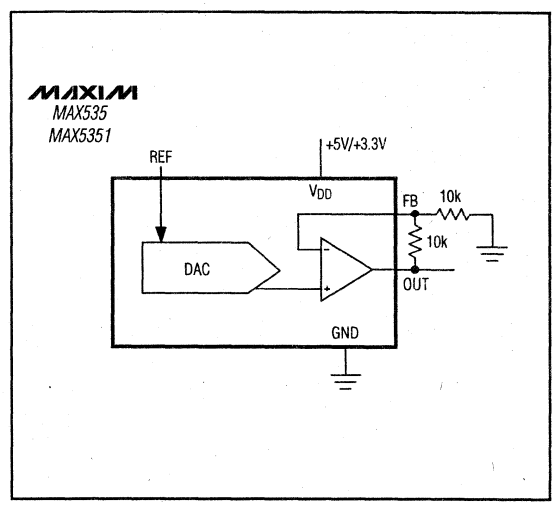


Figure 9. Unipolar Rail-to-Rail Output Circuit

9

Low-Power, 13-Bit Voltage-Output DACs with Serial Interface

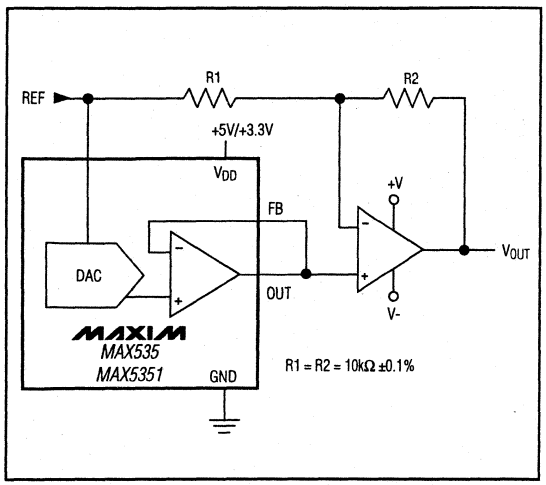


Figure 10. Bipolar Output Circuit

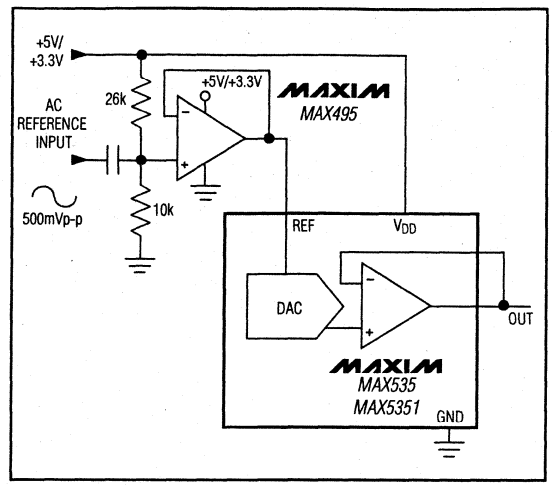


Figure 11. AC Reference Input Circuit

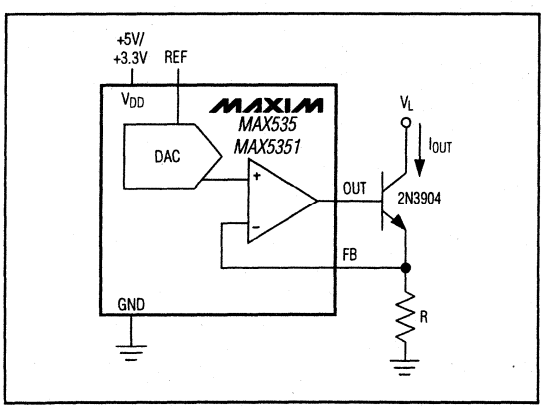


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX535/MAX5351 performance, REF should be at least 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX535AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX535BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX535AEUA	-40°C to +85°C	8 µMAX†	±1/2
MAX535BEUA	-40°C to +85°C	8 µMAX	±1
MAX535BMJA	-55°C to +125°C	8 CERDIP**	±2
MAX5351ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5351BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5351ACUA	0°C to +70°C	8 µMAX†	±1
MAX5351BCUA	0°C to +70°C	8 µMAX	±2
MAX5351BC/D	0°C to +70°C	Dice*	±2
MAX5351AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5351BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5351AEUA	-40°C to +85°C	8 µMAX†	±1
MAX5351BEUA	-40°C to +85°C	8 µMAX	±2
MAX5351BMJA	-55°C to +125°C	8 CERDIP**	±4

† *Contact factory for availability.*
* *Dice are tested at +25°C, DC parameters only.*
** *Contact factory for availability and processing to MIL-STD-883.*

Chip Information

TRANSISTOR COUNT: 1677

19-1206; Rev 0; 3/97

MAXIM

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

General Description

The MAX548A/MAX549A/MAX550A serial, 8-bit voltage-output digital-to-analog converters (DACs) operate from a single +2.5V to +5.5V supply. Their ±1LSB TUE specification is guaranteed over temperature. Operating current (supply current plus reference current) is typically 75µA per DAC with V_{DD} = 2.5V. In shutdown, the DAC is disconnected from the reference, reducing current drain to less than 1µA. The MAX548A/MAX549A allow each DAC to be shut down independently.

The 10MHz, 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™ interface standards. Double-buffered inputs provide flexibility when updating the DACs; the input and DAC registers can be updated individually or simultaneously.

The MAX548A is a dual DAC with an asynchronous load input; it uses V_{DD} as the reference input. The MAX549A is a dual DAC with an external reference input. The MAX550A is a single DAC with an external reference input and an asynchronous load input.

The MAX548A/MAX549A/MAX550A's low power consumption and small µMAX and DIP packages make these devices ideal for portable and battery-powered applications.

Applications

Battery-Powered Systems
VCXO Control
Comparator-Level Settings
GaAs Amp Bias Control
Digital Gain and Offset Control

Features

- **+2.5V to +5.5V Single-Supply Operation**
- **±1LSB (max) TUE**
- **Power-On Reset Clears All Registers to Zero**
- **Low Operating Current:**
  150µA (MAX548A/MAX549A, V_{REF} = +2.5V)
  75µA (MAX550A, V_{REF} = +2.5V)
- **1µA Shutdown Mode**
- **10MHz, 3-Wire Serial Interface Compatible with SPI/QSPI and Microwire**
- **µMAX Package—50% Smaller than 8-Pin SO**
- **Independent Shutdown of DACs (MAX548A/MAX549A)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE†
MAX548ACPA	0°C to +70°C	8 Plastic DIP
MAX548ACUA	0°C to +70°C	8 µMAX
MAX548AC/D	0°C to +70°C	Dice*
MAX548AEPA	-40°C to +85°C	8 Plastic DIP
MAX548AEUA	-40°C to +85°C	8 µMAX

Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C, DC parameters only.*
†Contact factory for availability of 8-pin SO package.

Selector Guide

FEATURE	MAX548A	MAX549A	MAX550A
Number of DACs	2	2	1
DAC Reference	V_{DD}	External	External
Asynchronous Load DAC Input	√	—	√
µMAX Package	√	√	√

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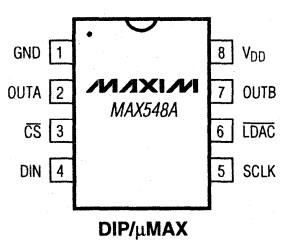
Microwire is a trademark of National Semiconductor Corp.

Pin Configurations



Pin Configurations continued at end of data sheet.

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+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

ABSOLUTE MAXIMUM RATINGS

V_{DD}, SCLK, DIN, $\overline{CS}$, $\overline{LDAC}$, OUT_ to GND .....-0.3V to 6V
REF to GND .....-0.3V to (V_{DD} + 0.3V)
Maximum Current (any pin) .....±50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
µMAX (derate 4.10mW/°C above +70°C) 330mW

Operating Temperature Ranges
MAX5_ _AC_ A.....0°C to +70°C
MAX5_ _AE_ A.....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Differential Nonlinearity	DNL	Guaranteed monotonic	MAX5_ _AEUA (Note 1)			±0.9	LSB
			All others			±0.9	
Total Unadjusted Error	TUE		MAX5_ _AEUA (Note 1)			±1	LSB
			All others			±1	
Zero-Code Error	ZCE					±1	LSB
Full-Scale Error	FSE					±1	LSB
REFERENCE INPUT							
Reference Input Voltage Range	V_{REF}	MAX549A/MAX550A for specified performance		2.5		V_{DD}	V
Reference Input Resistance DAC Code = 55 Hex (Note 2)	R_{REF}	MAX549A			16.7		kΩ
		MAX550A			33.3		
Reference Input Current DAC Code = 55 Hex (Note 3)	I_{REF}	MAX549A	V_{DD} = V_{REF} = 5.5V		330	550	µA
			V_{DD} = V_{REF} = 2.5V		150	250	
		MAX550A	V_{DD} = V_{REF} = 5.5V		165	275	
			V_{DD} = V_{REF} = 2.5V		75	125	
DAC OUTPUT							
DAC Output Voltage Swing		MAX548A		0		V_{DD}	V
		MAX549A/MAX550A		0		V_{REF}	
DAC Output Resistance	R_{OUT}				33.3		kΩ
DAC Output Resistance Matching	$\Delta R_{OUT}/R_{OUT}$	MAX548A/MAX549A			±0.2		%
DIGITAL INPUTS							
Input High Voltage	V_{IH}			0.7V_{DD}			V
Input Low Voltage	V_{IL}					0.3V_{DD}	V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}				±1	µA
Input Capacitance (Note 4)	C_{IN}					10	pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
Digital Feedthrough and Crosstalk		$\overline{CS}$ = high, all digital inputs from 0V to V_{DD}			50		nV-sec
Voltage-Output Settling Time		To ±1/2LSB, C_L = 20pF			4		µs
Voltage-Output Slew Rate		C_L = 20pF	V_{DD} = 2.5V		1.4		V/µs
			V_{DD} = 5.5V		3.1		
Wake-Up Time at Power-Up		C_L = 20pF			4		µs
POWER SUPPLIES							
Supply Voltage Range	V_{DD}	Outputs unloaded, all inputs = GND or V_{DD}		2.5		5.5	V
Supply Current (MAX548A)	I_{DD}	Outputs unloaded, all inputs = GND or V_{DD} (Note 5)	V_{DD} = 5.5V		330	550	µA
			V_{DD} = 2.5V		150	250	
Supply Current (MAX549A/MAX550A)	I_{DD}	Outputs unloaded, all inputs = GND or V_{DD}; V_{DD} = 5.5V			0.3	10	µA
Shutdown Current		Shutdown mode			0.3		µA

TIMING CHARACTERISTICS

(V_{DD} = +2.5V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Digital inputs switching from 0V to V_{DD}.) (Figure 3) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
DIN to SCLK High Setup	t_{DS}		30			ns
DIN to SCLK High Hold	t_{DH}	V_{DD} = 2.5V	0			ns
		V_{DD} = 5.5V	10			
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		30			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		30			ns
SCLK High to CS Low Hold	t_{CSH0}		10			ns
Delay, SCLK High to $\overline{CS}$ High	t_{CSH1}	V_{DD} = 2.5V	10			ns
		V_{DD} = 5.5V	20			
$\overline{CS}$ Pulse Width High	t_{CSW}		40			ns
SCLK Period	t_{CP}		80			ns
$\overline{LDAC}$ Pulse Width Low	$t_{\overline{LDAC}}$	MAX548A/MAX550A only	50			ns
CS High to $\overline{LDAC}$ Low	t_{CSLD}	MAX548A/MAX550A only	50			ns
V_{DD} High to $\overline{CS}$ Low			5			µs

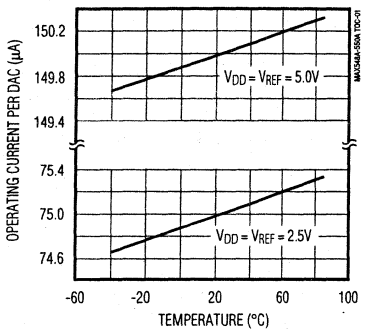
Note 1: Cold temperature specifications (to -40°C) guaranteed by design using six sigma design limits.
Note 2: Worst-case input resistance at REF occurs at DAC code 55 hex.
Note 3: Worst-case reference input current occurs at DAC code 55 hex.
Note 4: Guaranteed by design. Not production tested.
Note 5: I_{DD} measured with DACs loaded with worst-case DAC code 55 hex.

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

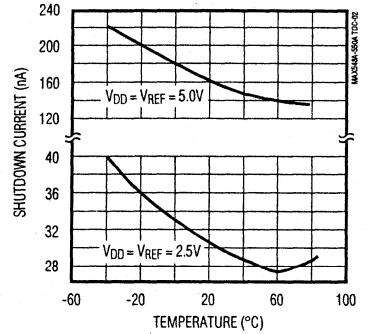
Typical Operating Characteristics

(V_{DD} = V_{REF} = 2.5V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

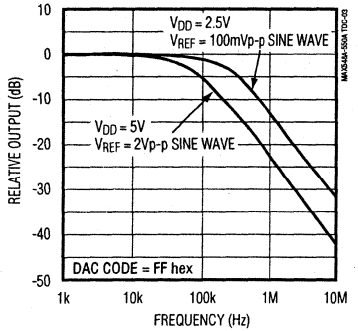
OPERATING CURRENT PER DAC vs. TEMPERATURE



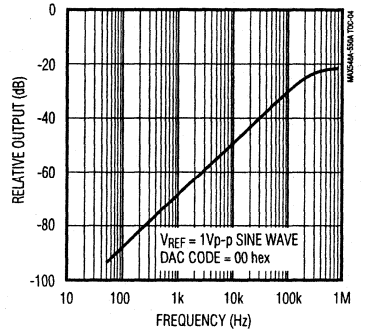
SHUTDOWN CURRENT vs. TEMPERATURE



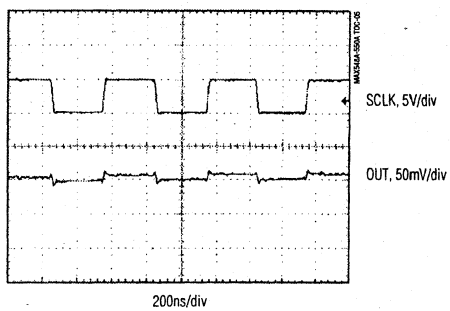
MAX549A/MAX550A REFERENCE SMALL-SIGNAL FREQUENCY RESPONSE



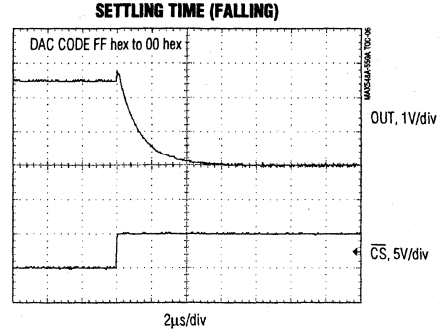
MAX549A/MAX550A REFERENCE AC FEEDTHROUGH vs. FREQUENCY



DIGITAL FEEDTHROUGH



SETTLING TIME (FALLING)

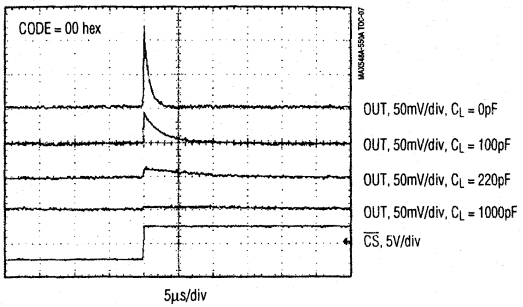


+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

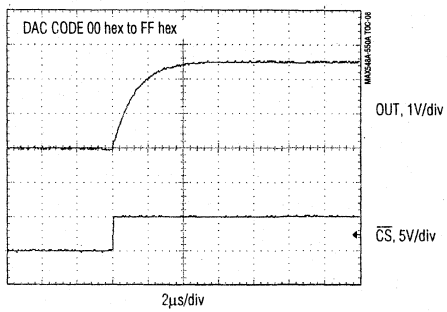
Typical Operating Characteristics (continued)

(V_{DD} = V_{REF} = 2.5V, R_L = 1MΩ, C_L = 15pF, T_A = +25°C, unless otherwise noted.)

OUTPUT GLITCH FILTERING



SETTLING TIME (RISING)



Pin Description

PIN			NAME	FUNCTION
MAX548A	MAX549A	MAX550A		
1	1	1	GND	Ground
2	2	—	OUTA	DAC A Output Voltage
—	—	2	OUT	DAC Output Voltage
3	3	3	$\overline{CS}$	Chip-Select Input. A logic low on $\overline{CS}$ enables serial data to be clocked into the input shift register. Programming commands are executed at $\overline{CS}$'s rising edge.
4	4	4	DIN	Serial-Data Input. Data is clocked into the 16-bit input shift register on SCLK's rising edge.
5	5	5	SCLK	Serial-Clock Input. Data is clocked in on SCLK's rising edge.
6	—	6	$\overline{LDAC}$	Load DAC Input. After $\overline{CS}$ goes high and if programmed by the control word, a falling edge on $\overline{LDAC}$ updates the DAC latch(es). Connect $\overline{LDAC}$ to V_{DD} if unused.
7	6	—	OUTB	DAC B Output Voltage
—	7	7	REF	External Reference Voltage Input for DAC(s)
8	8	8	V_{DD}	Positive Power Supply (+2.5V to +5.5V)

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Detailed Description

Analog Section

The MAX548A/MAX549A/MAX550A are 8-bit, voltage-output digital-to-analog converters (DACs). The MAX548A/MAX549A are dual DACs, and the MAX550A is a single DAC. Each DAC consists of an R-2R ladder network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage (Figure 1).

The DACs feature double-buffered inputs and unbuffered outputs. The MAX549A/MAX550A require an external reference. The MAX548A's reference inputs are internally connected to V_{DD}. The power-supply range is from +2.5V to +5.5V.

Reference Input

The voltage applied at REF (V_{DD} for the MAX548A) sets the full-scale output for all the DACs and may range from +2.5V to V_{DD}. The REF input resistance is code dependent, with the lowest value occurring with code 01010101 (55 hex). To minimize INL errors, the reference voltage source should have less than 3Ω output impedance.

DAC Output

The MAX548A/MAX549A/MAX550A contain DACs with unbuffered outputs; each output connects directly to an R-2R ladder. Typical output impedance is 33.3kΩ. This configuration minimizes power consumption and reduces offset errors. For highest accuracy, apply high resistive loads (1MΩ and up). Lower resistive loads can be driven, but output loading increases full-scale error. The magnitude of the expected error is the ratio of the DAC output resistance to the DC load resistance at the output.

Typically, an energy pulse is coupled into the DAC output on $\overline{CS}$'s rising edge. Since each DAC output is unbuffered, connecting a small capacitor (200pF to 1000pF) from the output to ground creates a lowpass filter that effectively suppresses the pulse for sensitive applications (see *Typical Operating Characteristics*).

Shutdown Mode

When the MAX548A/MAX549A/MAX550A are in shutdown mode, the R-2R ladder disconnects from the reference source. The MAX549A/MAX550A supply current does not change, but the REF input current decreases to less than 1µA. This allows the externally applied system reference to remain active with minimal power consumption. The MAX548A supply current also decreases to less than 1µA in shutdown mode. When the MAX548A/MAX549A/MAX550A exit shutdown mode, recovery time is equivalent to the DAC's settling time.

Serial Interface

The serial interface is SPI/QSPI and Microwire compatible. An active-low chip select ($\overline{CS}$) enables the input shift register to receive data from the serial input (DIN). Data is clocked into the shift register on the rising edge of the serial-clock signal (SCLK). The clock frequency can be as high as 10MHz.

Transmit data MSB first in one 16-bit word or two 8-bit bytes. The write cycle can be segmented to allow two 8-bit-wide transfers when $\overline{CS}$ remains low. After all 16 bits are clocked into the input shift register, a rising

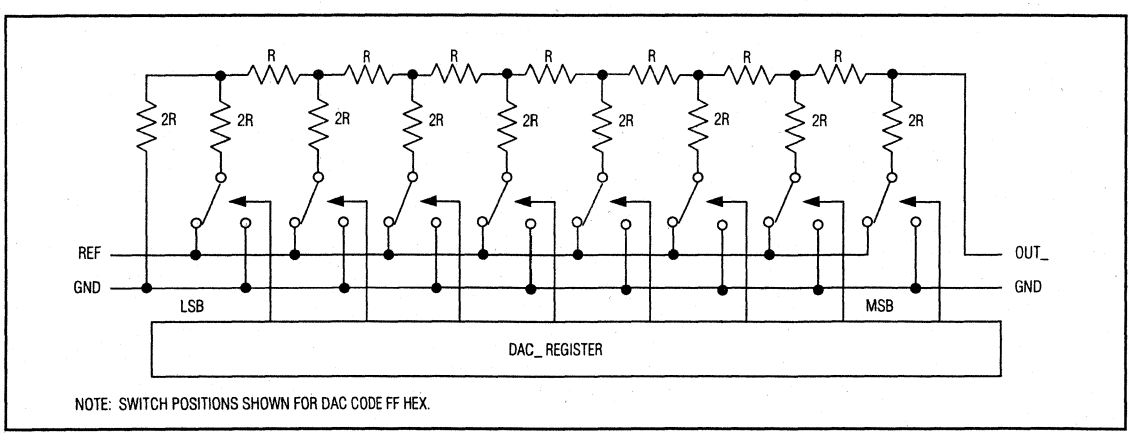


Figure 1. DAC Simplified Circuit Diagram

edge on $\overline{CS}$ programs the DAC. The input registers can be loaded independently or simultaneously without updating the DAC registers. This allows both DAC registers to be updated simultaneously with different digital values. The DAC outputs reflect the data stored in the DAC registers. $\overline{LDAC}$ can be used to asynchronously update the DAC registers independently of $\overline{CS}$ (MAX548A/MAX550A). With C1 set high, setting C0 in the control word forces the DAC register(s) to be updated on $\overline{LDAC}$'s falling edge, rather than $\overline{CS}$'s rising edge (Table 1).

Initialization

The MAX548A/MAX549A/MAX550A have an internal power-on reset. At power-up, all internal registers are reset to zero; therefore, an initialization write sequence is not necessary.

Serial-Input Data Format and Control Codes

The control byte determines which input registers/DAC registers are updated (Table 1). The DAC input registers are updated on the rising edge of $\overline{CS}$. The DAC registers can be updated on $\overline{CS}$'s rising edge or on $\overline{LDAC}$'s falling edge after $\overline{CS}$ goes high. Bit C0 of the control byte determines how the DAC registers are updated for the MAX548A/MAX550A. The MAX549A has no $\overline{LDAC}$ pin; the DAC registers are always updated on $\overline{CS}$'s rising edge (C0 in the control byte has no effect).

Tables 2, 3, and 4 list the serial-input command format for the MAX548A, MAX549A, and MAX550A, respectively. The 16-bit input word consists of an 8-bit control byte and an 8-bit data byte. The control byte is not decoded internally. Every control bit performs one

Table 1. Control-Byte/Input-Word Bit Definitions

	BIT NAME	STATE	OPERATION
CONTROL BYTE	UB1*	X	Unassigned Bit 1
	UB2	X	Unassigned Bit 2
	UB3	X	Unassigned Bit 3
	C2	0	Power-Up Mode
	C2	1	Power-Down Mode
	C1	0	DAC Register Load Operation Disabled
	C1	1	DAC Register Load Operation Enabled
	C0	0	DAC Register Updated on $\overline{CS}$'s Rising Edge
	C0	1	DAC Register Updated on $\overline{LDAC}$'s Falling Edge (MAX549A = Don't Care)
	A1	0	Do Not Address DAC B (MAX550A = Don't Care)
	A1	1	Address DAC B (MAX550A = Don't Care)
	A0	0	Do Not Address DAC A
	A0	1	Address DAC A
DATA BYTE	D7	—	DAC Data Bit 7 (MSB)
	D6	—	DAC Data Bit 6
	D5	—	DAC Data Bit 5
	D4	—	DAC Data Bit 4
	D3	—	DAC Data Bit 3
	D2	—	DAC Data Bit 2
	D1	—	DAC Data Bit 1
	D0**	—	DAC Data Bit 0 (LSB)

X = Don't care **Clocked in first* ***Clocked in last*

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

function. Data is clocked in starting with unassigned bit 1 (UB1), followed by the remaining control bits and the DAC data byte. The data byte's LSB (D0) is the last bit clocked into the input register (Figure 2).

Table 5 is an example of a 16-bit input word that performs the following functions:

- Loads 80 hex (128 decimal) into the DAC input register (DAC A for the MAX548A/MAX549A)
- Updates the DAC register(s) on $\overline{CS}$'s rising edge.

Table 6 shows how to calculate the output voltage based on the input code. Figure 3 gives detailed timing information.

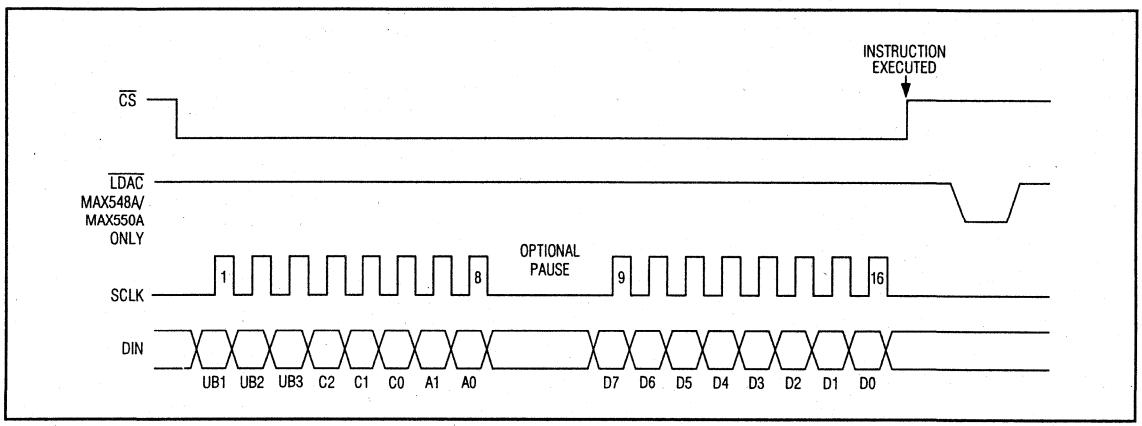


Figure 2. Serial-Interface Timing Diagram

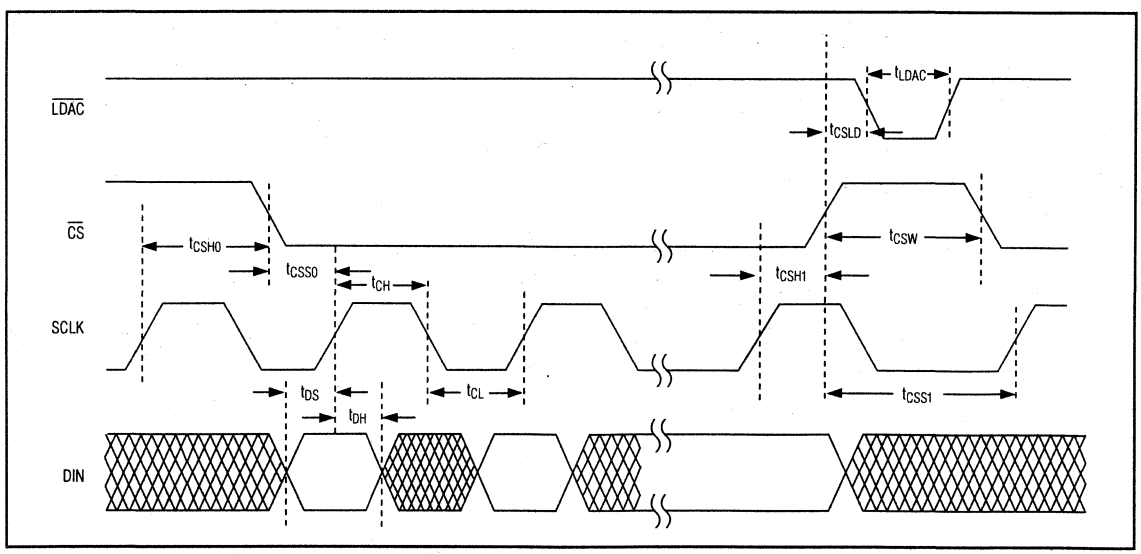


Figure 3. Detailed Serial-Interface Timing Diagram

Table 2. MAX548A Serial-Interface Programming Commands

CONTROL BYTE Loaded First								DATA BYTE Loaded Last	$\overline{LDAC}$	COMMAND (Commands executed on $\overline{CS}$'s rising edge)
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
UNASSIGNED COMMANDS										
X	X	X	0	0	X	0	0	XXXXXXXX	X	Unassigned command
X	X	X	1	X	X	0	0	XXXXXXXX	X	Unassigned operation
COMMANDS LOADING INPUT REGISTER(S) ONLY										
X	X	X	0	0	X	0	1	8-Bit DAC Data	X	Load DAC A input register. DAC B input register and both DAC registers unchanged.
X	X	X	0	0	X	1	0	8-Bit DAC Data	X	Load DAC B input register. DAC A input register and both DAC registers unchanged.
X	X	X	0	0	X	1	1	8-Bit DAC Data	X	Load both DAC input registers. Both DAC registers unchanged.
COMMANDS UPDATING DAC REGISTER(S)										
X	X	X	0	1	0	0	0	XXXXXXXX	X	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	0	0	1	8-Bit DAC Data	X	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	0	1	0	8-Bit DAC Data	X	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	0	1	1	8-Bit DAC Data	X	Load both DAC input registers and update both DAC registers.
X	X	X	0	1	1	0	0	XXXXXXXX	0	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	1	0	1	8-Bit DAC Data	0	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	1	1	0	8-Bit DAC Data	0	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	1	1	1	8-Bit DAC Data	0	Load both DAC input registers and update both DAC registers.
COMMANDS UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	0	1	1	0	0	XXXXXXXX	1	After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	1	0	1	8-Bit DAC Data	1	Load DAC A input register. After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update both DAC registers.
X	X	X	0	1	1	1	0	8-Bit DAC Data	1	Load DAC B input register. After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update both DAC registers.
X	X	X	0	1	1	1	1	8-Bit DAC Data	1	Load both DAC input registers. After $\overline{CS}$'s rising edge and on $\overline{LDAC}$'s falling edge, update both DAC registers.

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Table 2. MAX548A Serial-Interface Programming Commands (continued)

COMMANDS FOR POWERING DOWN

CONTROL BYTE Loaded First								DATA BYTE Loaded Last	LDAC	COMMAND (Commands executed on CS's rising edge)
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
COMMANDS POWERING DOWN AND LOADING INPUT REGISTER(S) ONLY										
X	X	X	1	0	X	0	1	8-Bit DAC Data	X	Load DAC A input register and power down DAC A. DAC B registers unchanged.
X	X	X	1	0	X	1	0	8-Bit DAC Data	X	Load DAC B input register and power down DAC B. DAC A registers unchanged.
X	X	X	1	0	X	1	1	8-Bit DAC Data	X	Load both DAC input registers and power down both DACs. Both DAC registers unchanged
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER(S)										
X	X	X	1	1	0	0	1	8-Bit DAC Data	X	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	0	1	0	8-Bit DAC Data	X	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	0	1	1	8-Bit DAC Data	X	Load both DAC input registers, power down both DACs, and update both DAC registers.
X	X	X	1	1	1	0	1	8-Bit DAC Data	0	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	1	1	0	8-Bit DAC Data	0	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	1	1	1	8-Bit DAC Data	0	Load both DAC input registers and power down both DACs. Update both DAC registers.
COMMANDS POWERING DOWN AND UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	1	1	1	0	1	8-Bit DAC Data	1	Load DAC A input register and power down DAC A. While powered down, on LDAC's falling edge, update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	1	1	0	8-Bit DAC Data	1	Load DAC B input register and power down DAC B. While powered down, on LDAC's falling edge, update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	1	1	1	8-Bit DAC Data	1	Load both DAC input registers and power down both DACs. While powered down, on LDAC's falling edge, update both DAC registers.

X = Don't care

Table 3. MAX549A Serial-Interface Programming Commands

CONTROL BYTE Loaded First								DATA BYTE Loaded Last	COMMAND (Commands executed on $\overline{CS}$'s rising edge)
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	
UNASSIGNED COMMAND									
X	X	X	X	0	X	0	0	XXXXXXXX	Unassigned command
COMMANDS LOADING INPUT REGISTER(S) ONLY									
X	X	X	0	0	X	0	1	8-Bit DAC Data	Load DAC A input register. DAC registers unchanged.
X	X	X	0	0	X	1	0	8-Bit DAC Data	Load DAC B input register. DAC registers unchanged.
X	X	X	0	0	X	1	1	8-Bit DAC Data	Load both DAC input registers. DAC registers unchanged.
COMMANDS UPDATING DAC REGISTER(S)									
X	X	X	X	1	X	0	0	XXXXXXXX	Update both DAC registers with current contents of their input registers. Both input registers unchanged.
X	X	X	0	1	X	0	1	8-Bit DAC Data	Load DAC A input register and update both DAC registers. DAC B input register unchanged.
X	X	X	0	1	X	1	0	8-Bit DAC Data	Load DAC B input register and update both DAC registers. DAC A input register unchanged.
X	X	X	0	1	X	1	1	8-Bit DAC Data	Load both DAC input registers and update both DAC registers.
COMMANDS POWERING DOWN AND LOADING INPUT REGISTER(S) ONLY									
X	X	X	1	0	X	0	1	8-Bit DAC Data	Load DAC A input register and power down DAC A. DAC B input register and both DAC registers unchanged.
X	X	X	1	0	X	1	0	8-Bit DAC Data	Load DAC B input register and power down DAC B. DAC A input register and both DAC registers unchanged.
X	X	X	1	0	X	1	1	8-Bit DAC Data	Load both DAC input registers and power down both DACs. Both DAC registers unchanged.
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER(S)									
X	X	X	1	1	X	0	1	8-Bit DAC Data	Load DAC A input register, power down DAC A, and update both DAC registers. DAC B input register unchanged.
X	X	X	1	1	X	1	0	8-Bit DAC Data	Load DAC B input register, power down DAC B, and update both DAC registers. DAC A input register unchanged.
X	X	X	1	1	X	1	1	8-Bit DAC Data	Load both DAC input registers, power down both DACs, and update both DAC registers.

X = Don't care

+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Table 4. MAX550A Serial-Interface Programming Commands

CONTROL BYTE Loaded First								DATA BYTE Loaded Last	LDAC	COMMAND (Commands executed on CS's rising edge)
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7.....D0	Pin 6	
UNASSIGNED COMMANDS										
X	X	X	0	0	X	X	0	XXXXXXXX	X	Unassigned command
X	X	X	1	X	X	X	0	XXXXXXXX	X	Unassigned operation
COMMANDS LOADING INPUT REGISTER ONLY										
X	X	X	0	0	X	X	1	8-Bit DAC Data	X	Load DAC input register. DAC register unchanged.
COMMANDS LOADING DAC REGISTER										
X	X	X	0	1	0	X	0	XXXXXXXX	X	Update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	0	X	1	8-Bit DAC Data	X	Load DAC input register and update DAC register.
X	X	X	0	1	1	X	0	XXXXXXXX	0	Update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	1	X	1	8-Bit DAC Data	0	Load DAC input register and update DAC register.
COMMANDS UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	0	1	1	X	0	XXXXXXXX	1	After CS's rising edge and on LDAC's falling edge, update DAC register with current contents of input register. Input register unchanged.
X	X	X	0	1	1	X	1	8-Bit DAC Data	1	Load DAC input register. After CS's rising edge and on LDAC's falling edge, update DAC register.
COMMAND POWERING DOWN AND LOADING INPUT REGISTER ONLY										
X	X	X	1	0	X	X	1	8-Bit DAC Data	X	Load DAC input register and power down DAC.
COMMANDS POWERING DOWN AND UPDATING DAC REGISTER										
X	X	X	1	1	0	X	1	8-Bit DAC Data	X	Load DAC input register, power down DAC, and update DAC register.
X	X	X	1	1	1	X	1	8-Bit DAC Data	0	Load DAC input register, power down DAC, and update DAC register.
COMMAND POWERING DOWN AND UTILIZING THE ASYNCHRONOUS LOAD FUNCTION										
X	X	X	1	1	1	X	1	8-Bit DAC Data	1	Load DAC input register and power down DAC. While powered down, on LDAC's falling edge, update DAC register.

X = Don't care

Table 5. Example Input Word

CONTROL BYTE Loaded First								DATA BYTE Loaded Last							
UB1	UB2	UB3	C2	C1	C0	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	0	1	0	0	1	1	0	0	0	0	0	0	0

X = Don't care

Microprocessor Interfacing

The MAX548A/MAX549A/MAX550A serial interface is SPI/QSPI and Microwire compatible. For SPI/QSPI, clear the CPOL and CPHA bits (CPOL = 0 and CPHA = 0). CPOL = 0 sets the clock idle state to zero, and CPHA = 0 changes data at SCLK's falling edge. This is the Microwire default condition. If a serial port is not available on your microprocessor, three bits of a parallel port can be used to emulate a serial port by bit manipulation. Operate the serial clock only when necessary, to minimize digital feedthrough at the DAC registers.

Applications Information

Power-Supply and Ground Considerations

Connect GND to the highest quality ground available. Bypass V_{DD} with a 0.1µF to 0.22µF capacitor to GND. The reference input can be used without bypassing. However, for optimum line/load-transient response and noise performance, bypass the reference input with a 0.1µF to 4.7µF capacitor to GND.

Careful PC board layout minimizes crosstalk in DAC registers, the reference, and the digital inputs. Separate analog traces by running ground traces between them. Make sure that high-frequency digital lines are not routed parallel to analog lines.

AC Considerations

Digital Feedthrough

High-speed data at any of the digital input pins can couple through a DAC's internal stray package capacitance and cause noise (digital feedthrough) at the DAC output, even though $\overline{LDAC}$ and/or $\overline{CS}$ are held high (see *Typical Operating Characteristics*). Test digital feedthrough by holding $\overline{LDAC}$ and/or $\overline{CS}$ high and toggling the digital inputs from all 1s to all 0s.

Analog Feedthrough

Due to internal stray capacitance, higher frequency analog input signals at REF can couple to the output, even when the input digital code is all 0s. This condition is shown in the MAX549A/MAX550A Reference AC Feedthrough vs. Frequency graph in the *Typical Operating Characteristics*. Test analog feedthrough by setting all DAC outputs to 0V and sweeping REF.

Table 6. Analog Output vs. Code

DAC CONTENTS								ANALOG OUTPUT (V)
D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	1	1	1	1	$+V_{REF}(255 / 256)$
1	0	0	0	0	0	0	1	$+V_{REF}(129 / 256)$
1	0	0	0	0	0	0	0	$+V_{REF}(128 / 256) = +V_{REF} / 2$
0	1	1	1	1	1	1	1	$+V_{REF}(127 / 256)$
0	0	0	0	0	0	0	1	$+V_{REF}(1 / 256)$
0	0	0	0	0	0	0	0	0

Note: 1LSB = $V_{REF} \times 2^{-8} = V_{REF}(1 / 256)$; ANALOG OUTPUT = $+V_{REF}(I / 256)$, where I = Integer Value of Digital Input.

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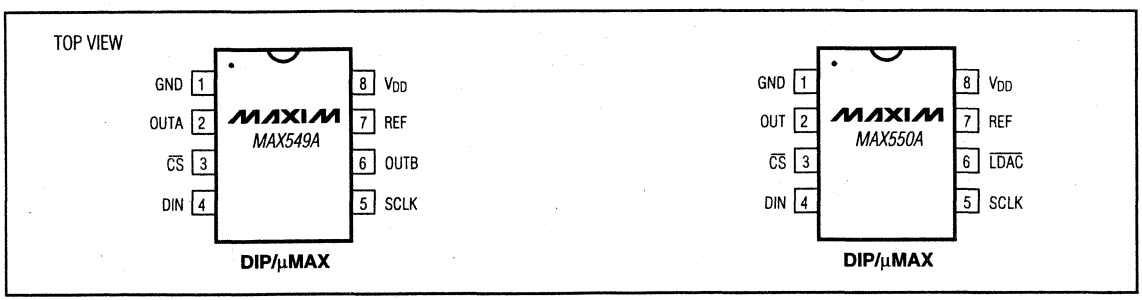
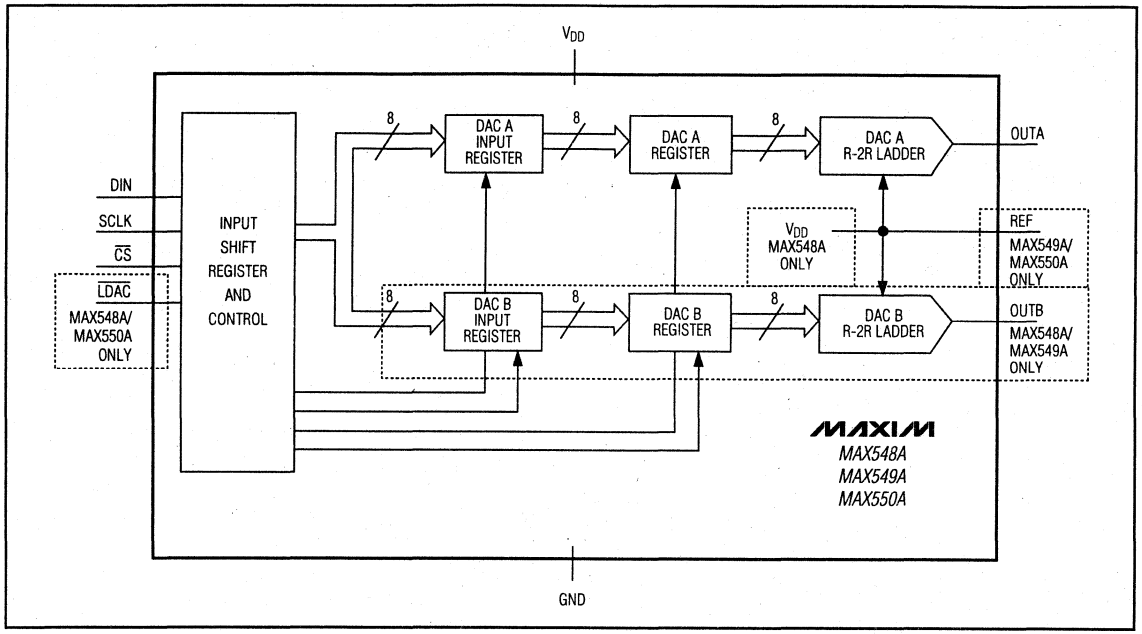
Pin Configurations (continued)



+2.5V to +5.5V, Low-Power, Single/Dual, 8-Bit Voltage-Output DACs in µMAX Package

Functional Diagram



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX549ACPA	0°C to +70°C	8 Plastic DIP
MAX549ACUA	0°C to +70°C	8 µMAX
MAX549AC/D	0°C to +70°C	Dice*
MAX549AEPA	-40°C to +85°C	8 Plastic DIP
MAX549AEUA	-40°C to +85°C	8 µMAX
MAX550ACPA	0°C to +70°C	8 Plastic DIP
MAX550ACUA	0°C to +70°C	8 µMAX
MAX550AC/D	0°C to +70°C	Dice*
MAX550AEPA	-40°C to +85°C	8 Plastic DIP
MAX550AEUA	-40°C to +85°C	8 µMAX

**Dice are specified at T_A = +25°C, DC parameters only.*

Chip Information

TRANSISTOR COUNT: 1562

19-1260; Rev 0; 10/97

MAXIM

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

General Description

The MAX551/MAX552 are 12-bit, current-output, 4-quadrant multiplying digital-to-analog converters (DACs). These devices are capable of providing unipolar or bipolar outputs when operating from either a single +5V (MAX551) or +3V (MAX552) power supply. An internal power-on-reset circuit clears all DAC registers on power-up, setting the DAC output voltage to 0V.

The SPI™/QSPI™ and Microwire™-compatible 3-wire serial interface saves board space and reduces power dissipation compared with parallel-interface devices. The MAX551/MAX552 feature double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. Data is loaded into the input register via the serial interface. The $\overline{LOAD}$ input transfers data from the input register to the DAC register, updating the DAC output voltage.

The MAX551/MAX552 are available in an 8-pin DIP package or a space-saving 10-pin µMAX package. The µMAX package provides an asynchronous clear ($\overline{CLR}$) input that clears all DAC registers when pulled to GND, setting the output voltage to 0V.

Applications

Automatic Calibration
Gain Adjustment
Transducer Drivers
Process-Control I/O Boards
Digitally Controlled Filters
Motion-Controlled Systems
µP-Controlled Systems
Programmable Amplifiers/Attenuators

Features

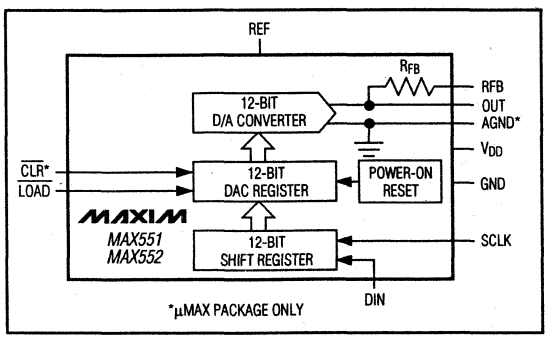
- **Single-Supply Operation:**
  +4.5V to +5.25V (MAX551)
  +2.7V to +3.6V (MAX552)
- **12.5MHz 3-Wire Serial Interface**
- **SPI/QSPI and Microwire Compatible**
- **Power-On Reset Clears DAC Output to Zero**
- **Asynchronous Clear Input Clears DAC Output to Zero**
- **Voltage Mode or Bipolar Mode Operation with a Single Power Supply**
- **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- **0.4µA Supply Current**
- **10-Pin µMAX Package**

Ordering Information

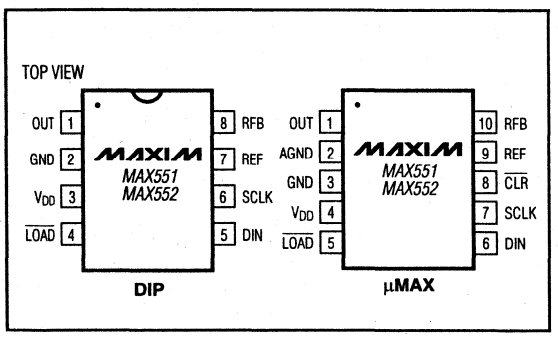
PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSB)
MAX551ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX551BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX551ACUB	0°C to +70°C	10 µMAX	±1/2
MAX551BCUB	0°C to +70°C	10 µMAX	±1
MAX551AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX551BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX551AEUB	-40°C to +85°C	10 µMAX	±1/2
MAX551BEUB	-40°C to +85°C	10 µMAX	±1

Ordering Information continued at end of data sheet.

Functional Diagram



Pin Configurations



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+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND 6V
REF, RFB to GND .....±12V
Digital Inputs (SCLK, DIN, $\overline{LOAD}$, $\overline{CLR}$)
to GND .....-0.3V to 6V
OUT to GND .....-0.3V to (V_{DD} + 0.3V)
AGND to GND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
µMAX (derate 5.60mW/°C above +70°C) 444mW

Operating Temperature Ranges
MAX55_ _C_ _ .....0°C to +70°C
MAX55_ _E_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX551

(V_{DD} = +4.5V to +5.25V, V_{REF} = 5V, OUT = AGND = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Integral Nonlinearity	INL		MAX551A			±1/2	LSB
			MAX551B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic over temperature	MAX551A			±1/2	LSB
			MAX551B			±1	
Gain Error		Using internal feedback resistor (R_{FB})	MAX551A			±1	LSB
			MAX551B			±2	
Gain Tempco (ΔGain/ΔTemp)		Using internal feedback resistor (R_{FB}) (Note 2)			±0.2	±1	ppm/°C
Power-Supply Rejection	PSR	ΔV_{DD} = +5%, -10%				2	ppm/%
DYNAMIC PERFORMANCE (Note 3)							
Current Settling Time	t_S	T_A = +25°C, to 1/2LSB, OUT load is 100Ω‖13pF, DAC register alternately loaded with 1s and 0s			0.08	1	µs
Digital-to-Analog Glitch		V_{REF} = 0V, OUT load is 100Ω‖13pF, DAC register alternately loaded with 1s and 0s			0.65	20	nV-s
AC Feedthrough at OUT		V_{REF} = 5Vp-p at 10kHz, DAC register loaded with all 0s			0.3	1	mVp-p
Total Harmonic Distortion	THD	V_{REF} = $6V_{RMS}$ at 1kHz, DAC register loaded with all 1s			-85		dB
Output Noise-Voltage Density		10Hz to 100kHz, measured between RFB and OUT			13	15	nV/√Hz

ELECTRICAL CHARACTERISTICS—MAX551 (continued)

(V_{DD} = +4.5V to +5.25V, V_{REF} = 5V, OUT = AGND = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT							
Input Resistance	R_{REF}	Measured between REF and OUT		7	11	15	kΩ
Input Resistance Tempco					6.5		ppm/°C
Reference -3dB Bandwidth	BW	V_{OUT} = 0.31V_{p-p}, R_L = 50Ω, code = full-scale			725		kHz
ANALOG OUTPUT							
OUT Leakage Current		DAC register loaded with all 0s	T_A = +25°C		±0.15	±5	nA
			T_A = T_{MIN} to T_{MAX}			±25	
OUT Capacitance	C_{OUT}	Code = zero scale (Note 2)			14	20	pF
		Code = full scale (Note 2)			20	30	
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Hysteresis	HYST	$\overline{LOAD}$, $\overline{CLR}$, DIN, and SCLK, V_{DD} = 5V			156		mV
Input Leakage Current	I_{IN}	$\overline{CLR}$	$V_{\overline{CLR}}$ = V_{DD}			±1	µA
			$V_{\overline{CLR}}$ = 0V		18	100	
		SCLK, $\overline{LOAD}$, DIN	Inputs at 0V or V_{DD}			±1	
Input Capacitance	C_{IN}	Inputs at 0V or V_{DD} (Note 2)				8	pF
SWITCHING CHARACTERISTICS							
SCLK Pulse Width High	t_{CH}			25			ns
SCLK Pulse Width Low	t_{CL}			25			ns
DIN Data to SCLK Setup	t_{DS}			15			ns
DIN Data to SCLK Hold	t_{DH}			15			ns
$\overline{LOAD}$ Pulse Width	t_{LD}			20			ns
LSB SCLK to $\overline{LOAD}$	t_{SL}			0			ns
$\overline{LOAD}$ High to SCLK	t_{LC}			15			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			20			ns
POWER SUPPLY							
Supply Voltage	V_{DD}			4.50		5.25	V
Supply Current	I_{DD}	All digital inputs at V_{IL} or V_{IH}, $\overline{CLR}$ = V_{DD}			0.5	1.5	mA
		All digital inputs at 0V or V_{DD}, $\overline{CLR}$ = V_{DD}			0.4	5	µA

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

ELECTRICAL CHARACTERISTICS —MAX552

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, OUT = AGND = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Integral Nonlinearity	INL		MAX552A			±1/2	LSB
			MAX552B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic over temperature	MAX552A			±1/2	LSB
			MAX552B			±1	
Gain Error		Using internal feedback resistor (R_{FB})	MAX552A			±1	LSB
			MAX552B			±2	
Gain Tempco (ΔGain/ΔTemp)		Using internal feedback resistor (R_{FB}) (Note 2)			±0.3	±1	ppm/°C
Power-Supply Rejection	PSR	ΔV_{DD} = +20%, -10%				1	ppm/%
DYNAMIC PERFORMANCE (Note 3)							
Current Settling Time	t_S	T_A = +25°C, to 1/2LSB, OUT load is 100Ω‖13pF, DAC register alternately loaded with 1s and 0s			0.12	1	µs
Digital-to-Analog Glitch		V_{REF} = 0V, OUT load is 100Ω‖13pF, DAC register alternately loaded with 1s and 0s			0.6	20	nV-s
AC Feedthrough at OUT		V_{REF} = 3Vp-p at 10kHz, DAC register loaded with all 0s			0.2	0.6	mVp-p
Total Harmonic Distortion	THD	V_{REF} = $6V_{RMS}$ at 1kHz, DAC register loaded with all 1s			-85		dB
Output Noise-Voltage Density		10Hz to 100kHz, measured between RFB and OUT			13	15	nV/√Hz
REFERENCE INPUT							
Input Resistance	R_{REF}	Measured between REF and OUT		7	11	15	kΩ
Input Resistance Tempco					7.5		ppm/°C
Reference -3dB Bandwidth	BW	V_{OUT} = 0.31Vp-p, R_L = 50Ω, code = full-scale			725		kHz
ANALOG OUTPUT							
OUT Leakage Current		DAC register loaded with all 0s	T_A = +25°C		±0.13	±5	nA
			T_A = T_{MIN} to T_{MAX}			±25	
OUT Capacitance	C_{OUT}	Code = zero code (Note 2)			14	20	pF
		Code = full scale (Note 2)			20	30	

ELECTRICAL CHARACTERISTICS —MAX552 (continued)

(V_{DD} = +2.7V to +3.6V, V_{REF} = 2.5V, VOUT = AGND = GND, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input High Voltage	V_{IH}			2.1			V
Input Low Voltage	V_{IL}					0.6	V
Input Hysteresis	HYST	$\overline{LOAD}$, $\overline{CLR}$, DIN, and SCLK, V_{DD} = 3V			135		mV
Input Leakage Current	I_{IN}	$\overline{CLR}$	$V_{\overline{CLR}} = V_{DD}$			±1	µA
			$V_{\overline{CLR}}$ = 0V		12	75	
		SCLK, $\overline{LOAD}$, DIN	Inputs at 0V or V_{DD}			±1	
Input Capacitance	C_{IN}	Inputs at 0V or V_{DD} (Note 2)				8	pF
SWITCHING CHARACTERISTICS							
SCLK Pulse Width High	t_{CH}			40			ns
SCLK Pulse Width Low	t_{CL}			40			ns
DIN Data to SCLK Setup	t_{DS}			15			ns
DIN Data to SCLK Hold	t_{DH}			15			ns
$\overline{LOAD}$ Pulse Width	t_{LD}			30			ns
LSB SCLK to $\overline{LOAD}$	t_{SL}			0			ns
$\overline{LOAD}$ High to SCLK	t_{LC}			15			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			30			ns
POWER SUPPLY							
Supply Voltage	V_{DD}			2.7		3.6	V
Supply Current	I_{DD}	All digital inputs at V_{IL} or V_{IH}, $\overline{CLR}$ = V_{DD}			0.1	0.5	mA
		All digital inputs at 0V or V_{DD}, $\overline{CLR}$ = V_{DD}			0.07	5	µA

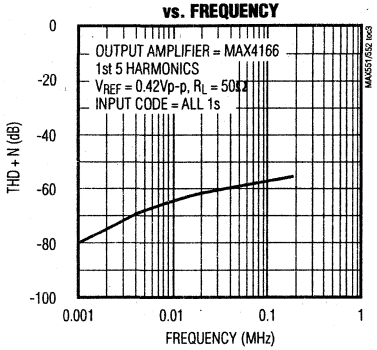
Note 1: AGND and $\overline{CLR}$ are for µMAX only.
Note 2: Guaranteed by design. Not subject to production testing.
Note 3: Parametric limits are provided for design guidance, and are not production tested.

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

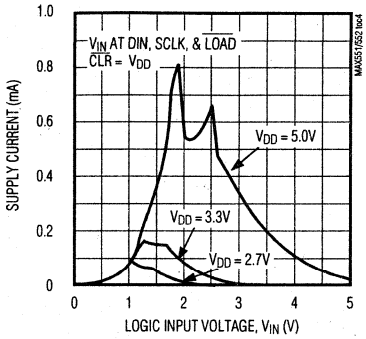
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

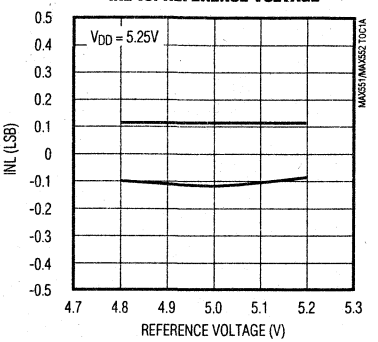
MAX551 TOTAL HARMONIC DISTORTION vs. FREQUENCY



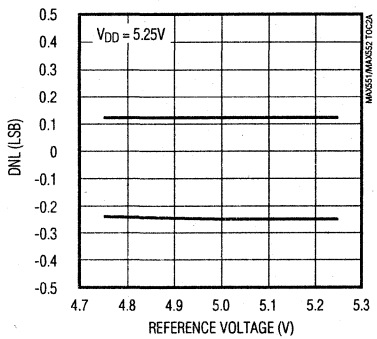
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



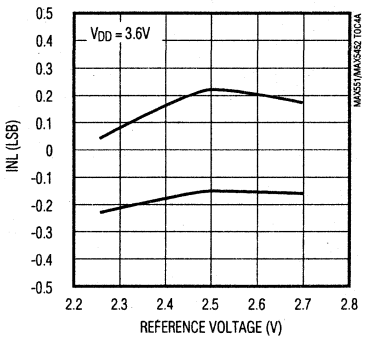
MAX551 INL vs. REFERENCE VOLTAGE



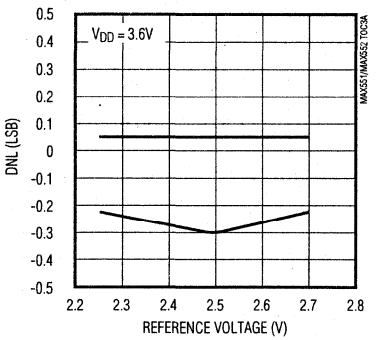
MAX551 DNL vs. REFERENCE VOLTAGE



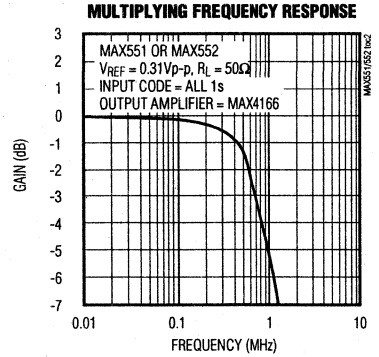
MAX552 INL vs. REFERENCE VOLTAGE



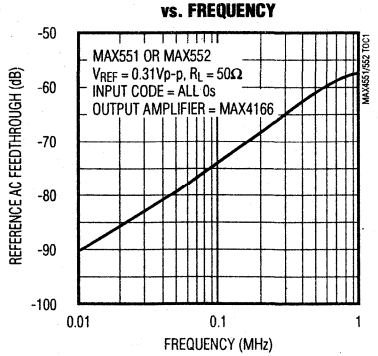
MAX552 DNL vs. REFERENCE VOLTAGE



MULTIPLYING FREQUENCY RESPONSE



REFERENCE AC FEEDTHROUGH vs. FREQUENCY



Pin Description

PIN		NAME	FUNCTION
DIP	µMAX		
1	1	OUT	DAC Current Output
—	2	AGND	Analog Ground
2	3	GND	Digital Ground. Also Analog Ground for DIP package.
3	4	V_{DD}	Supply Voltage
4	5	$\overline{LOAD}$	Active-Low Load DAC Input. Driving this asynchronous input low transfers the contents of the input register to the DAC register.
5	6	DIN	Serial-Data Input
6	7	SCLK	Serial-Clock Input. The serial input data is clocked in on SCLK's rising edge.
—	8	$\overline{CLR}$	Clear DAC Input. Clears the DAC register. Tie to V_{DD} or float if not used.
7	9	REF	Reference Input
8	10	RFB	Feedback Resistor

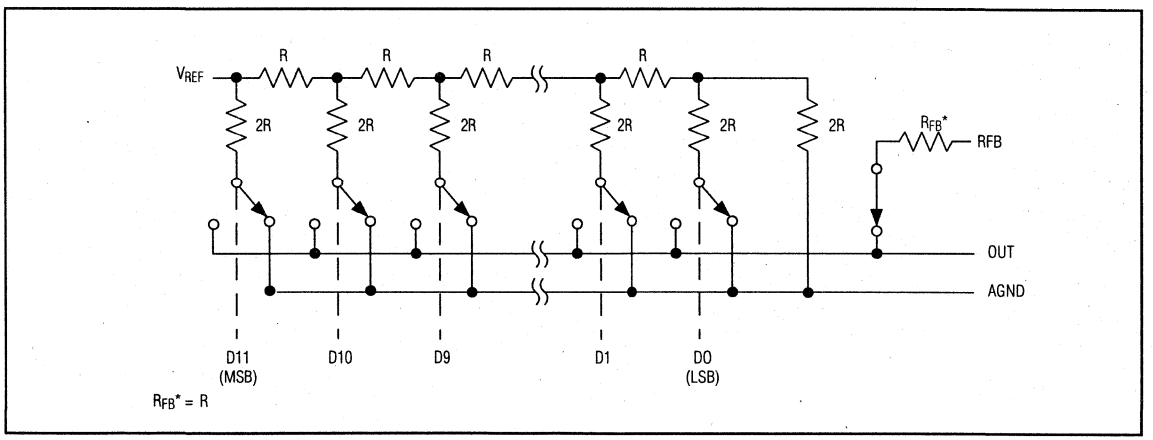


Figure 1. MAX551/MAX552 Simplified Circuit

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

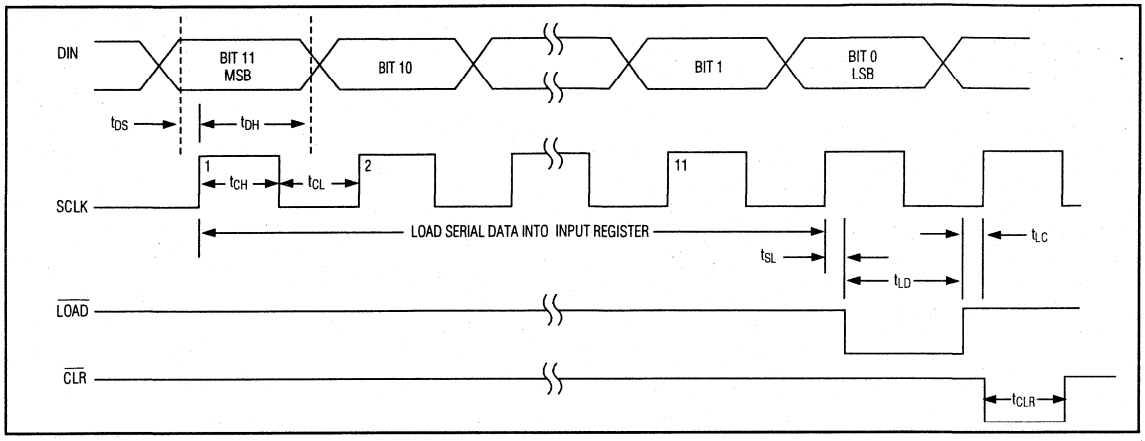


Figure 2. Write-Cycle Timing Diagram

Detailed Description

The MAX551/MAX552 digital-to-analog converter (DAC) circuits consist of a laser-trimmed, thin-film R-2R resistor array with NMOS current switches (Figure 1). Binary-weighted currents are switched to either OUT or AGND, depending on the status of each input data bit. Although the currents at OUT and AGND depend on the digital input code, the sum of the two output currents is always equal to the input current at REF.

The output current (I_{OUT}) can be converted into a voltage by adding an external output amplifier (Figure 3). The REF input accepts a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used at the reference input, use a low-tempco, external feedback resistor in place of the internal feedback resistor (R_{FB}) to minimize gain variation with temperature.

The internal feedback resistor (R_{FB}) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array, resulting in excellent supply rejection and gain-temperature coefficient.

The OUT pin output capacitance (C_{OUT}) is code dependent. C_{OUT} is typically 14pF at 000hex and 20pF at FFFhex.

Serial Interface

The MAX551/MAX552 serial interface is compatible with the SPI/QSPI and Microwire serial-interface standards. These devices accept serial clocks up to 12.5MHz (50% duty cycle). If the SCLK input is not

Table 1. Unipolar Binary-Code Table for Circuit of Figure 3

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000	0000	0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000	0000	0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000	0000	0000	0

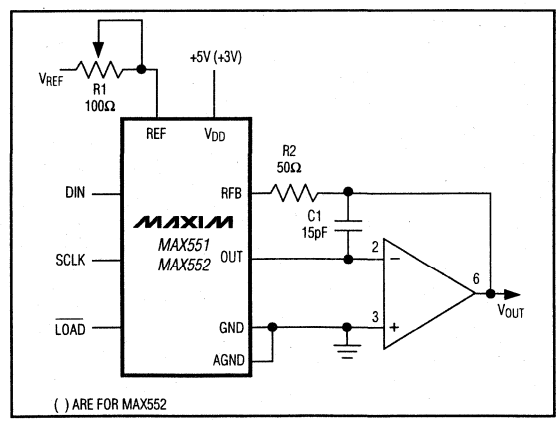


Figure 3. Unipolar Operation

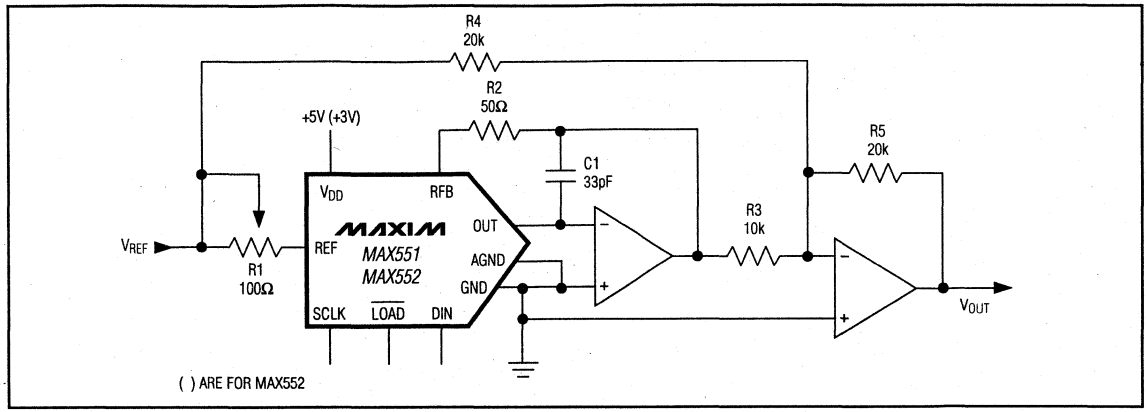


Figure 4. Bipolar Operation

Table 2. Offset Binary-Code Table for Circuit of Figure 4

DIGITAL INPUT MSB		LSB	ANALOG OUTPUT
1111	1111	1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000	0000	0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000	0000	0000	0
0111	1111	1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000	0000	0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

symmetrical, then the clock signal used must meet the t_{CH} and t_{CL} requirements given in the *Electrical Characteristics*.

Figure 2 shows the MAX551/MAX552 timing diagram. The most significant bit (MSB) is always loaded first on SCLK's rising edge. When all data is shifted into the input register, the DAC register is loaded by driving the $\overline{LOAD}$ signal low. The DAC register is transparent when $\overline{LOAD}$ is low and latched when $\overline{LOAD}$ is high. The MAX551/MAX552 digital inputs are compatible with CMOS logic levels. The MAX551's inputs are also compatible with TTL logic.

Unipolar Operation

Figure 3 shows the MAX551/MAX552's basic application. This circuit is used for unipolar operation or 2-quadrant multiplication. The code table for this mode is given in Table 1. Note that the output's polarity is the opposite of the reference voltage polarity.

In many applications the gain accuracy is sufficient and gain adjustment is not necessary. In these cases, resistors R1 and R2 in Figure 3 can be omitted. If the gain is trimmed and the DAC is operated over a wide temperature range, use low-tempco (<300ppm/°C) resistors for R1 and R2. Capacitor C1 provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the DAC's output.

Bipolar Operation

Figure 4 shows the MAX551/MAX552 operating in bipolar (or 4-quadrant multiplying) mode. Matched resistors R3, R4, and R5 must be of the same material (preferably metal film or wire-wound) for good temperature-tracking characteristics (<15ppm/°C) and should match to 0.01% for 12-bit performance. The output code is offset binary, as listed in Table 2.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is needed to adjust the ratio of R3 and R4 for 0V out. Trim full scale by loading the DAC with all 0s or 1s and adjusting the V_{REF} amplitude or varying R5 until the desired positive or negative output is obtained. In applications where gain trim is not required, omit resistors R1 and R2. If gain trim is desired and the DAC is operated over a wide tempera-

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

ture range, then low-tempco (<300ppm/°C) resistors should be used.

Applications Information

Output Amplifier

For best linearity, terminate OUT and GND at exactly 0V. In most applications, OUT is connected to an inverting op amp's summing junction. The amplifier's input offset voltage can degrade the DAC's linearity by causing OUT to be terminated to a nonzero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}(1 + R_{FB} / R_O)$$

where V_{OS} = is the op amp's offset and R_O is the DAC's output resistance, which is code dependent. The maximum error voltage ($R_O = R_{FB}$) is $2V_{OS}$; the minimum error voltage ($R_O = \infty$) is V_{OS}. To minimize this error, use a low-offset amplifier such as the MAX4166 (unipolar output) or the MAX427 (bipolar output). Otherwise, the amplifier offset must be trimmed to zero. A good guide rule is that V_{OS} should be no more than 1/10LSB.

The output amplifier's input bias current (I_B) can also limit performance, since $I_B \times R_{FB}$ generates an offset error. Choose an op amp with an I_B much less than (e.g., one-tenth) the DAC's 1LSB output current (typically 111nA when V_{REF} = 5V, and 55.5nA when V_{REF} = 2.5V). Offset and linearity can also be impaired if the output amplifier's noninverting input is grounded through a bias-current compensation resistor. This resistor adds to the offset at this pin and thus should not be used. For best performance, connect the noninverting input directly to ground.

In static or DC applications, the output amplifier's characteristics are not critical. In higher speed applications in which either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the output op amp's AC parameters must be considered.

A compensation capacitor, C1, may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. Its value depends on the type of op amp used but typically ranges from 14pF to 30pF. Too small a value causes output ringing, while excess capacitance overdamps the output. C1's size can be minimized and the output voltage settling time improved by keeping the circuit-board trace short and stray capacitance at OUT as low as possible.

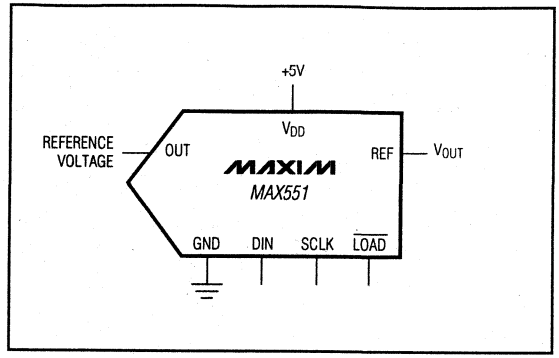


Figure 5. Single-Supply, Voltage Mode Operation

Single-Supply Operation

Reference Voltage

The MAX551/MAX552 are true 4-quadrant DACs, making them ideal for multiplying applications. The reference input accepts both AC and DC signals within a voltage range of ±6V. The R-2R ladder is implemented with thin-film resistors, enabling the use of unipolar or bipolar reference voltages with only a single power supply for the DAC. The voltage at the V_{REF} input sets the DAC's full-scale output voltage.

If the reference is too noisy, it should be bypassed to GND (AGND on the 10-pin µMAX package) with a 0.1µF ceramic capacitor located as close to the REF pin as possible.

Voltage Mode (MAX551)

The MAX551 can be conveniently used in voltage mode, single-supply operation with OUT biased at any voltage between GND and V_{DD}. OUT must not be allowed to go 0.3V lower than GND or 0.3V higher than V_{DD}. Otherwise, internal diodes will turn on, causing a high current flow that could damage the device.

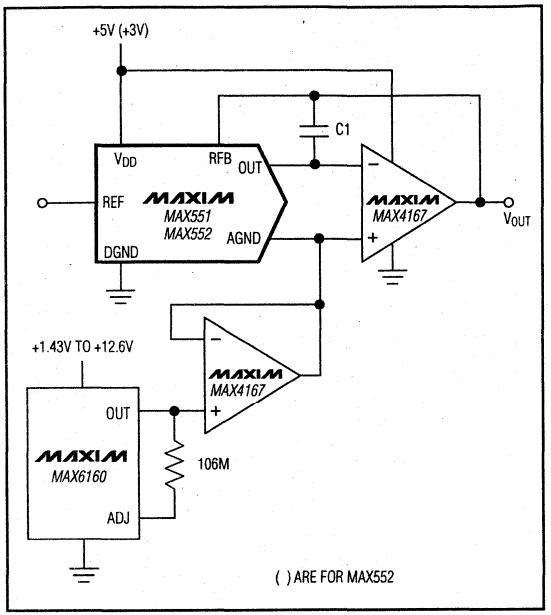


Figure 6. Single-Supply, Current Mode Operation

Figure 5 shows the MAX551 connected as a voltage output DAC. In this mode of operation, the OUT pin is connected to the reference-voltage source, and the GND pin is connected to the PCB ground plane. The DAC output now appears at the REF pin, which has a constant resistance equal to the reference input resistance (11kΩ typ). This output should be buffered with an op amp when a lower output impedance is required. The RFB pin is not used in this mode. The reference input (OUT) impedance is code dependent, and the circuit's response time depends on the reference source's behavior with changing load conditions.

An advantage of voltage mode operation is that a negative reference is not required for a positive output. Note that the reference input (OUT) must always be positive and is limited to no more than 2V when V_{DD} is 5V. The unipolar and bipolar circuits in Figures 3 and 4 can be converted to voltage mode.

Current Mode

Figure 6 shows the MAX551/MAX552 in a current output configuration in which the output amplifier is powered from a single supply, and AGND is biased to 1.23V. With 0V applied to the REF input, the output can be programmed from 1.23V (zero code) to 2.46V (full scale). With 2.45V applied to REF, the output can be programmed from 1.23V (zero code) to 0.01V (full scale).

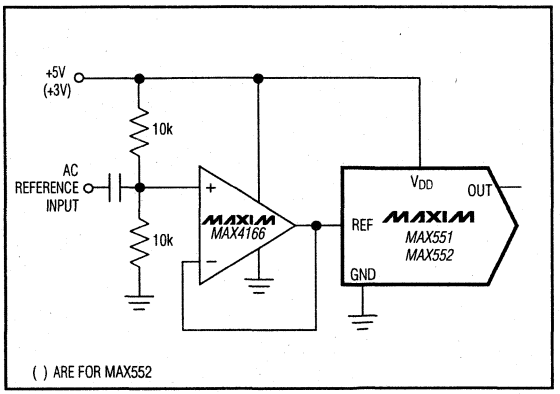


Figure 7. Single-Supply AC Reference Input Circuit

The MAX4166 op amp that drives AGND maintains the 1.23V bias as AGND's impedance changes with the DAC's digital code, from high impedance (zero code) to 7kΩ minimum (full scale).

Using an AC Reference

In applications where reference voltage has AC signal components, the MAX551/MAX552 have multiplying capability within the reference input range of ±6V. If the DAC and the output amplifier are operated with a single supply voltage, then an AC reference input can be offset with the circuit shown in Figure 7 to prevent the DAC output voltage from exceeding the output amplifier's negative output rail. The reference input's typical -3dB bandwidth is greater than 700kHz, as shown in the *Typical Operating Characteristics* graphs.

Offsetting AGND

The MAX551/MAX552 provide separate AGND and GND inputs in the µMAX package. With this package, AGND can be biased above GND to provide an arbitrary nonzero output voltage for a "0" input code (Figure 8).

Layout, Grounding, and Bypassing

Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and GND as possible. The ground pins (AGND and GND) should be connected in a star configuration to the highest quality ground available, which should be located as close to the MAX551/MAX552 as possible.

Since OUT and the output amplifier's noninverting input are sensitive to offset voltage, nodes that are to be

+3V/+5V, 12-Bit, Serial, Multiplying DACs in 10-Pin µMAX Package

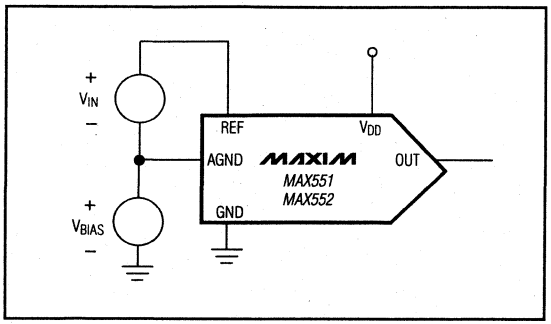


Figure 8. AGND Bias Current

grounded should be connected directly to a single-point ground through a separate, low-resistance (less than 0.2Ω) connection. The current at OUT and AGND varies with input code, creating a code-dependent error if these terminals are connected to ground (or virtual ground) through a resistive path.

Parasitic coupling of the signal from REF to OUT is an error source in dynamic applications. This coupling is normally a function of board layout and pin-to-pin package capacitance. Minimize digital feedthrough with guard traces between digital inputs, REF, and OUT pins.

The MAX551/MAX552 have high-impedance digital inputs. To minimize noise pick-up, tie them to either V_{DD} or GND when they are not in use. As a good practice, connect active inputs to V_{DD} or GND through high-value resistors (1MΩ) to prevent static charge accumulation if the pins are left floating, such as when a circuit card is left unconnected.

The $\overline{CLR}$ input on the µMAX device has an internal pull-up resistor with a typical value of 125kΩ. If the $\overline{CLR}$ input is not used, tie it to V_{DD} to minimize supply current.

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	LINEARITY (LSB)
MAX552ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX552BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX552ACUB	0°C to +70°C	10 µMAX	±1/2
MAX552BCUB	0°C to +70°C	10 µMAX	±1
MAX552AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX552BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX552AEUB	-40°C to +85°C	10 µMAX	±1/2
MAX552BEUB	-40°C to +85°C	10 µMAX	±1

Chip Information

TRANSISTOR COUNT: 887

SUBSTRATE CONNECTED TO V_{DD}

19-1271; Rev 0; 8/97

MAXIM

12-Bit, 100Msps ECL DAC

General Description

The MAX5012 is a 12-bit, 100Msps digital-to-analog converter (DAC) designed for digital modulation, direct digital synthesis, high-resolution imaging, and arbitrary-waveform-generation applications. This device is pin-for-pin compatible with the AD9712 with significantly improved settling time and glitch-energy performance.

The MAX5012 is an ECL-compatible device. It features a fast 13ns settling time and low 15pV-s glitch impulse energy, which results in excellent spurious-free dynamic range characteristics.

The MAX5012 is available in a 28-pin plastic DIP or PLCC package in the -40°C to +85°C extended-industrial temperature range.

Features

- ♦ **12-Bit, 100Msps DAC**
- ♦ **ECL-Compatible Inputs**
- ♦ **Low Power: 600mW**
- ♦ **1/2LSB DNL**
- ♦ **40MHz Multiplying Bandwidth**
- ♦ **Extended-Industrial Temperature Range**
- ♦ **Superior Performance over AD9712:**
  Improved Settling Time: 13ns
  Improved Glitch Energy: 15pV-s
  Master/Slave Latches

Applications

Fast-Frequency-Hopping Spread-Spectrum Radios

Direct-Sequence Spread-Spectrum Radios

Digital RF/IF Modulation

Microwave and Satellite Modems

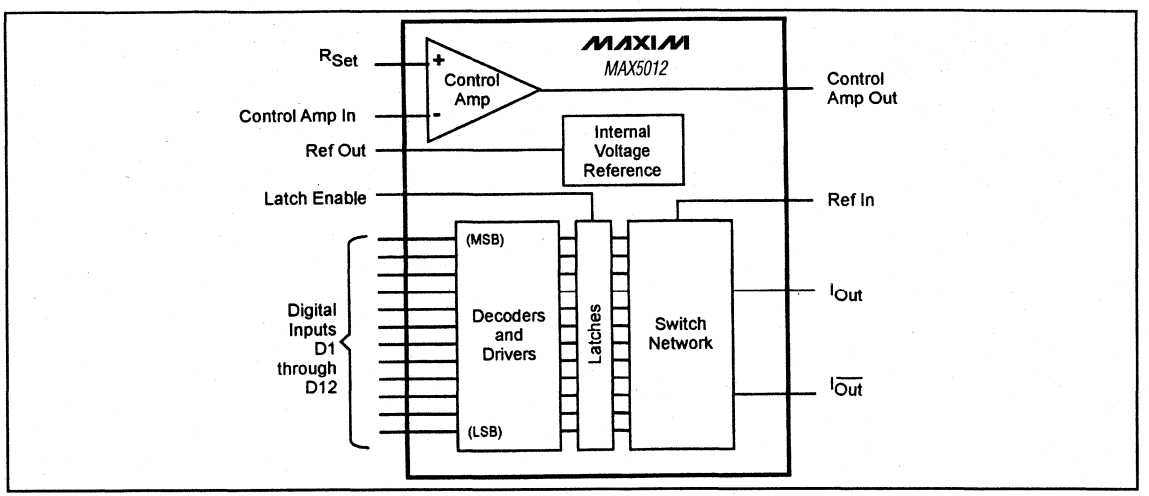
Test and Measurement Instrumentation

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5012AEPI	-40°C to +85°C	28 Plastic DIP
MAX5012BEPI	-40°C to +85°C	28 Plastic DIP
MAX5012AEQI	-40°C to +85°C	28 PLCC
MAX5012BEQI	-40°C to +85°C	28 PLCC

Pin Configurations appear at end of data sheet.

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

12-Bit, 100Msps ECL DAC

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- Negative Supply Voltage (V_{EE}) ..... -7V
- A/D Ground Voltage Differential 0.5V

Input Voltages
- Digital Input Voltage (D1–D12, Latch Enable) ..... 0V to V_{EE}
- Control Amp Input Voltage Range ..... 0V to -4V
- Reference Input Voltage Range (V_{REF}) ..... -3.7V to V_{EE}

Output Currents
- Internal-Reference Output Current 500µA
- Control-Amplifier Output Current ..... ±2.5mA

Continuous Power Dissipation
- Plastic DIP (derate 14.29mW/°C above +70°C) 1.14W
- PLCC (derate 10.53mW/°C above +70°C) 842mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C
Storage Temperature Range ..... -65 to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_{SET} = 7.5kΩ, CONTROL AMP IN = REF OUT, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX5012A MIN	MAX5012A TYP	MAX5012A MAX	MAX5012B MIN	MAX5012B TYP	MAX5012B MAX	UNITS
DC PERFORMANCE									
Resolution				12			12		Bits
Differential Nonlinearity		I		±0.5	±0.75		±1.0	±1.25	LSB
	Max at full temperature	VI			±1.5			±2.0	
Integral Nonlinearity	Best fit	I		±0.75	±1.0		±1.0	±1.5	LSB
	Max at full temperature	VI			±1.75			±2.0	
Output Capacitance	T_A = +25°C	V		10			10		pF
Gain Error (Note 1)	T_A = +25°C	I		1.0	5.0		1.0	5.0	% F.S.
	Full temperature	VI			8.0			8.0	
Gain-Error Tempco	Full temperature	V		150			150		ppm/°C
Zero-Scale Offset Error	T_A = +25°C	I		0.5	2.5		0.5	2.5	µA
	Full temperature	VI			5.0			5.0	
Offset Drift Coefficient	Full temperature	V		0.01			0.01		µA/°C
Output Compliance Voltage	T_A = +25°C	IV	-1.2		2.0	-1.2		2.0	V
Equivalent Output Resistance	T_A = +25°C	IV	0.8	1.0	1.2	0.8	1.0	1.2	kΩ
DYNAMIC PERFORMANCE									
Conversion Rate	T_A = +25°C	IV	100			100			Msps
Settling Time (t_{ST}) (Note 2)	T_A = +25°C	V		13			13		ns
Output Propagation Delay (t_D) (Note 3)	T_A = +25°C	V		1			1		ns
Glitch Energy (Note 4)	T_A = +25°C	V		15			15		pV-s
Full-Scale Output Current (Note 5)	T_A = +25°C	V		20.48			20.48		mA
Spurious-Free Dynamic Range	T_A = +25°C								
1.23MHz; 10Msps	2MHz span	V		70			70		dBc
5.055MHz; 20Msps				68			68		
10.1MHz; 50Msps				68			68		
16MHz; 40Msps	10MHz span			68			68		
Rise/Fall Time	R_L = 50Ω	V		2			2		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{EE} = -5.2V, R_{SET} = 7.5kΩ, CONTROL AMP IN = REF OUT, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETERS	CONDITIONS	TEST LEVEL	MAX5012A MIN	MAX5012A TYP	MAX5012A MAX	MAX5012B MIN	MAX5012B TYP	MAX5012B MAX	UNITS
POWER-SUPPLY REQUIREMENTS									
Negative Supply Voltage		IV	-5.46	-5.2	-4.94	-5.46	-5.2	-4.94	V
Negative Supply Current (-5.2V)	T_A = +25°C	I		115	140		115	140	mA
	Full temperature	VI			148			148	
Nominal Power Dissipation		V		600			600		mW
Power-Supply Rejection Ratio	±5% of V_{EE}, external reference, T_A = +25°C	I		30	100		30	100	µA/V
VOLTAGE INPUT AND CONTROL									
Reference Input Impedance	T_A = +25°C	V		3			3		kΩ
Reference Multiplying Bandwidth	T_A = +25°C	V		40			40		MHz
Internal Reference Voltage		VI	-1.15	-1.20	-1.25	-1.15	-1.20	-1.25	V
Internal Reference Voltage Drift		V		50			50		ppm/°C
Amplifier Input Impedance	T_A = +25°C	V		3			3		MΩ
Amplifier Input Bandwidth	T_A = +25°C	V		1			1		MHz
DIGITAL INPUTS									
Logic 1 Voltage	Full temperature	VI	-1.0	-0.8		-1.0	-0.8		V
Logic 0 Voltage	Full temperature	VI	-1.7	-1.5		-1.7	-1.5		V
Logic 1 Current	Full temperature	VI			20			20	µA
Logic 0 Current	Full temperature	VI			10			10	µA
Input Capacitance	T_A = +25°C	V		3			3		pF
Input Setup Time (t_S)	T_A = +25°C	IV	3	2		3	2		ns
	Full temperature	IV	3.5			3.5			ns
Input Hold Time (t_H)	T_A = +25°C	IV	0.5	0		0.5	0		ns
	Full temperature	IV	0.5			0.5			ns
Latch Pulse Width (t_{PWL}, t_{PWH})	T_A = +25°C	IV	5.0	4.0		5.0	4.0		ns

Note 1: Gain is measured as a ratio of the full-scale current to I_{SET}. The ratio is nominally 128.
Note 2: Measured as voltage at mid-scale transition to ±0.024%; R_L = 50Ω.
Note 3: Measured from the rising edge of Latch Enable to where the output signal has left a 1LSB error band.
Note 4: Glitch is measured as the largest single transient.

Note 5: Calculated using $I_{FS} = 128 \times \left(\frac{\text{Control Amp In}}{R_{SET}}\right)$

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any black section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

12-Bit, 100Msps ECL DAC

Pin Description

PIN	NAME	FUNCTION
1–10	D2–D11	Digital Input Bits 2–11
11	D12 (LSB)	Digital Input Bit 12 (LSB)
12, 21	Digital V_{EE}	Digital Negative Supply (-5.2V)
13	Analog Return	Analog Return Ground
14	I_{OUT}	Analog Current Output
15, 25	Analog V_{EE}	Analog Negative Supply (-5.2V)
16	$\overline{I_{OUT}}$	Complementary Analog Current Output
17	Ref In	Voltage Reference Input
18	Control Amp Out	Internal Control Amplifier Output. Control Amp Out is normally connected to Ref In.
19	Control Amp In	Internal Control Amplifier Input. Control Amp In is normally connected to Ref Out (if not connected to external reference).
20	Ref Out	Internal Voltage Reference Output. Ref Out is normally connected to Control Amp In.
22	Ref GND	Ground Return for Internal Voltage Reference and Amplifier
23	N.C.	No Connection. Not internally connected.
24	R_{SET}*	Connection for External Resistance Reference. R_{SET} is used with the internal amplifier (nominally 7.5kΩ).
26	Latch Enable	Latch Control Line
27	DGND	Digital Ground Return
28	D1 (MSB)	Digital Input Bit 1 (MSB)

**Full-Scale Current Out = 128 (Control Amp In/R_{SET})*

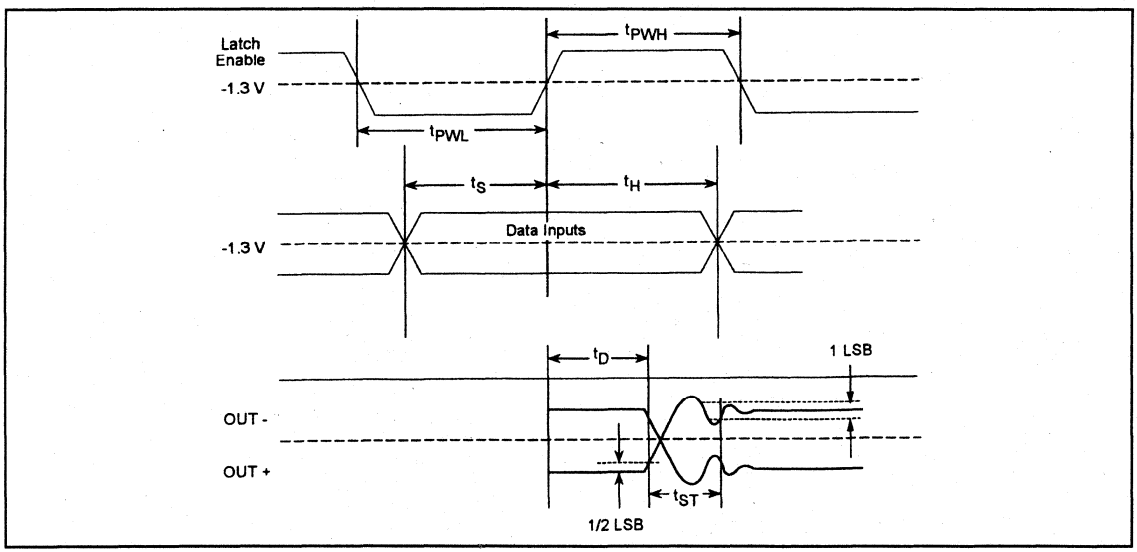


Figure 1. Timing Diagram

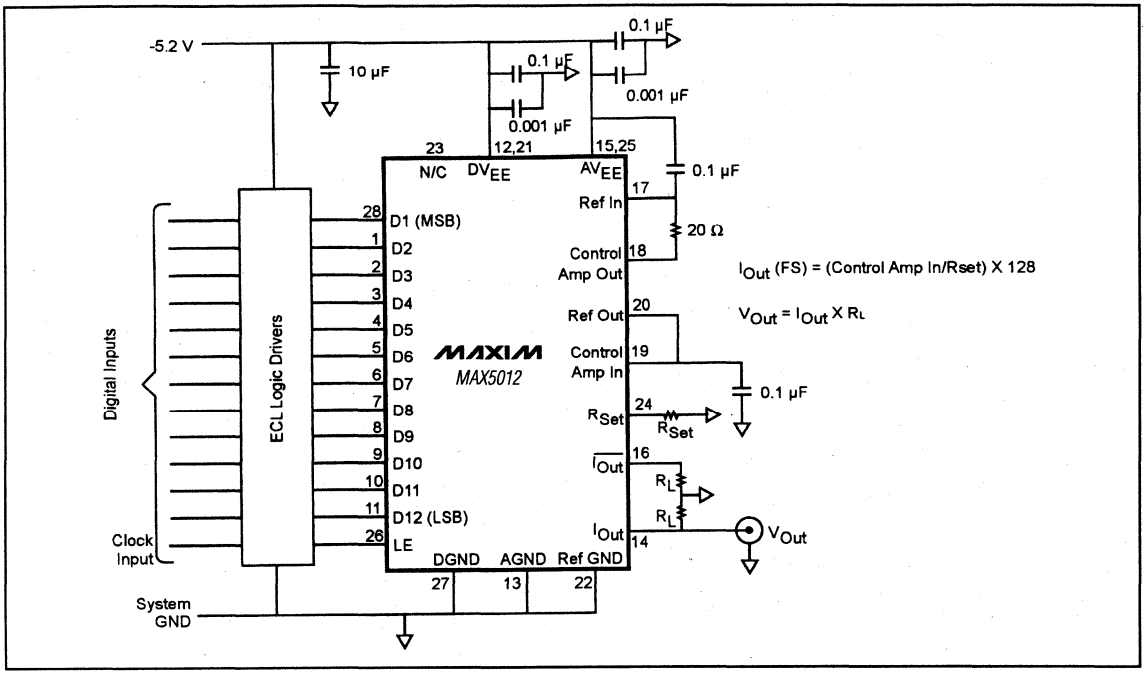
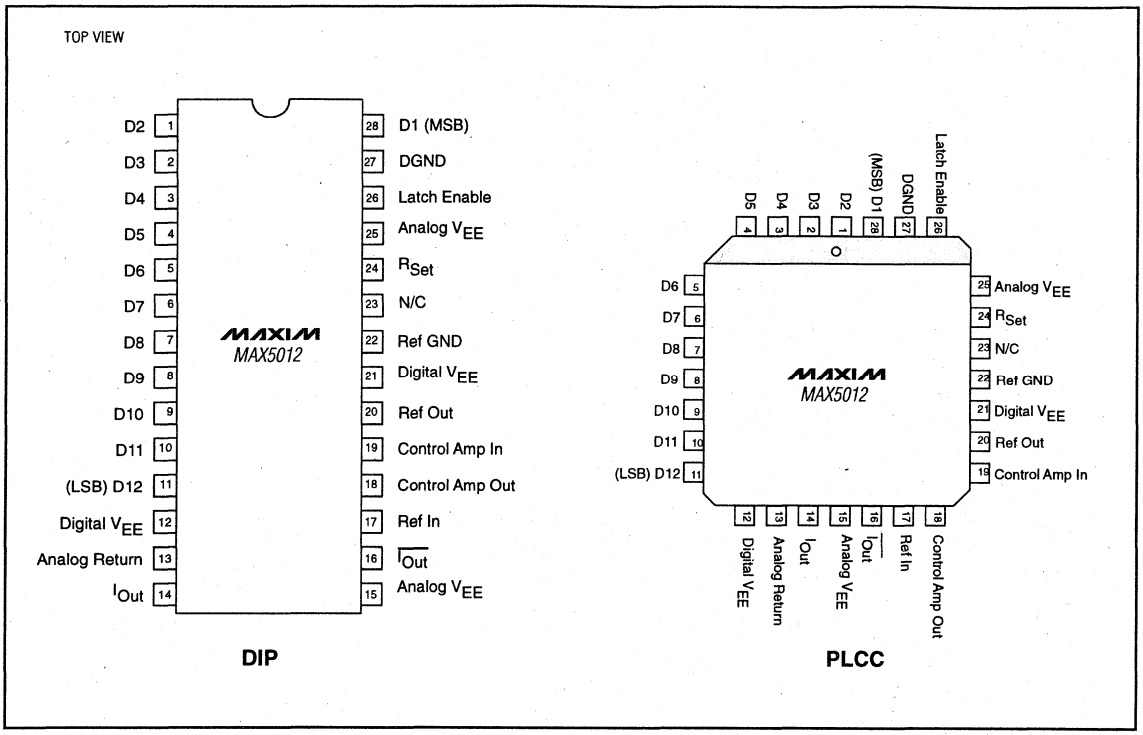


Figure 2. Typical Interface Circuit

12-Bit, 100Msps ECL DAC

Pin Configurations



19-1272; Rev 0; 8/97

MAXIM

12-Bit, 100Msps TTL DAC

General Description

The MAX5013 is a 12-bit, 100Msps digital-to-analog converter (DAC) designed for digital modulation, direct digital synthesis, high-resolution imaging, and arbitrary-waveform-generation applications. This device is pin-for-pin compatible with the AD9713 with significantly improved settling time and glitch-energy performance.

The MAX5013 is a TTL-compatible device. It features a fast 13ns settling time and low 15pV-s glitch impulse energy, which results in excellent spurious-free dynamic-range characteristics.

The MAX5013 is available in a 28-pin plastic DIP or PLCC package, in the -40°C to +85°C extended-industrial temperature range.

Features

- ♦ **12-Bit, 100Msps DAC**
- ♦ **TTL-Compatible Inputs**
- ♦ **Low Power: 640mW**
- ♦ **1/2LSB DNL**
- ♦ **40MHz Multiplying Bandwidth**
- ♦ **Extended-Industrial Temperature Range**
- ♦ **Superior Performance over AD9713:**
  Improved Settling Time: 13ns
  Improved Glitch Energy: 15pV-s
  Master/Slave Latches

Applications

Fast-Frequency-Hopping Spread-Spectrum Radios

Direct-Sequence Spread Spectrum Radios

Digital RF/IF Modulation

Microwave and Satellite Modems

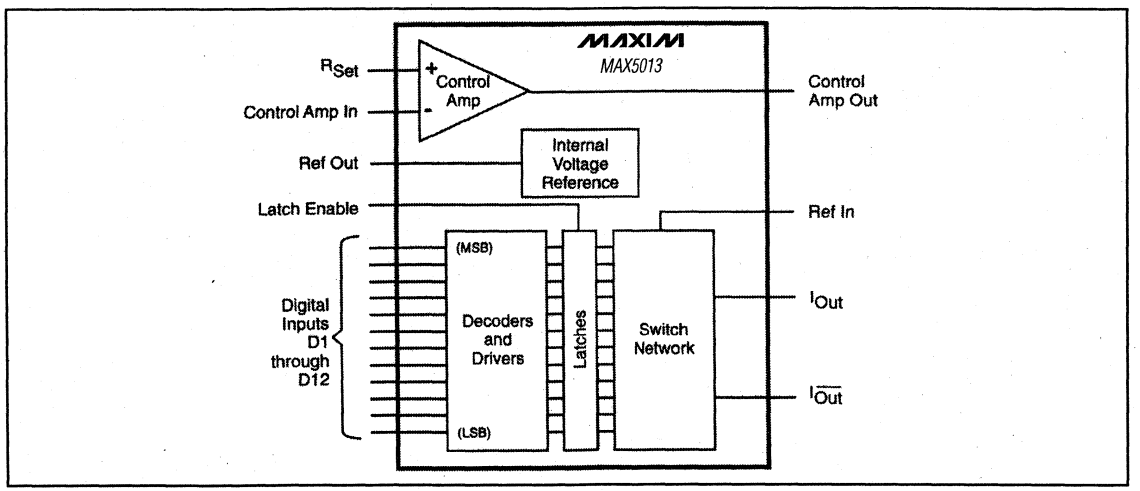
Test and Measurement Instrumentation

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5013AEPI	-40°C to +85°C	28 Plastic DIP
MAX5013BEPI	-40°C to +85°C	28 Plastic DIP
MAX5013AEQI	-40°C to +85°C	28 PLCC
MAX5013BEQI	-40°C to +85°C	28 PLCC

Pin Configurations appear at end of data sheet.

Functional Diagram



For the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

12-Bit, 100Msps TTL DAC

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- Positive Supply Voltage (V_{CC}) ..... +7V
- Negative Supply Voltage (V_{EE}) ..... -7V
- A/D Ground Voltage Differential 0.5V

Input Voltages
- Digital Input Voltage (D1–D12, Latch Enable) ..... 0V to V_{CC}
- Control Amp Input Voltage Range ..... 0V to -4V
- Reference Input Voltage Range (V_{REF}) ..... -3.7V to V_{EE}

Output Currents
- Internal-Reference Output Current 500µA
- Control-Amplifier Output Current ..... ±2.5mA

Continuous Power Dissipation
- Plastic DIP (derate 14.29mW/°C above +70°C) 1.14W
- PLCC (derate 10.53mW/°C above +70°C) 842mW

Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Lead Temperature (soldering, 10sec) ..... +300°C
Storage Temperature Range ..... -65°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5.0V, V_{EE} = -5.2V, R_{SET} = 7.5kΩ, Control Amp In = Ref Out, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	TEST LEVEL	MAX5013A MIN	MAX5013A TYP	MAX5013A MAX	MAX5013B MIN	MAX5013B TYP	MAX5013B MAX	UNITS
DC PERFORMANCE									
Resolution				12			12		Bits
Differential Nonlinearity		I		±0.5	±0.75		±1.0	±1.25	LSB
	Max at full temperature	VI			±1.5			±20	
Integral Nonlinearity	Best fit	I		±0.75	±1.0		±1.0	±1.5	LSB
	Max at full temperature	VI			±1.75			±2.0	
Output Capacitance	T_A = +25°C	V		10			10		pF
Gain Error (Note 1)	T_A = +25°C	I		1.0	5.0		1.0	5.0	% F.S.
	Full temperature	VI			8.0			8.0	
Gain-Error Tempco	Full temperature	V		150			150		ppm/°C
Zero-Scale Offset Error	T_A = +25°C	I		0.5	2.5		0.5	2.5	µA
	Full temperature	VI			5.0			5.0	
Offset-Drift Coefficient	Full temperature	V		0.01			0.01		µA/°C
Output Compliance Voltage	T_A = +25°C	IV	-1.2		2.0	-1.2		2.0	V
Equivalent Output Resistance	T_A = +25°C	IV	0.8	1.0	1.2	0.8	1.0	1.2	kΩ
DYNAMIC PERFORMANCE									
Conversion Rate	T_A = +25°C	IV	100			100			Msps
Settling Time (t_{ST}) (Note 2)	T_A = +25°C	V		13			13		ns
Output Propagation Delay (t_D) (Note 3)	T_A = +25°C	V		2			2		ns
Glitch Energy (Note 4)	T_A = +25°C	V		15			15		pV-s
Full-Scale Output Current (Note 5)	T_A = +25°C	V		20.48			20.48		mA
Spurious-Free Dynamic Range	T_A = +25°C								
1.23MHz; 10Msps	2MHz span	V		70			70		dBc
5.055MHz; 20Msps				68			68		
10.1MHz; 50Msps				68			68		
16MHz; 40Msps	10MHz span			68			68		
Rise/Fall Time	R_L = 50Ω	V		2			2		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5.0V, V_{EE} = -5.2V, R_{SET} = 7.5kΩ, Control Amp In = Ref Out, V_{OUT} = 0V, T_A = T_{MIN} - T_{MAX}, unless otherwise noted.)

PARAMETERS	CONDITIONS	TEST LEVEL	MAX5013A			MAX5013B			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS									
Positive Supply Voltage		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
Negative Supply Voltage		IV	-5.46	-5.2	-4.94	-5.46	-5.2	-4.94	
Positive Supply Current (+5.0V)	T_A = +25°C	I		8	14		8	14	mA
	Full temperature	VI			16			16	
Negative Supply Current (-5.2V)	T_A = +25°C	I		115	140		115	140	mA
	Full temperature	VI			148			148	
Nominal Power Dissipation		V		640			640		mW
Power-Supply Rejection Ratio	±5% of V_{EE} and V_{CC}, external reference, T_A = +25°C	I		30	100		30	100	µA/V
VOLTAGE INPUT AND CONTROL									
Reference Input Impedance	T_A = +25°C	V		3			3		kΩ
Reference Multiplying Bandwidth	T_A = +25°C	V		40			40		MHz
Internal Reference Voltage		VI	-1.15	-1.20	-1.25	-1.15	-1.20	-1.25	V
Internal Reference Voltage Drift	Full temperature	V		50			50		ppm/°C
Amplifier Input Impedance	T_A = +25°C	V		3			3		MΩ
Amplifier Input Bandwidth	T_A = +25°C	V		1			1		MHz
DIGITAL INPUTS									
Logic 1 Voltage	Full temperature	VI	2.0			2.0			V
Logic 0 Voltage	Full temperature	VI			0.8			0.8	V
Logic 1 Current	Full temperature	VI			20			20	µA
Logic 0 Current	Full temperature	VI			600			600	µA
Input Capacitance	T_A = +25°C	V		3			3		pF
Input Setup Time (t_S)	T_A = +25°C	IV	3	2		3	2		ns
	Full temperature	IV	3.5			3.5			
Input Hold Time (t_H)	T_A = +25°C	IV	0.5	0		0.5	0		ns
	Full temperature	IV	0.5			0.5			
Latch Pulse Width (t_{PWL}, t_{PWH})	T_A = +25°C	IV	5.0	4.0		5.0	4.0		ns

Note 1: Gain is measured as a ratio of the full-scale current to I_{SET}. The ratio is nominally 128.
Note 2: Measured as voltage at mid-scale transition to ±0.024%; R_L = 50Ω.
Note 3: Measured from the rising edge of Latch Enable to where the output signal has left a 1LSB error band.
Note 4: Glitch is measured as the largest single transient.

Note 5: Calculated using $I_{FS} = 128 \times \left(\frac{\text{Control Amp In}}{R_{SET}}\right)$

12-Bit, 100Msps TTL DAC

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any black section in the data column indicates that the specification is not tested at the specified condition.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

PIN	NAME	FUNCTION
1–10	D2–D11	Digital Input Bits 2–11
11	D12 (LSB)	Digital Input Bit 12 (LSB)
12, 21	Digital V_{EE}	Digital Negative Supply (-5.2V)
13	Analog Return	Analog Return Ground
14	I_{OUT}	Analog Current Output
15, 25	Analog V_{EE}	Analog Negative Supply (-5.2V)
16	$\overline{I_{OUT}}$	Complementary Analog Current Output
17	Ref In	Voltage Reference Input
18	Control Amp Out	Output of Internal Control Amplifier. Control Amp Out is normally connected to Ref In.
19	Control Amp In	Normally connected to Ref Out if not connected to external reference
20	Ref Out	Internal Voltage Reference Output. Ref Out is normally connected to Control Amp In.
22	Ref GND	Ground return for internal voltage reference and amplifier
23	Digital V_{CC}	Digital Positive Supply (+5.0V)
24	R_{SET}*	Connection for external resistance reference when using internal amplifier (nominally 7.5kΩ).
26	Latch Enable	Latch-Control Line
27	DGND	Digital Ground Return
28	D1 (MSB)	Digital Input Bit 1 (MSB)

**Full-Scale Current Out = 128 (Control Amp In / R_{SET}).*

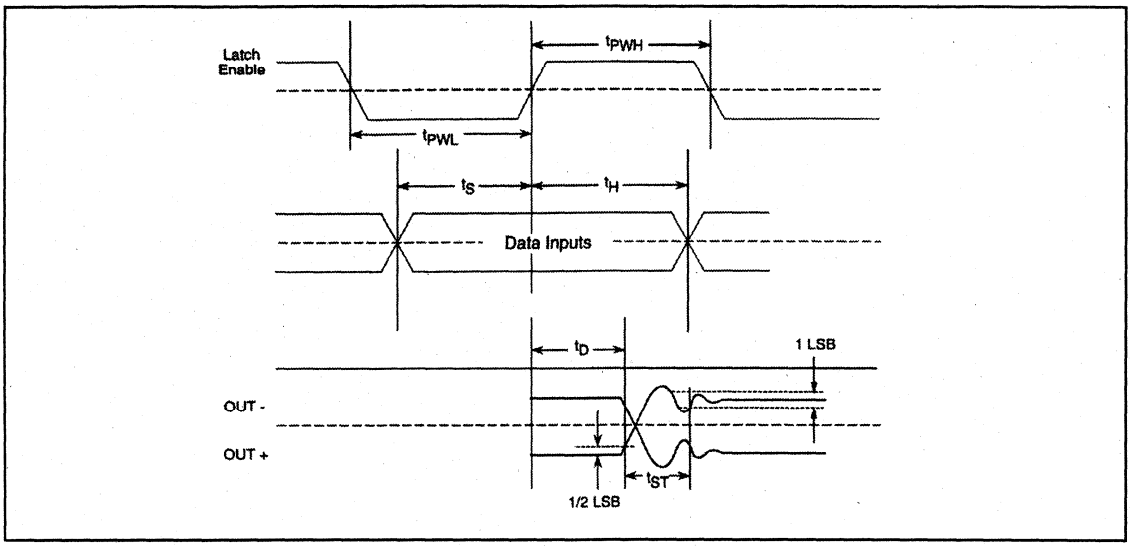


Figure 1. Timing Diagram

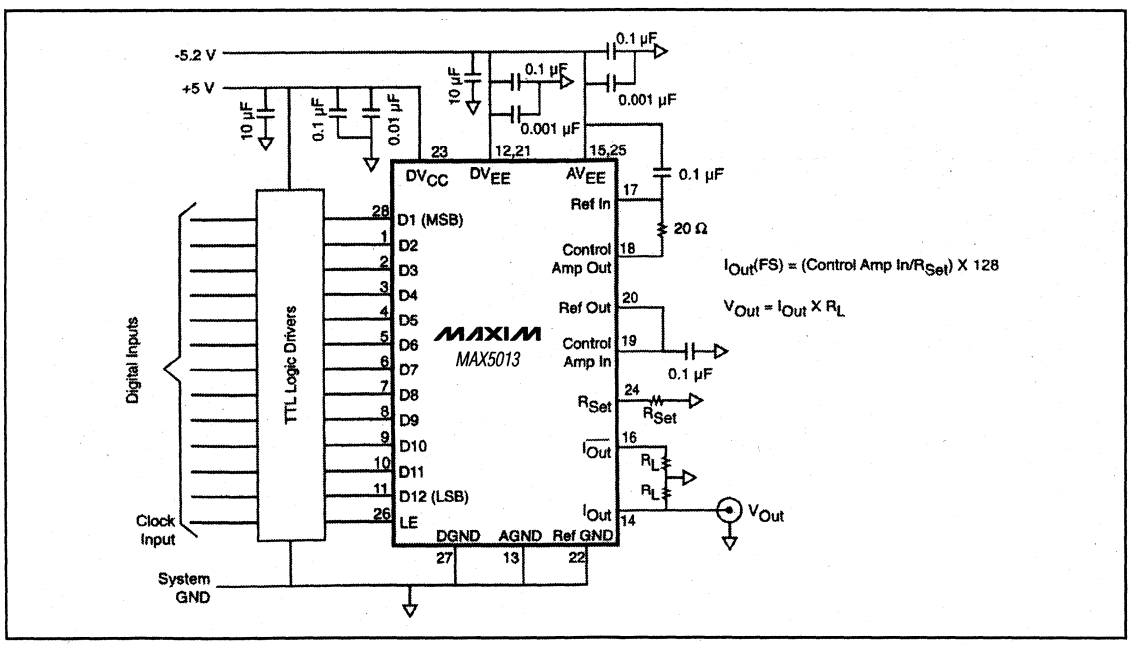


Figure 2. Typical Interface Circuit

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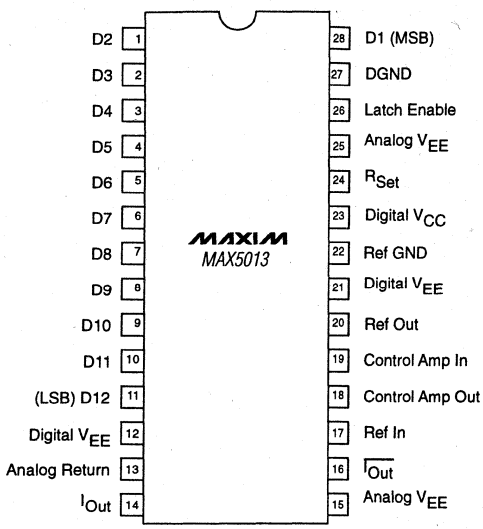
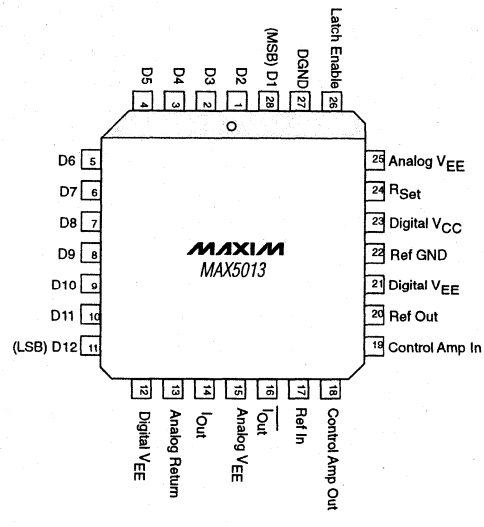
12-Bit, 100Msps TTL DAC

Pin Configurations



DIP



PLCC

19-1204; Rev 0; 3/97

MAXIM

8-Bit, High-Speed DAC

General Description

The MAX5018 is a monolithic, 8-bit digital-to-analog converter (DAC) capable of accepting video data at 165Msps or 275Msps. Complete with video controls (sync, blank, reference white (force high), and bright), the MAX5018 directly drives doubly terminated 50Ω or 75Ω loads to standard composite video levels. Standard setup level is 7.5IRE. The MAX5018 is pin compatible with the HDAC10180 and the TDC1018, with improved performance. The MAX5018 contains data and control input registers, video control logic, reference buffer, and current switches.

Two performance grades of the MAX5018 are available. Both are packaged in a 24-pin PDIP in the -20°C to +85°C industrial temperature range.

Applications

High-Resolution Color or Monochrome Raster Graphics Displays to 1500 x 1800 Pixels

Medical Electronics: CAT, PET, and MRI Displays

CAD/CAE Workstations

Solids Modeling

General-Purpose, High-Speed Digital-to-Analog Conversion

Digital Synthesizers

Automated Test Equipment

Digital Transmitters/Modulators

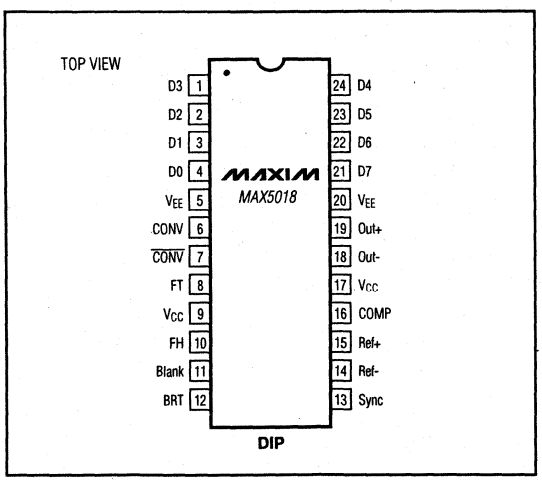
Features

- ♦ **275Msps Conversion Rate (MAX5018A)**
  165Msps Conversion Rate (MAX5018B)
- ♦ **TDC1018 and HDAC10180 Compatible with Improved Performance**
- ♦ **RS-343-A Compatible**
- ♦ **Complete Video Controls: Sync, Blank, Bright, and Reference White (force high)**
- ♦ **ECL Compatible**
- ♦ **Single Power Supply**
- ♦ **Registered Data and Video Controls**
- ♦ **Differential Current Outputs**
- ♦ **ESD-Protected Data and Control Inputs**

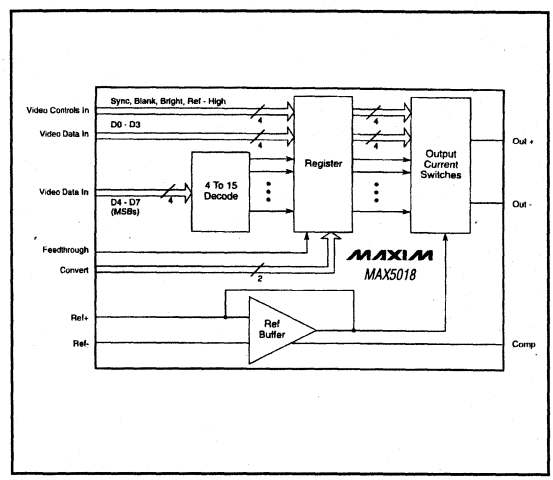
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5018AIPG	-20°C to +85°C	24 Plastic DIP
MAX5018BIPG	-20°C to +85°C	24 Plastic DIP

Pin Configuration



Functional Diagram



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For small orders, phone 408-737-7600 ext. 3468.

8-Bit, High-Speed DAC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{EE} (measured to V_{CC}) ..... -7.0V to 0.5V
Input Voltages
CONV, Data, and Controls (measured to V_{CC}) ..... V_{EE} to 0.5V
Ref+ (measured to V_{CC}) ..... V_{EE} to 0.5V
Ref- (measured to V_{CC}) ..... V_{EE} to 0.5V

Operating Temperature Ranges
Ambient ..... -20°C to +85°C
Junction ..... +175°C
Lead Temperature (soldering, 10sec) ..... +300°C
Storage Temperature Range ..... -60°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = ground, V_{EE} = -5.2V ±0.3V, C_C = 0pF, I_{SET} = 1.105mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Integral Linearity Error	ILE	1.0mA < I_{SET} < 1.3mA	VI	-0.37		0.37	% Full Scale
				-0.95		0.95	LSB
Differential Linearity Error	DLE	1.0mA < I_{SET} < 1.3mA	VI	-0.2		0.2	% Full Scale
				-0.5		0.5	LSB
Gain Error			VI	-6.5		6.5	% Full Scale
Gain-Error Tempco			V		150		ppm/°C
Input Capacitance, Ref+, Ref-	C_{REF}		V		5		pF
Compliance Voltage, Positive Output			VI	-1.2		1.5	V
Compliance Voltage, Negative Output			VI	-1.2		1.5	V
Equivalent Output Resistance	R_{OUT}		VI	20			kΩ
Output Capacitance	C_{OUT}		V		12		pF
Maximum Current, Positive Output	$IO+_{(MAX)}$		IV	45			mA
Maximum Current, Negative Output	$IO-_{(MAX)}$		IV	-45			mA
Output Offset Current	I_{OS}		VI		0.05	0.5	LSB
Input Voltage, Logic High	V_{IH}		VI	-1.0			V
Input Voltage, Logic Low	V_{IL}		VI			-1.5	V
Convert Voltage, Common-Mode Range			IV	-0.5		-2.5	V
Convert Voltage, Differential			IV	0.4		1.2	V
Input Current, Logic Low, Data and Controls	I_{IL}		VI		35	120	µA
Input Current, Logic High, Data and Controls	I_{IH}		VI		40	120	µA
Input Current, Convert	I_{CONV}		VI		2	60	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = ground, V_{EE} = -5.2V ±0.3V, C_C = 0pF, I_{SET} = 1.105mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Input Capacitance, Data and Controls	C_{IN}		V		3		pF
Power-Supply Sensitivity			VI	-120	20	120	µA/V
Supply Current	I_{EE}		VI		155	220	mA

AC ELECTRICAL CHARACTERISTICS

(R_L = 37.5Ω, C_L = 5pF, I_{SET} = 1.105mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Maximum Conversion Rate		MAX5018B	III	165			Msps
		MAX5018A	III	275			
Rise Time	t_R	10% to 90% G.S., T_A = T_{MIN} to T_{MAX}	III			1.6	ns
			IV			2.0	
		10% to 90% G.S., R_L = 25Ω	V		1.0		
Current Settling Time, Clocked Mode	t_{SI}	To 0.2% G.S.	V		7.0		ns
		To 0.8% G.S.	V		5.5		
		To 0.2% G.S., R_L = 25Ω	V		4.5		
Clock to Output Delay, Clocked Mode	t_{DSC}	T_A = T_{MIN} to T_{MAX}	III		2.2	4.0	ns
			IV			4.5	
Data to Output Delay, Transparent Mode	t_{DST}	T_A = T_{MIN} to T_{MAX}	III		3.2	6.0	ns
			IV			6.0	
Convert Pulse Width, (low or high)	t_{PWL}, t_{PWH}	B Grade	III	3.0			ns
		A Grade	III	1.8			
Glitch Energy		Area = 1/2VT	V		4		pV-s
Reference Bandwidth, -3dB			V		1.0		MHz
Setup Time, Data and Controls	t_S	T_A = +25°C	III	1.0			ns
		T_A = T_{MIN} to T_{MAX}	IV	1.0			
Hold Time, Data and Controls	t_H	T_A = +25°C	III	0.5			ns
		T_A = T_{MIN} to T_{MAX}	IV	0.5			
Slew Rate		20% to 80% G.S., T_A = +25°C	III	390			V/µs
		T_A = T_{MIN} to T_{MAX}	IV	325			
Clock Feedthrough		T_A = T_{MIN} to T_{MAX}	III			-48	dB
			IV			-48	

8-Bit, High-Speed DAC

TEST-LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample tested at the specified temperatures.
III	QA sample tested at only the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for reference only.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	D3, D2, D1	Data Bits 3, 2, and 1
4	D0	Data Bit 0 (LSB)
5, 20	V_{EE}	Negative Supply
6	CONV	Convert Clock Input
7	$\overline{CONV}$	Convert-Clock-Input Complement
8	FT	Register Feedthrough Control
9, 17	V_{CC}	Positive Supply
10	FH	Data Force-High Control
11	Blank	Video Blank Input
12	BRT	Video Bright Input
13	Sync	Video Sync Input
14	Ref-	Reference Current, Negative Input
15	Ref+	Reference Current, Positive Input
16	COMP	Compensation Input
18	Out-	Output Current Negative
19	Out+	Output Current Positive
21	D7	Data Bit 7 (MSB)
22, 23, 24	D6, D5, D4	Data Bits 6, 5, and 4

Detailed Description

The MAX5018 is an ultra-high-speed video digital-to-analog converter (DAC) capable of up to 275Msps conversion rates. This high speed makes the device suitable for driving 1500 x 1800 pixel displays at 70Hz to 90Hz update rates.

The MAX5018 is separated into different conversion-rate categories, as shown in Table 1.

The MAX5018 has ECL logic-level-compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The MAX5018 is segmented so that the input data's four MSBs are separated into a parallel thermometer code. From here, fifteen identical current sinks are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary-weighted current switches.

MSB currents are then summed with the LSBs that contribute one-sixteenth of full-scale to provide the 256 distinct analog output levels.

The video-control inputs drive weighted current sinks, which are added to the output current to produce composite video-output levels. These controls (sync, blank, reference white (force high), and bright) are required in video applications.

A feature that similar video DACs do not have is feedthrough control. The feedthrough pin (FT) allows registered or unregistered operation of the video control and data inputs. In registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions (generally found on unregistered video DACs).

Table 1. The MAX5018 Family and Speed Designations

PART	UPDATE	COMMENTS
MAX5018A	275Msps	Suitable for 1200 x 1500 to 1500 x 1800 displays at 60Hz to 90Hz update rate.
MAX5018B	165Msps	Suitable for 1024 x 1280 to 1200 x 1500 displays at 60Hz to 90Hz update rate.

Applications Information

General

Figure 1 shows a typical application using the MAX5018 in a color-raster circuit. The MAX5018 requires few external components and is extremely easy to use. The MAX5018's very high operating speeds require good circuit layout, supply decoupling, and proper transmission-line design. For best performance, note the following considerations.

Input Considerations

Video-input data and controls can be directly connected to the MAX5018. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk, and reflections. Maxim recommends that stripline or microstrip techniques be used for all ECL interfaces. A convenient and commonly used microstrip impedance is about 130Ω, which is easily terminated using a 330Ω resistor to V_{EE} and a 220Ω resistor to ground. This arrangement gives a Thevenin-equivalent termination of 130Ω to -2V without the need for a -2V supply. Standard single in-line package (SIP) 220/330 resistor networks are available for this purpose.

Figure 2 shows equivalent input circuits.

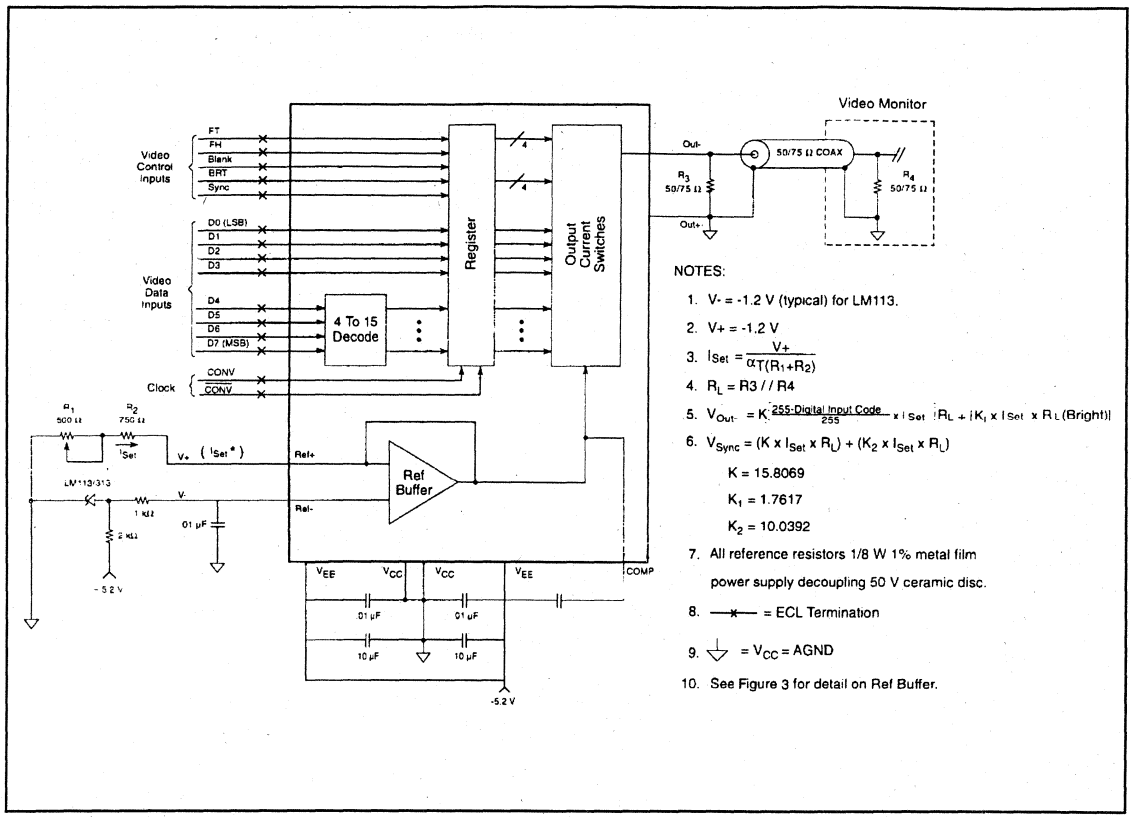
Output Considerations

The analog outputs are designed to directly drive a dual 50Ω or 75Ω load-transmission system as shown in Figure 1. The MAX5018 output source impedances are high-impedance current sinks. The load impedance (R_L) must be 25Ω or 37.5Ω to attain standard RS-343-A video levels. Any deviation from this impedance affects the resulting video output levels proportionally. As with the data interface, it is important that all analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source-termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system.

Power Considerations

The MAX5018 has two analog power-supply pins and operates from a standard -5.2V single supply. Proper supply bypassing augments the MAX5018's inherent supply-noise-rejection characteristics. As shown in Figure 1, each supply pin should be bypassed as close to the device as possible with 0.01µF and 10µF capacitors.

8-Bit, High-Speed DAC



NOTES:

1. V- = -1.2 V (typical) for LM113.
2. V+ = -1.2 V
3. $I_{Set} = \frac{V+}{\alpha T(R_1+R_2)}$
4. $R_L = R3 // R4$
5. $V_{Out-} = K \frac{255\text{-Digital Input Code}}{255} \times I_{Set} \left[R_L + (K_1 \times I_{Set} \times R_L (Bright))\right]$
6. $V_{Sync} = (K \times I_{Set} \times R_L) + (K_2 \times I_{Set} \times R_L)$

   K = 15.8069

   K_1 = 1.7617

   K_2 = 10.0392
7. All reference resistors 1/8 W 1% metal film

   power supply decoupling 50 V ceramic disc.
8. —×— = ECL Termination
9. ⏚ = V_{CC} = AGND
10. See Figure 3 for detail on Ref Buffer.

Figure 1. Typical Interface Circuit

This device also has two analog ground pins (V_{CC}). Tie both ground pins to the analog ground plane. All power and ground pins must be connected in any application. If a +5V power source is required, the V_{CC} ground pins become the positive supply pins, while the V_{EE} supply pins become the ground pins. The relative polarities of the other input and output voltages must be maintained.

Reference Considerations

The MAX5018 has two reference inputs (Ref+ and Ref-). The input pins are connected to the inverting and non-inverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The buffer amplifier's output is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks for better accuracy. (See Figure 3.)

Since the analog output currents are proportional to the digital input data and I_{Set}, full-scale output can be adjusted by varying the reference current. I_{Set} is controlled through the MAX5018's Ref+ input. Figure 1 shows the method and the necessary equations for setting I_{Set}. The MAX5018 uses an external negative-voltage reference. The external reference must be stable to achieve a satisfactory output, and Ref- should be driven through a resistor to minimize offsets caused by bias current. To change the full-scale output, vary the value for I_{Set} with the 500Ω trimmer. A double 50Ω load (25Ω) can be driven if I_{Set} is increased by 50% for doubly terminated 75Ω video applications.

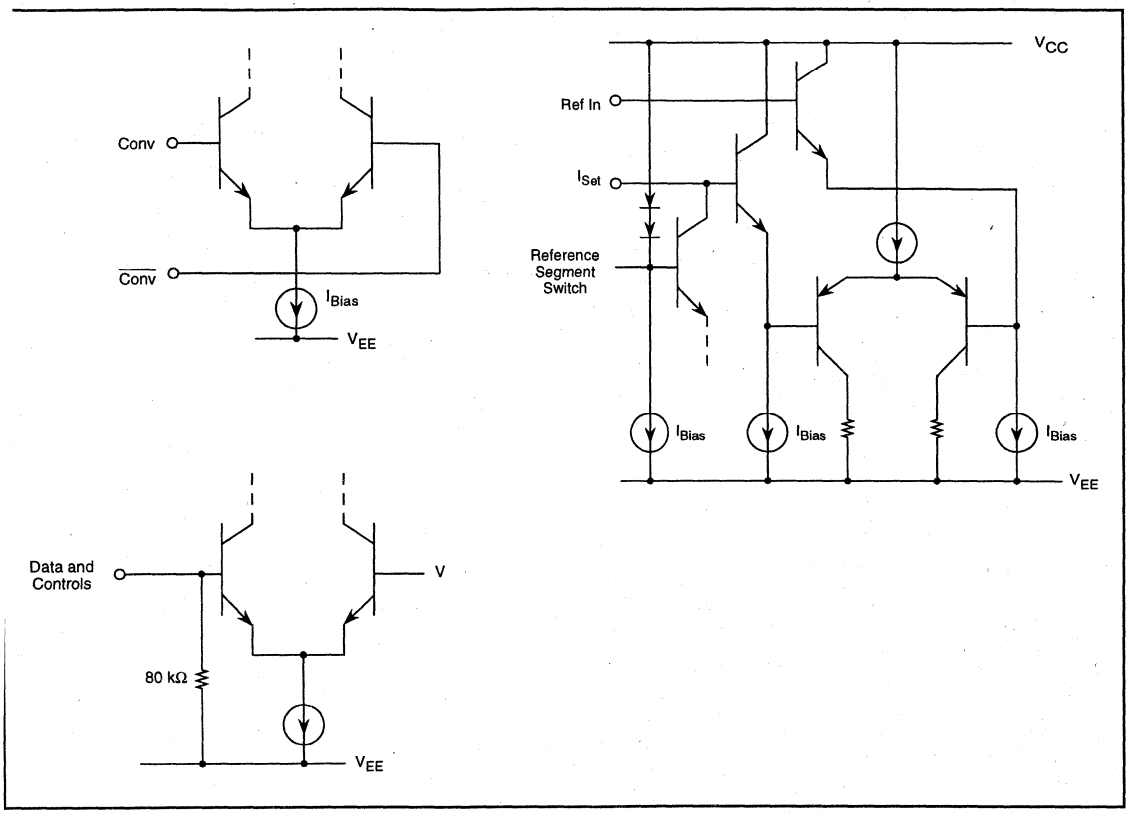


Figure 2. Equivalent Input Circuits—Data, Clock, Controls, and Reference

Compensation

The MAX5018 provides an external compensation input (COMP) for the reference buffer amplifier. To use this pin correctly, connect a capacitor between COMP and V_{EE}, as shown in Figure 1. Keep lead lengths as short as possible. Use a large capacitor (0.01µF) if the reference is to be kept as a constant. The capacitor's value determines the amplifier's bandwidth. If reference modulation is required, smaller capacitance values can be used to achieve up to a 1MHz bandwidth.

Data Inputs and Video Controls

The MAX5018 has standard, single-ended data inputs. The inputs are registered to produce the lowest differential data-propagation delay (skew) to minimize glitching. Also, four video-control inputs generate composite video outputs: sync, blank, bright, and reference white (force high). Feedthrough control is also provided. All of the controls and data inputs are ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This feature is useful if the devices are applied as standard DACs without the need for video controls, or if fewer than eight bits are used.

The MAX5018 is usually configured in synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. With the FT control open (low), each rising edge of the convert clock (CONV) latches decoded data and control values into a D-type internal register. The switched-current

8-Bit, High-Speed DAC

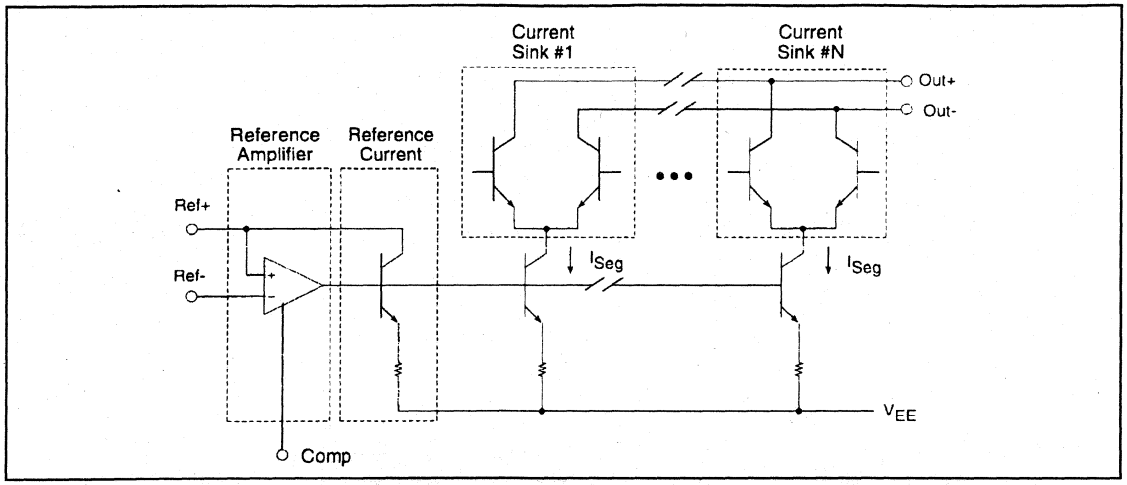


Figure 3. Reference Buffer and DAC Output Circuit

sinks convert the registered data into the appropriate analog output. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and is usually used as a DC control.

To be registered synchronously, control and data inputs must be present at the input pins for a specific setup time (t_S) before and a specific hold time (t_H) after CONV's rising edge. Setup and hold times are not important in asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}), as well as settling time, become the limiting factors (Figure 4).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video-system standards as described in RS-343-A. Table 2 shows the video-control effects on the analog output. Internal logic governs blank, sync, and force high so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 5).

Reference-white, video-level output is provided by force high, which drives the internal digital data to full-scale output (100IRE units). Bright gives an additional 10% of full-scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors, or warning messages. If the devices are used in non-video applications, the video controls can be left open.

Convert Clock

For best performance, the clock should be differentially ECL driven by using CONV and $\overline{CONV}$ (Figure 6). Driving the clock in this manner minimizes clock noise and power-supply/output intermodulation. The clock's rising edge synchronizes the data and control inputs to the MAX5018. Since $\overline{CONV}$ determines the actual switching threshold of CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{CONV}$. This bias voltage sets the converter clock's switching threshold.

Analog Outputs

The MAX5018 has two analog outputs that are high-impedance, complementary current sinks. The outputs vary in proportion to the input data, controls, and reference-current values so that the full-scale output can be changed by setting I_{Set}.

In video applications, the outputs can drive a doubly terminated 50Ω or 75Ω load to standard video levels. In the standard configuration shown in Figure 7, the output voltage is the product of the output current and load impedance and is between 0V and -1.07V. Out- (Figure 5) provides a video output waveform with the Sync pulse bottom at -1.07V. Out+ is inverted with Sync up.

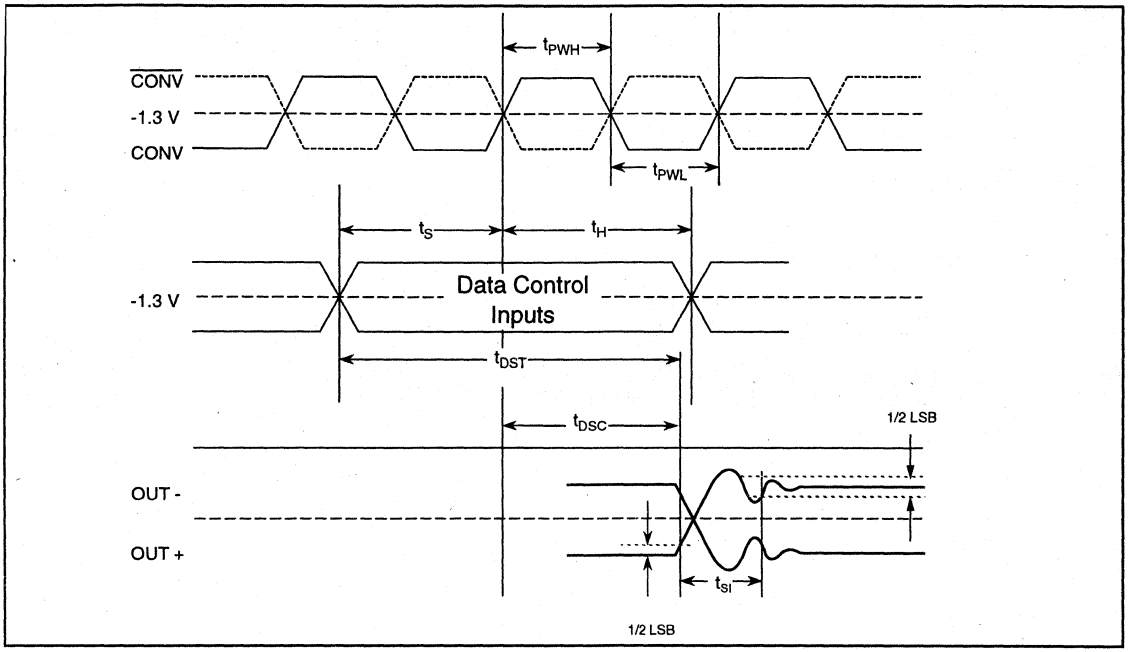


Figure 4. Timing Diagram

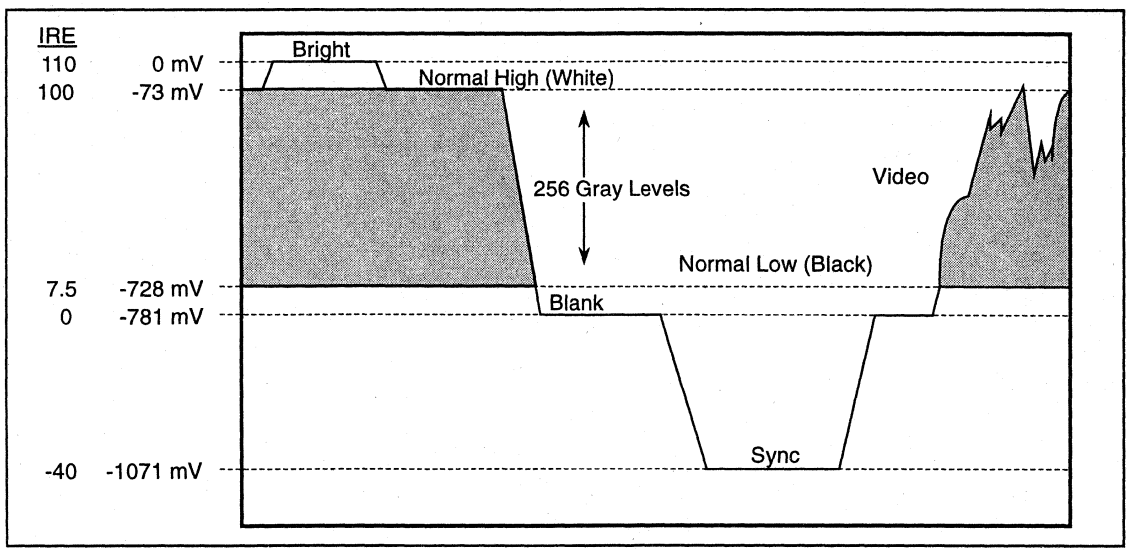


Figure 5. Video-Output Waveform for Standard Load

Table 2. Video-Control Operation (output values for setup: 10IRE, 75Ω standard load)

SYNC	BLANK	REF WHITE	BRIGHT	DATA INPUT	OUT- (mA)	OUT- (V)	OUT- (IRE)	DESCRIPTION
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

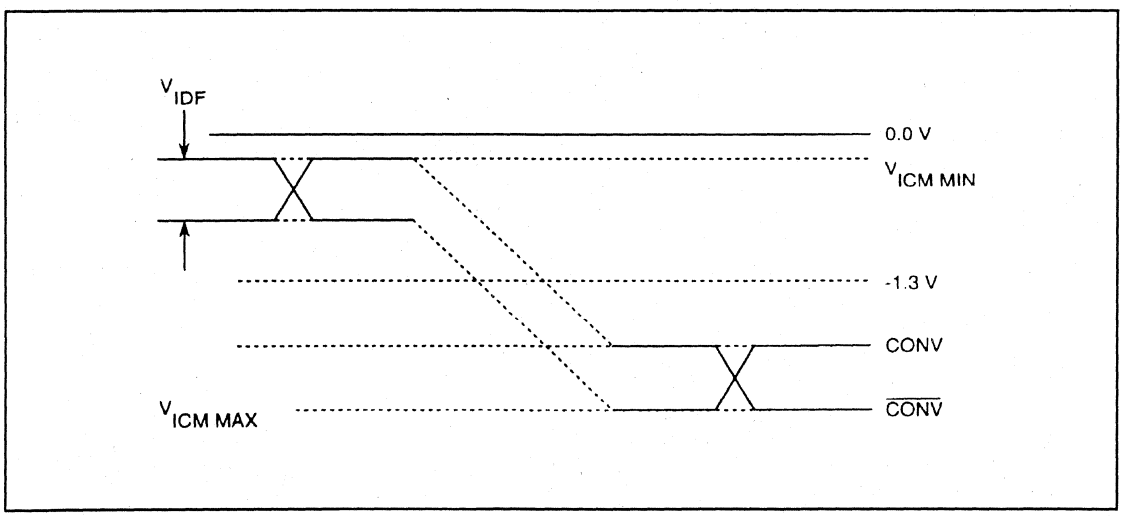


Figure 6. CONV, $\overline{CONV}$ Switching Levels

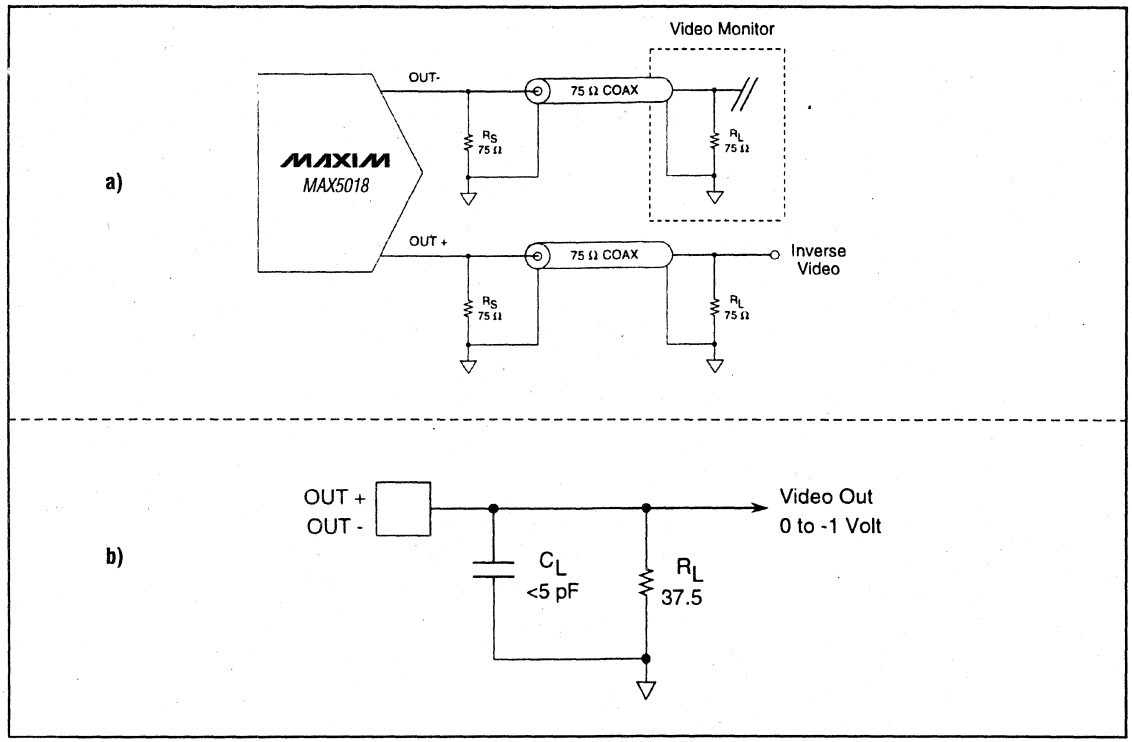


Figure 7. Standard Load (a) and Test Load (b)

19-1205; Rev 1; 5/97

MAXIM

8-Bit, Ultra-High-Speed DAC

General Description

The MAX5140 is a monolithic, 8-bit digital-to-analog converter (DAC) capable of accepting video data at 400Msps. Complete with video controls (sync, blank, reference white (force high), and bright), the MAX5140 directly drives doubly terminated 50Ω or 75Ω loads to standard composite video levels. Standard setup level is 7.5IRE. The MAX5140 includes an internal precision bandgap reference that can drive two other MAX5140s in an RGB graphics system.

The MAX5140 is available in a 24-pin PDIP package in the -20°C to +85°C industrial temperature range.

Applications

Raster Graphics

High-Resolution Color or Monochrome Displays to 2k x 2k Pixels

Medical Electronics: CAT, PET, and MR Imaging Displays

CAD/CAE Workstations

Solids Modeling

General-Purpose, High-Speed Digital-to-Analog Conversion

Digital Synthesizers

Automated Test Equipment

Digital Transmitters/Modulators

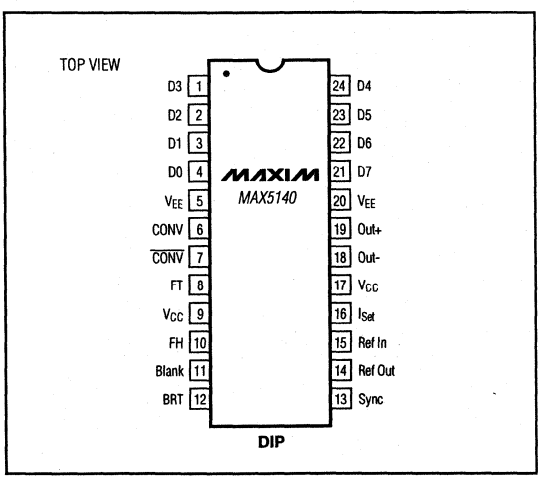
Features

- ♦ **400Msps Nominal Conversion Rate**
- ♦ **RS-343-A Compatible**
- ♦ **Complete Video Controls: Sync, Blank, Bright, and Reference White (force high)**
- ♦ **ECL Compatible**
- ♦ **Single Power Supply**
- ♦ **Registered Data and Video Controls**
- ♦ **Differential Current Outputs**
- ♦ **Stable On-Chip Bandgap Reference**
- ♦ **50Ω and 75Ω Output Drive**
- ♦ **ESD-Protected Data and Control Inputs**

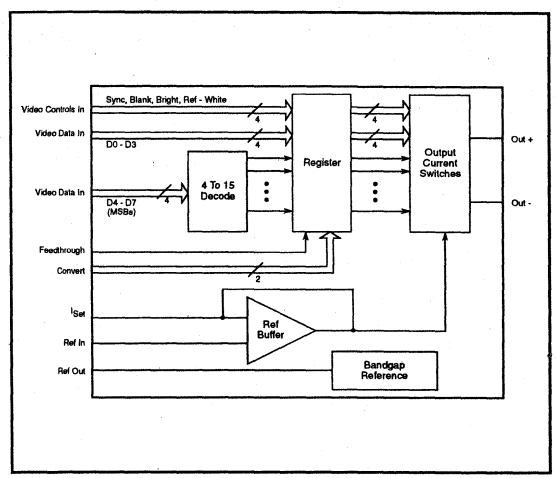
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX5140IPG	-20°C to +85°C	24 Plastic DIP

Pin Configuration



Functional Diagram



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For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

8-Bit, Ultra-High-Speed DAC

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{EE} (measured to V_{CC}) ..... -7.0V to 0.5V
Input Voltages
CONV, Data, and Controls (measured to V_{CC}) ..... V_{EE} to 0.5V
Ref+ (measured to V_{CC}) ..... V_{EE} to 0.5V
Ref- (measured to V_{CC}) ..... V_{EE} to 0.5V

Operating Temperature Ranges
Ambient ..... -20°C to +85°C
Junction ..... +175°C
Lead Temperature (soldering, 10sec) ..... +300°C
Storage Temperature Range ..... -60°C to +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = ground, V_{EE} = -5.2V ±0.3V, C_C = 0pF, I_{SET} = 1.105mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Integral Linearity Error	ILE	1.0mA < I_{SET} < 1.3mA	VI	-0.37		0.37	% Full Scale
				-0.95		0.95	LSB
Differential Linearity Error	DLE	1.0mA < I_{SET} < 1.3mA	VI	-0.2		0.2	% Full Scale
				-0.5		0.5	LSB
Gain Error			VI	-6.5		6.5	% Full Scale
Gain-Error Tempco			V		150		ppm/°C
Bandgap Tempco			V		100		ppm/°C
Input Capacitance, I_{SET}, Ref Out	C_{REF}		V		5		pF
Compliance Voltage, Positive Output			VI	-1.2		1.5	V
Compliance Voltage, Negative Output			VI	-1.2		1.5	V
Equivalent Output Resistance	R_{OUT}		VI	20			kΩ
Output Capacitance	C_{OUT}		V		9		pF
Maximum Current, Positive Output	$I_{O+(MAX)}$		IV	45			mA
Maximum Current, Negative Output	$I_{O-(MAX)}$		IV	-45			mA
Output Offset Current	I_{OS}		VI		0.05	0.5	LSB
Input Voltage, Logic High	V_{IH}		VI	-1.0			V
Input Voltage, Logic Low	V_{IL}		VI			-1.5	V
Convert Voltage, Common-Mode Range			IV	-0.5		-2.5	V
Convert Voltage, Differential			IV	0.4		1.2	V
Input Current, Logic Low, Data and Controls	I_{IL}		VI		35	120	µA
Input Current, Logic High, Data and Controls	I_{IH}		VI		40	120	µA
Input Current, Convert	I_{CONV}		VI		2	60	µA

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = ground, V_{EE} = -5.2V ±0.3V, C_C = 0pF, I_{SET} = 1.105mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Reference Voltage (measured to V_{CC})	V_{REF}		VI	-1.3	-1.2	-1.0	V
Reference Output Current	I_{REF}		VI	-50			µA
Input Capacitance, Data and Controls	C_{IN}		V		3		pF
Power-Supply Sensitivity			VI	-120	20	120	µA/V
Supply Current	I_{EE}		VI		155	220	mA

AC ELECTRICAL CHARACTERISTICS

(R_L = 37.5Ω, C_L = 5pF, I_{SET} = 1.105mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEST LEVEL	MIN	TYP	MAX	UNITS
Maximum Conversion Rate				IV	385	400		Msps
Rise Time	t_R	10% to 90% G.S.		IV			900	ps
			R_L = 25Ω				600	
Current-Settling Time, Clocked Mode	t_{SI}	To 0.2% G.S.		V		4		ns
			R_L = 25Ω			3		
Clock to Output Delay, Clocked Mode	t_{DSC}	T_A = T_{MIN} to T_{MAX}		III		2.2	4	ns
				IV			4.5	
Data to Output Delay, Transparent Mode	t_{DST}	T_A = T_{MIN} to T_{MAX}		III		3.2	6	ns
				IV			6	
Glitch Energy		Area = 1/2VT		V		4		pV-s
Convert Pulse Width	t_{PWH}, t_{PWL}			III	1.3			ns
Reference Bandwidth	-3dB			V		1.25		MHz
Setup Time, Data and Controls	t_S			III	1.0			ns
Hold Time, Data and Controls	t_H			III	0.5			ns
Slew Rate		20% to 80% G.S.		V		700		V/µs
Clock Feedthrough				III			-48	dB

TEST-LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, T_j = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = +25°C, and sample-tested at the specified temperatures.
III	QA sample tested at only the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for reference.
VI	100% production tested at T_A = +25°C. Parameter is guaranteed over specified temperature range.

8-Bit, Ultra-High-Speed DAC

Pin Description

PIN	NAME	FUNCTION
1, 2, 3	D3, D2, D1	Data Bits 3, 2, and 1
4	D0	Data Bit 0 (LSB)
5, 20	V_{EE}	Negative Supply
6	CONV	Convert Clock Input
7	$\overline{CONV}$	Convert-Clock-Input Complement
8	FT	Register Feedthrough Control
9, 17	V_{CC}	Positive Supply
10	FH	Data Force-High Control
11	Blank	Video Blank Input
12	BRT	Video Bright Input
13	Sync	Video Sync Input
14	Ref Out	Reference Output
15	Ref In	Reference Input
16	I_{Set}	Reference Current
18	Out-	Output Current Negative
19	Out+	Output Current Positive
21	D7	Data Bit 7 (MSB)
22, 23, 24	D6, D5, D4	Data Bits 6, 5, and 4

Detailed Description

The MAX5140 is an ultra-high-speed video digital-to-analog converter (DAC) capable of up to 400Msps conversion rates. This high speed makes the device suitable for driving 2048 x 2048 pixel displays at 60Hz to 90Hz update rates.

In addition, the MAX5140 includes an internal bandgap reference, which may be used to drive two other MAX5140s, if desired.

The MAX5140 has ECL logic-level-compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The MAX5140 is segmented so that the input data's four MSBs are separated into a parallel thermometer code. From here, fifteen identical current sinks are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary-weighted current switches.

MSB currents are then summed with the LSBs that contribute one-sixteenth of full-scale to provide the 256 distinct analog output levels.

The video-control inputs drive weighted current sinks, which are added to the output current to produce composite video-output levels. These controls (sync, blank, reference white (force high), and bright) are required in video applications.

A feature that similar video DACs do not have is feedthrough control. The feedthrough pin (FT) allows registered or unregistered operation of the video control and data inputs. In registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions (generally found on unregistered video DACs).

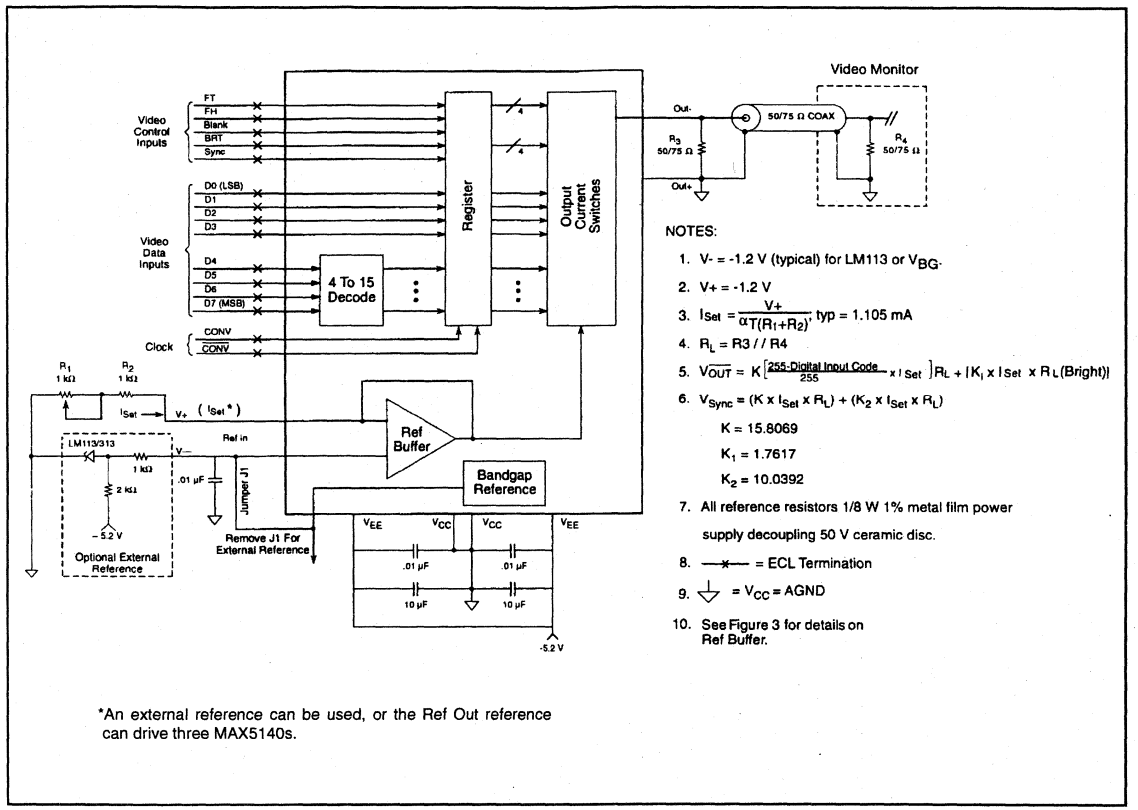


Figure 1. Typical Interface Circuit

Applications Information

General

Figure 1 shows a typical interface circuit using the MAX5140 in a color-raster application. The MAX5140 requires few external components and is extremely easy to use. The MAX5140's ultra-high operating speeds require good circuit layout, supply decoupling, and proper transmission-line design. For best performance, note the following considerations.

Input Considerations

Video-input data and controls can be directly connected to the MAX5140. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk, and reflections. Maxim recommends that stripline or microstrip techniques be used for all ECL interfaces. A convenient and commonly used microstrip impedance is about 130Ω, which is easily terminated using a 330Ω resistor to V_{EE} and a 220Ω resistor to ground. This arrangement gives a Thevenin-equivalent termination of 130Ω to -2V without the need for a -2V supply. Standard single in-line package (SIP) 220/330 resistor networks are available for this purpose.

Figure 2 shows equivalent input circuits.

8-Bit, Ultra-High-Speed DAC

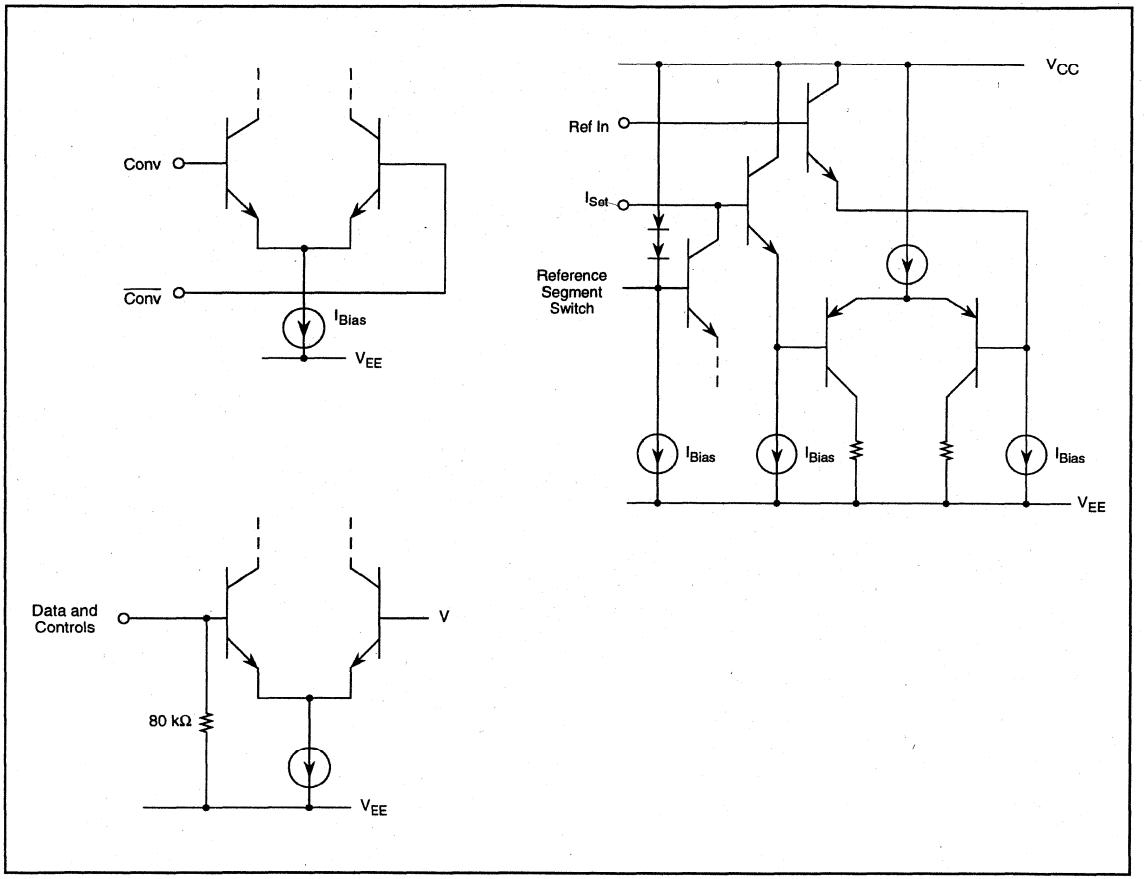


Figure 2. Equivalent Input Circuits—Data, Clock, Controls, and Reference

Output Considerations

The analog outputs are designed to directly drive a doubly terminated 50Ω or 75Ω load-transmission system as shown. The MAX5140 output source impedances are high-impedance current sinks. The load impedance (R_L) must be 25Ω or 37.5Ω to attain standard RS-343-A video levels. Any deviation from this impedance affects the resulting video output levels proportionally. As with the data interface, it is important that all analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source-termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system.

Power Considerations

The MAX5140 has two analog power-supply pins and operates from a standard -5.2V single supply. Proper supply bypassing augments the MAX5140's inherent supply-noise-rejection characteristics. As shown in Figure 1, each supply pin should be bypassed as close to the device as possible with 0.01µF and 10µF capacitors.

This device also has two analog ground pins (V_{CC}). Tie both ground pins to the analog ground plane. All power and ground pins must be connected in any application. If a +5V power source is required, the V_{CC} ground pins become the positive supply pins, while the V_{EE} supply pins become the ground pins. The relative polarities of the other input and output voltages must be maintained.

Reference Considerations

The MAX5140 has two reference inputs (Ref In and I_{Set}) and one reference output (Ref Out). The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The buffer amplifier's output is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 3.)

Since the analog output currents are proportional to the digital input data and I_{Set}, full-scale output can be adjusted by varying the reference current. I_{Set} is controlled through the MAX5140's I_{Set} input. Figure 1 shows the method and the necessary equations for setting I_{Set}. The MAX5140 can use an external negative-voltage reference. The external reference must be stable to achieve a satisfactory output, and Ref In should be driven through a resistor to minimize offsets caused by bias current. To change the full-scale output, vary the value for I_{Set} with the 500Ω to 1kΩ trimmer. A double 50Ω load (25Ω) can be driven if I_{Set} is increased by 50% for doubly terminated 75Ω video applications.

Data Inputs and Video Controls

The MAX5140 has standard, single-ended data inputs. The inputs are registered to produce the lowest differential data-propagation delay (skew) to minimize glitching. Also, four video-control inputs generate composite video outputs: sync, blank, bright, and reference white (force high). Feedthrough control is also provided. All of the controls and data inputs are ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls, or if fewer than eight bits are used.

The MAX5140 is usually configured in synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. With the FT control open (low), each rising edge of the convert clock (CONV) latches decoded data and control values into a D-type internal register. The switched-current sinks convert the registered data into the appropriate analog output. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and is usually used as a DC control.

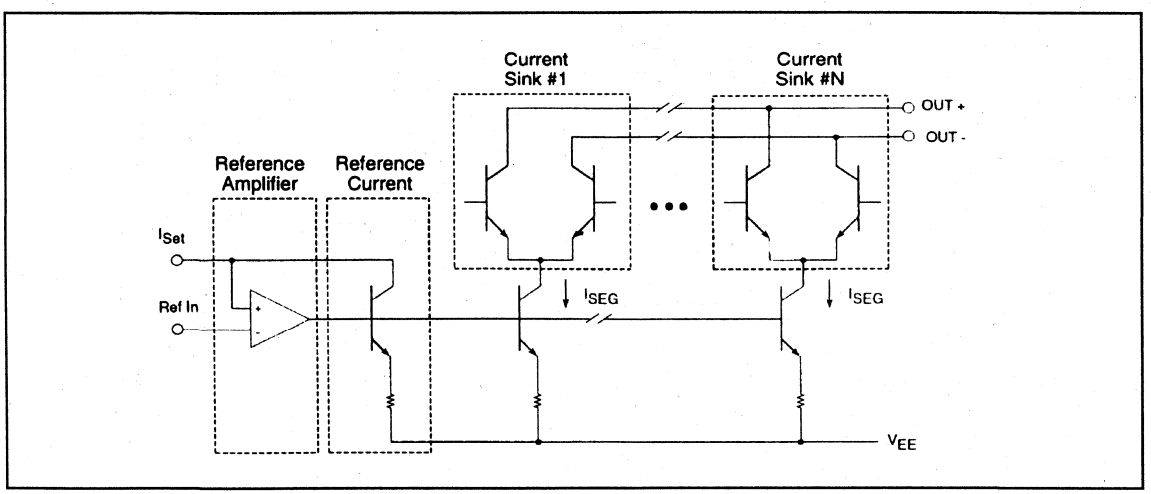


Figure 3. Reference Buffer and DAC Output Circuit

8-Bit, Ultra-High-Speed DAC

To be registered synchronously, control and data inputs must be present at the input pins for a specific setup time (t_S) before and a specific hold time (t_H) after CONV's rising edge. Setup and hold times are not important in asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}), as well as settling time, become the limiting factors (Figure 4).

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video-system standards as described in RS-343-A. Table 1 shows the video-control effects on the analog output. Internal logic governs blank, sync, and force high so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (Figure 5).

Reference-white, video-level output is provided by force high, which drives the internal digital data to full-scale output (100IRE units). Bright gives an additional 10% of full-scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors, or warning messages. If the devices are used in nonvideo applications, the video controls can be left open.

Convert Clock

For best performance, the clock should be differentially ECL driven by using CONV and $\overline{CONV}$ (Figure 6). Driving the clock in this manner minimizes clock noise and power-supply/output intermodulation. The clock's rising edge synchronizes the data and control inputs to the MAX5140. Since $\overline{CONV}$ determines the actual switching threshold of CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{CONV}$. This bias voltage sets the converter clock's switching threshold.

Analog Outputs

The MAX5140 has two analog outputs that are high-impedance, complementary current sinks. The outputs vary in proportion to the input data, controls, and reference-current values so that the full-scale output can be changed by setting I_{SET}.

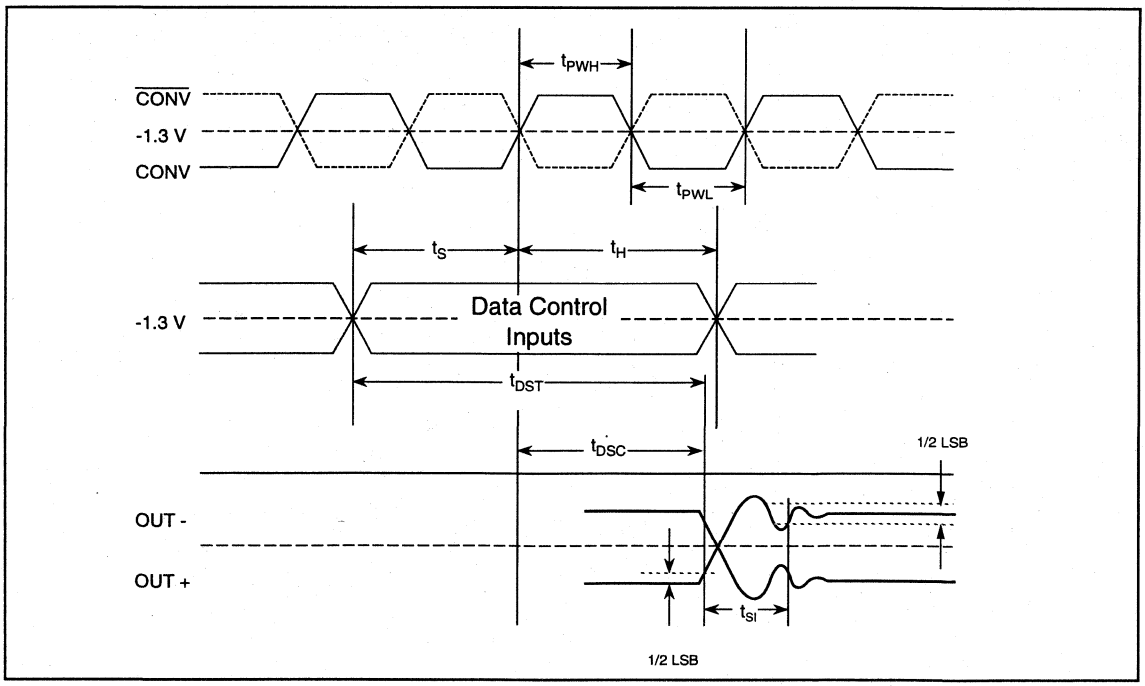


Figure 4. Timing Diagram

Table 1. Video-Control Operation (output values for setup: 10IRE, 75Ω standard load)

SYNC	BLANK	REF WHITE	BRIGHT	DATA INPUT	OUT- (mA)	OUT- (V)	OUT- (IRE)	DESCRIPTION
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

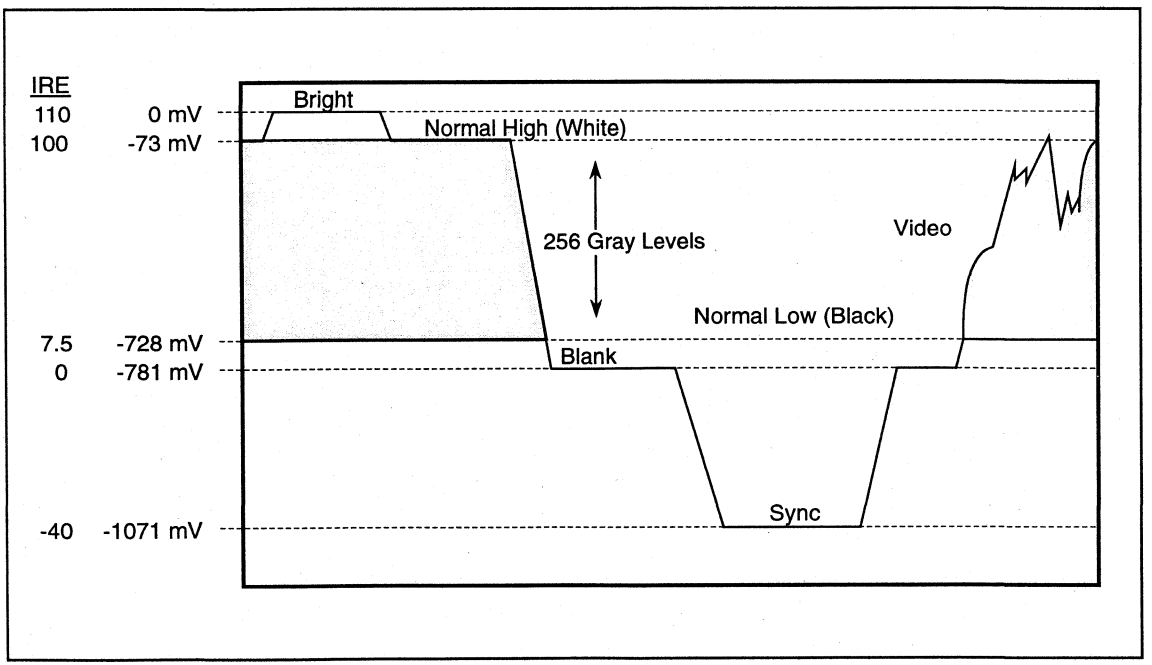


Figure 5. Video-Output Waveform for Standard Load

8-Bit, Ultra-High-Speed DAC

In video applications, the outputs can drive a doubly terminated 50Ω or 75Ω load to standard video levels. In the standard configuration shown in Figure 7, the output voltage is the product of the output current and load impedance and is between 0V and -1.07V. Out- (Figure 5) provides a video output waveform with the Sync pulse bottom at -1.07V. Out+ is inverted with Sync up.

Typical RGB Graphics System

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green, and blue (RGB) DAC outputs. A change in gain or offset in any of the RGB outputs affects the apparent hue displayed on the CRT screen. Thus, it is very important that the DAC's outputs track each other over a wide range of operating conditions. Since the DAC output is proportional to the product of the reference and digital input code, use a common reference to drive all three DACs in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The MAX5140 contains an internal precision-bandgap reference that completely eliminates the need for an external reference. The reference can supply up to 50µA to an external load, such as two other DAC reference inputs.

The circuits shown in Figure 8 show how a single MAX5140 can be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the MAX5140's reference output.

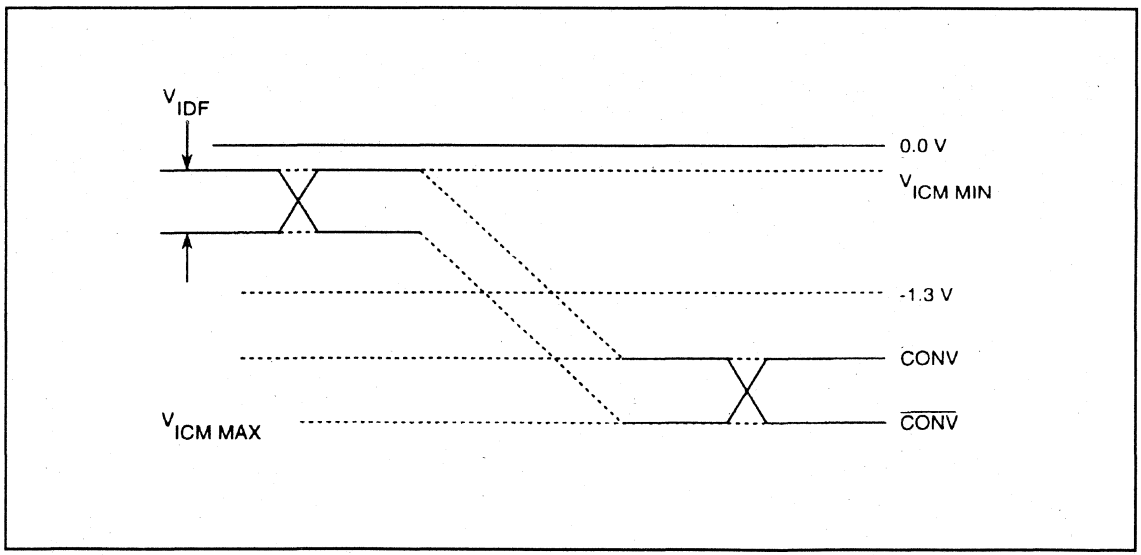


Figure 6. CONV, $\overline{CONV}$ Switching Levels

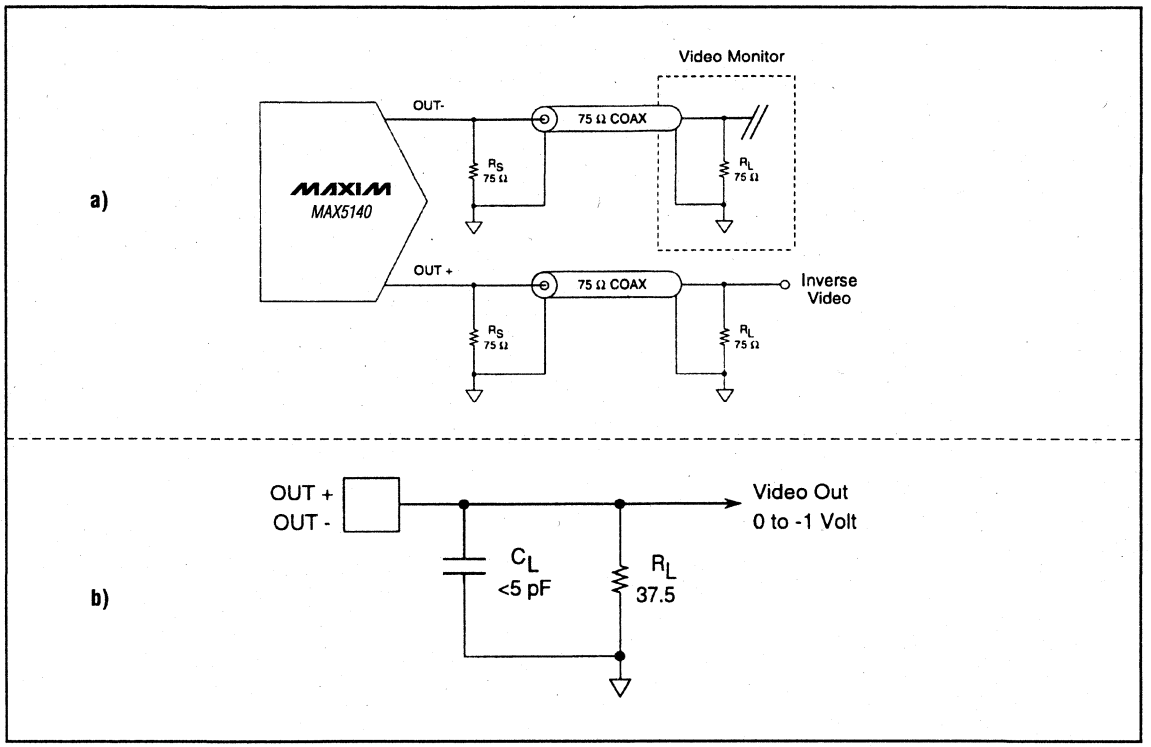


Figure 7. Standard Load (a) and Test Load (b)

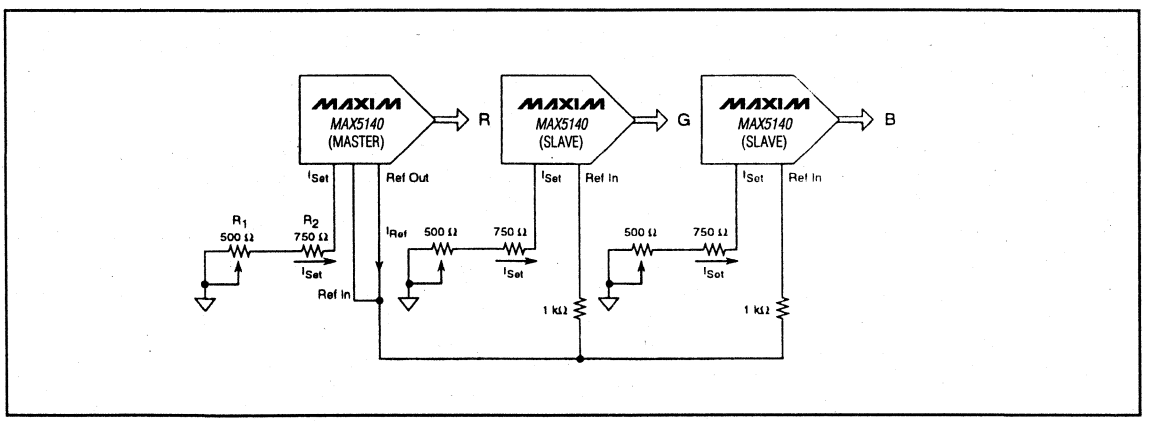


Figure 8. Typical RGB Graphics System

19-1255; Rev 0; 8/97

MAXIM

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5150/MAX5151 low-power, serial, voltage-output, dual 13-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5150) or +3V (MAX5151) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. To maximize the dynamic range, the DAC output amplifiers are configured with an internal gain of +2.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include programmable shutdown (2µA), hardware-shutdown lockout, a separate reference voltage input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality, and a serial-data output pin for daisy-chaining.

Applications

Industrial Process Control

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Automatic Test Equipment (ATE)

Features

- ♦ **13-Bit Dual DAC with Internal Gain of +2**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **16µs Settling Time**
- ♦ **Single-Supply Operation: +5V (MAX5150)**
  +3V (MAX5151)
- ♦ **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Available in Space-Saving 16-Pin QSOP Package**
- ♦ **Power-On Reset Clears Registers and DACs to Zero**
- ♦ **Adjustable Output Offset**

Ordering Information

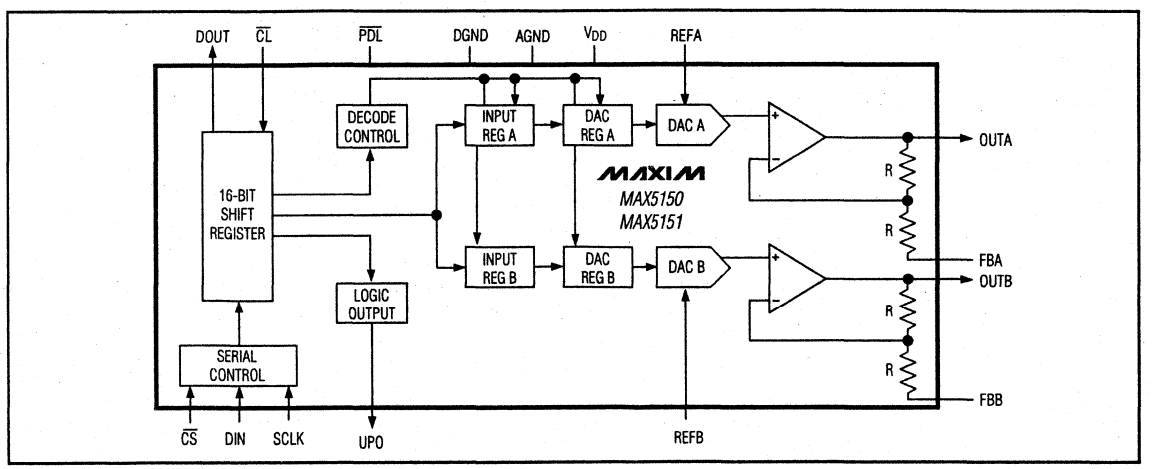
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5150ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX5150BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX5150ACEE	0°C to +70°C	16 QSOP	±1/2
MAX5150BCEE	0°C to +70°C	16 QSOP	±1
MAX5150BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued at end of data sheet.

**Dice are tested at T_A = +25°C, DC parameters only.*

Pin Configuration appears at end of data sheet.

Functional Diagram



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SPI and QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Semiconductor Corp.

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For small orders, phone 408-737-7600 ext. 3468.

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
OSA, OSB to AGND .....(AGND - 4V) to (V_{DD} + 0.3V)
REF_, OUT_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs (SCLK, DIN, $\overline{CS}$, $\overline{CL}$, $\overline{PDL}$)
to DGND .....-0.3V to +6V
Digital Outputs (DOUT, UPO)
to DGND .....-0.3V to (V_{DD} + 0.3V)

Maximum Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 10.5mW/°C above +70°C) 842mW
QSOP (derate 8.30mW/°C above +70°C) 667mW
CERDIP (derate 10.00mW/°C above +70°C) 800mW
Operating Temperature Ranges
MAX515_ _C_ E .....0°C to +70°C
MAX515_ _E_ E .....-40C° to +85°C
MAX515_ _MJE .....-55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX5150

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = 2.048V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25°C (OS_ tied to AGND for a gain of +2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION							
Resolution				13			Bits
Integral Nonlinearity	INL	(Note 1)	MAX5150A			±1/2	LSB
			MAX5150B			±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	Code = 12				±6	mV
Offset Tempco	TCV_{OS}	Normalized to 2.048V			4		ppm/°C
Gain Error					-0.2	±3	mV
Gain-Error Tempco		Normalized to 2.048V			4		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			20	260	µV/V
REFERENCE INPUT							
Reference Input Range	REF			0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1555 hex		14	20		kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		Input code = 1FFF hex, $V_{REF_}$ = 0.67Vp-p at 2.5V_{DC}			300		kHz
Reference Feedthrough		Input code = 0000 hex, $V_{REF_}$ = (V_{DD} - 1.4Vp-p) at 1kHz			-82		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FFF hex, $V_{REF_}$ = 1Vp-p at 1.25V_{DC}, f = 25kHz			75		dB
DIGITAL INPUTS							
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK		3.0			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK				0.8	V
Input Hysteresis	V_{HYS}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}			0.001	±1	µA
Input Capacitance	C_{IN}				8		pF

ELECTRICAL CHARACTERISTICS—MAX5150 (continued)

(V_{DD} = +5V ±10%, V_{REFA} = V_{REFB} = 2.048V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A= +25°C (OS_ tied to AGND for a gain of +2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 4V		16		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
OSA or OSB Input Resistance	R_{OS}		24	34		kΩ
Time Required to Exit Shutdown				25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{DIN} = 100kHz, V_{SCLK} = 5Vp-p		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		4.5		5.5	V
Power-Supply Current	I_{DD}	(Note 3)		0.5	0.65	mA
Power-Supply Current in Shutdown	$I_{DD\ (SHDN)}$	(Note 3)		2	10	µA
Reference Current in Shutdown				0	±1	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		40			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Accuracy is specified from code 12 to code 8191.

Note 2: Accuracy is better than 1LSB for $V_{OUT_}$ greater than 6mV and less than V_{DD} - 50mV. Guaranteed by PSRR test at the end points.

Note 3: Digital inputs are set to either V_{DD} or DGND, code = 0000 hex, R_L = ∞.

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS—MAX5151

(V_{DD} = +2.7V to +3.6V, V_{REFA} = V_{REFB} = 1.25V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C (OS_ pins tied to AGND for a gain of +2).)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG							
Resolution				13			Bits
Integral Nonlinearity	INL	(Note 4)	MAX5151A			±1	LSB
			MAX5151B			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error	V_{OS}	Code = 20				±6	mV
Offset Tempco	TCV_{OS}	Normalized to 1.25V			6.5		ppm/°C
Gain Error					-0.2	±5	mV
Gain-Error Tempco		Normalized to 1.25V			6.5		ppm/°C
V_{DD} Power-Supply Rejection Ratio	PSRR	2.7V ≤ V_{DD} ≤ 3.6V			40	320	µV/V
REFERENCE INPUT (VREF)							
Reference Input Range	REF			0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Minimum with code 1555 hex		14	20		kΩ
MULTIPLYING-MODE PERFORMANCE							
Reference 3dB Bandwidth		Input code = 1FFF hex, $V_{REF_}$ = 0.67Vp-p at 0.75V_{DC}			300		kHz
Reference Feedthrough		Input code = 0000 hex, $V_{REF_}$ = (V_{DD} - 1.4)Vp-p at 1kHz			-82		dB
Signal-to-Noise plus Distortion Ratio	SINAD	Input code = 1FFF hex, $V_{REF_}$ = 1Vp-p at 1V_{DC}, f = 15kHz			73		dB
DIGITAL INPUTS							
Input High Voltage	V_{IH}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK		2.2			V
Input Low Voltage	V_{IL}	$\overline{CL}$, $\overline{PDL}$, $\overline{CS}$, DIN, SCLK				0.8	V
Input Hysteresis	V_{HYS}				200		mV
Input Leakage Current	I_{IN}	V_{IN} = 0V to V_{DD}			0	±1	µA
Input Capacitance	C_{IN}				8		pF
DIGITAL OUTPUTS							
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA		V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA			0.13	0.4	V
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate	SR				0.75		V/µs
Output Settling Time		To 1/2LSB of full-scale, V_{STEP} = 2.5V			16		µs
Output Voltage Swing		Rail-to-rail (Note 5)			0 to V_{DD}		V
OSA or OSB Input Resistance	R_{OS}			24	34		kΩ
Time Required for Valid Operation after Shutdown					25		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, f_{DIN} = 100kHz, V_{SCLK} = 3Vp-p			5		nV-s
Digital Crosstalk					5		nV-s

ELECTRICAL CHARACTERISTICS—MAX5151 (continued)

(V_{DD} = +2.7V to +3.6V, V_{REFA} = V_{REFB} = 1.25V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C (OS_ pins tied to AGND for a gain of +2).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}		2.7		3.6	V
Power-Supply Current	I_{DD}	(Note 6)		0.45	0.6	mA
Power-Supply Current in Shutdown	$I_{DD (SHDN)}$	(Note 6)		1	8	µA
Reference Current in Shutdown				0	±1	µA
TIMING CHARACTERISTICS						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
SDI Setup Time	t_{DS}		50			ns
SDI Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{DO1}	C_{LOAD} = 200pF			120	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{DO2}	C_{LOAD} = 200pF			120	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		10			ns
$\overline{CS}$ Rise to SCLK Rise Hold	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: Accuracy is specified from code 20 to code 8191.

Note 5: Accuracy is better than 1LSB for V_{OUT} greater than 6mV and less than V_{DD} - 80mV. Guaranteed by PSRR test at the end points.

Note 6: Digital inputs are set to either V_{DD} or DGND, code = 0000 hex, R_L = ∞.

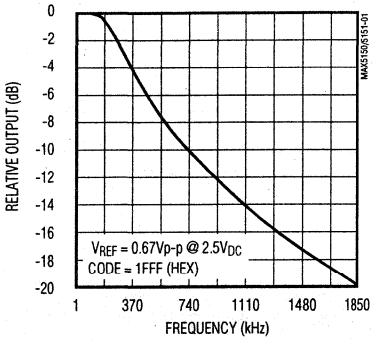
Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

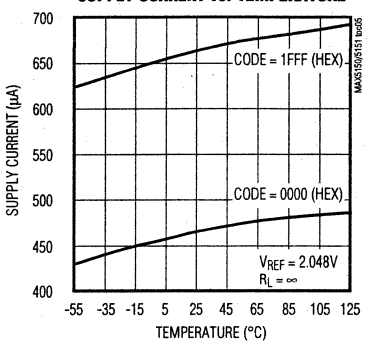
(V_{DD} = +5V, R_L = 10kΩ, C_L = 100pF, OS_ pins tied to AGND, unless otherwise noted.)

MAX5150

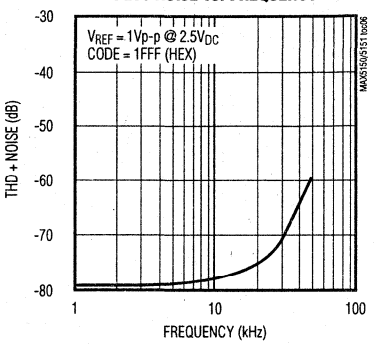
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



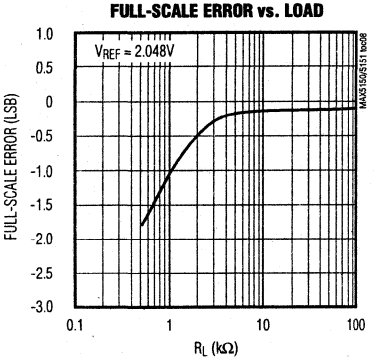
SUPPLY CURRENT vs. TEMPERATURE



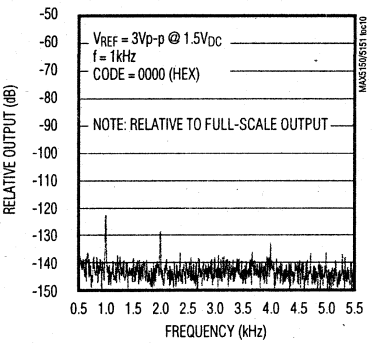
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



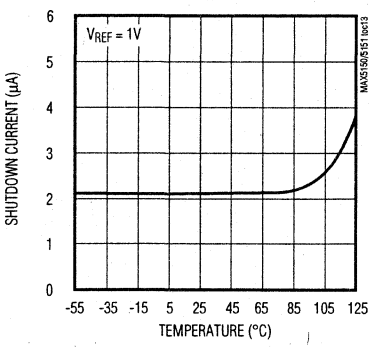
FULL-SCALE ERROR vs. LOAD



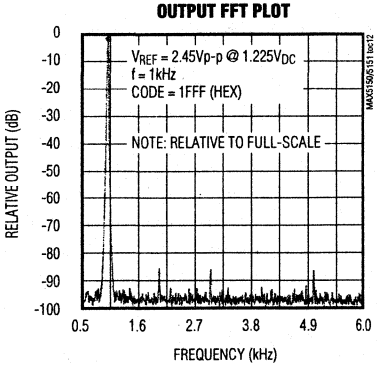
REFERENCE FEEDTHROUGH AT 1kHz



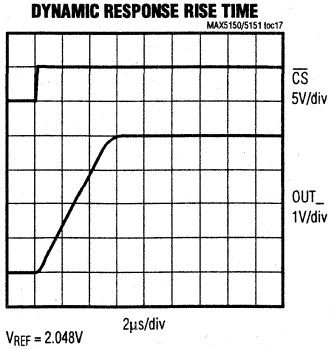
SHUTDOWN CURRENT vs. TEMPERATURE



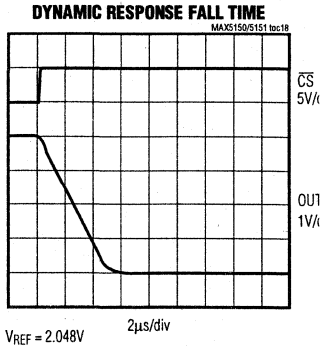
OUTPUT FFT PLOT



DYNAMIC RESPONSE RISE TIME



DYNAMIC RESPONSE FALL TIME

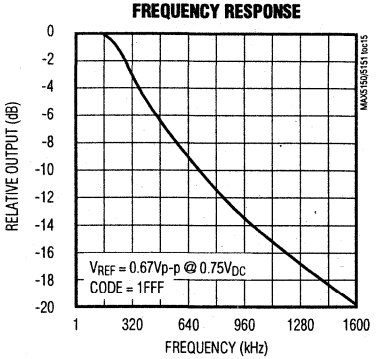


Typical Operating Characteristics (continued)

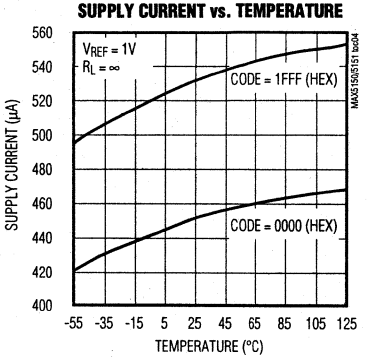
(V_{DD} = +3V, R_L = 10kΩ, C_L = 100pF, OS_pins tied to AGND, unless otherwise noted.)

MAX5151

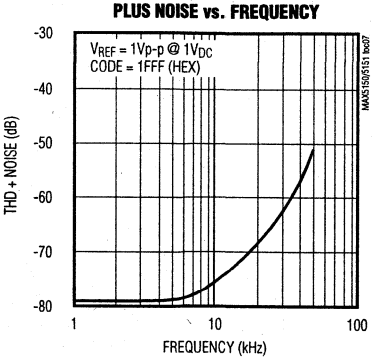
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



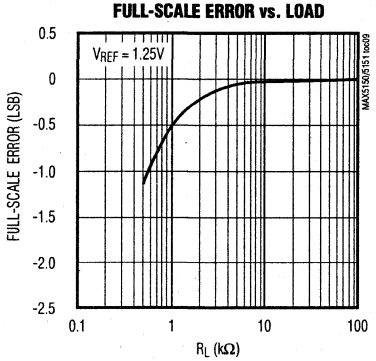
SUPPLY CURRENT vs. TEMPERATURE



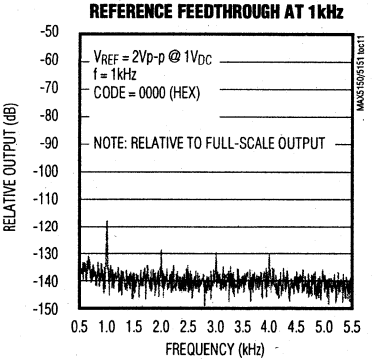
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



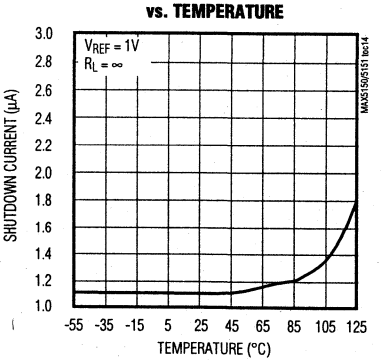
FULL-SCALE ERROR vs. LOAD



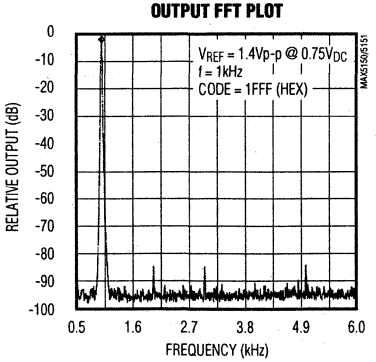
REFERENCE FEEDTHROUGH AT 1kHz



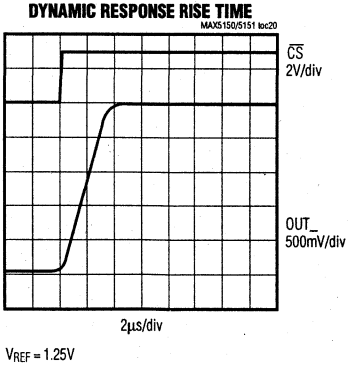
SHUTDOWN CURRENT vs. TEMPERATURE



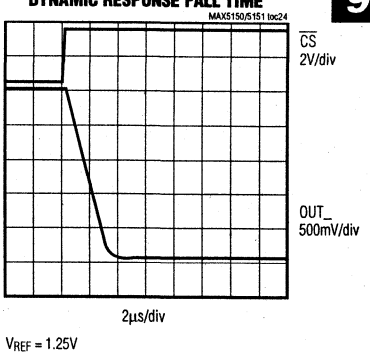
OUTPUT FFT PLOT



DYNAMIC RESPONSE RISE TIME



DYNAMIC RESPONSE FALL TIME



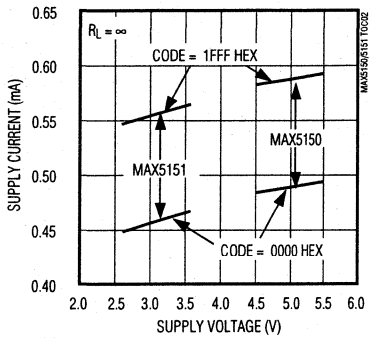
Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

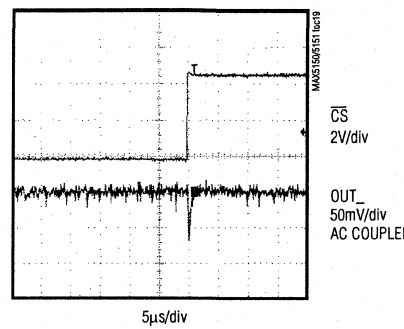
(V_{DD} = +5V (MAX5150), V_{DD} = +3V (MAX5151), R_L = 10kΩ, C_L = 100pF, OS_ pins tied to AGND, unless otherwise noted.)

MAX5150/MAX5151

SUPPLY CURRENT vs. SUPPLY VOLTAGE

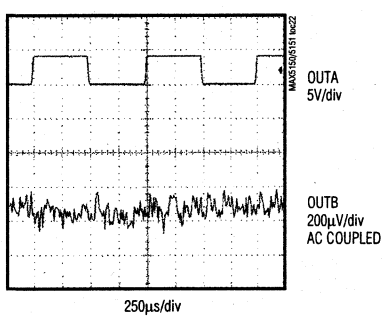


MAX5150 MAJOR-CARRY TRANSITION



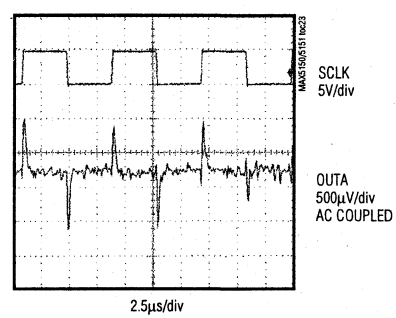
TRANSITION FROM 1000 HEX TO 0FFF HEX

MAX5150 ANALOG CROSSTALK



V_{REF} = 2.048V, GAIN = +2, CODE = 1FFF HEX

MAX5150 DIGITAL FEEDTHROUGH



Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	OUTA	DAC A Output Voltage
3	OSA	DAC A Offset Adjustment
4	REFA	Reference for DAC A
5	$\overline{CL}$	Clears all DACs and registers (resets to 0).
6	$\overline{CS}$	Chip-Select Input
7	DIN	Serial-Data Input
8	SCLK	Serial-Register Clock Input
9	DGND	Digital Ground
10	DOUT	Serial-Data Output
11	UPO	User-Programmable Output
12	$\overline{PDL}$	Power-Down Lockout. The device cannot be powered down when $\overline{PDL}$ is low.
13	REFB	Reference for DAC B
14	OSB	DAC B Offset Adjustment
15	OUTB	DAC B Output Voltage
16	V_{DD}	Positive Power Supply

Detailed Description

The MAX5150/MAX5151 dual, 13-bit, voltage-output DACs are easily configured with a 3-wire serial interface. These devices include a 16-bit data-in/data-out shift register, and each DAC has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition, trimmed internal resistors produce an internal gain of +2 that maximizes output voltage swing. The amplifier's offset-adjust pin allows for a DC shift in the DAC's output.

Both DACs use an inverted R-2R ladder network that produces a weighted voltage proportional to the input voltage value. Each DAC has its own reference input to facilitate independent full-scale values. Figure 1 depicts a simplified circuit diagram of one of the two DACs.

Reference Inputs

The reference inputs accept both AC and DC values with a voltage range extending from 0V to (V_{DD} - 1.4V). Determine the output voltage using the following equation (OS_ = AGND):

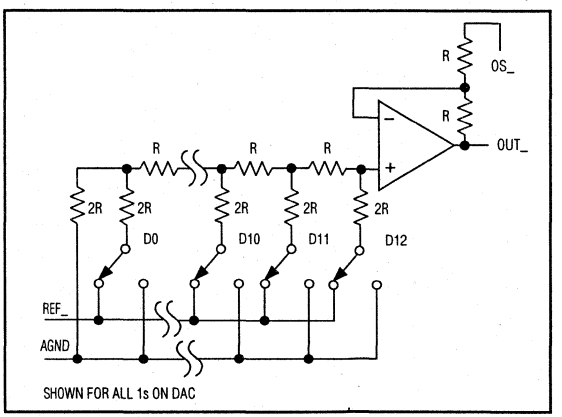


Figure 1. Simplified DAC Circuit Diagram

$$V_{OUT} = (V_{REF} \times NB / 8192) \times 2$$

where NB is the numeric value of the DAC's binary input code (0 to 8191) and V_{REF} is the reference voltage.

The reference input impedance ranges from 14kΩ (1555 hex) to several giga ohms (with an input code of 0000 hex). The reference input capacitance is code dependent and typically ranges from 15pF with an input code of all zeros to 50pF with an input code of all ones.

Output Amplifier

The output amplifiers on the MAX5150/MAX5151 have internal resistors that provide for a gain of +2 when OS_ is connected to AGND. These resistors are trimmed to minimize gain error. The output amplifiers have a typical slew rate of 0.75V/µs and settle to 1/2LSB within 16µs, with a load of 10kΩ in parallel with 100pF. Loads less than 2kΩ degrade performance.

The OS_ pin can be used to produce an adjustable offset voltage at the output. For instance, to achieve a 1V offset, apply -1V to the OS_ pin to produce an output range from 1V to (1V + V_{REF} x 2). Note that the DAC's output range is still limited by the maximum output voltage specification.

Power-Down Mode

The MAX5150/MAX5151 feature a software-programmable shutdown mode that reduces the typical supply current to 2µA. The two DACs can be shutdown independently, or simultaneously using the appropriate programming command. Enter shutdown mode by writing the appropriate input-control word (Table 1). In shutdown mode, the reference inputs and amplifier out-

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD				
A0	C1	C0	D12.....D0 (MSB) (LSB)	FUNCTION
0	0	1	13-bit DAC data	Load input register A; DAC registers are unchanged.
1	0	1	13-bit DAC data	Load input register B; DAC registers are unchanged.
0	1	0	13-bit DAC data	Load input register A; all DAC registers are updated.
1	1	0	13-bit DAC data	Load input register B; all DAC registers are updated.
0	1	1	13-bit DAC data	Load all DAC registers from the shift register (start up both DACs with new data.).
1	0	0	xxxxxxxxxxxxx	Update both DAC registers from their respective input registers (start up both DACs with data previously stored in the input registers).
1	1	1	xxxxxxxxxxxxx	Shut down both DACs (provided $\overline{PDL}$ = 1).
0	0	0	0 0 1 x xxxxxxxxx	Update DAC register A from input register A (start up DAC A with data previously stored in input register A).
0	0	0	1 0 1 x xxxxxxxxx	Update DAC register B from input register B (start up DAC B with data previously stored in input register B).
0	0	0	1 1 0 x xxxxxxxxx	Shut down DAC A (provided $\overline{PDL}$ = 1).
0	0	0	1 1 1 x xxxxxxxxx	Shut down DAC B (provided $\overline{PDL}$ = 1).
0	0	0	0 1 0 x xxxxxxxxx	UPO goes low (default).
0	0	0	0 1 1 x xxxxxxxxx	UPO goes high.
0	0	0	1 0 0 1 xxxxxxxxx	Mode 1, DOUT clocked out on SCLK's rising edge.
0	0	0	1 0 0 0 xxxxxxxxx	Mode 0, DOUT clocked out on SCLK's falling edge (default).
0	0	0	0 0 0 x xxxxxxxxx	No operation (NOP).

x = Don't care

Note: When A0, C1, and C0 = 0, then D12, D11, D10, and D9 become control bits.

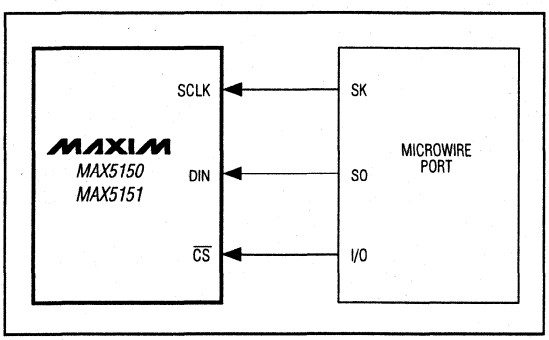


Figure 2. Connections for Microwire

puts become high impedance, and the serial interface remains active. Data in the input registers is saved, allowing the MAX5150/MAX5151 to recall the output state prior to entering shutdown when returning to normal mode. Exit shutdown by recalling the previous condition or by updating the DAC with new information. When returning to normal operation (exiting shutdown), wait 20µs for output stabilization.

Serial Interface

The MAX5150/MAX5151 3-wire serial interface is compatible with both Microwire (Figure 2) and SPI/QSPI (Figure 3) serial-interface standards. The 16-bit serial input word consists of an address bit, two control bits, and 13 bits of data (MSB to LSB) as shown in Figure 4.

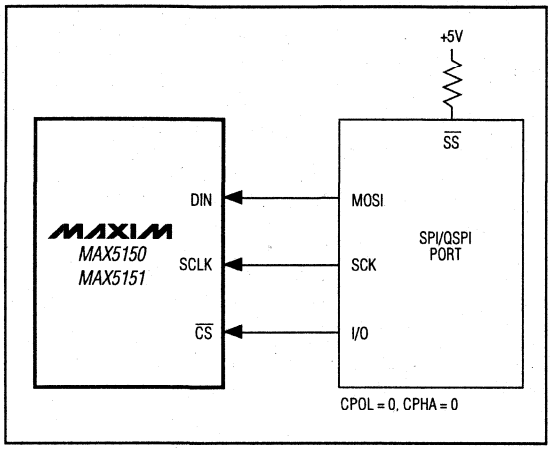


Figure 3. Connections for SPI/QSPI

MSB ..... LSB		
◄ 16 Bits of Serial Data ►		
Address Bits	Control Bits	MSB.....Data Bits.....LSB
A0	C1, C0	D12.....D0
◄ 1 Address/2 Control Bits ►		◄ 13 Data Bits ►

Figure 4. Serial-Data Format

The address and control bits determine the MAX5150/MAX5151's response, as outlined in Table 1.

The MAX5150/MAX5151's digital inputs are double buffered, which allows any of the following: loading the input register(s) without updating the DAC register(s), updating the DAC register(s) from the input register(s), or updating the input and DAC registers concurrently. The address and control bits allow the DACs to act independently.

The 16-bit data can be sent as two 8-bit packets (SPI, Microwire), with $\overline{CS}$ low during this period. The address and control bits determine which register will be updated, and the state of the registers when exiting shutdown. The 3-bit address/control determines the following:

- registers to be updated
- clock edge on which data is to be clocked out via the serial-data output (DOUT)
- state of the user-programmable logic output
- configuration of the device after shutdown.

The general timing diagram of Figure 5 illustrates how data is acquired. Driving $\overline{CS}$ low enables the device to receive data. Otherwise, the interface control circuitry is disabled. With $\overline{CS}$ low, data at DIN is clocked into the register on the rising edge of SCLK. As $\overline{CS}$ goes high, data is latched into the input and/or DAC registers depending on the address and control bits. The maximum clock frequency guaranteed for proper operation is 10MHz. Figure 6 depicts a more detailed timing diagram of the serial interface.

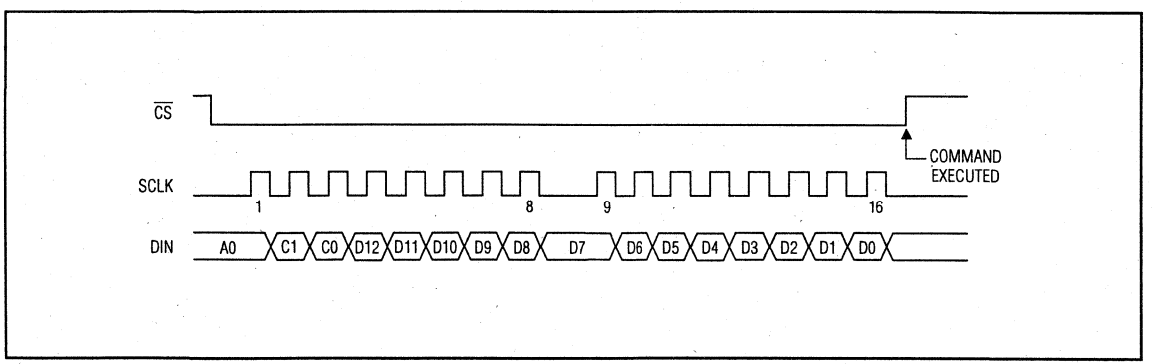


Figure 5. Serial-Interface Timing Diagram

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

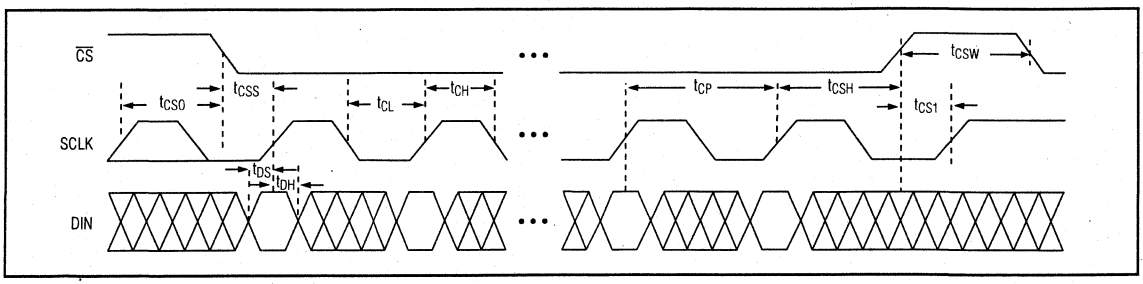


Figure 6. Detailed Serial-Interface Timing Diagram

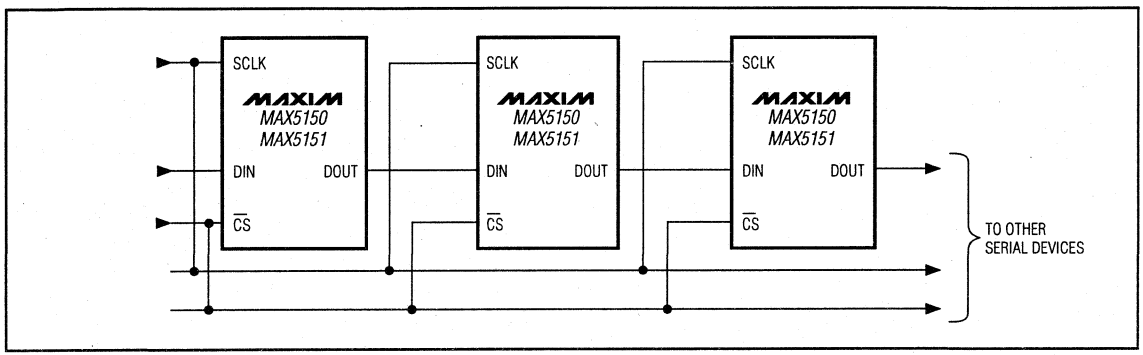


Figure 7. Daisy Chaining MAX5150/MAX5151s

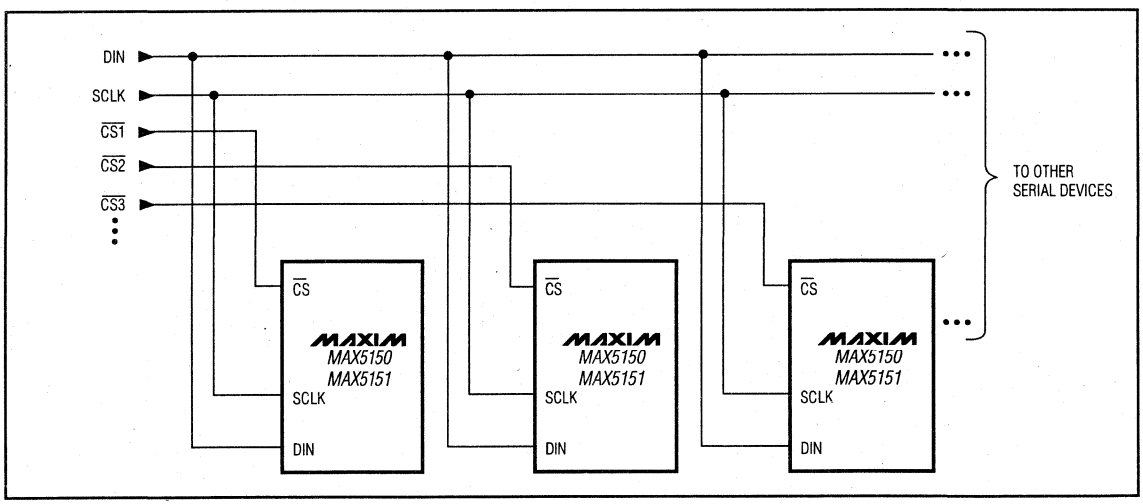


Figure 8. Multiple MAX5150/MAX5151s Sharing a Common DIN Line

Table 2. Unipolar Code Table (Gain = +2)

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
11111	1111	1111	$+V_{REF}\left(\frac{8191}{8192}\right) \times 2$
10000	0000	0001	$+V_{REF}\left(\frac{4097}{8192}\right) \times 2$
10000	0000	0000	$+V_{REF}\left(\frac{4096}{8192}\right) \times 2 = V_{REF}$
01111	1111	1111	$+V_{REF}\left(\frac{4095}{8192}\right) \times 2$
00000	0000	0001	$+V_{REF}\left(\frac{1}{8192}\right) \times 2$
00000	0000	0000	0V

Serial-Data Output

The serial-data output, DOUT, is the internal shift register's output. DOUT allows for daisy chaining of devices and data readback. The MAX5150/MAX5151 can be programmed to shift data out of DOUT on SCLK's falling edge (Mode 0) or on the rising edge (Mode 1). Mode 0 provides a lag of 16 clock cycles, which maintains compatibility with SPI/QSPI and Microwire interfaces. In Mode 1, the output data lags 15.5 clock cycles. On power-up, the device defaults to Mode 0.

User-Programmable Logic Output (UPO)

UPO allows an external device to be controlled through the serial interface (Table 1), thereby reducing the number of microcontroller I/O pins required.

Power-Down Lockout Input ($\overline{PDL}$)

The power-down lockout pin ($\overline{PDL}$) disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ can also be used to asynchronously wake up the device.

Daisy Chaining Devices

Any number of MAX5150/MAX5151s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5150/MAX5151's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

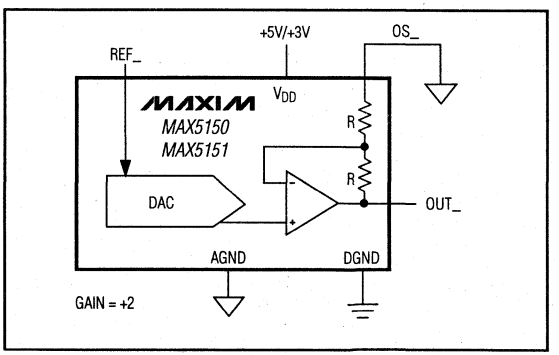


Figure 9. Unipolar Output Circuit (Rail-to-Rail)

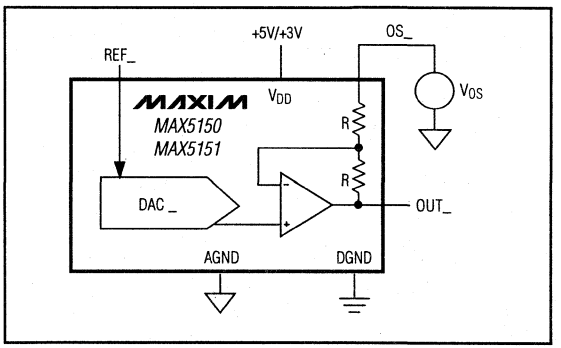


Figure 10. Setting OS_ for Output Offset

Figure 8 shows an alternate method of connecting several MAX5150/MAX5151s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

Applications Information

Unipolar Output

Figure 9 shows the MAX5150/MAX5151 configured for unipolar, rail-to-rail operation with a gain of +2. The MAX5150 can produce a 0V to 4.096V output with 2.048V reference (Figure 9), while the MAX5151 can produce a range of 0V to 2.5V with a 1.25V reference. Table 2 lists the unipolar output codes. An offset to the output can be achieved by connecting a voltage to OS_, as shown in Figure 10. By applying $V_{OS_}$ = -1V, the output values will range between 1V and (1V + V_{REF} x 2).

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
11111	1111	1111	$+V_{REF}\left(\frac{4095}{4096}\right)$
10000	0000	0001	$+V_{REF}\left(\frac{1}{4096}\right)$
10000	0000	0000	0V
01111	1111	1111	$-V_{REF}\left(\frac{1}{4096}\right)$
00000	0000	0001	$-V_{REF}\left(\frac{4095}{4096}\right)$
00000	0000	0000	$-V_{REF}\left(\frac{4096}{4096}\right) = -V_{REF}$

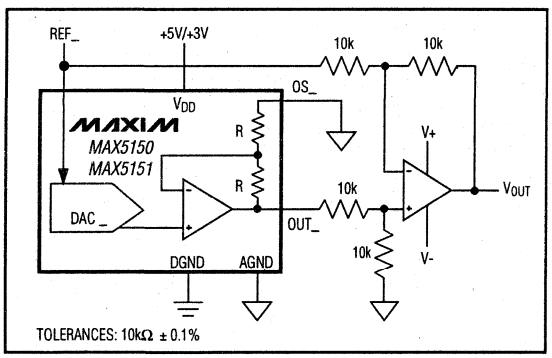


Figure 11. Bipolar Output Circuit

Bipolar Output

The MAX5150/MAX5151 can be configured for a bipolar output, as shown in Figure 11. The output voltage is given by the equation (OS_ = AGND):

$$V_{OUT} = V_{REF}\,[((2 \times NB) / 8192) - 1]$$

where NB represents the numeric value of the DAC's binary input code. Table 3 shows digital codes and the corresponding output voltage for Figure 11's circuit.

Using an AC Reference

In applications where the reference has an AC signal component, the MAX5150/MAX5151 have multiplying capabilities within the reference input voltage range specifications. Figure 12 shows a technique for applying a sinusoidal input to REF_, where the AC signal is offset before being applied to REF.

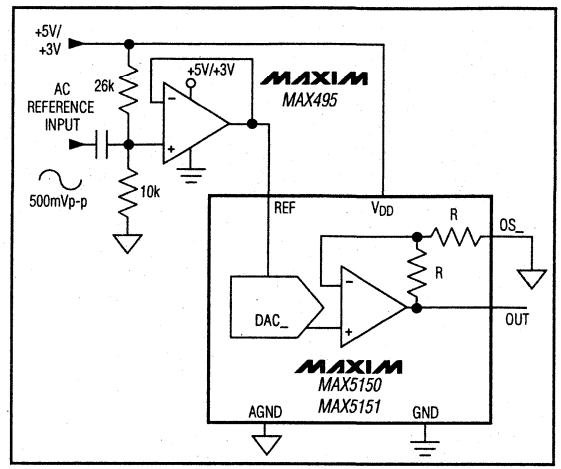


Figure 12. AC Reference Input Circuit

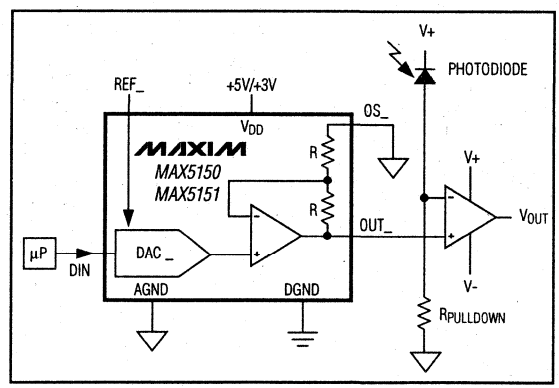


Figure 13. Digital Calibration

Harmonic Distortion and Noise

The total harmonic distortion plus noise (THD+N) is typically less than -78dB at full scale with a 1Vp-p input swing at 5kHz. The typical -3dB frequency is 300kHz for both devices, as shown in the *Typical Operating Characteristics.*

Digital Calibration and Threshold Selection

Figure 13 shows the MAX5150/MAX5151 in a digital calibration application. With a bright light value applied to the photodiode (on), the DAC is digitally ramped until it trips the comparator. The microprocessor stores this "high" calibration value. Repeat the process with a dim light (off) to obtain the dark current calibration.

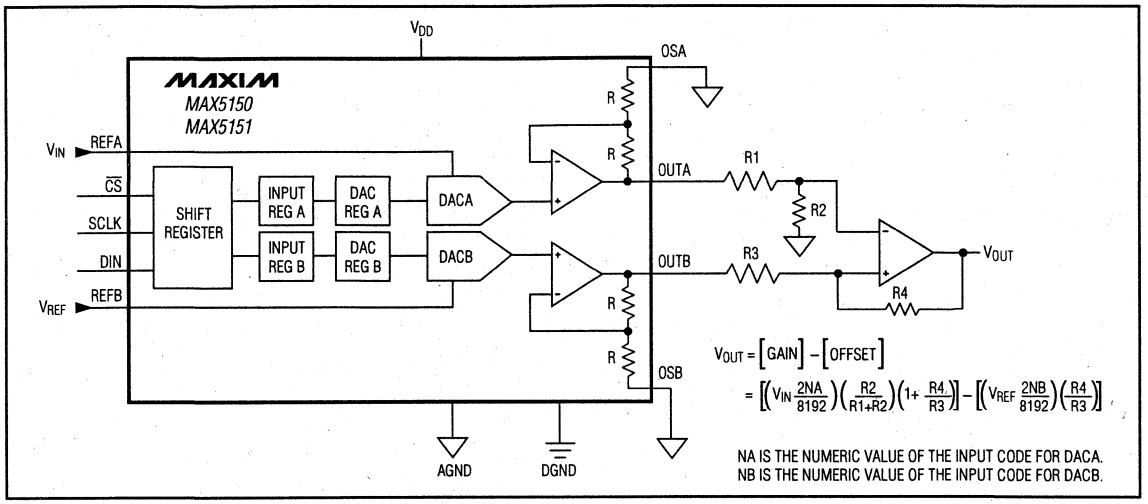


Figure 14. Digital Control of Gain and Offset

The microprocessor then programs the DAC to set an output voltage at the midpoint of the two calibrated values. Applications include tachometers, motion sensing, automatic readers, and liquid clarity analysis.

Digital Control of Gain and Offset

The two DACs can be used to control the offset and gain for curve-fitting nonlinear functions, such as transducer linearization or analog compression/expansion applications. The input signal is used as the reference for the gain-adjust DAC, whose output is summed with the output from the offset-adjust DAC. The relative weight of each DAC output is adjusted by R1, R2, R3, and R4 (Figure 14).

Power-Supply Considerations

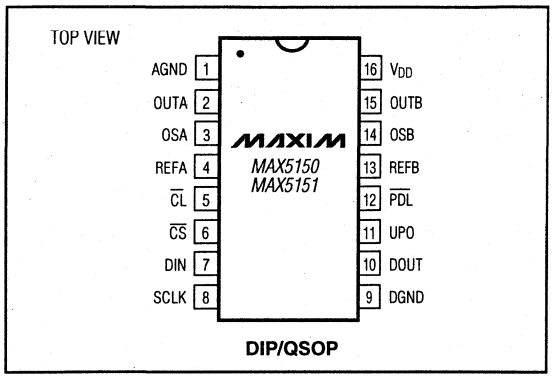
On power-up, the input and DAC registers clear (set to zero code). For rated performance, $V_{REF_}$ should be at least 1.4V below V_{DD}. Bypass the power supply with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Minimize lead lengths to reduce lead inductance.

Grounding and Layout Considerations

Digital and AC transient signals on AGND can create noise at the output. Connect AGND to the highest quality ground available. Use proper grounding techniques, such as a multilayer board with a low-inductance ground plane. Carefully lay out the traces between channels to reduce AC cross-coupling and crosstalk. Wire-wrapped boards and sockets are not recommended. If noise becomes an issue, shielding may be required.

Low-Power, Dual, 13-Bit Voltage-Output DACs with Serial Interface

Pin Configuration



Chip Information

TRANSISTOR COUNT: 3053

SUBSTRATE CONNECTED TO AGND

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5150AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX5150BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5150AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX5150BEEE	-40°C to +85°C	16 QSOP	±1
MAX5150BMJE	-55°C to +125°C	16 CERDIP**	±1
MAX5151ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX5151BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX5151ACEE	0°C to +70°C	16 QSOP	±1
MAX5151BCEE	0°C to +70°C	16 QSOP	±2
MAX5151BC/D	0°C to +70°C	Dice*	±1
MAX5151AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5151BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX5151AEEE	-40°C to +85°C	16 QSOP	±1
MAX5151BEEE	-40°C to +85°C	16 QSOP	±2
MAX5151BMJE	-55°C to +125°C	16 CERDIP**	±2

**Dice are tested at T_A = +25°C, DC parameters only.*

***Contact factory for availability.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Output

General Description

The MAX5152/MAX5153 low-power, serial, voltage-output, dual, 13-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5152) or +3V (MAX5153) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. Access to the output amplifier's inverting input allows for specific gain configurations, remote sensing, and high output current capability, making these devices ideal for industrial process controls. They are also well suited for digitally programmable, 4-20mA current loops.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously. Additional features include a 2µA programmable shutdown, a hardware-shutdown lockout, a separate voltage reference input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality and a serial-data output pin for daisy-chaining.

Applications

Industrial Process Control

Digital Offset and Gain Adjustment

Digitally Programmable, 4-20mA Current Loops

Motion Control

Remote Industrial Controls

µP-Controlled Systems

Automatic Test Equipment

Features

- **13-Bit Dual DAC with Configurable Output Amplifiers**
- **Rail-to-Rail Output Swing**
- **16µs Settling Time**
- **Single-Supply Operation: +5V (MAX5152)**
  +3V (MAX5153)
- **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- **SPI/QSPI and Microwire Compatible**
- **Space-Saving 16-Pin QSOP Package**
- **Power-On Reset Clears DAC Outputs to Zero**

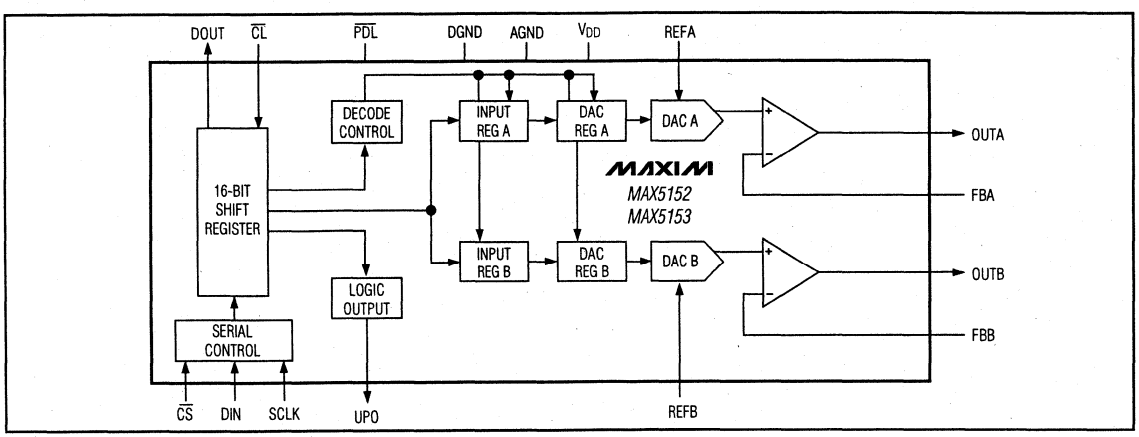
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5152ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX5152BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX5152ACEE	0°C to +70°C	16 QSOP	±1/2
MAX5152BCPE	0°C to +70°C	16 QSOP	±1
MAX5152BC/D	0°C to +70°C	Dice*	±1

Ordering Information continued on next page.

**Dice are tested at T_A = +25°C, DC parameters only.*

Functional Diagram



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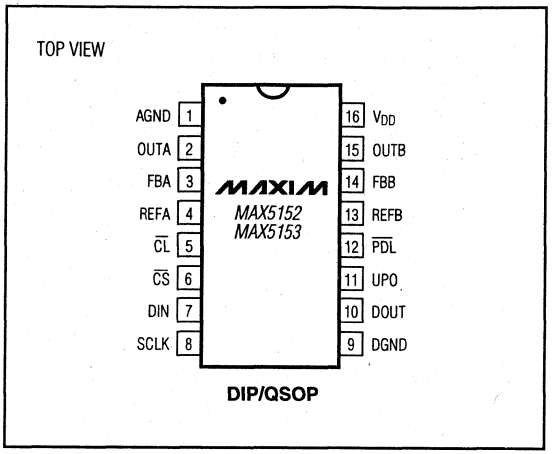
Low-Power, Dual, 13-Bit Voltage-Output DACs with Configurable Output

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5152AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX5152BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5152AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX5152BEEE	-40°C to +85°C	16 QSOP	+1
MAX5152BMJE	-55°C to +125°C	16 CERDIP	±1
MAX5153ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX5153BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX5153ACEE	0°C to +70°C	16 QSOP	±1
MAX5153BCPE	0°C to +70°C	16 QSOP	±2
MAX5153BC/D	0°C to +70°C	Dice*	±2
MAX5153AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5153BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX5153AEEE	-40°C to +85°C	16 QSOP	±1
MAX5153BEEE	-40°C to +85°C	16 QSOP	±2
MAX5153BMJE	-55°C to +125°C	16 CERDIP	±2

*Dice are tested at T_A = +25°C, DC parameters only.

Pin Configuration



ADVANCE INFORMATION
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8/97

MAXIM

Low-Power, Dual, 12-Bit, Voltage-Output DACs with Serial Interface

General Description

The MAX5154/MAX5155 low-power, serial, voltage-output, dual, 12-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5154) or +3V (MAX5155) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. To maximize dynamic range, the DAC output amplifiers are configured with an internal gain of +2.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register. This allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include a 2µA programmable shutdown, hardware-shutdown lockout, a separate reference-voltage input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality and a serial-data output pin for daisy chaining.

Applications

Industrial Process Control
Digital Offset and Gain Adjustment
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems
Automatic Test Equipment

Features

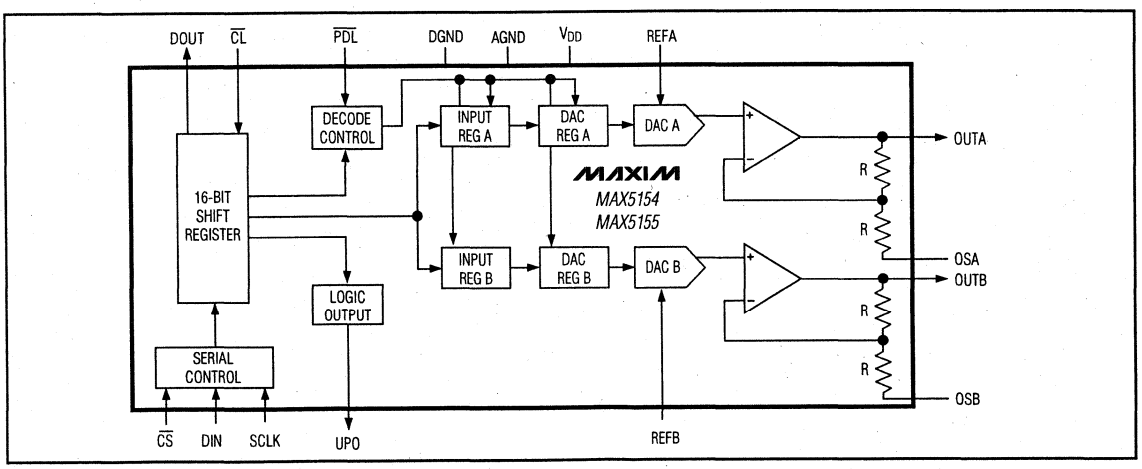
- **12-Bit Dual DAC with Internal Gain of +2**
- **Rail-to-Rail Output Swing**
- **16µs Settling Time**
- **Single-Supply Operation: +5V (MAX5154)**
  +3V (MAX5155)
- **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- **SPI/QSPI and Microwire Compatible**
- **Available in Space-Saving 16-Pin QSOP Package**
- **Power-On Reset Clears Registers and DACs to Zero**
- **Adjustable Output Offset**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5154ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX5154BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX5154ACEE	0°C to +70°C	16 QSOP	±1/2
MAX5154BCPE	0°C to +70°C	16 QSOP	±1

Ordering Information continued on next page.

Functional Diagram



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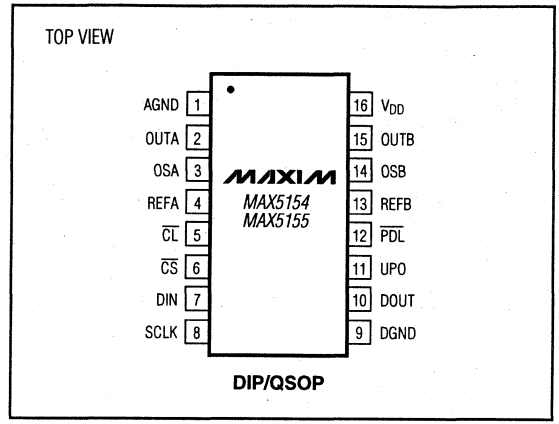
Low-Power, Dual, 12-Bit, Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5154AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX5154BEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5154AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX5154BEEE	-40°C to +85°C	16 QSOP	±1
MAX5154BMJE	-55°C to +125°C	16 CERDIP*	±1
MAX5155ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX5155BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX5155ACEE	0°C to +70°C	16 QSOP	±1
MAX5155BCPE	0°C to +70°C	16 QSOP	±2
MAX5155AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5155BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX5155AEEE	-40°C to +85°C	16 QSOP	±1
MAX5155BEEE	-40°C to +85°C	16 QSOP	±2
MAX5155BMJE	-55°C to +125°C	16 CERDIP*	±2

Contact factory for availability.

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Low-Power, Dual, 12-Bit, Voltage-Output DACs with Configurable Output

General Description

The MAX5156/MAX5157 low-power, serial, voltage-output, dual, 12-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5156) or +3V (MAX5157) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. Access to the output amplifier's inverting input allows for specific gain configurations, remote sensing, and high output current capability, making these devices ideal for industrial process controls. They are also well suited for digitally programmable, 4-20mA current loops.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously. Additional features include a programmable shutdown (2µA), a hardware-shutdown lockout, a separate voltage reference input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. These devices provide a programmable logic pin for added functionality and a serial-data output pin for daisy-chaining.

Applications

Industrial Process Control
Digital Offset and Gain Adjustment
Digitally Programmable, 4-20mA Current Loops
Motion Control
Remote Industrial Controls
Microprocessor-Controlled Systems
Automatic Test Equipment

Features

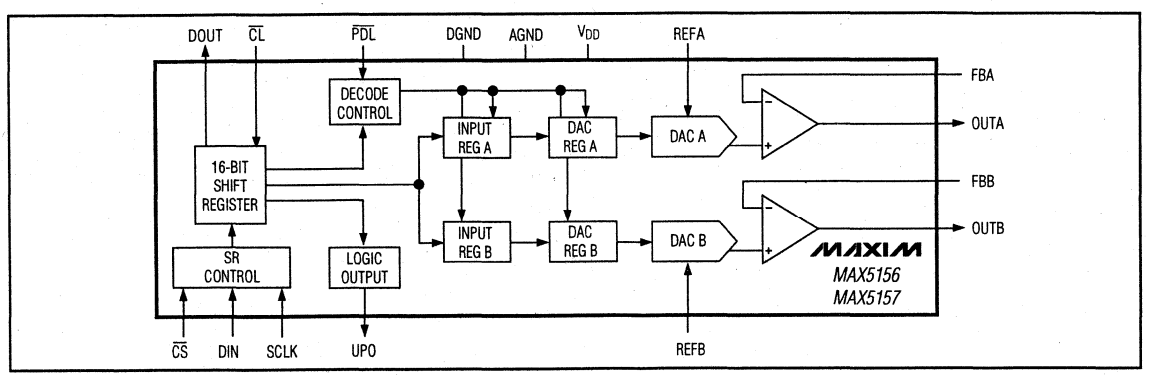
- ♦ **12-Bit Dual DAC with Configurable Output Amplifier**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **16µs Settling Time**
- ♦ **Single-Supply Operation: +5V (MAX5156)**
  +3V (MAX5157)
- ♦ **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Space-Saving 16-Pin QSOP Package**
- ♦ **Power-On Reset Clears DAC Outputs to Zero**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5156ACPE	0°C to +70°C	16 Plastic DIP	±1/2
MAX5156BCPE	0°C to +70°C	16 Plastic DIP	±1
MAX5156ACEE	0°C to +70°C	16 QSOP	±1/2
MAX5156BCPE	0°C to +70°C	16 QSOP	±1
MAX5156AEPE	-40°C to +85°C	16 Plastic DIP	±1/2
MAX5156BEPE	-40°C to +85°C	16 Plastic DIP	±1

Ordering Information continued on next page.

Functional Diagram



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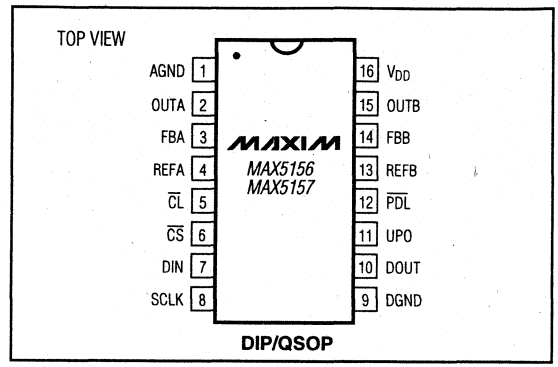
Low-Power, Dual, 12-Bit, Voltage-Output DACs with Configurable Output

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5156AEEE	-40°C to +85°C	16 QSOP	±1/2
MAX5156BEEE	-40°C to +85°C	16 QSOP	±1
MAX5156BMJE	-55°C to +125°C	16 CERDIP*	±1
MAX5157ACPE	0°C to +70°C	16 Plastic DIP	±1
MAX5157BCPE	0°C to +70°C	16 Plastic DIP	±2
MAX5157ACEE	0°C to +70°C	16 QSOP	±1
MAX5157BCPE	0°C to +70°C	16 QSOP	±2
MAX5157AEPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5157BEPE	-40°C to +85°C	16 Plastic DIP	±2
MAX5157AEEE	-40°C to +85°C	16 QSOP	±1
MAX5157BEEE	-40°C to +85°C	16 QSOP	±2
MAX5157BMJE	-55°C to +125°C	16 CERDIP*	±2

Contact factory for availability.

_Pin Configuration



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Power, Dual, 10-Bit, Voltage-Output DACs with Serial Interface

General Description

The MAX5158/MAX5159 low-power, serial, voltage-output, dual, 10-bit digital-to-analog converters (DACs) consume only 500µA from a single +5V (MAX5158) or +3V (MAX5159) supply. These devices feature Rail-to-Rail® output swing and are available in a space-saving 16-pin QSOP package. To maximize dynamic range, the DAC output amplifiers are configured with an internal gain of +2.

The 3-wire serial interface is SPI™/QSPI™ and Microwire™ compatible. Each DAC has a double-buffered input organized as an input register followed by a DAC register, which allows the input and DAC registers to be updated independently or simultaneously with a 16-bit serial word. Additional features include a 2µA programmable shutdown, hardware-shutdown lockout, a separate reference-voltage input for each DAC that accepts AC and DC signals, and an active-low clear input ($\overline{CL}$) that resets all registers and DACs to zero. The MAX5158/MAX5159 provide a programmable logic pin for added functionality and a serial-data output pin for daisy-chaining.

Applications

Digital Offset and Gain Adjustment

Digitally Programmable, 4-20mA Current Loops

Motion Control

Remote Industrial Controls

µP-Controlled Systems

Features

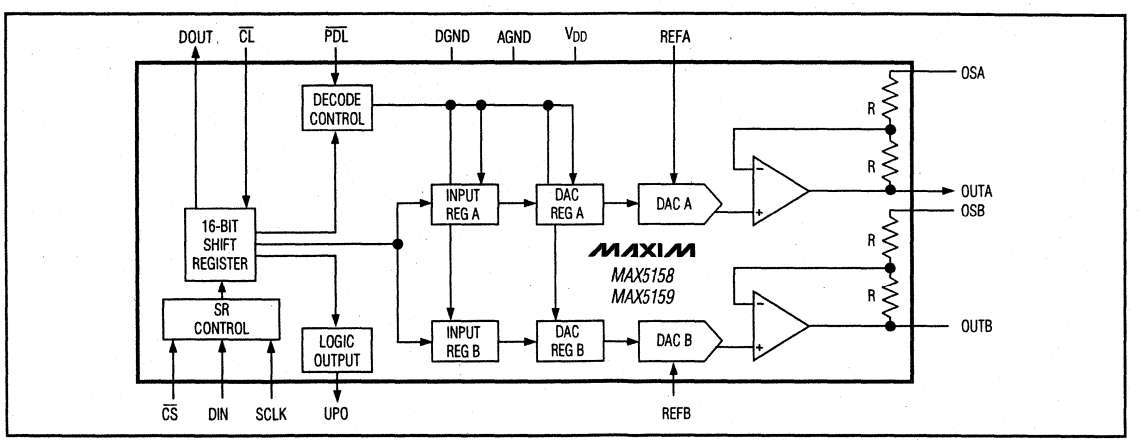
- ♦ **10-Bit Dual DAC with Internal Gain of +2**
- ♦ **Rail-to-Rail Output Swing**
- ♦ **16µs Settling Time**
- ♦ **Single-Supply Operation: +5V (MAX5158)**
  +3V (MAX5159)
- ♦ **Low Quiescent Current: 500µA (normal operation)**
  2µA (shutdown mode)
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Available in Space-Saving 16-Pin QSOP Package**
- ♦ **Power-On Reset Clears Registers and DACs to Zero**
- ♦ **Adjustable Output Offset**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5158CPE	0°C to +70°C	16 Plastic DIP	±1
MAX5158CPE	0°C to +70°C	16 QSOP	±1
MAX5158EPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5158EEE	-40°C to +85°C	16 QSOP	±1
MAX5158MJE	-55°C to +125°C	16 CERDIP*	±1

Ordering Information continued on next page.
**Contact factory for availability.*

Functional Diagram



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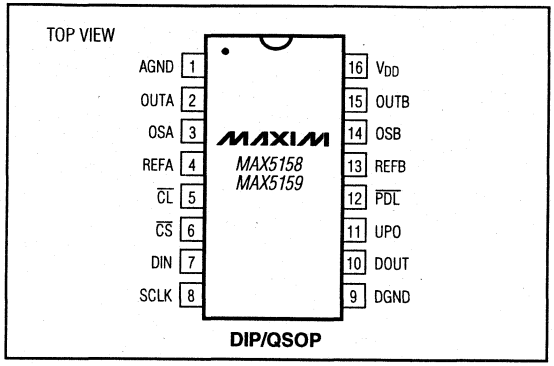
Low-Power, Dual, 10-Bit, Voltage-Output DACs with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5159CPE	0°C to +70°C	16 Plastic DIP	±1
MAX5159CEE	0°C to +70°C	16 QSOP	±1
MAX5159EPE	-40°C to +85°C	16 Plastic DIP	±1
MAX5159EEE	-40°C to +85°C	16 QSOP	±1
MAX5159MJE	-55°C to +125°C	16 CERDIP*	±1

Contact factory for availability.

Pin Configuration



19-1171; Rev 0; 12/96

MAXIM

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

General Description

The +5V MAX5250 combines four low-power, voltage-output, 10-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5250 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset that clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. All logic inputs are TTL/CMOS-logic compatible.

Applications

Digital Offset and Gain Adjustment
Microprocessor-Controlled Systems
Industrial Process Controls
Automatic Test Equipment
Remote Industrial Controls
Motion Control

Features

- ♦ **Four 10-Bit DACs with Configurable Output Amplifiers**
- ♦ **+5V Single-Supply Operation**
- ♦ **Low Supply Current: 0.85mA Normal Operation**
  10µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP and DIP Packages**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**
- ♦ **Schmitt-Trigger Inputs for Direct Optocoupler Interface**
- ♦ **12-Bit Upgrade Available: MAX525**

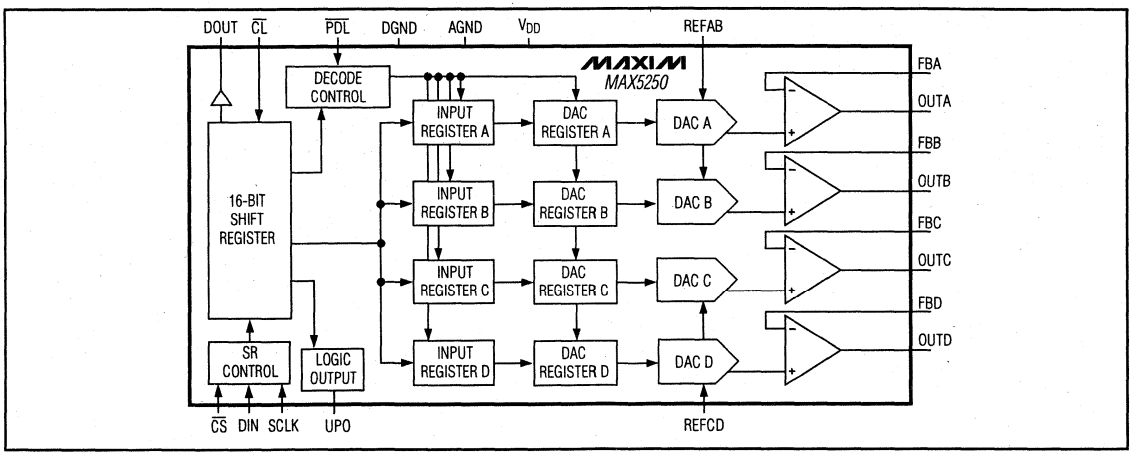
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5250ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX5250BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX5250ACAP	0°C to +70°C	20 SSOP	±1/2
MAX5250BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



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Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges
MAX5250_C_P .....0°C to +70°C
MAX5250_E_P .....-40°C to +85°C
MAX5250BMJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		10			Bits
Integral Nonlinearity (Note 1)	INL	MAX5250A		±0.25	±0.5	LSB
		MAX5250B			±1.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE				±1.0	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V		100	800	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 554 hex	10			kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		10		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				15		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.85	0.98	mA
Supply Current in Shutdown		(Note 3)		10	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 3 to code 1023 in unity-gain configuration.

Note 2: Accuracy is better than 1LSB for V_{OUT} = 6mV to V_{DD} - 60mV, guaranteed by a power-supply rejection test at the end points.

Note 3: R_L = ∞, digital inputs at DGND or V_{DD}.

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

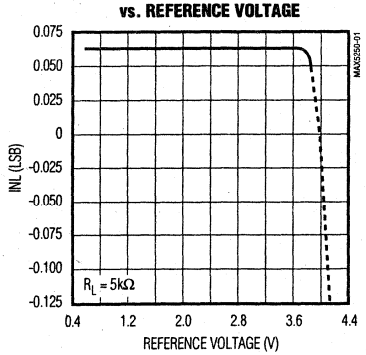
(V_{DD} = +5V ±10%, AGND = DGND = 0V, REFAB = REFCD = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Raise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_{LOAD} = 200pF			80	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_{LOAD} = 200pF			80	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

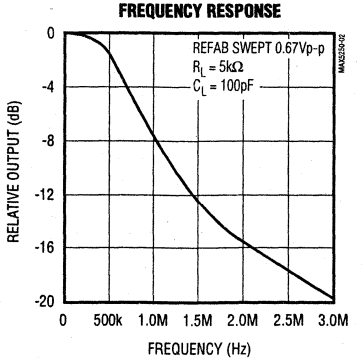
Typical Operating Characteristics

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

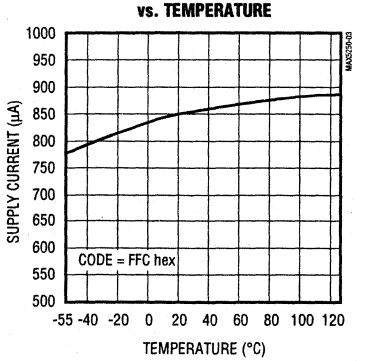
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



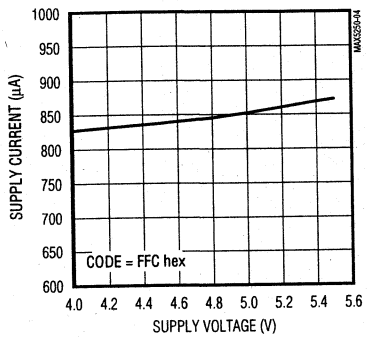
SUPPLY CURRENT vs. TEMPERATURE



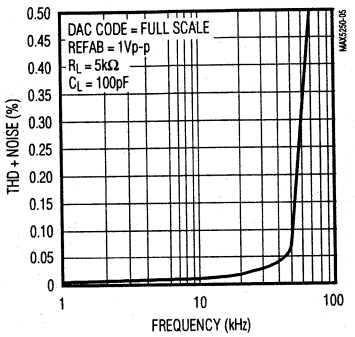
Typical Operating Characteristics (continued)

(V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

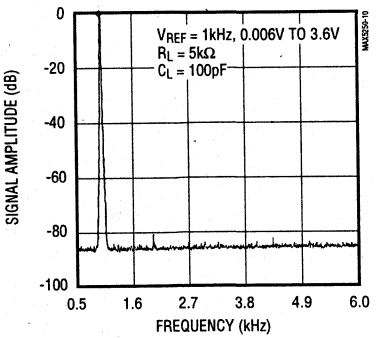
SUPPLY CURRENT vs. SUPPLY VOLTAGE



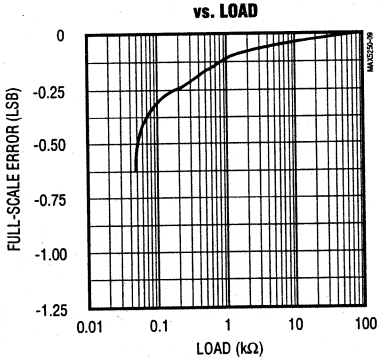
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



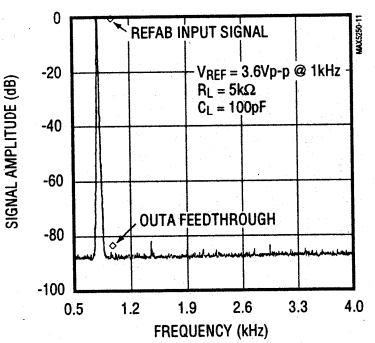
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

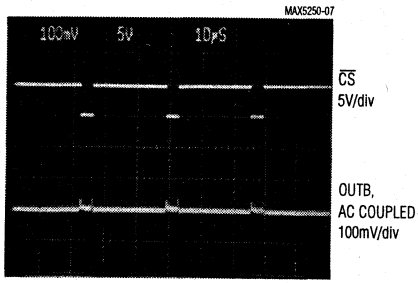


Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

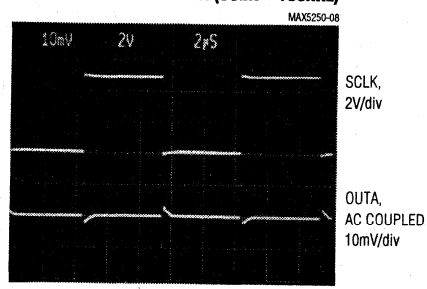
(V_{DD} = +5V, V_{REF} = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAJOR-CARRY TRANSITION



10µs/div

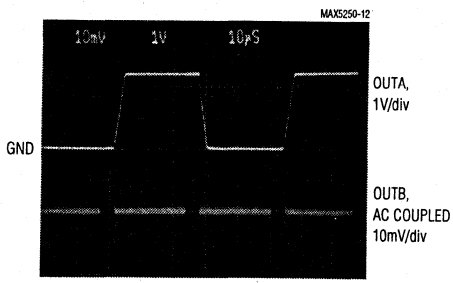
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

$\overline{CS}$ = $\overline{PDL}$ = $\overline{CL}$ = 5V, DIN = 0V
DAC A CODE SET TO 800 hex

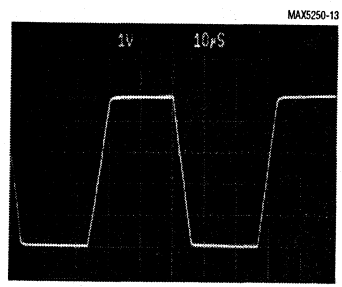
ANALOG CROSSTALK



10µs/div

DAC A CODE SWITCHING FROM 00C hex TO FFC hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clear All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial-Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

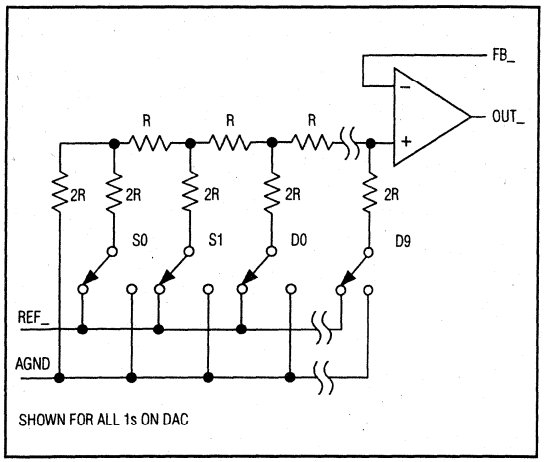


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX5250 contains four 10-bit, voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert a digital input (10 data bits plus 2 sub-bits) into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT_} = (V_{REF} \times NB / 1024) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 1023), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 554 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 000 hex. Because the input impedance at the reference pins is code dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. A voltage reference with a load regulation of 6ppm/mA, such as the MAX873, would typically deviate by 0.006LSB (0.015LSB worst case) when driving both MAX5250 reference inputs simultaneously at 2.5V. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX5250's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF at full scale.

Output Amplifiers

All MAX5250 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to each output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5250 output, the typical settling time to ±1/2LSB is 10µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX5250 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Power-Down Mode

The MAX5250 features a software-programmable shutdown that reduces supply current to a typical value of 10µA. The power-down lockout pin ($\overline{PDL}$) must be high to enable shutdown mode. Writing 1100XXXXXXXXXXXX as the input-control word puts the MAX5250 in power-down mode (Table 1).

In power-down mode, the MAX5250 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in power-down, allowing the MAX5250 to recall the output states prior to entering shutdown. Start up from power-down either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 15µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX5250's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 10+2 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX5250's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX5250's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX5250's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX5250 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 10+2 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 10+2 data bits D9...D0, S1, S0 (Figure 4). Set both sub-bits (S1, S0) to zero. The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when coming out of shutdown mode.

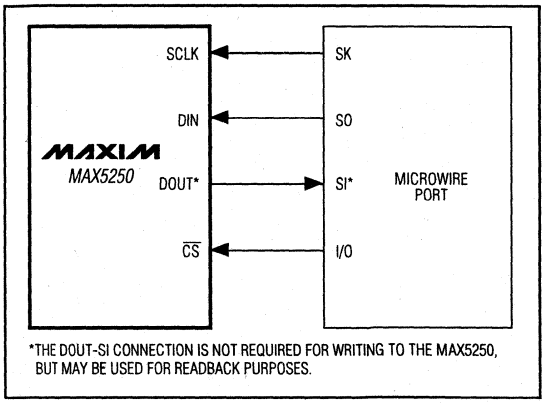


Figure 2. Connections for Microwire

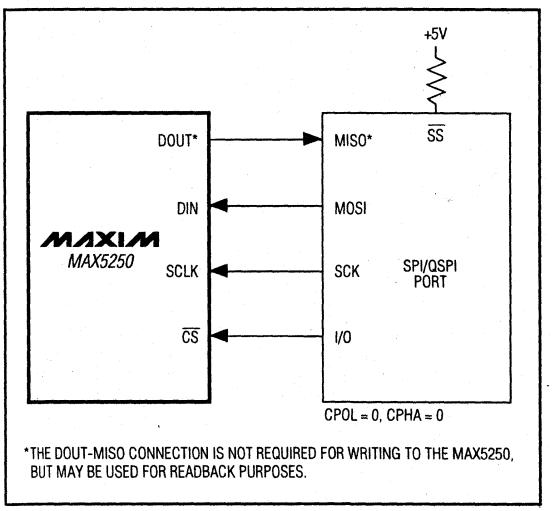


Figure 3. Connections for SPI/QSPI

MSB ..... LSB			
← 16 Bits of Serial Data →			
Address Bits		Control Bits	Data Bits MSB ..... LSB
A1	A0	C1 C0	D9 ..... D0, S1, S0
← 4 Address/Control Bits →			← 10+2 Data Bits →

Figure 4. Serial-Data Format

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD							FUNCTION
A1	A0	C1	C0	D9.....D0 MSB.....LSB	S1	S0	
0	0	0	1	10-bit DAC data	0	0	Load input register A; DAC registers unchanged.
0	1	0	1	10-bit DAC data	0	0	Load input register B; DAC registers unchanged.
1	0	0	1	10-bit DAC data	0	0	Load input register C; DAC registers unchanged.
1	1	0	1	10-bit DAC data	0	0	Load input register D; DAC registers unchanged.
0	0	1	1	10-bit DAC data	0	0	Load input register A; all DAC registers updated.
0	1	1	1	10-bit DAC data	0	0	Load input register B; all DAC registers updated.
1	0	1	1	10-bit DAC data	0	0	Load input register C; all DAC registers updated.
1	1	1	1	10-bit DAC data	0	0	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXX	X	X	Update all DAC registers from their respective input registers (also exit shutdown mode).
1	0	0	0	10-bit DAC data	0	0	Load all DAC registers from shift register (also exit shutdown mode).
1	1	0	0	XXXXXXXXXX	X	X	Enter shutdown mode (provided $\overline{PDL}$ = 1).
0	0	1	0	XXXXXXXXXX	X	X	UPO goes low (default).
0	1	1	0	XXXXXXXXXX	X	X	UPO goes high.
0	0	0	0	XXXXXXXXXX	X	X	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXX	X	X	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXX	X	X	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX5250 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX5250 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX5250 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX5250 serial interface (Table 1).

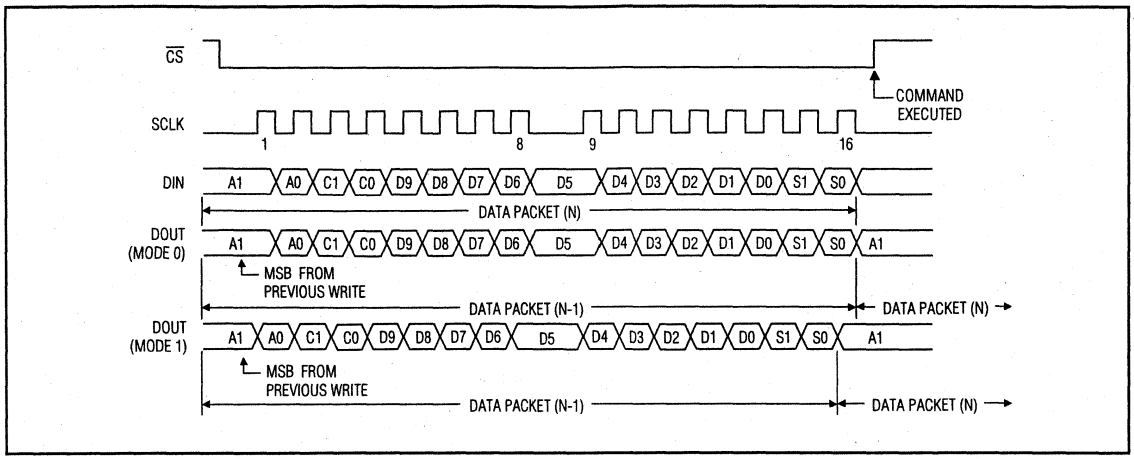


Figure 5. Serial-Interface Timing Diagram

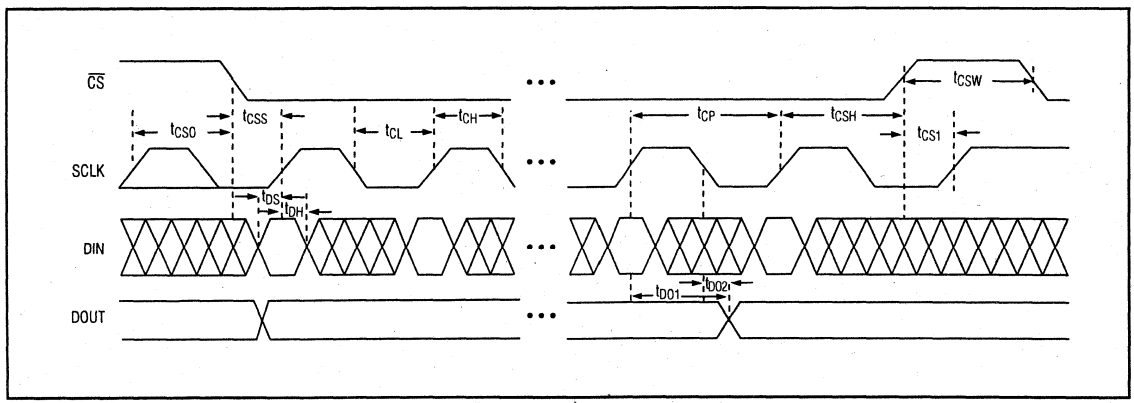


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down (PDL)

The power-down lockout pin $\overline{PDL}$ disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ can also be used to wake up the device asynchronously.

Daisy Chaining Devices

Any number of MAX5250s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5250's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX5250s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

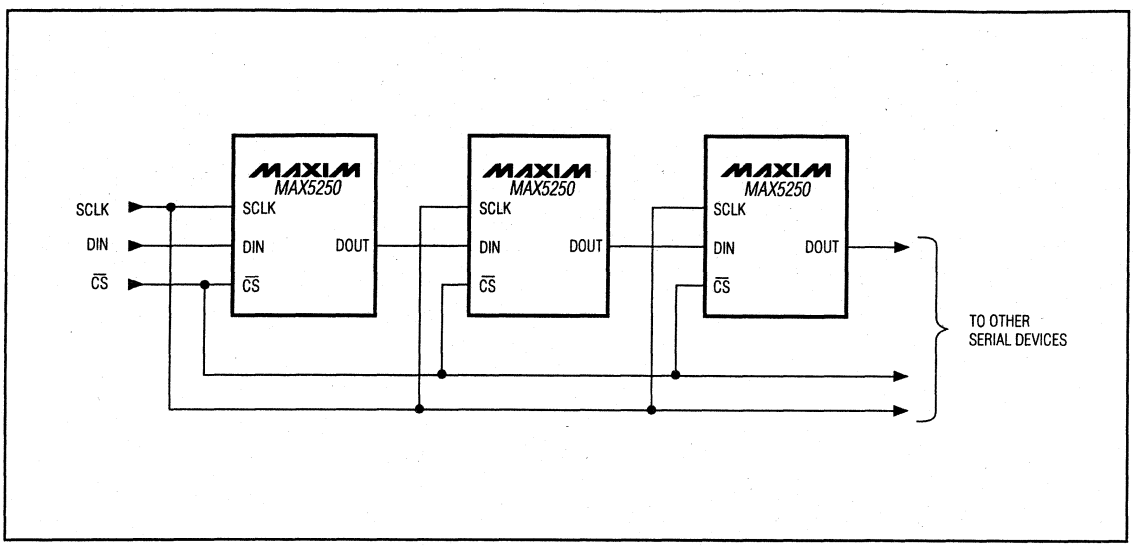


Figure 7. Daisy-Chaining MAX5250s

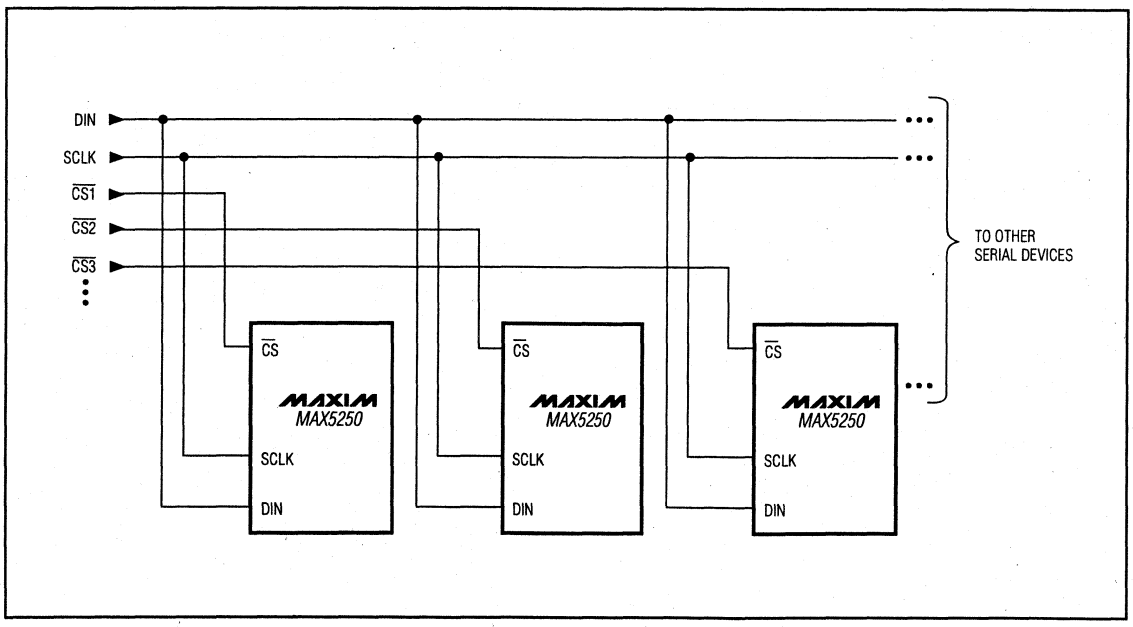


Figure 8. Multiple MAX5250s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX5250 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX5250 with the output amplifiers configured with a closed-loop gain of +2 to provide 0V to 5V full-scale range when a 2.5V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	11(00)	$+V_{REF}\left(\frac{1023}{1024}\right)$
1000	0000	01(00)	$+V_{REF}\left(\frac{513}{1024}\right)$
1000	0000	00(00)	$+V_{REF}\left(\frac{512}{1024}\right)=\frac{+V_{REF}}{2}$
0111	1111	11(00)	$+V_{REF}\left(\frac{511}{1024}\right)$
0000	0000	01(00)	$+V_{REF}\left(\frac{1}{1024}\right)$
0000	0000	00(00)	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB		LSB	ANALOG OUTPUT
1111	1111	11(00)	$+V_{REF}\left(\frac{511}{512}\right)$
1000	0000	01(00)	$+V_{REF}\left(\frac{1}{512}\right)$
1000	0000	00(00)	0V
0111	1111	11(00)	$-V_{REF}\left(\frac{1}{512}\right)$
0000	0000	01(00)	$-V_{REF}\left(\frac{511}{512}\right)$
0000	0000	00(00)	$-V_{REF}\left(\frac{512}{512}\right)=-V_{REF}$

( ) Sub-bits

Bipolar Output

The MAX5250 outputs can be configured for bipolar operation using Figure 11's circuit:

$$V_{OUT} = V_{REF}[(2NB / 1024) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

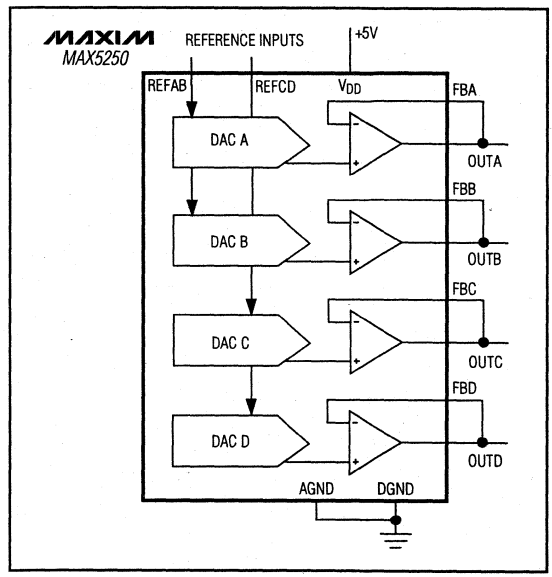


Figure 9. Unipolar Output Circuit

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

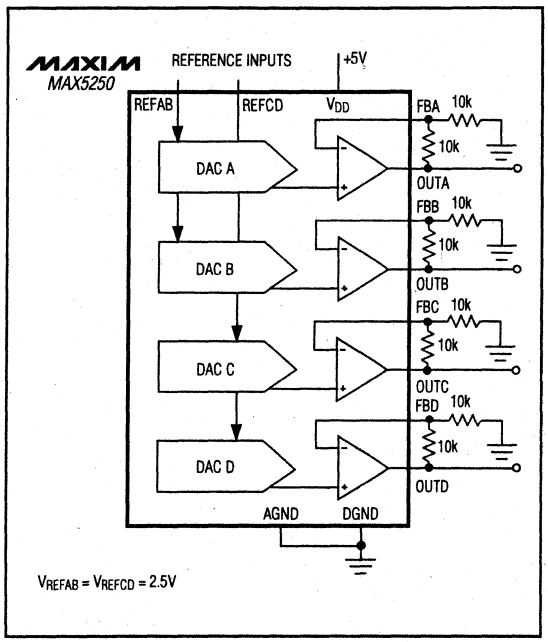


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX5250 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX5250's total harmonic distortion plus noise (THD + N) is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4–20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 1024)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

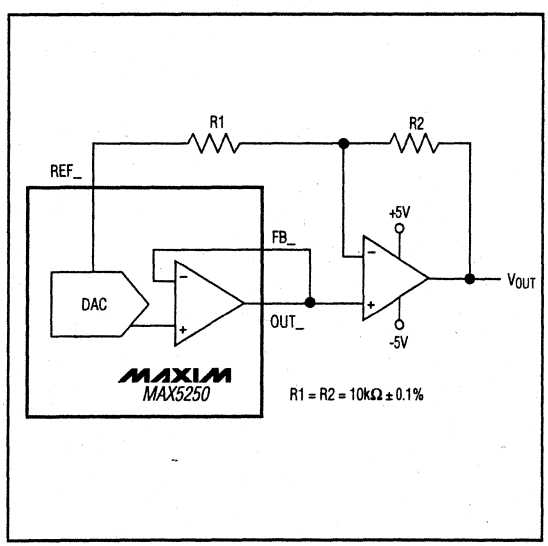


Figure 11. Bipolar Output Circuit

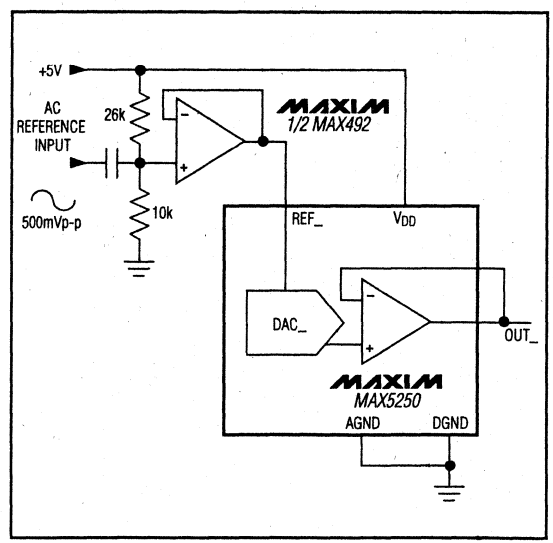


Figure 12. AC Reference Input Circuit

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

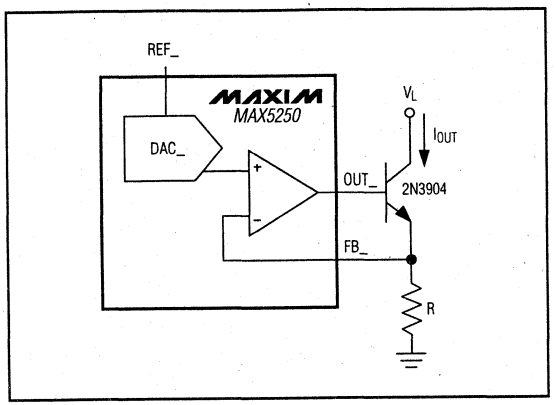
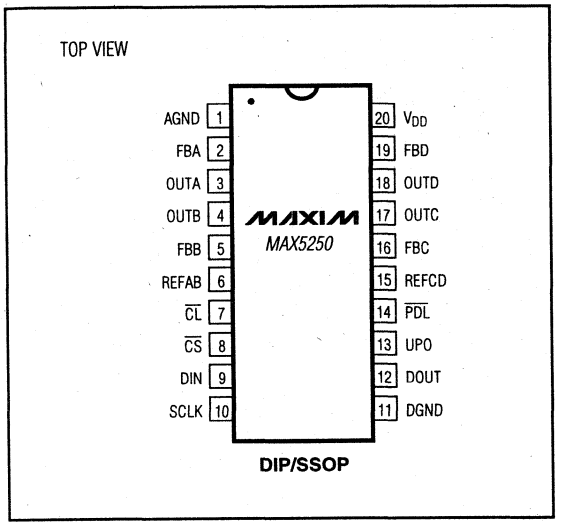


Figure 13. Digitally Programmable Current Source

Pin Configuration



Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

For rated MAX5250 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Low-Power, Quad, 10-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5250AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX5250BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX5250AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX5250BEAP	-40°C to +85°C	20 SSOP	±1
MAX5250BMJP	-55°C to +125°C	20 CERDIP*	±1

*Contact factory for availability and processing to MIL-STD-883.

_____Chip Information

TRANSISTOR COUNT: 4337

19-1172; Rev 0; 12/96

MAXIM

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

General Description

The +3V MAX5251 combines four low-power, voltage-output, 10-bit digital-to-analog converters (DACs) and four precision output amplifiers in a space-saving, 20-pin package. In addition to the four voltage outputs, each amplifier's negative input is also available to the user. This facilitates specific gain configurations, remote sensing, and high output drive capacity, making the MAX5251 ideal for industrial-process-control applications. Other features include software shutdown, hardware shutdown lockout, an active-low reset that clears all registers and DACs to zero, a user-programmable logic output, and a serial-data output.

Each DAC has a double-buffered input organized as an input register followed by a DAC register. A 16-bit serial word loads data into each input/DAC register. The 3-wire serial interface is compatible with SPI™/QSPI™ and Microwire™. It allows the input and DAC registers to be updated independently or simultaneously with a single software command. All logic inputs are TTL/CMOS-logic compatible.

Applications

Digital Offset and Gain Adjustment

Microprocessor-Controlled Systems

Industrial Process Controls

Automatic Test Equipment

Remote Industrial Controls

Motion Control

Features

- ♦ **Four 10-Bit DACs with Configurable Output Amplifiers**
- ♦ **+3.0V to +3.6V Single-Supply Operation**
- ♦ **Low Supply Current: 0.8mA Normal Operation**
  3µA Shutdown Mode
- ♦ **Available in 20-Pin SSOP**
- ♦ **Power-On Reset Clears all Registers and DACs to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Simultaneous or Independent Control of DACs via 3-Wire Serial Interface**
- ♦ **User-Programmable Digital Output**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- ♦ **12-Bit Upgrade Available: MAX5253**

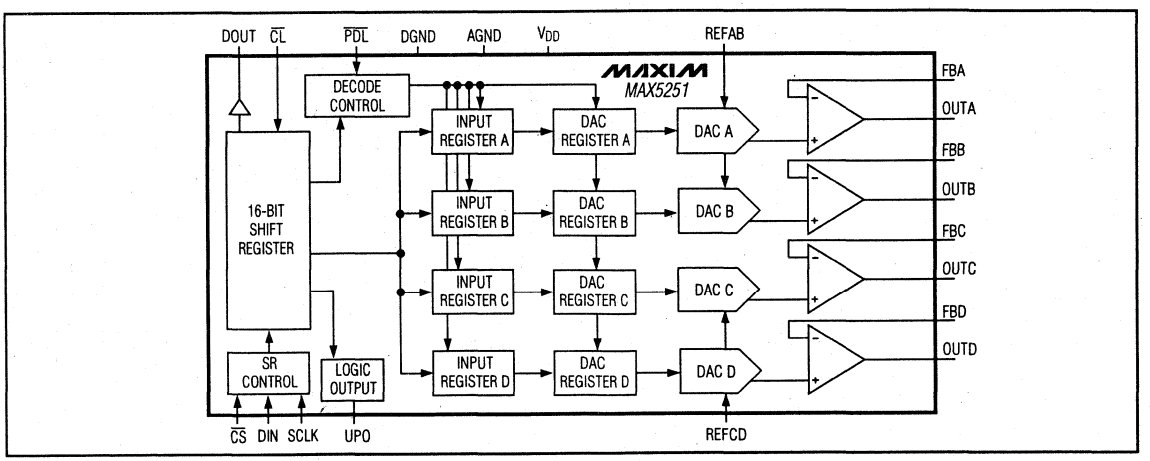
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5251ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX5251BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX5251ACAP	0°C to +70°C	20 SSOP	±1/2
MAX5251BCAP	0°C to +70°C	20 SSOP	±1

Ordering Information continued on last page.

Pin Configuration appears at end of data sheet.

Functional Diagram



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+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND .....-0.3V to +6V
V_{DD} to DGND .....-0.3V to +6V
AGND to DGND .....±0.3V
REFAB, REFCD to AGND .....-0.3V to (V_{DD} + 0.3V)
OUT_, FB_ to AGND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND .....-0.3V to +6V
DOUT, UPO to DGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Current into Any Pin .....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.00mW/°C above +70°C) 640mW
SSOP (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW

Operating Temperature Ranges
MAX5251_C_P .....0°C to +70°C
MAX5251_E_P .....-40°C to +85°C
MAX5251BMJP .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		10			Bits
Integral Nonlinearity (Note 1)	INL	MAX5251AC/E		±0.25	±0.5	LSB
		MAX5251BC/E			±1.0	
		MAX5251BMJP			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}				±6.0	mV
Offset-Error Tempco				6		ppm/°C
Gain Error (Note 1)	GE				±2.4	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	V_{DD} = +3.0V to +3.6V		100	800	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 554 hex	10			kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.01	±1.0	µA
Input Capacitance	C_{IN}			8		pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 2mA	V_{DD} - 0.5			V
Output Low Voltage	V_{OL}	I_{SINK} = 2mA		0.13	0.4	V
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		12		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB_				0	0.1	µA
OUT_ Leakage Current in Shutdown		R_L = ∞		0.01	±1	µA
Start-Up Time Exiting Shutdown Mode				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
Digital Crosstalk				5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}	(Note 3)	3.0		3.6	V
Supply Current	I_{DD}	(Note 4)		0.82	0.98	mA
Supply Current in Shutdown		(Note 4)		3	20	µA
Reference Current in Shutdown				0.01	±1	µA

Note 1: Guaranteed from code 5 to code 1023 in unity-gain configuration.
Note 2: Accuracy is better than 1LSB for V_{OUT} = 6mV to V_{DD} - 80mV, guaranteed by PSR test at the endpoints.
Note 3: Remains operational with supply voltage as low as +2.7V.
Note 4: R_L = ∞, digital inputs at DGND or V_{DD}.

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

ELECTRICAL CHARACTERISTICS (continued)

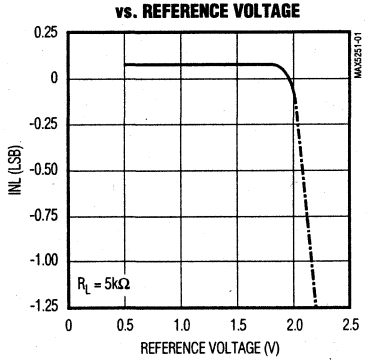
(V_{DD} = +3.0V to +3.6V, AGND = DGND = 0V, REFAB = REFCD = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 9).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to DOUT Valid Propagation Delay	t_{D01}	C_L = 200pF			120	ns
SCLK Fall to DOUT Valid Propagation Delay	t_{D02}	C_L = 200pF			120	ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

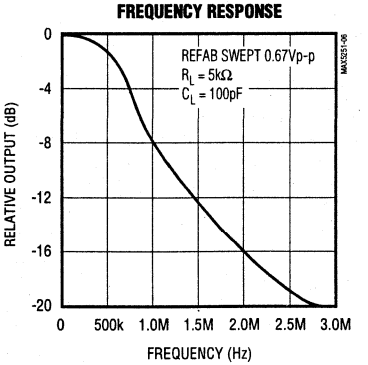
Typical Operating Characteristics

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

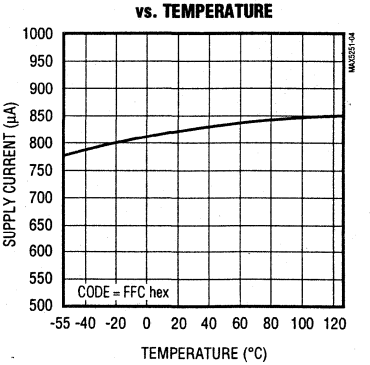
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



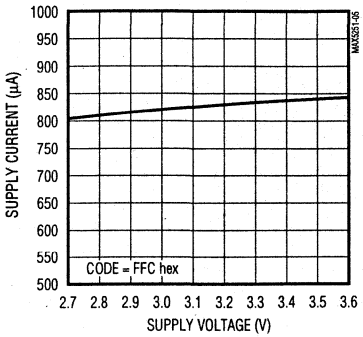
SUPPLY CURRENT vs. TEMPERATURE



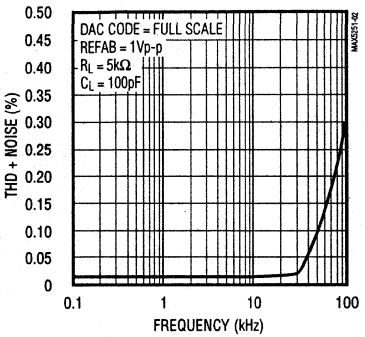
Typical Operating Characteristics (continued)

(V_{DD} = +3.3V, T_A = +25°C, unless otherwise noted.)

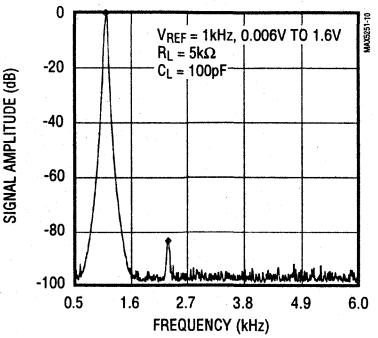
SUPPLY CURRENT vs. SUPPLY VOLTAGE



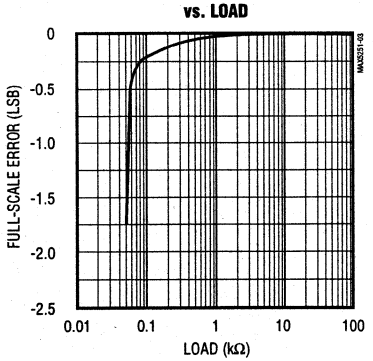
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



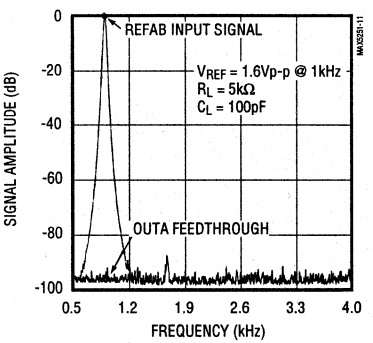
OUTPUT FFT PLOT



FULL-SCALE ERROR vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

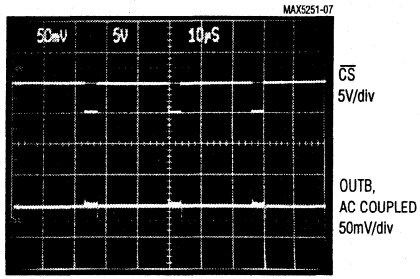


+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

Typical Operating Characteristics (continued)

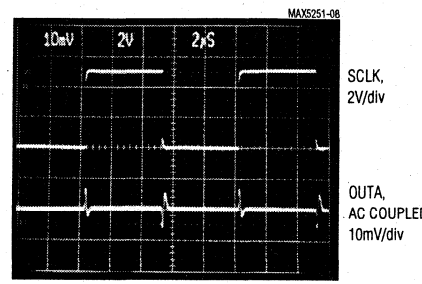
(V_{DD} = +3.3V, V_{REF} = 1.25V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAJOR-CARRY TRANSITION



10µs/div

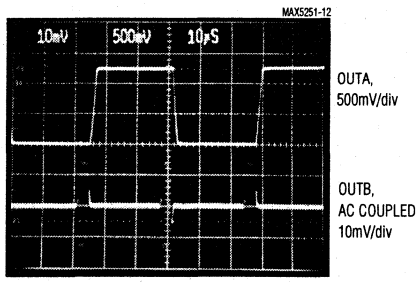
DIGITAL FEEDTHROUGH (SCLK = 100kHz)



2µs/div

CS = PDL = CL = 3.3V, DIN = 0V
DAC A CODE SET TO 800 hex

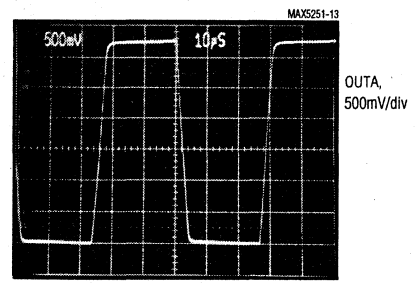
ANALOG CROSSTALK



10µs/div

DAC A CODE SWITCHING FROM 00C hex TO FFC hex
DAC B CODE SET TO 800 hex

DYNAMIC RESPONSE



10µs/div

SWITCHING FROM CODE 000 hex TO FB4 hex
OUTPUT AMPLIFIER GAIN = +2.6

Pin Description

PIN	NAME	FUNCTION
1	AGND	Analog Ground
2	FBA	DAC A Output Amplifier Feedback
3	OUTA	DAC A Output Voltage
4	OUTB	DAC B Output Voltage
5	FBB	DAC B Output Amplifier Feedback
6	REFAB	Reference Voltage Input for DAC A and DAC B
7	$\overline{CL}$	Clears All DACs and Registers. Resets all outputs (OUT_, UPO, DOUT) to 0, active low.
8	$\overline{CS}$	Chip-Select Input. Active low.
9	DIN	Serial-Data Input
10	SCLK	Serial-Clock Input
11	DGND	Digital Ground
12	DOUT	Serial-Data Output
13	UPO	User-Programmable Logic Output
14	$\overline{PDL}$	Power-Down Lockout. Active low. Locks out software shutdown if low.
15	REFCD	Reference Voltage Input for DAC C and DAC D
16	FBC	DAC C Output Amplifier Feedback
17	OUTC	DAC C Output Voltage
18	OUTD	DAC D Output Voltage
19	FBD	DAC D Output Amplifier Feedback
20	V_{DD}	Positive Power Supply

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

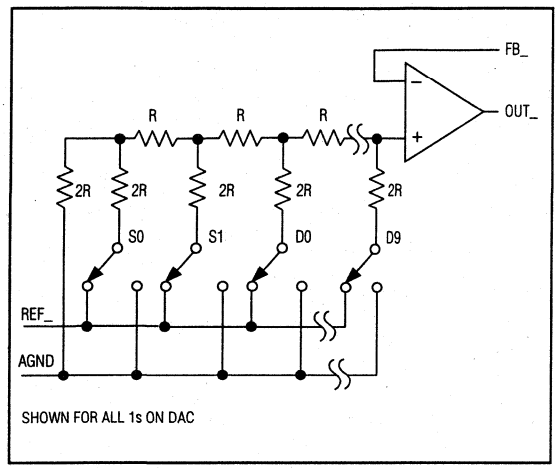


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX5251 contains four voltage-output digital-to-analog converters (DACs) that are easily addressed using a simple 3-wire serial interface. It includes a 16-bit data-in/data-out shift register, and each DAC has a doubled-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the four voltage outputs, each amplifier's negative input is available to the user.

The DACs are inverted R-2R ladder networks that convert a digital input (10 data bits plus 2 sub-bits) into equivalent analog output voltages in proportion to the applied reference voltage inputs. DACs A and B share the REFAB reference input, while DACs C and D share the REFCD reference input. The two reference inputs allow different full-scale output voltage ranges for each pair of DACs. Figure 1 shows a simplified circuit diagram of one of the four DACs.

Reference Inputs

The two reference inputs accept positive DC and AC signals. The voltage at each reference input sets the full-scale output voltage for its two corresponding DACs. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltages ($V_{OUT_}$) are represented by a digitally programmable voltage source as:

$$V_{OUT_} = (V_{REF} \times NB / 1024) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 1023), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at each reference input is code dependent, ranging from a low value of 10kΩ when both DACs connected to the reference have an input code of 554 hex, to a high value exceeding several giga ohms (leakage current) with an input code of 000 hex. Because the input impedance at the reference pins is code dependent, load regulation of the reference source is important.

The REFAB and REFCD reference inputs have a 10kΩ guaranteed minimum input impedance. When the two reference inputs are driven from the same source, the effective minimum impedance is 5kΩ. Driving the REFAB and REFCD pins separately improves reference accuracy.

In shutdown mode, the MAX5251's REFAB and REFCD inputs enter a high-impedance state with a typical input leakage current of 0.01µA.

The reference input capacitance is also code dependent and typically ranges from 20pF with an input code of all 0s to 100pF at full scale.

Output Amplifiers

All MAX5251 DAC outputs are internally buffered by precision amplifiers with a typical slew rate of 0.6V/µs. Access to each output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5251 output, the typical settling time to ±1/2LSB is 12µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The MAX5251 output amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Power-Down Mode

The MAX5251 features a software-programmable shutdown that reduces supply current to a typical value of 3µA. The power-down lockout pin ($\overline{PDL}$) must be high to enable shutdown mode. Writing 1100XXXXXXXXXXX as the input-control word puts the MAX5251 in shutdown mode (Table 1).

In shutdown mode, the MAX5251 output amplifiers and the reference inputs enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5251 to recall the output states prior to entering shutdown. Exit shutdown mode either by recalling the previous configuration or by updating the DACs with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX5251's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of two address bits and two control bits followed by 10+2 data bits (MSB first), as shown in Figure 4. The 4-bit address/control code determines the MAX5251's response outlined in Table 1. The connection between DOUT and the serial-interface port is not necessary, but may be used for data echo. Data held in the MAX5251's shift register can be shifted out of DOUT and returned to the microprocessor (µP) for data verification.

The MAX5251's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register(s) can be loaded without affecting the DAC register(s), the DAC register(s) can be loaded directly, or all four DAC registers can be updated simultaneously from the input registers (Table 1).

Serial-Interface Description

The MAX5251 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 10+2 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of two DAC address bits (A1, A0) and two control bits (C1, C0), followed by the 10+2 data bits D9...D0, S1, S0 (Figure 4). Set both sub-bits (S0, S1) to zero. The 4-bit address/control code determines:

- The register(s) to be updated
- The clock edge on which data is to be clocked out via the serial-data output (DOUT)
- The state of the user-programmable logic output (UPO)
- If the part is to go into shutdown mode (assuming $\overline{PDL}$ is high)
- How the part is configured when exiting shutdown mode.

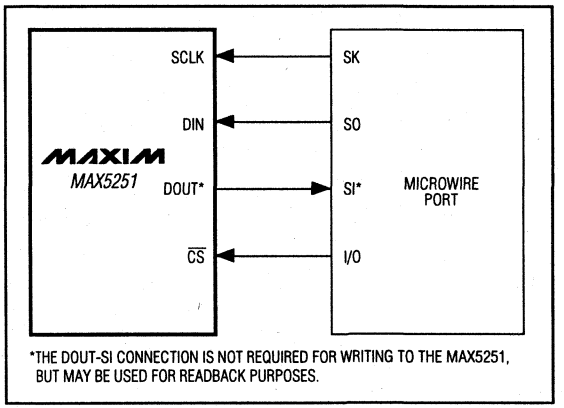


Figure 2. Connections for Microwire

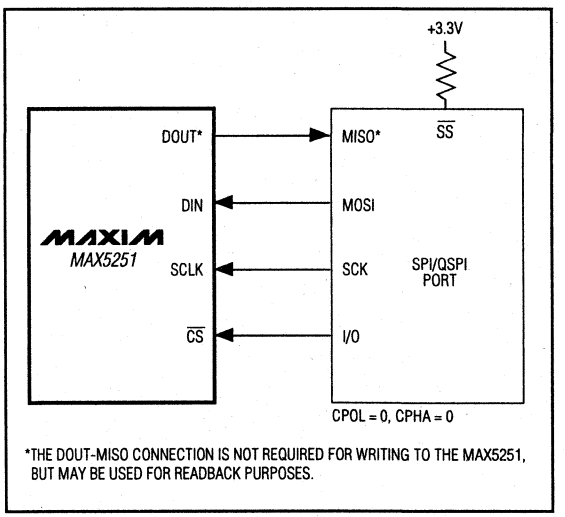


Figure 3. Connections for SPI/QSPI

MSB ..... LSB			
← 16 Bits of Serial Data →			
Address Bits		Control Bits	Data Bits MSB ..... LSB
A1	A0	C1 C0	D9 ..... D0 S1 S0
← 4 Address/ Control Bits →			← 10+2 Data Bits →

Figure 4. Serial-Data Format

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD						FUNCTION
A1	A0	C1	C0	D9.....D0 MSB.....LSB	S1	S0	
0	0	0	1	10-bit DAC data	0	0	Load input register A; DAC registers unchanged.
0	1	0	1	10-bit DAC data	0	0	Load input register B; DAC registers unchanged.
1	0	0	1	10-bit DAC data	0	0	Load input register C; DAC registers unchanged.
1	1	0	1	10-bit DAC data	0	0	Load input register D; DAC registers unchanged.
0	0	1	1	10-bit DAC data	0	0	Load input register A; all DAC registers updated.
0	1	1	1	10-bit DAC data	0	0	Load input register B; all DAC registers updated.
1	0	1	1	10-bit DAC data	0	0	Load input register C; all DAC registers updated.
1	1	1	1	10-bit DAC data	0	0	Load input register D; all DAC registers updated.
0	1	0	0	XXXXXXXXXX	X	X	Update all DAC registers from their respective input registers (also exit shutdown mode).
1	0	0	0	10-bit DAC data	0	0	Load all DAC registers from shift register (also exit shutdown mode).
1	1	0	0	XXXXXXXXXX	X	X	Enter shutdown mode (provided $\overline{PDL}$ = 1).
0	0	1	0	XXXXXXXXXX	X	X	UPO goes low (default).
0	1	1	0	XXXXXXXXXX	X	X	UPO goes high.
0	0	0	0	XXXXXXXXXX	X	X	No operation (NOP) to DAC registers
1	1	1	0	XXXXXXXXXX	X	X	Mode 1, DOUT clocked out on SCLK's rising edge. All DAC registers updated.
1	0	1	0	XXXXXXXXXX	X	X	Mode 0, DOUT clocked out on SCLK's falling edge. All DAC registers updated (default).

"X" = Don't care

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the appropriate MAX5251 input/DAC registers on $\overline{CS}$'s rising edge.

The programming command Load-All-DACs-From-Shift-Register allows all input and DAC registers to be simultaneously loaded with the same digital code from the input shift register. The no operation (NOP) command leaves the register contents unaffected and is useful when the MAX5251 is configured in a daisy chain (see the *Daisy Chaining Devices* section). The command to change the clock edge on which serial data is shifted out of DOUT also loads data from all input registers to their respective DAC registers.

Serial-Data Output (DOUT)

The serial-data output, DOUT, is the internal shift register's output. The MAX5251 can be programmed so that data is clocked out of DOUT on SCLK's rising edge (Mode 1) or falling edge (Mode 0). In Mode 0, output data at DOUT lags input data at DIN by 16.5 clock cycles, maintaining compatibility with Microwire, SPI/QSPI, and other serial interfaces. In Mode 1, output data lags input data by 16 clock cycles. On power-up, DOUT defaults to Mode 0 timing.

User-Programmable Logic Output (UPO)

The user-programmable logic output, UPO, allows an external device to be controlled via the MAX5251 serial interface (Table 1).

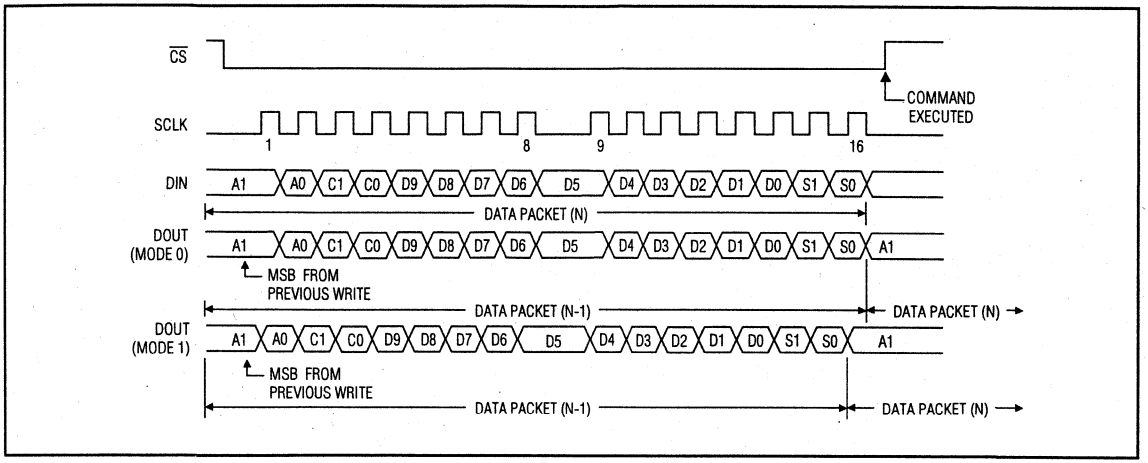


Figure 5. Serial-Interface Timing Diagram

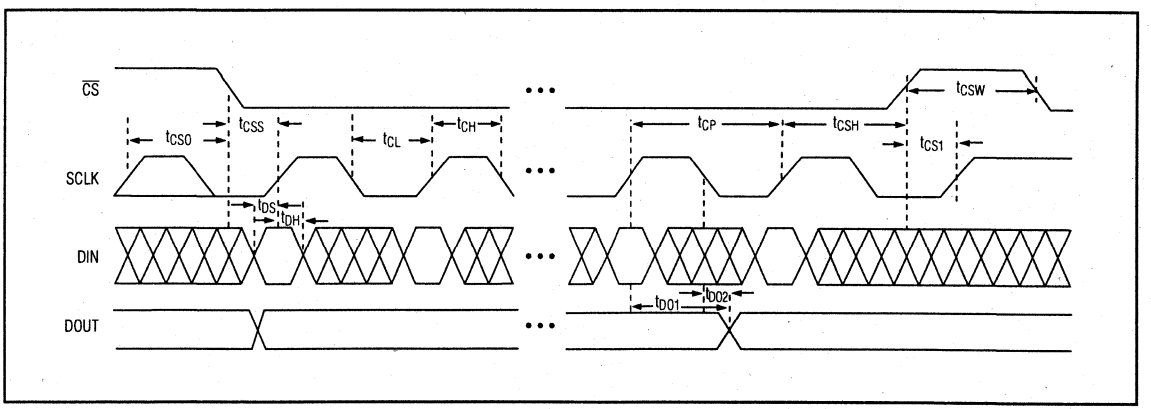


Figure 6. Detailed Serial-Interface Timing Diagram

Power-Down Lockout ($\overline{PDL}$)

The power-down lockout pin $\overline{PDL}$ disables software shutdown when low. When in shutdown, transitioning $\overline{PDL}$ from high to low wakes up the part with the output set to the state prior to shutdown. $\overline{PDL}$ could also be used to wake up the device asynchronously.

Daisy Chaining Devices

Any number of MAX5251s can be daisy chained by connecting the DOUT pin of one device to the DIN pin of the following device in the chain (Figure 7).

Since the MAX5251's DOUT pin has an internal active pull-up, the DOUT sink/source capability determines the time required to discharge/charge a capacitive load. Refer to the serial-data-out V_{OH} and V_{OL} specifications in the *Electrical Characteristics*.

Figure 8 shows an alternate method of connecting several MAX5251s. In this configuration, the data bus is common to all devices; data is not shifted through a daisy chain. More I/O lines are required in this configuration because a dedicated chip-select input ($\overline{CS}$) is required for each IC.

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

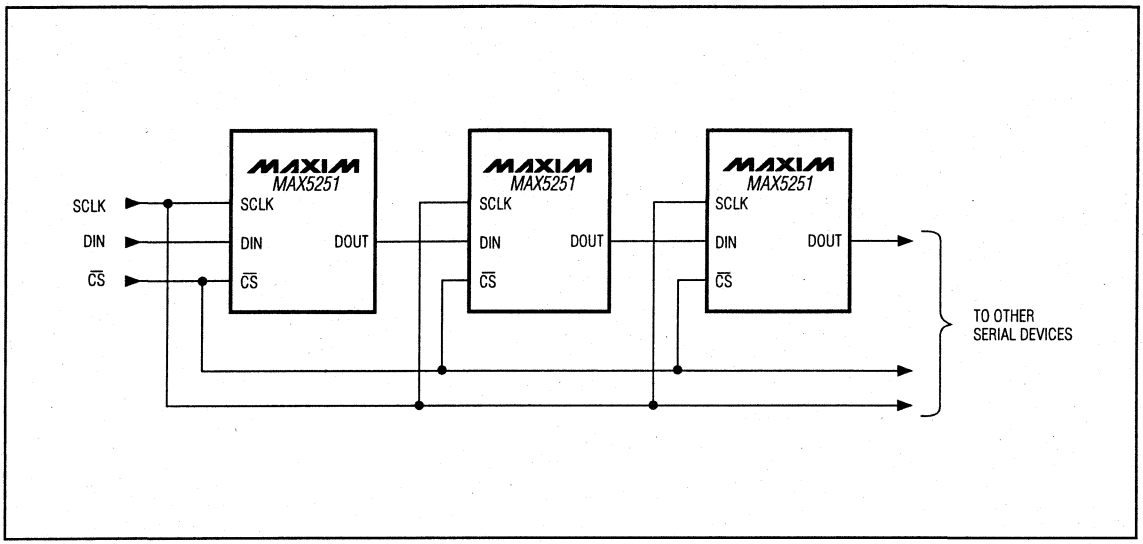


Figure 7. Daisy-Chaining MAX5251s

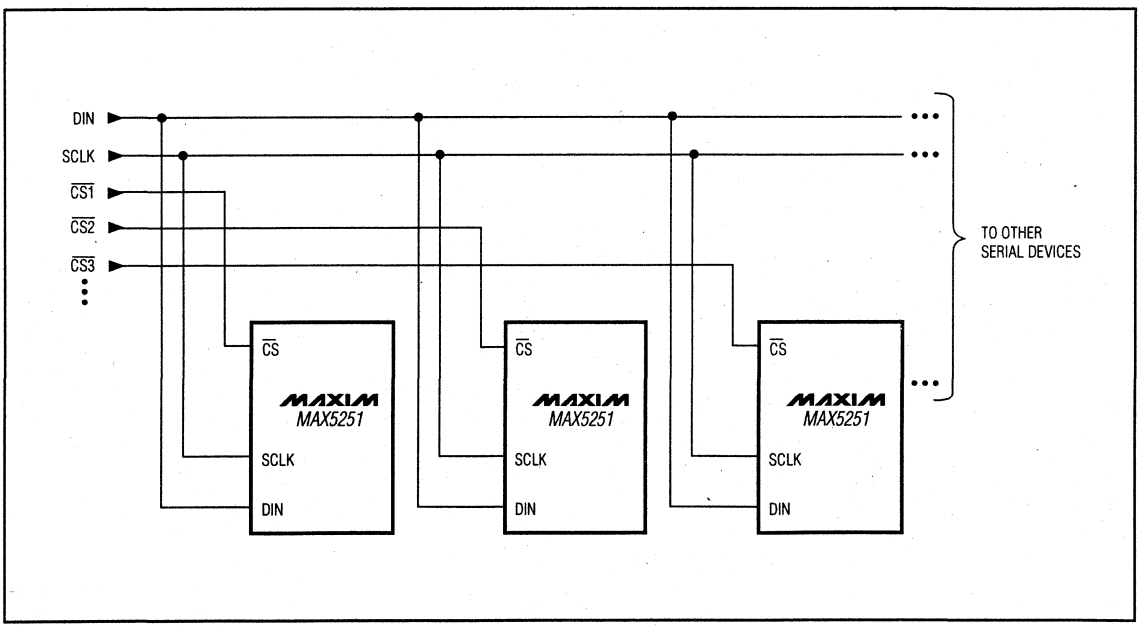


Figure 8. Multiple MAX5251s Sharing a Common DIN Line

Applications Information

Unipolar Output

For a unipolar output, the output voltages and the reference inputs have the same polarity. Figure 9 shows the MAX5251 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

For rail-to-rail outputs, see Figure 10. This circuit shows the MAX5251 with the output amplifiers configured with a closed-loop gain of +2.6 to provide 0V to 3.25V full-scale range when a 1.25V reference is used.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 11(00)	$+V_{REF}\left(\frac{1023}{1024}\right)$
1000 0000 01(00)	$+V_{REF}\left(\frac{513}{1024}\right)$
1000 0000 00(00)	$+V_{REF}\left(\frac{512}{1024}\right)=\frac{+V_{REF}}{2}$
0111 1111 11(00)	$+V_{REF}\left(\frac{511}{1024}\right)$
0000 0000 01(00)	$+V_{REF}\left(\frac{1}{1024}\right)$
0000 0000 00(00)	0V

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 11(00)	$+V_{REF}\left(\frac{511}{512}\right)$
1000 0000 01(00)	$+V_{REF}\left(\frac{1}{512}\right)$
1000 0000 00(00)	0V
0111 1111 11(00)	$-V_{REF}\left(\frac{1}{512}\right)$
0000 0000 01(00)	$-V_{REF}\left(\frac{511}{512}\right)$
0000 0000 00(00)	$-V_{REF}\left(\frac{512}{512}\right)=-V_{REF}$

( ) Sub-bits

Bipolar Output

The MAX5251 outputs can be configured for bipolar operation using Figure 11's circuit:

$$V_{OUT} = V_{REF}[(2NB / 1024) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 11's circuit.

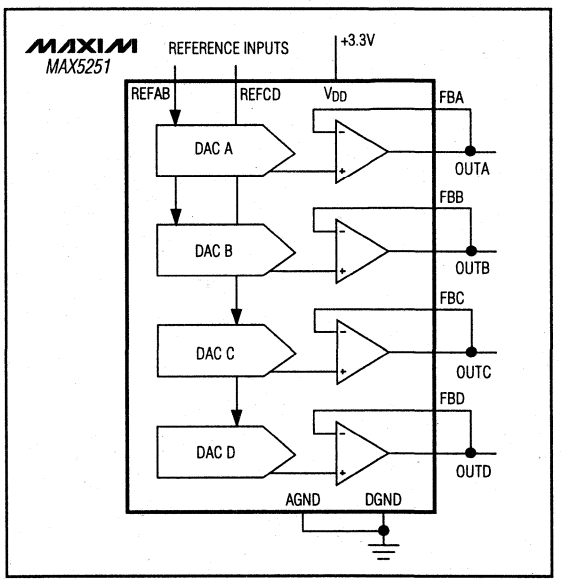


Figure 9. Unipolar Output Circuit

+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

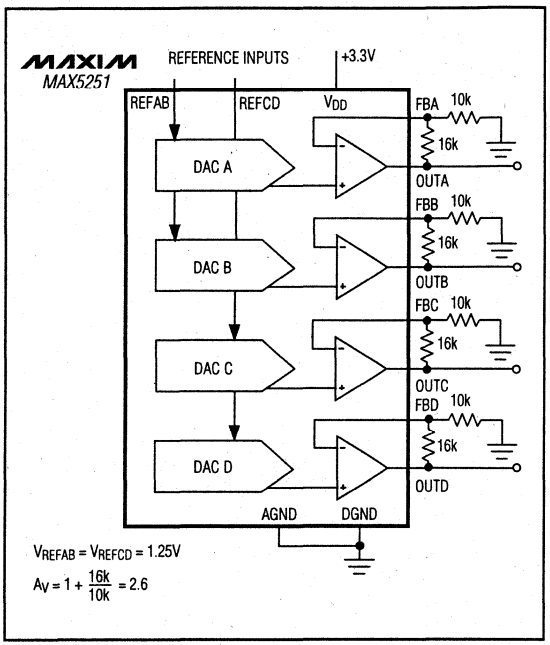


Figure 10. Unipolar Rail-to-Rail Output Circuit

Using an AC Reference

In applications where the reference has AC signal components, the MAX5251 has multiplying capability within the reference input range specifications. Figure 12 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REFAB/REFCD. The reference voltage must never be more negative than DGND.

The MAX5251's total harmonic distortion plus noise (THD + N) is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 13 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. This circuit can be used to drive 4–20mA current loops, which are commonly used in industrial-control applications. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R) \times (NB / 1024)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 13.

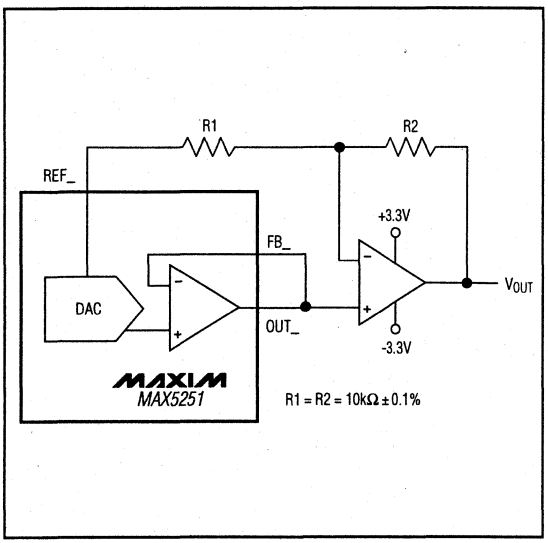


Figure 11. Bipolar Output Circuit

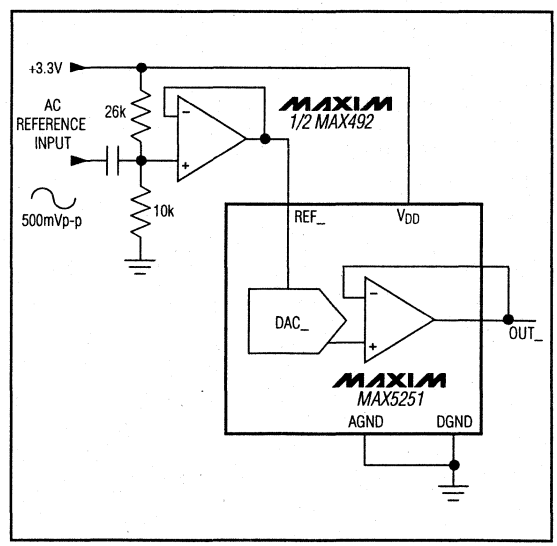


Figure 12. AC Reference Input Circuit

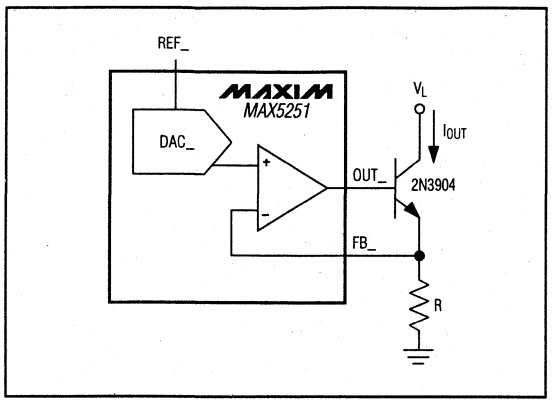


Figure 13. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, all input and DAC registers are cleared (set to zero code) and DOUT is in Mode 0 (serial data is shifted out of DOUT on the clock's falling edge).

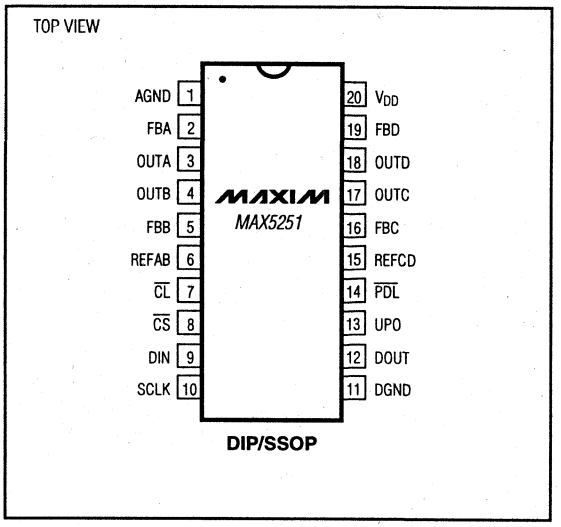
For rated MAX5251 performance, limit REFAB/REFCD to less than 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. Tie AGND and DGND together at the DAC, then tie this point to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Pin Configuration



+3V, Quad, 10-Bit Voltage-Output DAC with Serial Interface

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5251AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX5251BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX5251AEAP	-40°C to +85°C	20 SSOP	±1/2
MAX5251BEAP	-40°C to +85°C	20 SSOP	±1
MAX5251BMJP	-55°C to +125°C	20 CERDIP*	±2

*Contact factory for availability and processing to MIL-STD-883.

_____Chip Information

TRANSISTOR COUNT: 4337

19-1196; Rev 0; 2/97

MAXIM

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

General Description

The MAX5352/MAX5353 combine a low-power, voltage-output, 12-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX5352 operates from a single +5V supply, and the MAX5353 operates from a single +3.3V supply. Both devices draw less than 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5352/MAX5353 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with SPI™/QSPI™ and Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Industrial Process Controls

Automatic Test Equipment

Digital Offset and Gain Adjustment

Motion Control

Remote Industrial Controls

Microprocessor-Controlled Systems

Features

- **12-Bit DAC with Configurable Output Amplifier**
- **+5V Single-Supply Operation (MAX5352)**
  +3.3V Single-Supply Operation (MAX5353)
- **Low Supply Current: 0.28mA Normal Operation**
  2µA Shutdown Mode
- **Available in 8-Pin µMAX**
- **Power-On Reset Clears DAC Output to Zero**
- **SPI/QSPI and Microwire Compatible**
- **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- **+3.3V MAX5353 Directly Interfaces with +5V Logic**

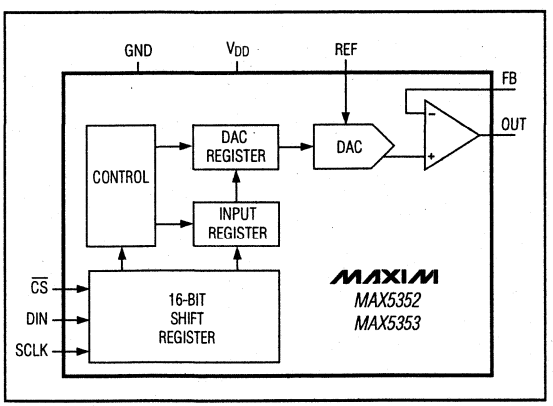
Ordering Information

PART*	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352ACPA	0°C to +70°C	8 Plastic DIP	±1/2
MAX5352BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX5352ACUA	0°C to +70°C	8 µMAX	±1/2
MAX5352BCUA	0°C to +70°C	8 µMAX	±1

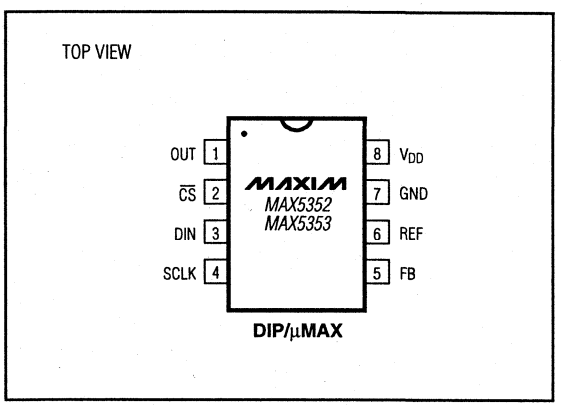
Ordering Information continued at end of data sheet.

**Contact factory for availability of 8-pin SO package.*

Functional Diagram



Pin Configuration



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For small orders, phone 408-737-7600 ext. 3468.

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V, +6V
REF, OUT, FB to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C).....727mW
µMAX (derate 4.10mW/°C above +70°C) 330mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX5352_C_A/MAX5353_C_A.....0°C to +70°C
MAX5352_E_A/MAX5353_E_A .....-40°C to +85°C
MAX5352BMJA/MAX5353BMJA .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX5352

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 1)	INL	MAX5352A			±0.5	LSB
		MAX5352B			±1.0	
		MAX5352BMJA			±2.0	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 1)	GE			-0.3	±3	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1554 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		77		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS: MAX5352 (continued)

(V_{DD} = +5V ±10%, REF = 2.5V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		14		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.28	0.4	mA
Supply Current in Shutdown		(Note 3)		4	20	µA
Reference Current in Shutdown				0.001	±0.5	µA
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 11 to code 4095 in unity-gain configuration.

Note 2: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 100mV, guaranteed by a power-supply rejection test at the end points.

Note 3: R_L = ∞, digital inputs at GND or V_{DD}.

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

ELECTRICAL CHARACTERISTICS: MAX5353

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		12			Bits
Integral Nonlinearity (Note 4)	INL	MAX5353A			±1	LSB
		MAX5353B			±2	
		MAX5353BMJA			±4	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 4)	GE			-0.3	±3	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR				600	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1554 hex	14	20		kΩ
MULTIPLYING-MODE PERFORMANCE (V_{DD} = +3.3V)						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.9Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		14		µs
Output Voltage Swing		Rail-to-rail (Note 5)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		3.15		3.6	V
Supply Current	I_{DD}	(Note 6)		0.24	0.4	mA
Supply Current in Shutdown		(Note 6)		1.6	10	µA
Reference Current in Shutdown				0.001	±0.5	µA

ELECTRICAL CHARACTERISTICS: MAX5353 (continued)

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: Guaranteed from code 22 to code 4095 in unity-gain configuration.

Note 5: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 150mV, guaranteed by a power-supply rejection test at the end points.

Note 6: R_L = ∞, digital inputs at GND or V_{DD}.

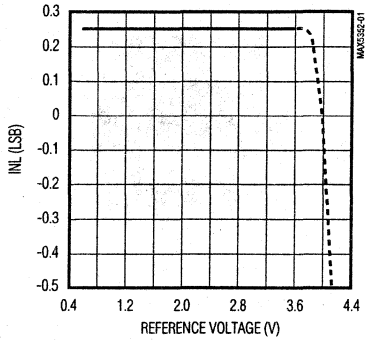
Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics

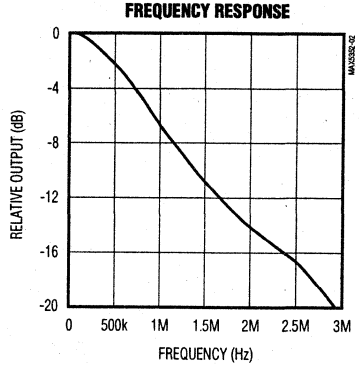
(MAX5352 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5352

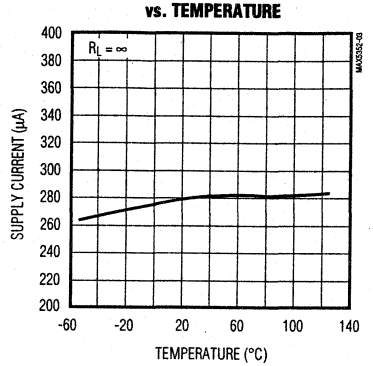
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



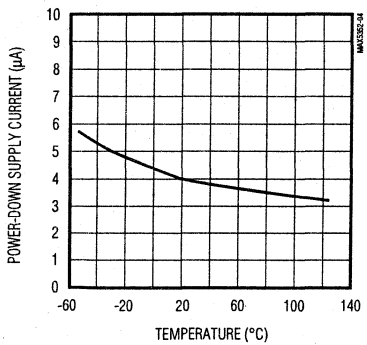
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



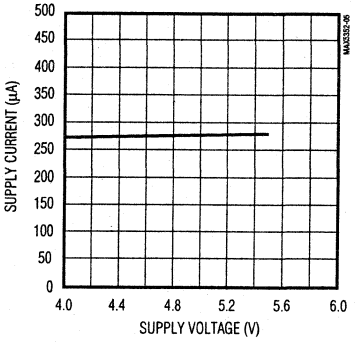
SUPPLY CURRENT vs. TEMPERATURE



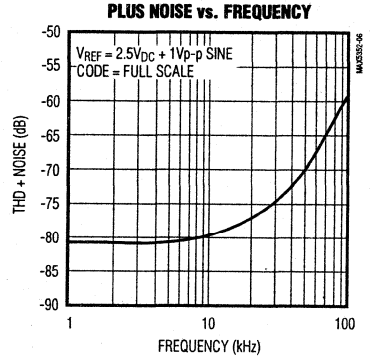
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



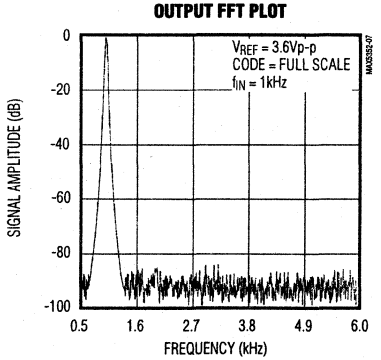
SUPPLY CURRENT vs. SUPPLY VOLTAGE



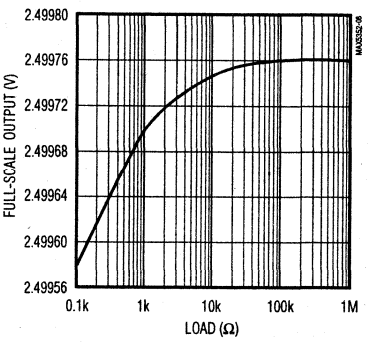
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



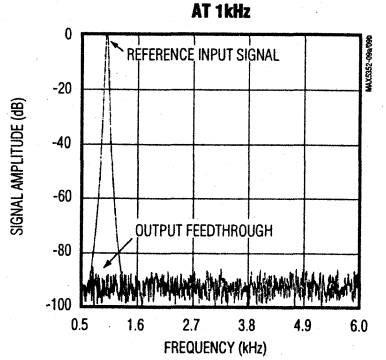
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

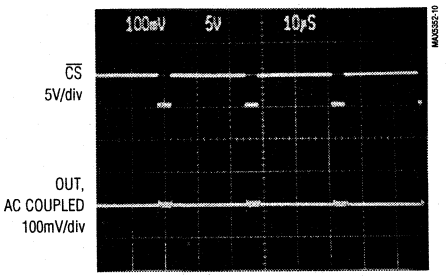


Typical Operating Characteristics (continued)

(MAX5352 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

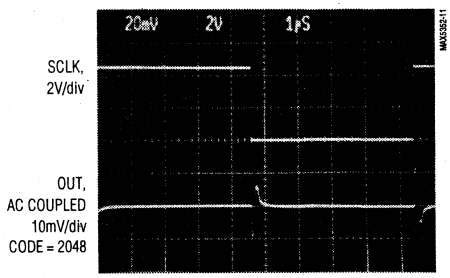
MAX5352 (continued)

MAJOR-CARRY TRANSITION



10µs/div

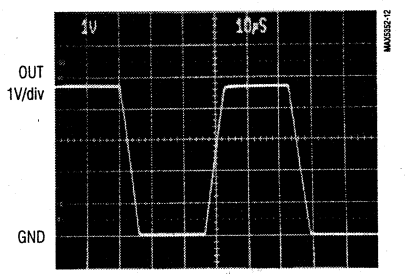
DIGITAL FEEDTHROUGH (f_{SCLK} = 100kHz)



2µs/div

CS = 5V

DYNAMIC RESPONSE



10µs/div

GAIN = 2, SWITCHING FROM CODE 0 TO 4020

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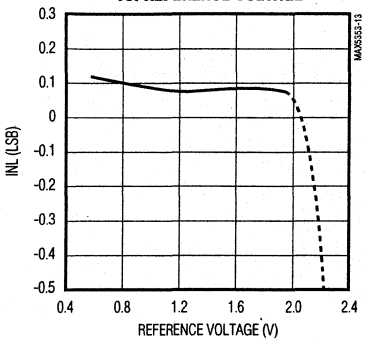
Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Typical Operating Characteristics (continued)

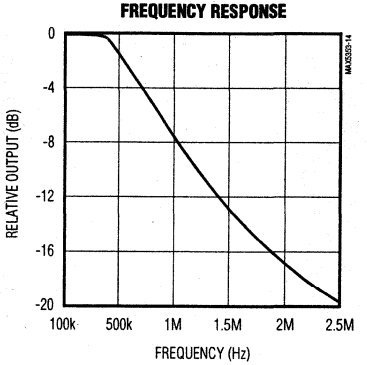
(MAX5353 only, V_{DD} = +3.3V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5353

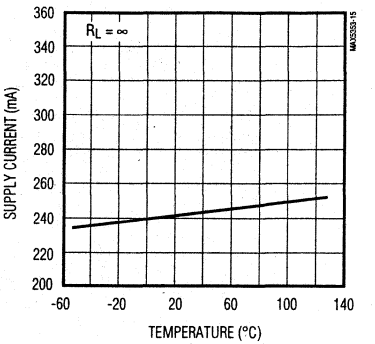
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



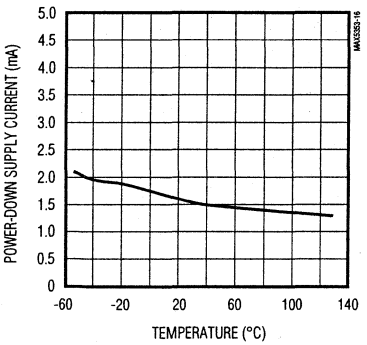
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



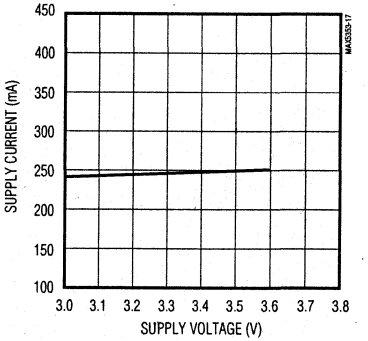
SUPPLY CURRENT vs. TEMPERATURE



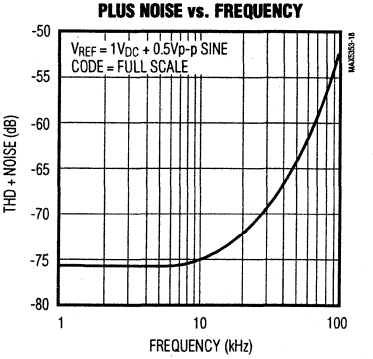
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



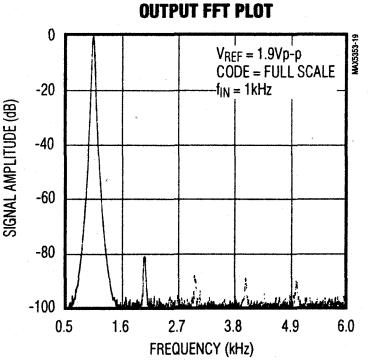
SUPPLY CURRENT vs. SUPPLY VOLTAGE



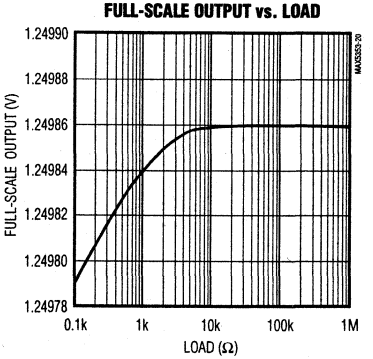
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



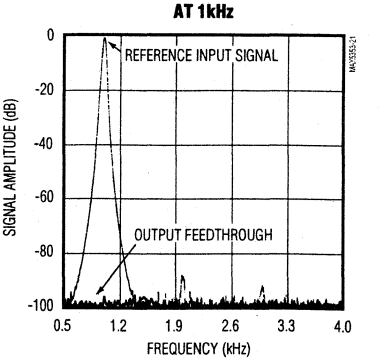
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz



Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{CS}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V_{DD}	Positive Power Supply

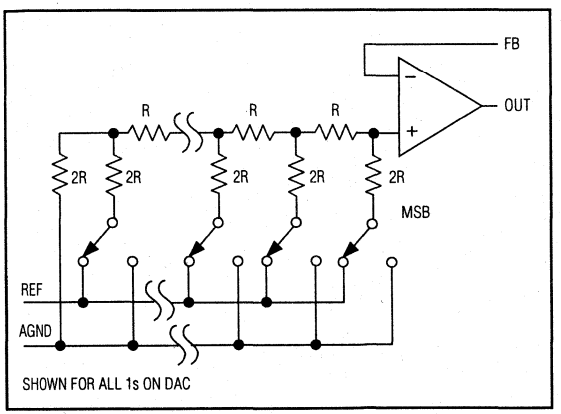


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX5352/MAX5353 contain a voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. Each IC includes a 16-bit shift register, and has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a digital input (12 data bits plus one sub-bit) into an equivalent analog output voltage in proportion to the applied reference voltage. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source, as expressed in the following equation:

$$V_{OUT} = (V_{REF} \times NB / 4096) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 4095), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 14kΩ when the DAC has an input code of 1554 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

In shutdown mode, the MAX5352/MAX5353's REF input enters a high-impedance state with a typical input leakage current of 0.001µA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (at full scale).

The MAX873 +2.5V reference is recommended for the MAX5352.

Output Amplifier

The MAX5352/MAX5353's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5352/MAX5353 output, the typical settling time to ±1/2LSB is 14µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Shutdown Mode

The MAX5352/MAX5353 feature a software-programmable shutdown that reduces supply current to a typical value of 4µA. Writing 111X XXXX XXXX XXXX as the input-control word puts the device in shutdown mode (Table 1).

In shutdown mode, the amplifier's output and the reference input enter a high-impedance state. The serial interface remains active. Data in the input registers is retained in shutdown, allowing the MAX5352/MAX5353

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or by updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the output to stabilize.

Serial-Interface Configurations

The MAX5352/MAX5353's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 12+1 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX5352/MAX5353's response outlined in Table 1.

The MAX5352/MAX5353's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

The +3.3V MAX5353 can also directly interface with +5V logic.

Serial-Interface Description

The MAX5352/MAX5353 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 12+1 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 12+1 data bits D11...D0, S0 (Figure 4). Set the sub-bit (S0) to zero. The 3-bit control code determines:

- the register to be updated,
- the configuration when exiting shutdown.

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX5352/MAX5353 input/DAC register on $\overline{CS}$'s rising edge.

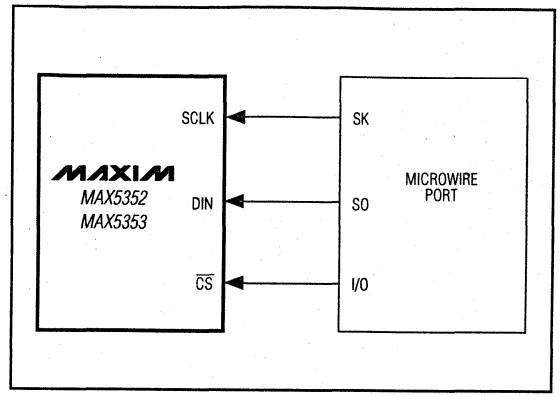


Figure 2. Connections for Microwire

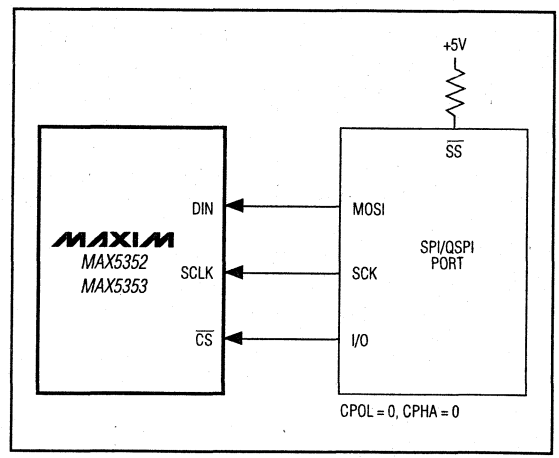


Figure 3. Connections for SPI/QSPI

MSB ..... LSB				
← 16 Bits of Serial Data →				
Control Bits			Data Bits MSB ..... LSB Sub-Bit	
C2	C1	C0	D11	D0, S0
← 3 Control Bits →			← 12+1 Data Bits →	

Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D11.....D0 MSB LSB	S0	
X	0	0	12 bits of data	0	Load input register; DAC register immediately updated (also exit shutdown).
X	0	1	12 bits of data	0	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXXXX	X	Update DAC register from input register (also exit shutdown; recall previous state).
1	1	1	XXXXXXXXXXXX	X	Shutdown
0	1	1	XXXXXXXXXXXX	X	No operation (NOP)

"X" = Don't care

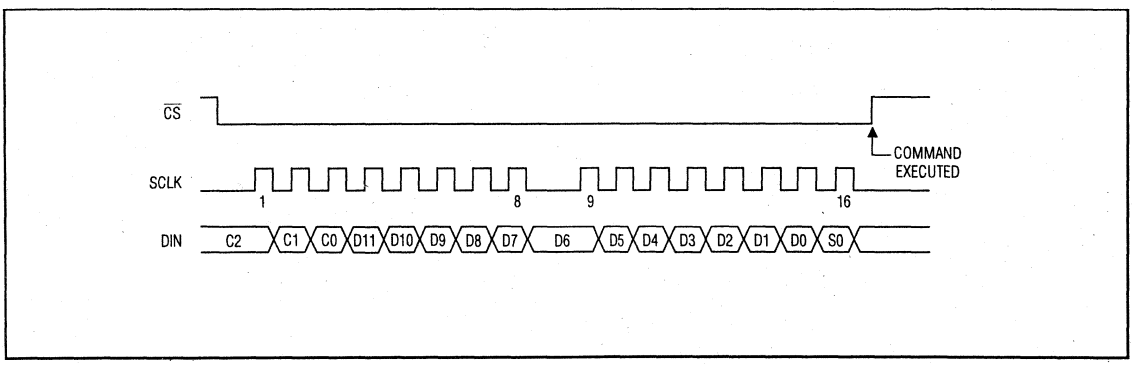


Figure 5. Serial-Interface Timing Diagram

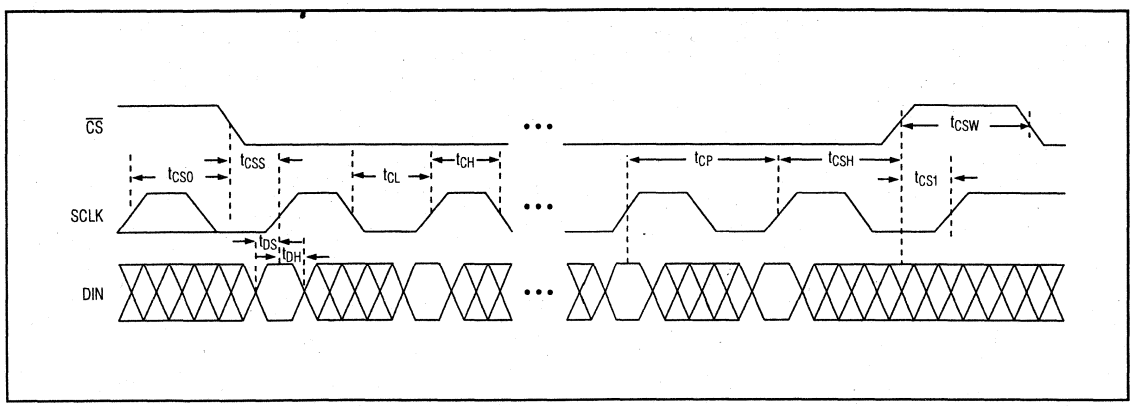


Figure 6. Detailed Serial-Interface Timing Diagram

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

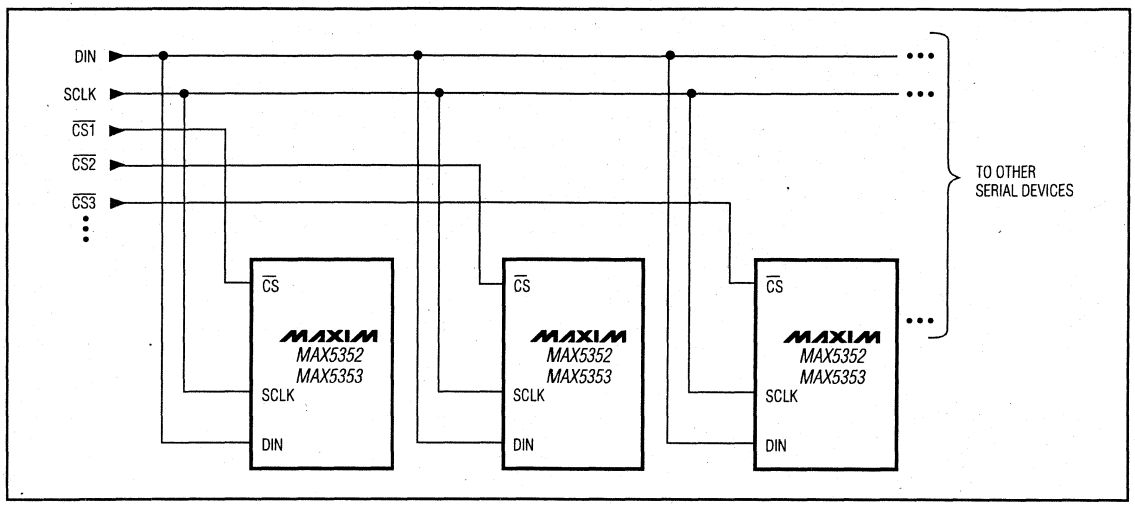


Figure 7. Multiple MAX5352/MAX5353s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX5352/MAX5353s. In this configuration, the clock and the data bus are common to all devices, and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX5352/MAX5353 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

Figure 9 illustrates a rail-to-rail output. This circuit shows the MAX5352 with the output amplifier configured with a closed-loop gain of +2 to provide a 0V to 5V full-scale range when a 2.5V reference is used. When the MAX5353 is used with a 1.25V reference, this circuit provides a 0V to 2.5V full-scale range.

Bipolar Output

The MAX5352/MAX5353 output can be configured for bipolar operation using Figure 10's circuit according to the following equation:

$$V_{OUT} = V_{REF}[(2NB / 4096) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and the corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 (0)	$+V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001 (0)	$+V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000 (0)	$+V_{REF}\left(\frac{2048}{4096}\right) = \frac{+V_{REF}}{2}$
0111 1111 1111 (0)	$+V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000 (0)	0V

NOTE: ( ) are for sub-bit.

Using an AC Reference

In applications where the reference has AC-signal components, the MAX5352/MAX5353 have multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111 (0)	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001 (0)	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000 (0)	0V
0111 1111 1111 (0)	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001 (0)	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000 (0)	$-V_{REF}\left(\frac{2048}{2048}\right) = -V_{REF}$

NOTE: ( ) are for sub-bit.

The MAX5352's total harmonic distortion plus noise (THD+N) is typically less than -77dB (full-scale code), and the MAX5353's THD+N is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz for both devices, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF}/R) \times (NB/4096)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

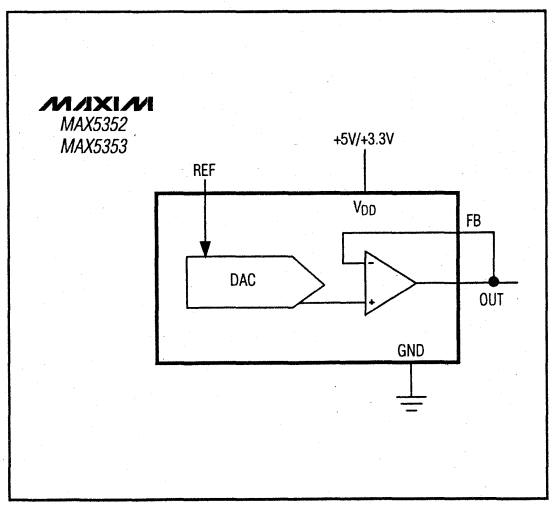


Figure 8. Unipolar Output Circuit

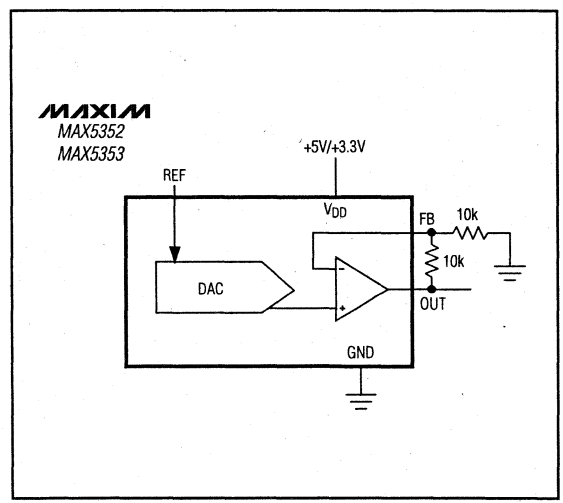


Figure 9. Unipolar Rail-to-Rail Output Circuit

Low-Power, 12-Bit Voltage-Output DACs with Serial Interface

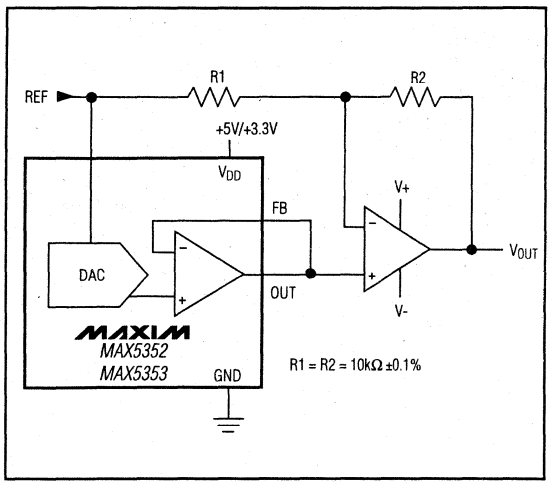


Figure 10. Bipolar Output Circuit

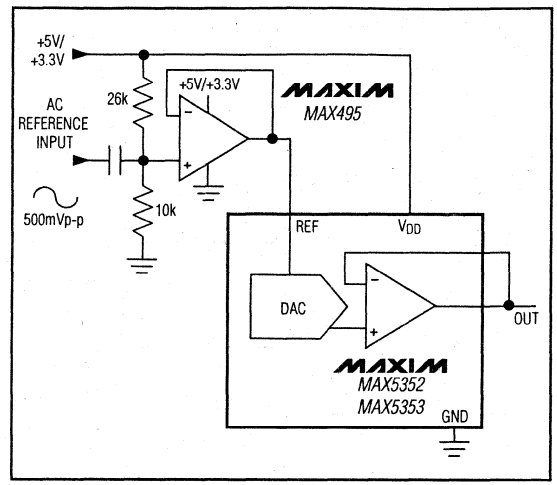


Figure 11. AC Reference Input Circuit

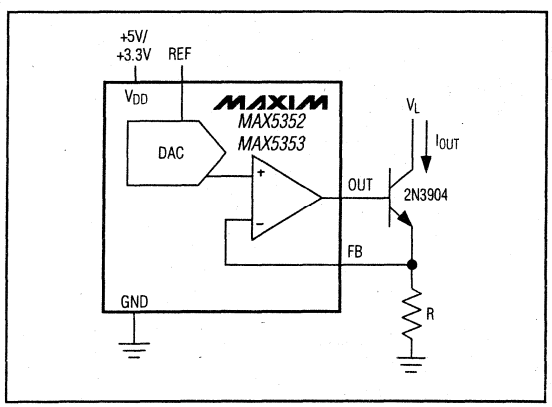


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX5352/MAX5353 performance, REF must be at least 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX5352AEPA	-40°C to +85°C	8 Plastic DIP	±1/2
MAX5352BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5352AEUA	-40°C to +85°C	8 µMAX	±1/2
MAX5352BEUA	-40°C to +85°C	8 µMAX	±1
MAX5352BMJA	-55°C to +125°C	8 CERDIP**	±2
MAX5353ACPA	0°C to +70°C	8 Plastic DIP	±1
MAX5353BCPA	0°C to +70°C	8 Plastic DIP	±2
MAX5353ACUA	0°C to +70°C	8 µMAX	±1
MAX5353BCUA	0°C to +70°C	8 µMAX	±2
MAX5353AEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX5353BEPA	-40°C to +85°C	8 Plastic DIP	±2
MAX5353AEUA	-40°C to +85°C	8 µMAX	±1
MAX5353BEUA	-40°C to +85°C	8 µMAX	±2
MAX5353BMJA	-55°C to +125°C	8 CERDIP**	±4

*Contact factory for availability of 8-pin SO package.
**Contact factory for availability and processing to MIL-STD-883.

Chip Information

TRANSISTOR COUNT: 1677

19-1167; Rev 1; 2/97

MAXIM

10-Bit Voltage-Output DACs in 8-Pin µMAX

General Description

The MAX5354/MAX5355 combine a low-power, voltage-output, 10-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin µMAX or DIP package. The MAX5354 operates from a single +5V supply, and the MAX5355 operates from a single +3.3V supply. Both devices draw less than 280µA of supply current.

The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output current capability. This makes the MAX5354/MAX5355 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is compatible with SPI™/QSPI™ and Microwire™. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Digital Offset and Gain Adjustment

Industrial Process Controls

Microprocessor-Controlled Systems

Portable Test Instruments

Remote Industrial Controls

Features

- ♦ **10-Bit DAC with Configurable Output Amplifier**
- ♦ **+5V Single-Supply Operation (MAX5354)**
  +3.3V Single-Supply Operation (MAX5355)
- ♦ **Low Supply Current: 0.28mA Normal Operation**
  2µA Shutdown Mode
- ♦ **Available in 8-Pin µMAX**
- ♦ **Power-On Reset Clears DAC Output to Zero**
- ♦ **SPI/QSPI and Microwire Compatible**
- ♦ **Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface**
- ♦ **+3.3V MAX5355 Directly Interfaces with +5V Logic**

Ordering Information

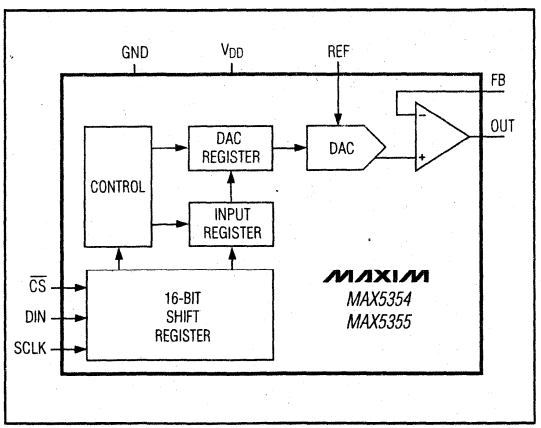
PART*	TEMP. RANGE	PIN-PACKAGE
MAX5354CPA	0°C to +70°C	8 Plastic DIP
MAX5354CUA	0°C to +70°C	8 µMAX
MAX5354EPA	-40°C to +85°C	8 Plastic DIP
MAX5354EUA	-40°C to +85°C	8 µMAX
MAX5354MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued at end of data sheet.

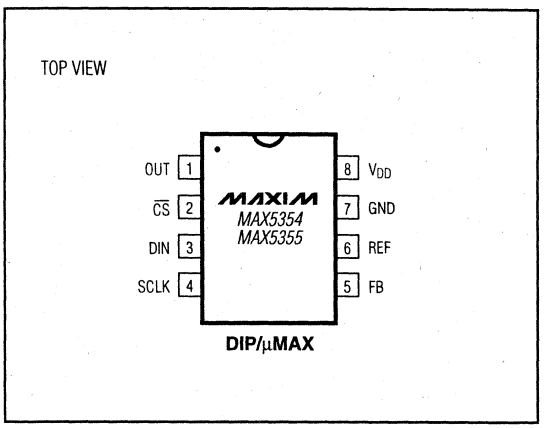
**Contact factory for availability of 8-pin SO package.*

***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



DIP/µMAX

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For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

10-Bit Voltage-Output DACs in 8-Pin µMAX

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
REF, OUT, FB to GND .....-0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND .....-0.3V to +6V
Continuous Current into Any Pin.....±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C).....727mW
µMAX (derate 4.10mW/°C above +70°C).....330mW
CERDIP (derate 8.00mW/°C above +70°C).....640mW

Operating Temperature Ranges
MAX5354C_A/MAX5355C_A .....0°C to +70°C
MAX5354E_A/MAX5355E_A.....-40°C to +85°C
MAX5354MJA/MAX5355MJA .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: MAX5354

(V_{DD} = +5V ±10%, GND = 0V, REF = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		10			Bits
Integral Nonlinearity (Note 1)	INL	MAX5354C/E			±1	LSB
		MAX5354M			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 1)	GE			-0.3	±2	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR	4.5V ≤ V_{DD} ≤ 5.5V			800	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1550 hex	18	30		kΩ
MULTIPLYING-MODE PERFORMANCE						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 3.6Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		77		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF

ELECTRICAL CHARACTERISTICS: MAX5354 (continued)

(V_{DD} = +5V ±10%, GND = 0V, REF = 2.5V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 2.5V		10		µs
Output Voltage Swing		Rail-to-rail (Note 2)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		4.5		5.5	V
Supply Current	I_{DD}	(Note 3)		0.28	0.4	mA
Supply Current in Shutdown		(Note 3)		4	20	µA
Reference Current in Shutdown				0.001	±0.5	µA
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 1: Guaranteed from code 3 to code 1023 in unity-gain configuration.

Note 2: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 100mV, guaranteed by a power-supply rejection test at the end points.

Note 3: R_L = ∞, digital inputs at GND or V_{DD}.

10-Bit Voltage-Output DACs in 8-Pin µMAX

ELECTRICAL CHARACTERISTICS: MAX5355

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE—ANALOG SECTION						
Resolution	N		10			Bits
Integral Nonlinearity (Note 4)	INL	MAX5355C/E			±1	LSB
		MAX5355M			±2	
Differential Nonlinearity	DNL	Guaranteed monotonic			±1.0	LSB
Offset Error	V_{OS}			±0.3	±8	mV
Offset-Error Tempco	TCV_{OS}			6		ppm/°C
Gain Error (Note 4)	GE			-0.3	±2	LSB
Gain-Error Tempco				1		ppm/°C
Power-Supply Rejection Ratio	PSRR				800	µV/V
REFERENCE INPUT						
Reference Input Range	V_{REF}		0		V_{DD} - 1.4	V
Reference Input Resistance	R_{REF}	Code dependent, minimum at code 1550 hex	18	30		kΩ
MULTIPLYING-MODE PERFORMANCE (V_{DD} = +3.3V)						
Reference -3dB Bandwidth		V_{REF} = 0.67Vp-p		650		kHz
Reference Feedthrough		Input code = all 0s, V_{REF} = 1.9Vp-p at 1kHz		-84		dB
Signal-to-Noise Plus Distortion Ratio	SINAD	V_{REF} = 1Vp-p at 25kHz, code = full scale		72		dB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.6	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}		0.001	±0.5	µA
Input Capacitance	C_{IN}			8		pF
DYNAMIC PERFORMANCE						
Voltage Output Slew Rate	SR			0.6		V/µs
Output Settling Time		To ±1/2LSB, V_{STEP} = 1.25V		10		µs
Output Voltage Swing		Rail-to-rail (Note 5)		0 to V_{DD}		V
Current into FB				0.001	±0.1	µA
Start-Up Time				20		µs
Digital Feedthrough		$\overline{CS}$ = V_{DD}, DIN = 100kHz		5		nV-s
POWER SUPPLIES						
Supply Voltage	V_{DD}		3.15		3.6	V
Supply Current	I_{DD}	(Note 6)		0.24	0.4	mA
Supply Current in Shutdown		(Note 6)		1.6	10	µA
Reference Current in Shutdown				0.001	±0.5	µA

ELECTRICAL CHARACTERISTICS: MAX5355 (continued)

(V_{DD} = +3.15V to +3.6V, REF = 1.25V, GND = 0V, R_L = 5kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C. Output buffer connected in unity-gain configuration (Figure 8).)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS (Figure 6)						
SCLK Clock Period	t_{CP}		100			ns
SCLK Pulse Width High	t_{CH}		40			ns
SCLK Pulse Width Low	t_{CL}		40			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time	t_{CSS}		40			ns
SCLK Rise to $\overline{CS}$ Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		40			ns
DIN Hold Time	t_{DH}		0			ns
SCLK Rise to $\overline{CS}$ Fall Delay	t_{CS0}		40			ns
$\overline{CS}$ Rise to SCLK Rise Hold Time	t_{CS1}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSW}		100			ns

Note 4: Guaranteed from code 6 to code 1023 in unity-gain configuration.

Note 5: Accuracy is better than 1LSB for V_{OUT} = 8mV to V_{DD} - 150mV, guaranteed by a power-supply rejection test at the end points.

Note 6: R_L = ∞, digital inputs at GND or V_{DD}.

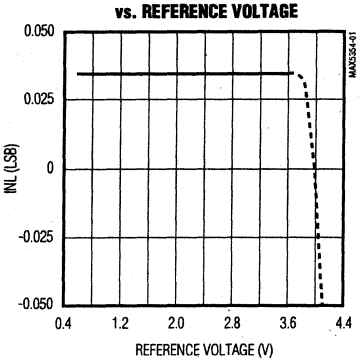
10-Bit Voltage-Output DACs in 8-Pin µMAX

Typical Operating Characteristics

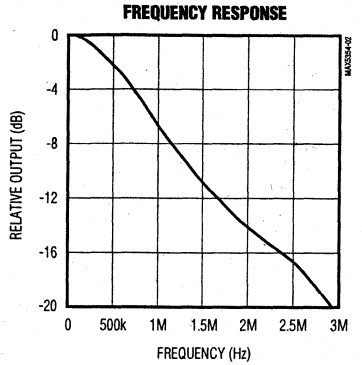
(MAX5354 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5354

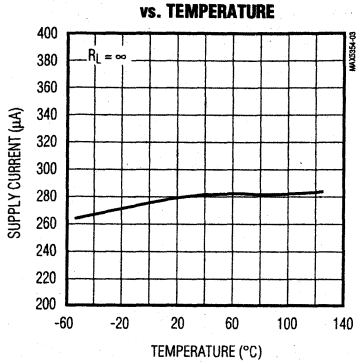
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



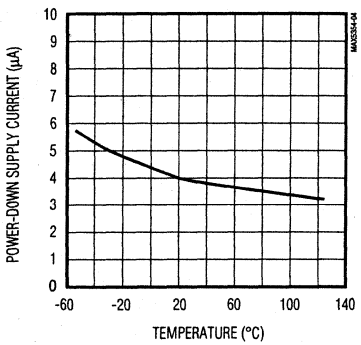
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



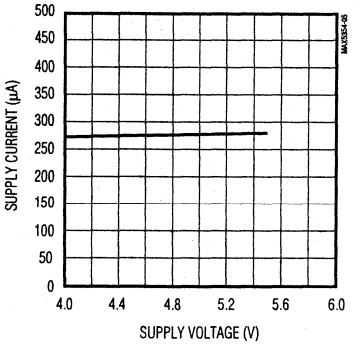
SUPPLY CURRENT vs. TEMPERATURE



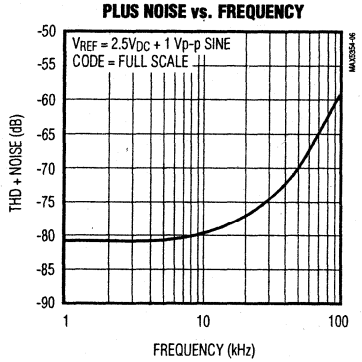
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



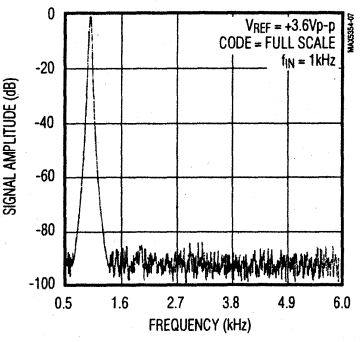
SUPPLY CURRENT vs. SUPPLY VOLTAGE



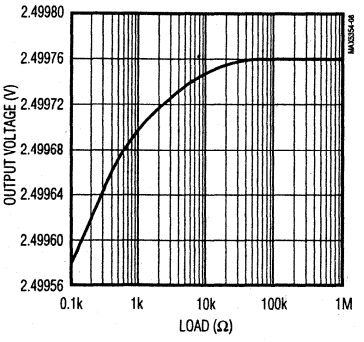
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



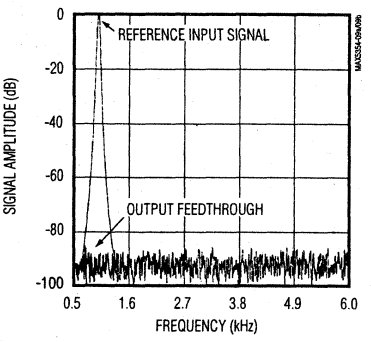
OUTPUT FFT PLOT



OUTPUT VOLTAGE vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz

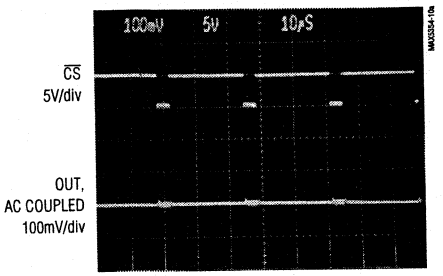


Typical Operating Characteristics (continued)

(MAX5354 only, V_{DD} = +5V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

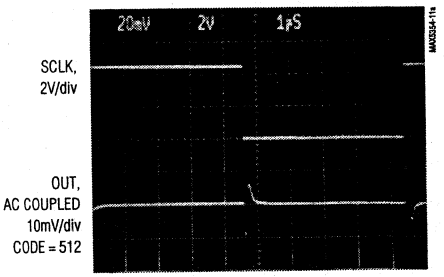
MAX5354 (continued)

MAJOR-CARRY TRANSITION



10µs/div

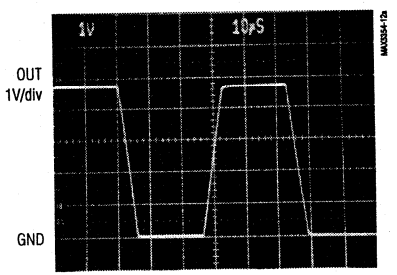
DIGITAL FEEDTHROUGH (f_{SCLK} = 100kHz)



2µs/div

CS = 5V

DYNAMIC RESPONSE



10µs/div

GAIN = +2, SWITCHING FROM CODE 0 TO 1005

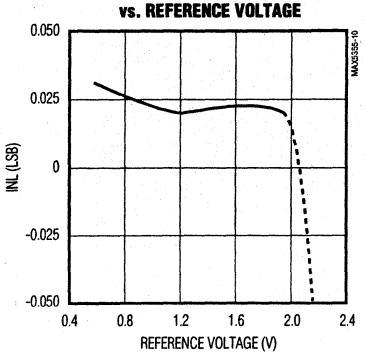
10-Bit Voltage-Output DACs in 8-Pin µMAX

Typical Operating Characteristics (continued)

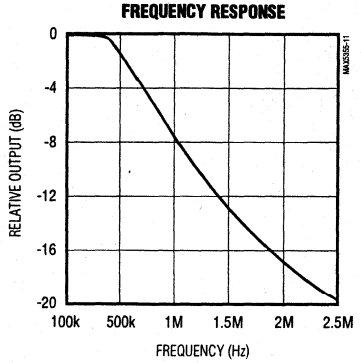
(MAX5355 only, V_{DD} = +3.3V, R_L = 5kΩ, C_L = 100pF, T_A = +25°C, unless otherwise noted.)

MAX5355

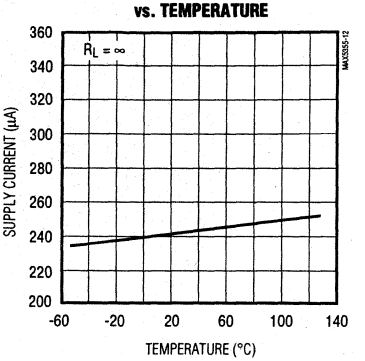
INTEGRAL NONLINEARITY vs. REFERENCE VOLTAGE



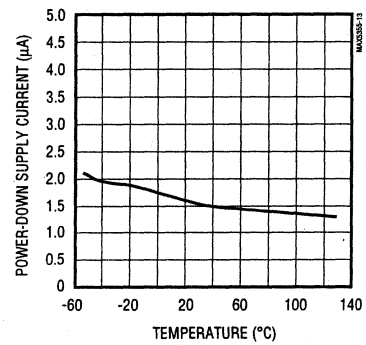
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



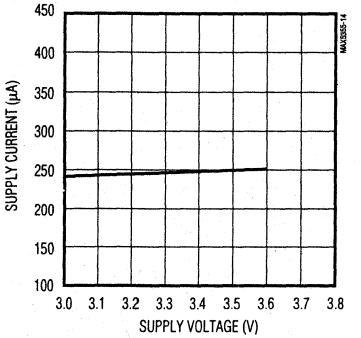
SUPPLY CURRENT vs. TEMPERATURE



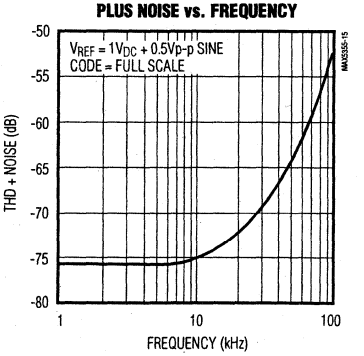
POWER-DOWN SUPPLY CURRENT vs. TEMPERATURE



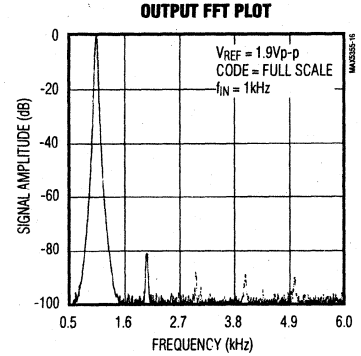
SUPPLY CURRENT vs. SUPPLY VOLTAGE



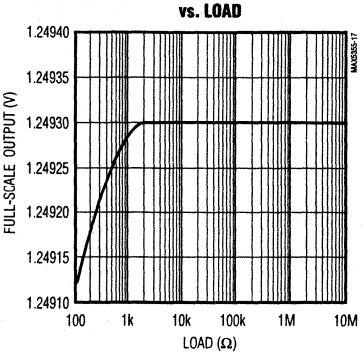
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



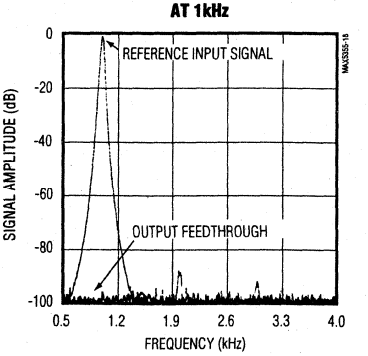
OUTPUT FFT PLOT



FULL-SCALE OUTPUT vs. LOAD



REFERENCE FEEDTHROUGH AT 1kHz



Pin Description

PIN	NAME	FUNCTION
1	OUT	DAC Output Voltage
2	$\overline{CS}$	Chip-Select Input. Active low.
3	DIN	Serial-Data Input
4	SCLK	Serial-Clock Input
5	FB	DAC Output Amplifier Feedback
6	REF	Reference Voltage Input
7	GND	Ground
8	V_{DD}	Positive Power Supply

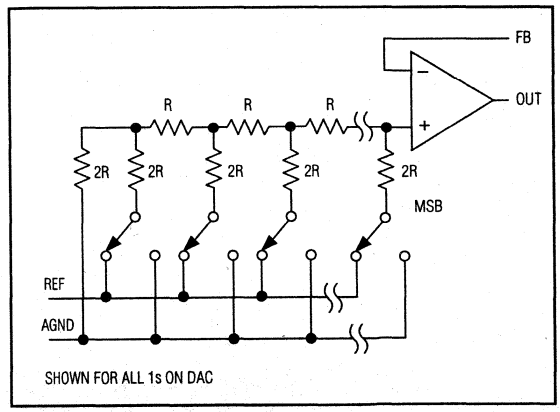


Figure 1. Simplified DAC Circuit Diagram

Detailed Description

The MAX5354/MAX5355 contain a voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. Each IC includes a 16-bit shift register, and has a double-buffered input composed of an input register and a DAC register (see *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a digital input (10 data bits plus three sub-bits) into an equivalent analog output voltage in proportion to the applied reference voltage. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source, as expressed in the following equation:

$$V_{OUT} = (V_{REF} \times NB / 1024) \times Gain$$

where NB is the numeric value of the DAC's binary input code (0 to 1023), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 18kΩ when the DAC has an input code of 1550 hex, to a high value exceeding several giga ohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

In shutdown mode, the MAX5354/MAX5355's REF input enters a high-impedance state with a typical input leakage current of 0.001µA.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (at full scale).

The MAX873 +2.5V reference is recommended for use with the MAX5354.

Output Amplifier

The MAX5354/MAX5355's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/µs. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5354/MAX5355 output, the typical settling time to ±1/2LSB is 10µs when loaded with 5kΩ in parallel with 100pF (loads less than 2kΩ degrade performance).

The amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Shutdown Mode

The MAX5354/MAX5355 feature a software-programmable shutdown that reduces supply current to a typical value of 4µA. Writing 111X XXXX XXXX XXXX as the input-control word puts the device in shutdown mode (Table 1).

10-Bit Voltage-Output DACs in 8-Pin µMAX

In shutdown mode, the amplifier's output and the reference input enter a high-impedance state. The serial interface remains active. Data in the input register is retained in shutdown, allowing the MAX5354/MAX5355 to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20µs for the outputs to stabilize.

Serial-Interface Configurations

The MAX5354/MAX5355's 3-wire serial interface is compatible with both Microwire™ (Figure 2) and SPI™/QSPI™ (Figure 3). The serial input word consists of three control bits followed by 10+3 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX5354/MAX5355's response outlined in Table 1.

The MAX5354/MAX5355's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

The +3.3V MAX5355 can also directly interface with +5V logic.

Serial-Interface Description

The MAX5354/MAX5355 require 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 10+3 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word ($\overline{CS}$ must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 10+3 data bits D9...D0, S2, S1, S0 (Figure 4). Set the sub-bits (S2, S1, S0) to zero. The 3-bit control code determines:

- the register to be updated,
- the configuration when exiting shutdown.

Figure 5 shows the serial-interface timing requirements. The chip-select pin ($\overline{CS}$) must be low to enable the DAC's serial interface. When $\overline{CS}$ is high, the interface control circuitry is disabled. $\overline{CS}$ must go low at least t_{CSS} before the rising serial clock (SCLK) edge to properly clock in the first bit. When $\overline{CS}$ is low, data is clocked into the internal shift register via the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX5354/MAX5355 input/DAC register on $\overline{CS}$'s rising edge.

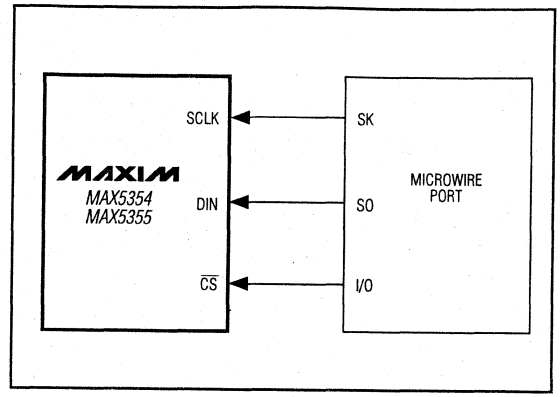


Figure 2. Connections for Microwire

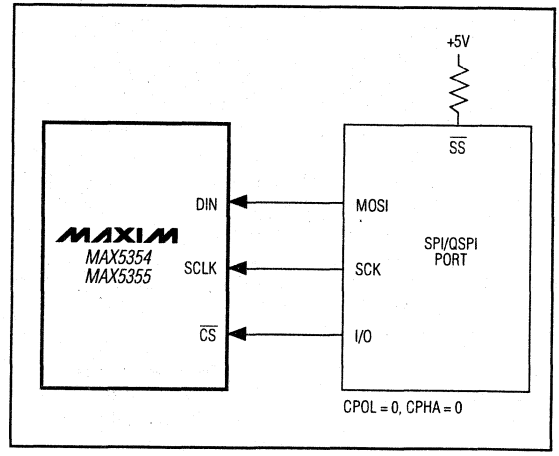


Figure 3. Connections for SPI/QSPI

MSB ..... LSB				
← 16 Bits of Serial Data →				
Control Bits			Data Bits MSB ..... LSB	Sub-Bits
C2	C1	C0	D9 ..... D0	S2, S1, S0
← 3 Control Bits →			← 10+3 Data Bits →	

Figure 4. Serial-Data Format

Table 1. Serial-Interface Programming Commands

16-BIT SERIAL WORD					FUNCTION
C2	C1	C0	D9.....D0 MSB LSB	S2...S0	
X	0	0	10 bits of data	000	Load input register; DAC register immediately updated (also exit shutdown).
X	0	1	10 bits of data	000	Load input register; DAC register unchanged.
X	1	0	XXXXXXXXXX	XXX	Update DAC register from input register (also exit shutdown; recall previous state).
1	1	1	XXXXXXXXXX	XXX	Shutdown
0	1	1	XXXXXXXXXX	XXX	No operation (NOP)

"X" = Don't care

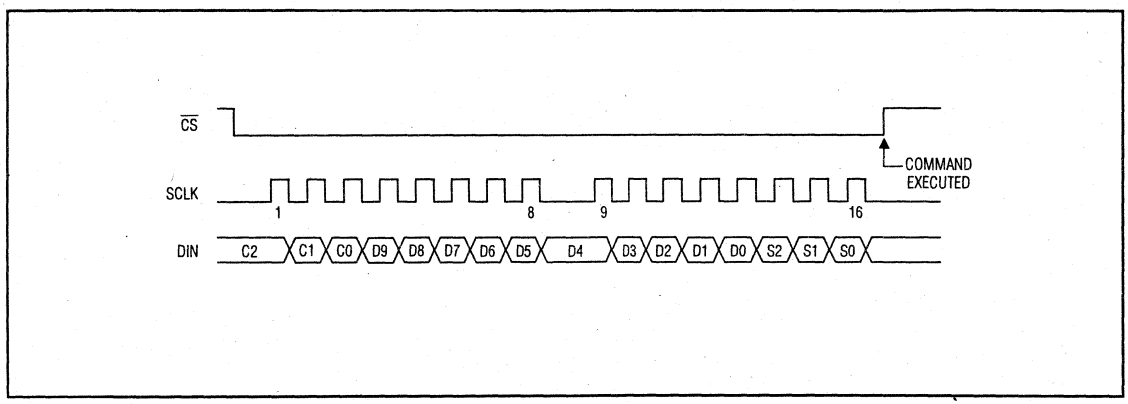


Figure 5. Serial-Interface Timing Diagram

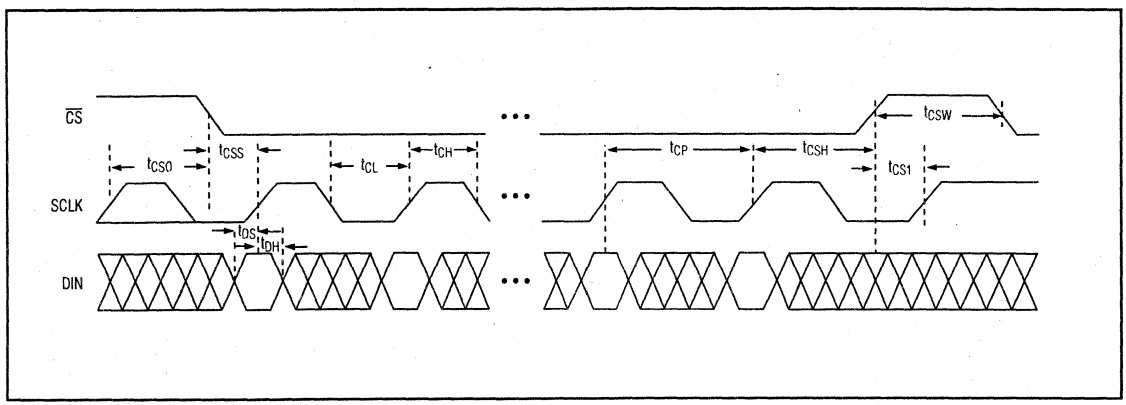


Figure 6. Detailed Serial-Interface Timing Diagram

10-Bit Voltage-Output DACs in 8-Pin µMAX

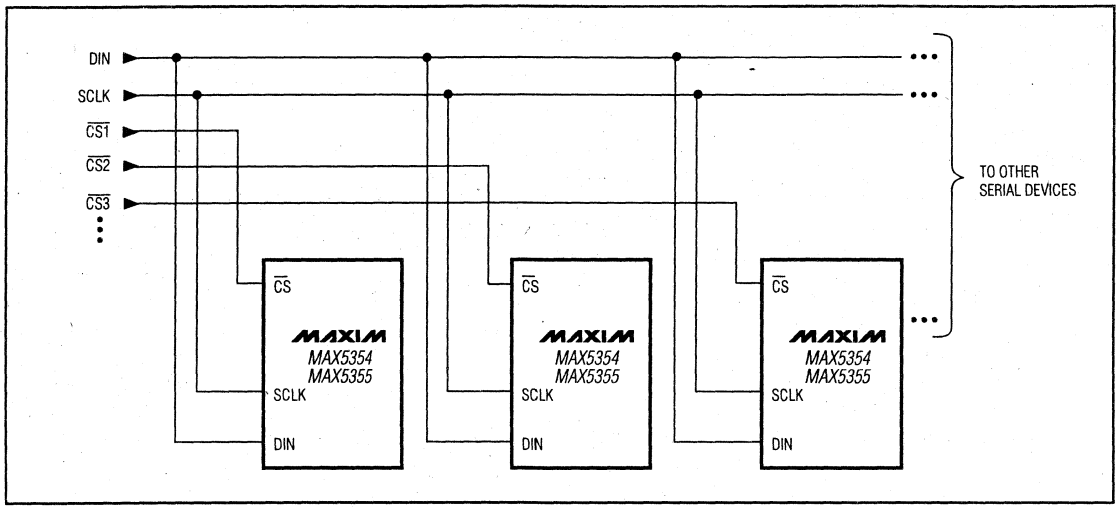


Figure 7. Multiple MAX5354/MAX5355s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX5354/MAX5355s. In this configuration, the clock and the data bus are common to all devices, and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX5354/MAX5355 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

Figure 9 illustrates a rail-to-rail output configuration. This circuit shows the MAX5354 with the output amplifier configured for a closed-loop gain of +2, to provide a 0V to 5V full-scale range when a 2.5V reference is used. When the MAX5355 is used with a 1.25V reference, this circuit provides a 0V to 2.5V full-scale range.

Bipolar Output

The MAX5354/MAX5355 output can be configured for bipolar operation using Figure 10's circuit, according to the following equation:

$$V_{OUT} = V_{REF}[(2NB / 1024) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltage for Figure 10's circuit.

Table 2. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 (000)	$+V_{REF}\left(\frac{1023}{1024}\right)$
10 0000 0001 (000)	$+V_{REF}\left(\frac{513}{1024}\right)$
10 0000 0000 (000)	$+V_{REF}\left(\frac{512}{1024}\right) = \frac{+V_{REF}}{2}$
01 1111 1111 (000)	$+V_{REF}\left(\frac{511}{1024}\right)$
00 0000 0001 (000)	$+V_{REF}\left(\frac{1}{1024}\right)$
00 0000 0000 (000)	0V

NOTE: ( ) are for sub-bits.

Using an AC Reference

In applications where the reference has AC-signal components, the MAX5354/MAX5355 have multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

Table 3. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
11 1111 1111 (000)	$+V_{REF}\left(\frac{511}{512}\right)$
10 0000 0001 (000)	$+V_{REF}\left(\frac{1}{512}\right)$
10 0000 0000 (000)	0V
01 1111 1111 (000)	$-V_{REF}\left(\frac{1}{512}\right)$
00 0000 0001 (000)	$-V_{REF}\left(\frac{511}{512}\right)$
00 0000 0000 (000)	$-V_{REF}\left(\frac{512}{512}\right) = -V_{REF}$

NOTE: ( ) are for sub-bits.

The MAX5354's total harmonic distortion plus noise (THD+N) is typically less than -77dB (full-scale code), and the MAX5355's THD+N is typically less than -72dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz for both devices, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

The circuit of Figure 12 places an NPN transistor (2N3904 or similar) within the op-amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF}/R) \times (NB/1024)$$

where NB is the numeric value of the DAC's binary input code and R is the sense resistor shown in Figure 12.

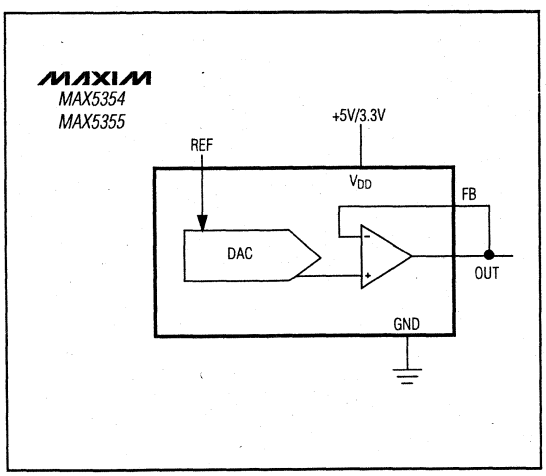


Figure 8. Unipolar Output Circuit

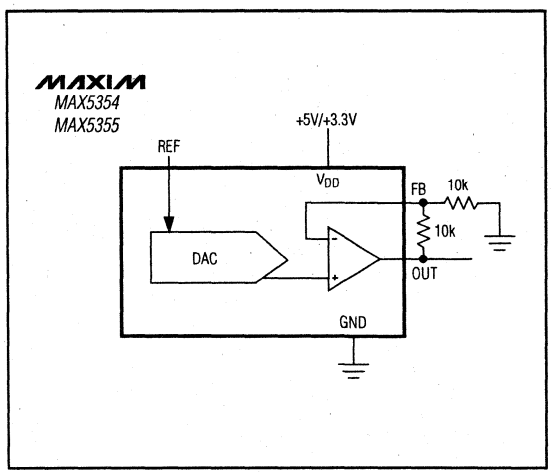


Figure 9. Unipolar Rail-to-Rail Output Circuit

10-Bit Voltage-Output DACs in 8-Pin µMAX

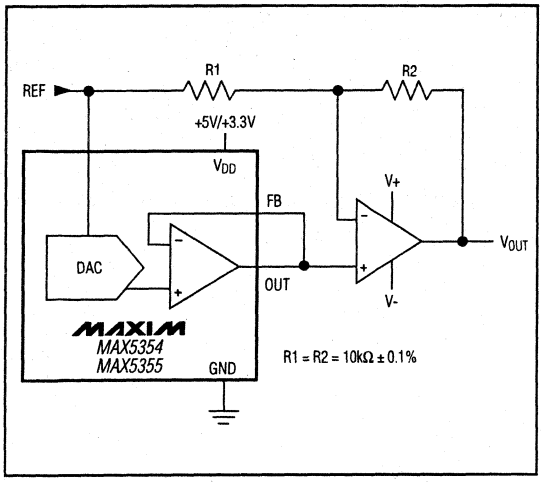


Figure 10. Bipolar Output Circuit

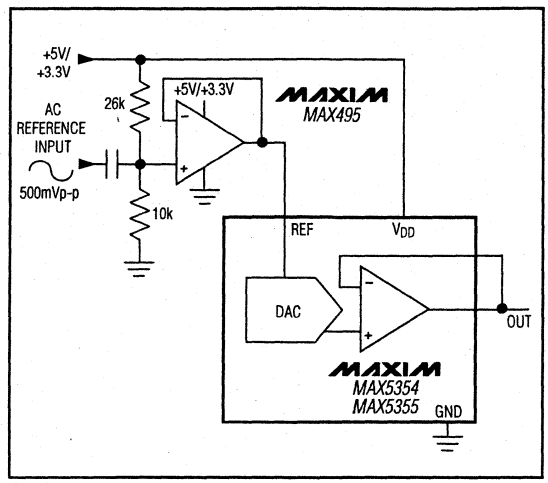


Figure 11. AC Reference Input Circuit

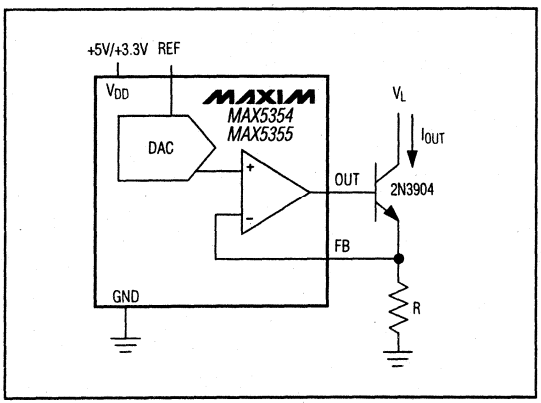


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code).

For rated MAX5354/MAX5355 performance, REF must be at least 1.4V below V_{DD}. Bypass V_{DD} with a 4.7µF capacitor in parallel with a 0.1µF capacitor to GND. Use short lead lengths and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Tie GND to the highest-quality ground available.

Good printed circuit board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

_Ordering Information (continued)

PART*	TEMP. RANGE	PIN-PACKAGE
MAX5355CPA	0°C to +70°C	8 Plastic DIP
MAX5355CUA	0°C to +70°C	8 µMAX
MAX5355EPA	-40°C to +85°C	8 Plastic DIP
MAX5355EUA	-40°C to +85°C	8 µMAX
MAX5355MJA	-55°C to +125°C	8 CERDIP**

*Contact factory for availability of 8-pin SO package.
**Contact factory for availability and processing to MIL-STD-883.

_____Chip Information

TRANSISTOR COUNT: 1677

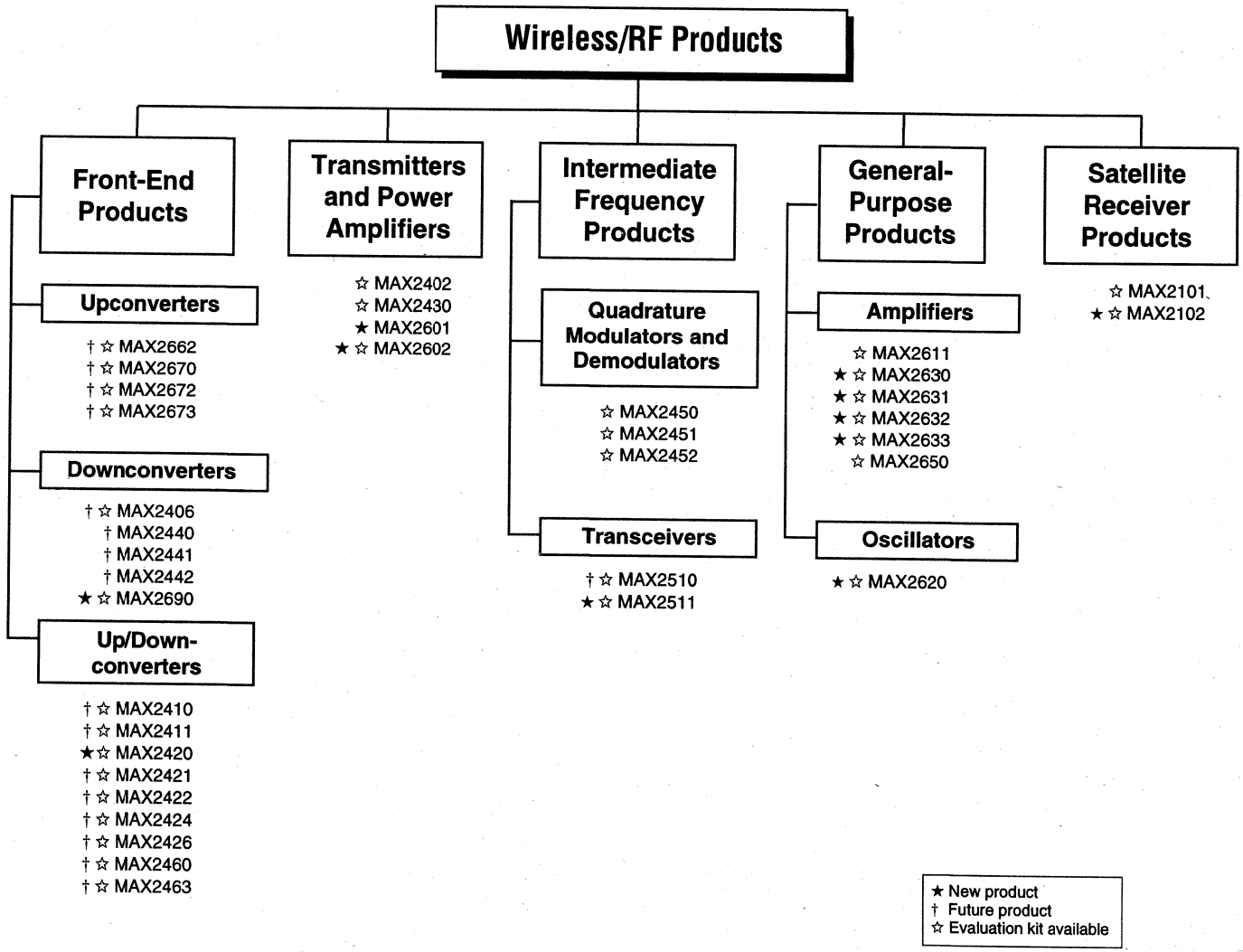
MAXIM

Wireless/RF Products

Wireless/RF Products, Product Table 10-2

MAX2102 Direct-Conversion Tuner IC for Digital DBS Applications 10-7
MAX2406 Low-Cost Downconverter with Low-Noise Amplifier 10-21*
MAX2410 Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver 10-23*
MAX2411A Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver with Common-Differential IF Port 10-25*
MAX2420 900MHz Image-Reject Transceiver for 10.7MHz IF Frequencies 10-27*
MAX2421 900MHz Image-Reject Transceiver for 46MHz IF Frequencies 10-27*
MAX2422 900MHz Image-Reject Transceiver for 70MHz IF Frequencies 10-27*
MAX2426 900MHz Image-Reject Transceiver with Transmit Mixer 10-29*
MAX2460 900MHz Image-Reject Transceiver with Low-Side LO Injection for 10.7MHz IF Frequencies 10-27*
MAX2463 900MHz Image-Reject Transceiver for 110MHz IF Frequencies 10-27*
MAX2510 Low-Voltage IF Transceiver with Limiter/RSSI and Quadrature Modulator 10-31*
MAX2511 Low-Voltage IF Transceiver with Limiter and RSSI 10-33*
MAX2601 3.6V, 1W RF Power Transistor for 900MHz Applications 10-49
MAX2602 3.6V, 1W RF Power Transistor with On-Chip Diode for 900MHz Applications 10-49
MAX2620 650MHz to 1050MHz Integrated Oscillator with Buffered Outputs 10-55
MAX2630 VHF-to-Microwave, +3V, General-Purpose Amplifier in SOT143 Package 10-63
MAX2631 VHF-to-Microwave, +3V, General-Purpose Amplifier in SOT23-5 Package 10-63
MAX2632 VHF-to-Microwave, +3V, General-Purpose Amplifier with Adjustable Bias 10-63
MAX2633 VHF-to-Microwave, +3V, General-Purpose Amplifier in SOT23-6 Package 10-63
MAX2662 Low-Noise, 2.5GHz Upconverter Mixer 10-73*
MAX2690 High-Linearity, Low-Noise, 400MHz to 2.5GHz Downconverter Mixer 10-75*

*Advance Information–first page of a data sheet in preparation.


Wireless/RF Products
Front-End Products
Upconverters
† ☆ MAX2662
† ☆ MAX2670
† ☆ MAX2672
† ☆ MAX2673
Downconverters
† ☆ MAX2406
† MAX2440
† MAX2441
† MAX2442
★ ☆ MAX2690
Up/Down-converters
† ☆ MAX2410
† ☆ MAX2411
★☆ MAX2420
† ☆ MAX2421
† ☆ MAX2422
† ☆ MAX2424
† ☆ MAX2426
† ☆ MAX2460
† ☆ MAX2463
Transmitters and Power Amplifiers
☆ MAX2402
☆ MAX2430
★ MAX2601
★ ☆ MAX2602
Intermediate Frequency Products
Quadrature Modulators and Demodulators
☆ MAX2450
☆ MAX2451
☆ MAX2452
Transceivers
† ☆ MAX2510
★ ☆ MAX2511
General-Purpose Products
Amplifiers
☆ MAX2611
★ ☆ MAX2630
★ ☆ MAX2631
★ ☆ MAX2632
★ ☆ MAX2633
☆ MAX2650
Oscillators
★ ☆ MAX2620
Satellite Receiver Products
☆ MAX2101
★ ☆ MAX2102
★ New product
† Future product
☆ Evaluation kit available

Part Number	Supply Voltage (V)	Input Frequency (MHz)	Input Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	AGC Range (dB)	Pins-Package Options*	Features	Applications	Price† 25,000-up ($)
SATELLITE RECEIVER PRODUCTS										
MAX2101	4.75 to 5.25	400 to 700	60	0.5	1.5	40	100-MQFP	I/Q demodulator with dual 5th-order Butterworth filters, 10MHz to 30MHz bandwidth, and dual 6-bit ADCs	DBS, VSAT	11.49
MAX2102	4.75 to 5.25	950 to 2150	120	0.5	3(max)	50	28-SO	Direct downconversion tuner IC, tunes L-band to baseband I and Q outputs	DBS, DAB, DVB	4.00

Part Number	Supply Voltage (V)	Supply Current (mA)	IF Frequency (MHz)	IF Bandwidth (MHz)	I/Q Gain Balance (dB)	I/Q Phase Balance (degrees)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
MODULATORS AND DEMODULATORS										
MAX2450	2.7 to 3.3	5.9	70	9	0.45	3	20-SO, 20-QSOP	70MHz I/Q modulator/demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.99
MAX2451	2.7 to 3.3	5.5	70	9	0.45	3	16-SO	70MHz I/Q demodulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23
MAX2452	2.7 to 3.3	4.1	70	15	0.45	3	16-SO	70MHz I/Q modulator with on-chip VCO and quad generator, shutdown mode	Cellular, ISM, WLANs	3.23

Part Number	Supply Voltage (V)	Receive Input IP3 (dBm)	Transmit Output (dBm)	RF Frequency (MHz typ)	IF Frequency (MHz typ)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
UPCONVERTERS AND DOWNCONVERTERS									
MAX2406	2.7 to 5.5	-12.5	—	1900	45 to 450	24-QSOP	Low-noise amplifier and low-noise, high-input IP3 mixer	PCS and cellular phones	††
MAX2410	2.7 to 5.5	-12.5	+3	1900	45 to 450	28-QSOP	Low-noise amplifier and RX mixer with high IP3, low-noise TX mixer and variable-gain PA driver (separate IF ports)	PCS and cellular phones	††
MAX2411	2.7 to 5.5	-12.5	+3	1900	45 to 450	28-QSOP	Low-noise amplifier and RX mixer with high IP3, low-noise TX mixer and variable-gain PA driver (common IF ports)	PCS and cellular phones	††
MAX2420/1/2	2.7 to 4.8	-17/-8/+2**	0	800 to 1000	10/46/70	28-SSOP	Image-reject up/downconverter, VCO, prescaler, 30dB transmit VGA, programmable-gain LNA and 0dBm PA predriver; high-side LO injection	Cordless phones, cellular phones, ISM spread spectrum, RF transceivers	4.49/††/††
MAX2424/6	2.7 to 4.8	-17/-8/+2**	-3	800 to 1000	10/70	28-SSOP	Image-reject up/downconverter, VCO, prescaler, balanced transmit modulator, programmable-gain LNA and 0dBm PA predriver; high-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2440/1/2	2.7 to 4.8	-17/-8/+2**	—	800 to 1000	10/46/70	28-SSOP	Image-reject downconverter, VCO, prescaler, programmable-gain LNA, high-side LO injection	Cordless phones, ISM spread spectrum, RF receivers	††
MAX2460/3	2.7 to 4.8	-17/-8/+2**	0	800 to 1000	10/110	28-SSOP	Image-reject up/downconverter, VCO, prescaler, balanced transmit modulator, programmable-gain LNA and 0dBm PA predriver; low-side LO injection	Cordless phones, ISM spread spectrum, RF transceivers	††
MAX2662	2.7 to 5.5	12(OIP3)	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter, 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2670	2.7 to 5.5	10(OIP3)	-8	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter, 9mA supply current, 1µA shutdown, buffered LO	Hand-held receivers, WLANs, ISM PCS, portable phones	††

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package

** Depending on LNA gain setting.

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product—contact factory for pricing and availability. Specifications are preliminary.

NOTE: IF = Intermediate Frequency, I/Q = In-Phase/Quadrature-Phase, VGA = variable-gain amplifier

Part Number	Supply Voltage (V)	Receive Input IP3 (dBm)	Transmit Output (dBm)	RF Frequency (MHz typ)	IF Frequency (MHz typ)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
UPCONVERTERS AND DOWNCONVERTERS (continued)									
MAX2672	2.7 to 5.5	12(OIP3)	-1	40 to 2500	10 to 500	SOT23-6	Low-noise, low-voltage upconverter, 15mA supply current, 1µA shutdown	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2673	2.7 to 5.5	12(OIP3)	-1	40 to 2500	10 to 500	8-µMAX	Low-noise, low-voltage upconverter, 15mA supply current, 1µA shutdown, differential inputs	Hand-held receivers, WLANs, ISM PCS, portable phones	††
MAX2690	2.7 to 5.5	7.6	—	400 to 2500	10 to 500	10-µMAX	Low-noise, 10dB NF, low-voltage downconverter, 15mA supply current, 1µA shutdown, differential IF port	Hand-held receivers, WLANs, ISM PCS, portable phones	††

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Output Power (mW)	Power Control (dB)	Class	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
TRANSMITTERS AND POWER AMPLIFIERS									
MAX2402	4.75 to 5.5	800 to 1000	100	40	AB to B, adj.	20-SSOP	Power amplifier with balanced modulator, linear modulation to 2V, shutdown mode	ISM spread spectrum, DS, FH, BPSK, ASK, FSK	3.78
MAX2430	3 to 5.5	800 to 1000	125 @ 3.6V	15	AB	16-SO, 16-QSOP	True single-supply power amplifier, power on/off ramp control, more than 32dB gain, shutdown mode	900MHz cordless phones, ISM spread spectrum	2.97
MAX2601	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor in a thermally enhanced plastic package	AMPS phones, two-way paging, CDPD, ISM radios	2.32
MAX2602	2.7 to 5.5	DC to >1000	1W	—	AB/C	8-SO	3.6V, 1W power transistor with an on-chip thermally matched bias diode	AMPS phones, two-way paging, CDPD, ISM radios	2.38

Part Number	Supply Voltage (V)	IF Frequency 1st/2nd (MHz)	RSSI Range (dB)	Tx Power Control (dB)	Image-Reject Mixers	Features	Applications	Price† 1000-up ($)
INTERMEDIATE-FREQUENCY PRODUCTS								
MAX2510	2.7 to 5.5	30 to 500/ 1 to 25	>90	40	No	IF transceiver with downconverter mixer, limiting amplifier, transmit I/Q mixers, and VGA	PCS phones (PWT1900, PACS, PHS), wireless local loop, RF transceivers	††
MAX2511	2.7 to 5.5	200 to 450/ 10.7	>90	40	Yes	IF transceiver with image-reject downconverter, limiting amplifier, transmit image-reject mixer, and VGA	PCS phones (PWT1900, PACS, PHS), wireless local loop, RF transceivers	5.94

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Gain (dB) @ Icc (mA)	P1 (dBm)	Noise Figure (dB)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
GENERAL-PURPOSE RF PRODUCTS									
MAX2611	4.5 to 6.5	DC to 1100	18.5 @ 16	3	3.5	SOT143	Wideband gain block, low noise and high output capability	Satellite receivers, TV, tuners, wireless LANs, ISM radios	0.66
MAX2630	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT143	3V LNA with internal biasing	Portable phones, wireless LANs, ISM radios	0.70
MAX2631	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-5	3V LNA with shutdown. No external bias resistor.	Cordless phones, wireless LANs, ISM radios	0.74
MAX2632	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-5	3V LNA with bias control	Cordless phones, wireless LANs, ISM radios	0.74

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Gain (dB) @ ICC (mA)	P1 (dBm)	Noise Figure (dB)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
GENERAL-PURPOSE RF PRODUCTS (continued)									
MAX2633	2.7 to 5.5	100 to 1000	13.7 @ 7	-11	3.7	SOT23-6	3V LNA with shutdown and bias control	Cordless phones, wireless LANs, ISM radios	0.79
MAX2650	4.5 to 5.5	DC to 1000	19 @ 18	0	3.6	SOT143	5V low-noise amp with internal biasing	Satellite receivers, TV tuners, wireless LANs, ISM radios	0.66

Part Number	Supply Voltage (V)	Frequency Range (MHz)	Supply Current (mA)	Phase Noise (dBc/Hz)	Output Power (dBm)	Pins-Package Options*	Features	Applications	Price† 1000-up ($)
OSCILLATORS									
MAX2620	2.7 to 5.25	650 to 1050	9	-110 (at 25kHz offset from 900MHz carrier)	-3 (2 outputs) 0 (differential)	8-µMAX	Low voltage, lowest phase noise, dual outputs, superior isolation	Digital and analog cellular and cordless phones, PCS, pagers, ISM radios	1.98

* Package Options: MQFP = Modular Quad Flat Pack, SO = Small Outline, SSOP = Shrink Small-Outline Package, QSOP = Quarter Small-Outline Package

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†† Future product—contact factory for pricing and availability. Specifications are preliminary.

NOTE: IF = Intermediate Frequency, I/Q = In-Phase/Quadrature-Phase, VGA = variable-gain amplifier

19-1256; Rev 0; 7/97

EVALUATION KIT AVAILABLE

MAXIM

Direct-Conversion Tuner IC for Digital DBS Applications

General Description

The MAX2102† is a low-cost direct-conversion tuner IC designed for use in digital direct-broadcast satellite (DBS) television set-top box units. Its direct-conversion architecture reduces system cost compared to devices with IF-based architectures.

The MAX2102 directly tunes L-band signals to baseband using a broadband I/Q downconverter. Operating frequency range spans from at least 950MHz to 2150MHz.

The IC includes an LNA with AGC, two downconverter mixers, an oscillator buffer with 90° quadrature generator and prescaler, and baseband amplifiers.

Applications

DirecTV, PrimeStar, EchoStar DBS Tuners

DVB-Compliant DBS Tuners

Cellular Basestations

Wireless Local Loop

Broadband Systems

LMDS

Features

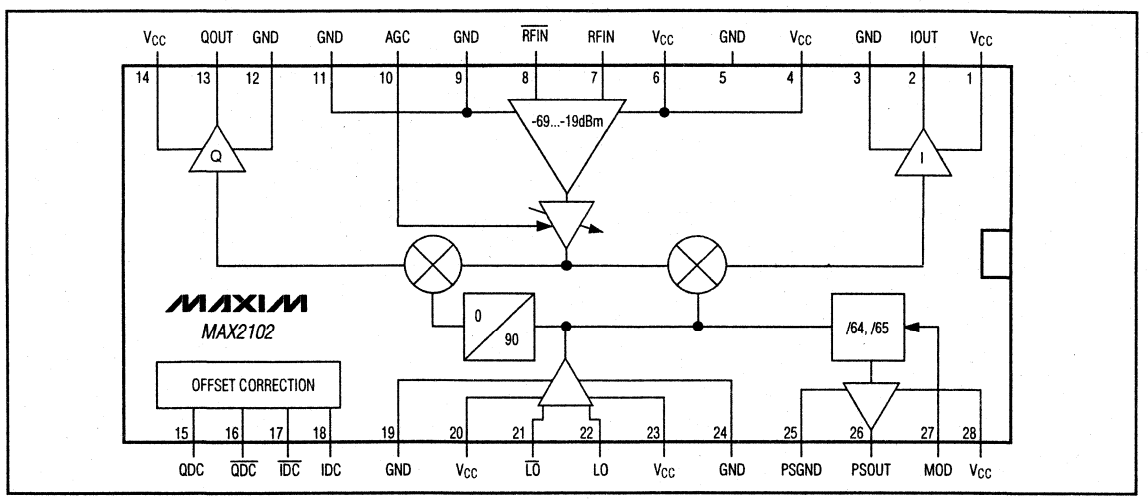
- ♦ **Low-Cost Bipolar Design, Lowest Cost Architecture**
- ♦ **Operates from Single +5V Supply**
- ♦ **950MHz to 2150MHz Input Frequency Range***
- ♦ **On-Chip Quadrature Generator, Dual-Modulus Prescaler (/64, /65)**
- ♦ **Input Levels: -19dBm to -69dBm per Carrier**
- ♦ **Over 50dB AGC Control Range**
- ♦ **Noise Figure = 13.2dB; IIP3 = 6.5dBm (at 1450MHz)**
- ♦ **Automatic Baseband Offset Correction**
- ♦ **Easy Interface to MAX1002/MAX1003 Dual ADC and Popular Baseband ICs**
- ♦ **Evaluation Kit Available, Tuner Reference Design Assistance Available**

**Contact factory for MAX2102 versions with expanded frequency range.*

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2102CWI	0°C to +70°C	28 SO

Functional Diagram



†*Patents Pending*

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

Direct-Conversion Tuner IC for Digital DBS Applications

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.5V to 7V
RFIN to $\overline{RFIN}$ .....±2V
LO- to $\overline{LO}$ .....±2V
AGC, MOD, RFIN, $\overline{RFIN}$, LO, $\overline{LO}$ to GND...-0.5V to (V_{CC} + 0.5V)
AGC CURRENT .....±50mA
IDC to $\overline{IDC}$, QDC to $\overline{QDC}$.....±2V
IOUT or QOUT to GND Short-Circuit Duration 10sec
PSOUT to GND Short-Circuit Duration.....None

IDC, $\overline{IDC}$, QDC, $\overline{QDC}$ to GND .....-0.5V to (V_{CC} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
SO (derate 12.50mW/°C above + 70°C).....1.025W
Operating Temperature Range
MAX2102CWI.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.25V; GND = 0V; PSGND = GND; AGC = 1.3V; MOD = 0.8V; P_{RFIN} = OFF; f_{LO} = 1450.125MHz; P_{LO} = -15dBm; I_{OUT}, Q_{OUT} = open; T_A = 0°C to +70°C; unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY					
Supply Voltage		4.75		5.25	V
Supply Current			150	195	mA
CONTROL INPUTS, PRESCALER					
MOD Input Low Level				0.8	V
MOD Input High Level		2.0			V
MOD Input Bias Current	0V < MOD < V_{CC}	-80		10	µA
AGC Input Bias Current	1V < AGC < 4V	-180		180	µA
IOUT, QOUT Common-Mode Voltage		2.2		2.6	V

AC ELECTRICAL CHARACTERISTICS

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF FRONT END					
RFIN Carrier Frequency Range	(Note 1)	950		2150	MHz
RFIN Maximum Single-Carrier Input Power	Refers to single-carrier power generating V_{IOUT} = V_{QOUT} = 0.5Vp-p. 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Note 4)	-19			dBm
RFIN Minimum Single-Carrier Input Power	Refers to single-carrier power generating V_{IOUT} = V_{QOUT} = 0.5Vp-p. 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Note 4)			-69	dBm
AGC Range	1V < V_{AGC} < 4V	50			dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RFIN Input Third-Order Intercept Point	P_{RFIN} = -19dBm per tone, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p per tone, $f1_{RFIN}$ = 1448.1MHz, $f2_{RFIN}$ = 1449MHz, f_{LO} = 1451MHz			6.5		dBm
RFIN Input Second-Order Intercept Point	P_{RFIN} = -19dBm per tone, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p per tone, $f1_{RFIN}$ = 1200MHz, $f2_{RFIN}$ = 2150MHz, f_{LO} = 951MHz			15.1		dBm
Noise Figure	f_{RFIN} = 1441MHz, f_{LO} = 1451MHz	P_{RFIN} = -69dBm		13.2		dB
	f_{RFIN} = 2141MHz, f_{LO} = 2151MHz	P_{RFIN} = -69dBm		12.9		
		AGC = 4V, P_{RFIN} set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p		11.2		
Maximum Noise-Figure Variation with AGC Gain Setting	Defined as ΔNF/ΔGain; for AGC range, defined as single-carrier power range of -69dBm to -59dBm			-0.5		dB/dB
RFIN Worst-Case VSWR across Band	f_{RFIN} = 950MHz to 2150MHz, 50Ω source			2.3:1		
Maximum Power of Spurious Downconversion Products	950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz. Dominated by LO second-harmonic power causing downconversion of unwanted channel. Test conditions: f_{LO} = 1075.5MHz, f_{RFIN} = 2150MHz, P_{RFIN} = -69dBm			32.3		dBc
LO Leakage at RFIN	P_{LO} = -15dBm, 950MHz < f_{LO} < 2150MHz (Note 2)				-49	dBm
	P_{LO} = -15dBm, $P_{\overline{LO}}$ = -15dBm (differentially driven), 950MHz < f_{LO} < 2150MHz (Note 2)				-54	

Direct-Conversion Tuner IC for Digital DBS Applications

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
OSCILLATOR BUFFER, QUADRATURE GENERATOR, PRESCALER						
LO Input Frequency Range	(Note 1)		950		2150	MHz
LO Input Worst-Case VSWR over Band	f_{LO} = 950MHz to 2150MHz, 50Ω source into MAX2102 EV kit match circuit			1.75:1		
LO Input Power Level	(Note 3)		-15		-5	dBm
	Refers to power level driven into LO, $\overline{LO}$ (differentially driven) (Notes 3, 4)		-15			
RFIN to LO Input Isolation	(Notes 4, 5)		28			dB
IOUT, QOUT Phase Imbalance	950MHz < f_{RFIN} < 2150MHz; 950MHz < f_{LO} < 2150MHz; P_{RFIN} = -40dBm; f_{IOUT}, f_{QOUT} = 125kHz (Note 4)				3	degrees
Worst-Case Additional Phase Imbalance Over Temperature	T_A = +25°C to +70°C (Notes 4 and 8)			-0.1	0.6	degrees
	T_A = +25°C to +0°C (Note 4)			0.07	1	
IOUT, QOUT Amplitude Imbalance	950MHz < f_{RFIN} < 2150MHz; 950MHz < f_{LO} < 2150MHz; P_{RFIN} = -40dBm; f_{IOUT}, f_{QOUT} = 125kHz (Note 4)				0.5	dB
Prescaler Divide Ratio	T_A = 0°C to +70°C (Note 4)	MOD = low	64		64	
		MOD = high	65		65	
Prescaler Output Swing at PSOUT	2kΩ || 10pF load		0.8			Vp-p
Prescaler Duty Cycle at PSOUT	PSOUT load = 2kΩ || 5pF (Note 2)		35		65	%
BASEBAND AC CHARACTERISTICS						
IOUT, QOUT Clipping Level	P_{RFIN} = -50dBm; AGC = 4V, V_{CC} = 5.0V			2.7		Vp-p
Baseband Bandwidth (at IOUT, QOUT)	At -3dB attenuation			94		MHz
Baseband Gain Ripple (at IOUT, QOUT)	1kHz > $f_{IOUT, QOUT}$ > 25MHz, 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Notes 2, 6, 7)			0.45	0.85	dB
Baseband Group Delay Ripple (at IOUT, QOUT)	1kHz > $f_{IOUT, QOUT}$ > 25MHz, 950MHz < f_{RFIN} < 2150MHz, 950MHz < f_{LO} < 2150MHz (Notes 2, 6)			0.45		ns

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2102 EV kit circuit (Figure 1); V_{CC} = 5V; PSGND = open; MOD = GND; f_{RFIN} = 2150MHz; P_{RFIN} = -19dBm; f_{LO} = 2150.125MHz; P_{LO} = -15dBm driven single-ended into LO; AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p; IOUT, QOUT drives AC-coupled 100Ω load; 2kΩ from PSOUT to GND; T_A = +25°C; unless otherwise noted.)

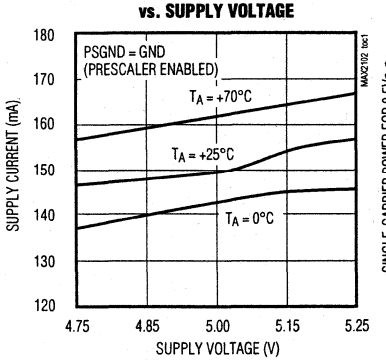
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IOUT, QOUT Output Impedance	(Note 2)		4.7	10	Ω
Maximum IOUT to QOUT Output Impedance Difference	(Note 2)		±1		Ω
Power-Supply Ripple Rejection (measured at IOUT, QOUT)	V_{CC} = 5V + 50mVp-p at 300kHz. Amplitude of 300kHz relative to 500mVp-p measured at IOUT, QOUT. Measured using MAX2102 EV kit.		32		dBc

Note 1: All specifications with guaranteed min/max limits are met within this frequency range. Contact factory for MAX2102 versions with expanded frequency range.
Note 2: Guaranteed by design and characterization.
Note 3: IOUT, QOUT Phase and Amplitude Imbalance specifications are met within this LO power range.
Note 4: Guaranteed by production test and/or design and characterization.
Note 5: Tested under two conditions: 1) Normal test: P_{RFIN} = -20dBm, and 2) Overdrive test: P_{RFIN} = -5dBm but AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p for P_{RFIN} = 30dBm.
Note 6: Includes contribution from front-end gain tilt and delay variations produced by varying f_{RFIN} by ±30MHz.
Note 7: 1kHz minimum frequency determined by 0.22µF offset-correction capacitors. Different value capacitors yield proportionally different low-frequency cutoffs. Group delay at low frequencies will also be affected. See *Applications Information* section.
Note 8: Negative numbers (-0.1°) indicate improvement in quadrature accuracy with increasing temperature.

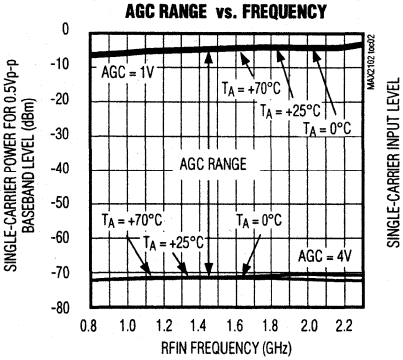
Typical Operating Characteristics

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

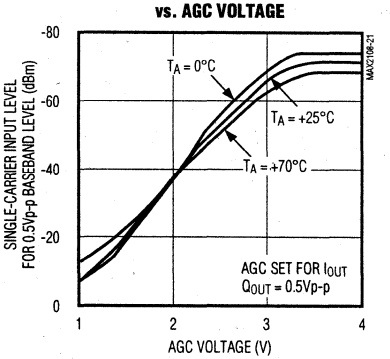
SUPPLY CURRENT vs. SUPPLY VOLTAGE



AGC RANGE vs. FREQUENCY



CARRIER LEVEL vs. AGC VOLTAGE

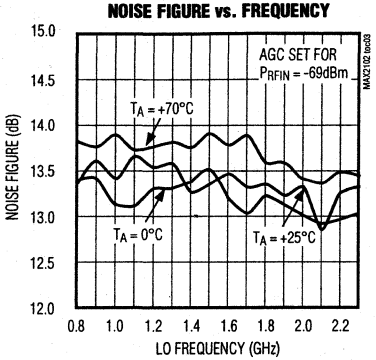


Direct-Conversion Tuner IC for Digital DBS Applications

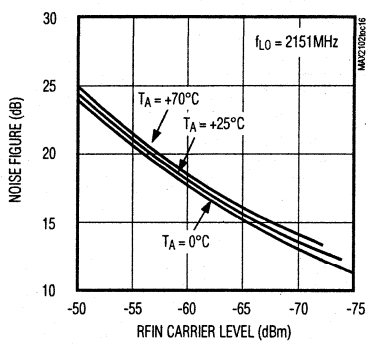
Typical Operating Characteristics (continued)

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

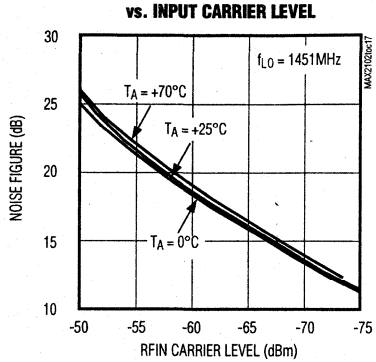
NOISE FIGURE vs. FREQUENCY



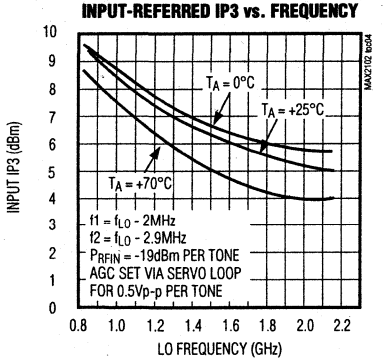
NOISE FIGURE vs. INPUT CARRIER LEVEL



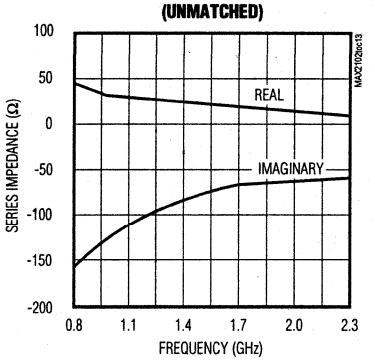
NOISE FIGURE vs. INPUT CARRIER LEVEL



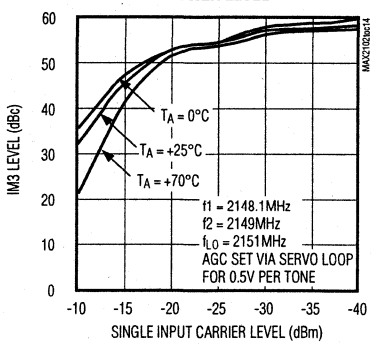
INPUT-REFERRED IP3 vs. FREQUENCY



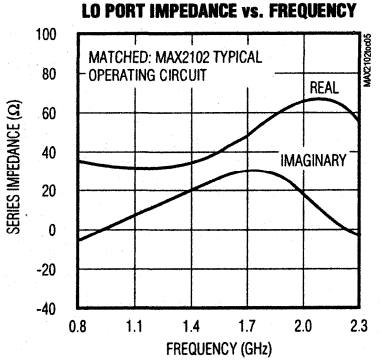
LO PORT IMPEDANCE vs. FREQUENCY (UNMATCHED)



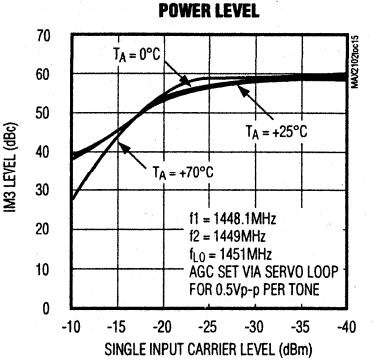
IM3 LEVELS vs. INPUT CARRIER POWER LEVEL



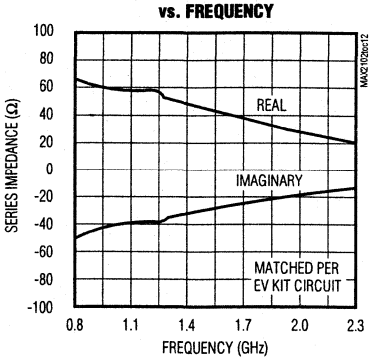
LO PORT IMPEDANCE vs. FREQUENCY



IM3 LEVELS vs. INPUT CARRIERS POWER LEVEL



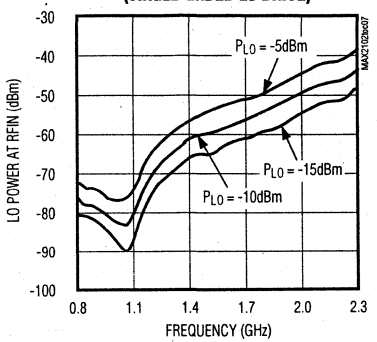
RFIN PORT IMPEDANCE vs. FREQUENCY



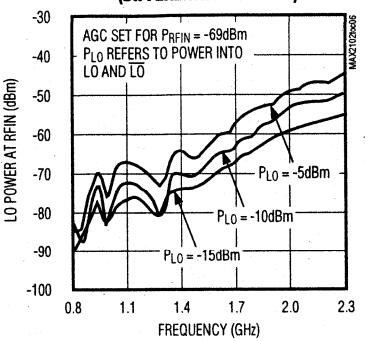
Typical Operating Characteristics (continued)

(MAX2102 EV kit circuit (Figure 1), V_{CC} = 5V, PSGND = open, MOD = GND, f_{RFIN} = 2150MHz, P_{RFIN} = -19dBm, f_{LO} = 2150.125MHz, P_{LO} = -15dBm driven single-ended into LO, AGC set via servo loop for V_{IOUT} = V_{QOUT} = 0.5Vp-p, IOUT, QOUT drives AC-coupled 100Ω load, 2kΩ from PSOUT to GND, T_A = +25°C, unless otherwise noted.)

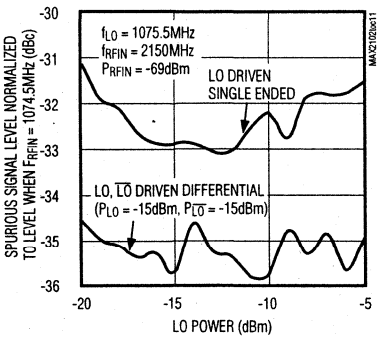
LO LEAKAGE AT RFIN vs. FREQUENCY (SINGLE-ENDED LO DRIVE)



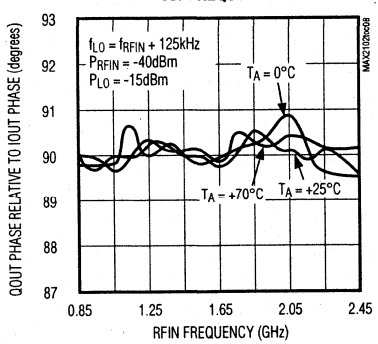
LO LEAKAGE AT RFIN vs. FREQUENCY (DIFFERENTIAL LO DRIVE)



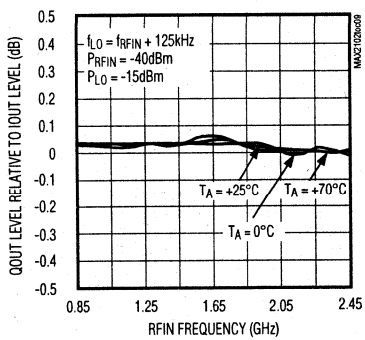
SPURIOUS DOWNCONVERSION DUE TO INTERNALLY GENERATED LO 2ND HARMONIC



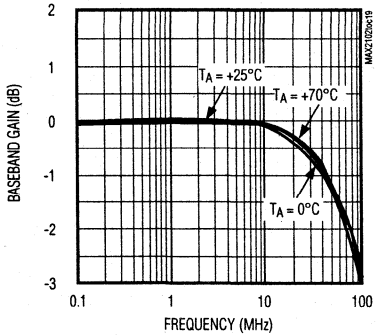
QUADRATURE PHASE IMBALANCE vs. FREQUENCY



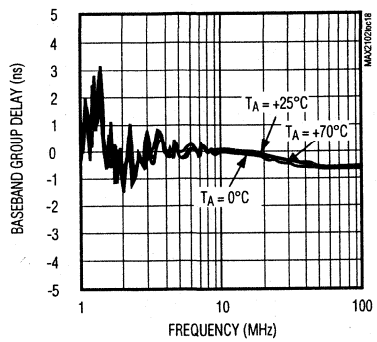
QUADRATURE GAIN IMBALANCE vs. FREQUENCY



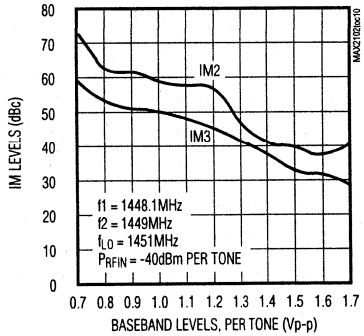
BASEBAND GAIN FLATNESS vs. FREQUENCY



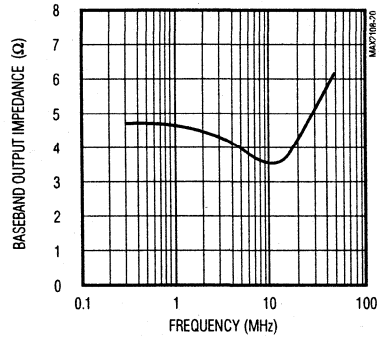
BASEBAND GROUP DELAY FLATNESS vs. FREQUENCY



BASEBAND IM LEVELS



BASEBAND OUTPUT IMPEDANCE vs. FREQUENCY



Direct-Conversion Tuner IC for Digital DBS Applications

Pin Description

PIN	NAME	FUNCTION
1	V_{CC}	Baseband +5V Supply. Bypass with a 10pF capacitor from this pin to pin 3 (GND), as close to the IC as possible. Connect an additional 0.1µF capacitor in parallel with the 10pF capacitor (placement less critical).
2	IOUT	I Channel Baseband Output
3, 12	GND	Baseband Ground
4	V_{CC}	RF +5V Supply. Bypass with a 22pF capacitor from this pin to pin 11 (GND), as close to the IC as possible.
5	GND	Ground (substrate)
6	V_{CC}	RF +5V Supply. Bypass with a 22pF capacitor from this pin to pin 9 (GND), as close to the IC as possible.
7	RFIN	RF Noninverting Input. Couple through a 22pF capacitor directly to a 50Ω signal source.
8	$\overline{RFIN}$	RF Inverting Input. Connect to a 22pF series capacitor and a 51Ω resistor to ground.
9, 11, 19, 24	GND	RF Ground. Connect directly to the ground plane.
10	AGC	Automatic Gain-Control Input. Bypass this pin with a 1000pF capacitor close to the pin, to minimize coupling.
13	QOUT	Q Channel Baseband Output
14	V_{CC}	Baseband +5V Supply. Bypass with a 10pF capacitor from this pin to pin 12 (GND), as close to the IC as possible. Connect an additional 0.1µF capacitor in parallel with the 10pF capacitor (placement less critical).
15	QDC	Q Channel Offset-Correction Noninverting Input. Connect a 0.22µF (typ) capacitor between QDC and $\overline{QDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
16	$\overline{QDC}$	Q Channel Offset-Correction Inverting Input. Connect a 0.22µF (typ) capacitor between QDC and $\overline{QDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
17	$\overline{IDC}$	I Channel Offset-Correction Inverting Input. Connect a 0.22µF (typ) capacitor between IDC and $\overline{IDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
18	IDC	I Channel Offset-Correction Noninverting Input. Connect a 0.22µF (typ) capacitor between IDC and $\overline{IDC}$. This capacitor must be placed as close to the IC as possible. See *Layout Considerations* section.
20	V_{CC}	RF +5V Supply. Bypass with a 10pF capacitor from this pin to pin 19 (GND) as close to the IC as possible.
21	$\overline{LO}$	Local-Oscillator Complementary Input Port (Figure 1)
22	LO	Local-Oscillator Input Port (Figure 1)
23	V_{CC}	RF +5V Supply. Bypass with a 10pF capacitor from this pin to pin 24 (GND) as close to the IC as possible.
25	PSGND	Prescaler Ground. To disable the prescaler, leave this pin open.
26	PSOUT	Prescaler Output. Drives CMOS load. Connect 2kΩ from this pin to GND (if the prescaler is enabled).
27	MOD	Prescaler Modulus Control. Leave open when the prescaler is disabled.
28	V_{CC}	Prescaler +5V Supply. Bypass with a 1000pF capacitor. **Must be connected even if the prescaler is disabled.**

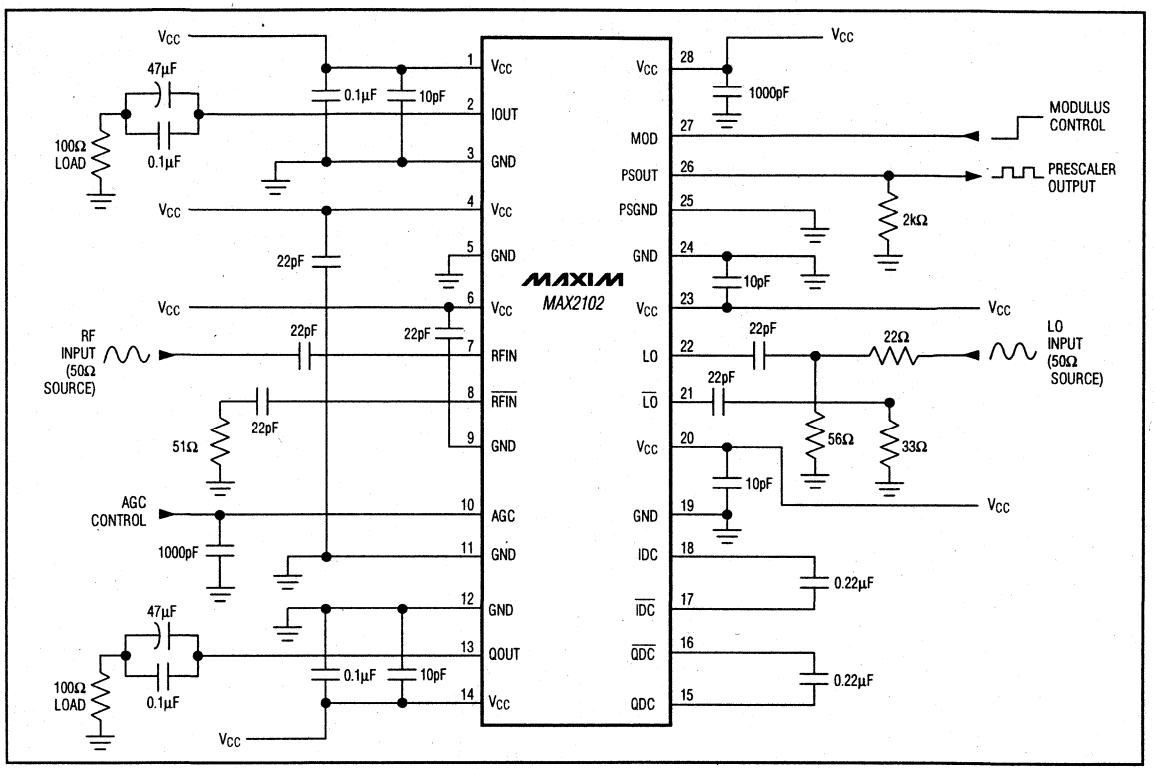


Figure 1. Typical Operating Circuit

Detailed Description

The MAX2102 downconverts signals in the range 950MHz to 2150MHz directly to baseband I/Q signals. It is targeted for digital DBS tuner applications where a direct downconversion provides a cost savings over prior-art multiple-conversion approaches. However, the MAX2102 is applicable to any system requiring a broadband I/Q downconversion.

Internally, the MAX2102 consists of a broadband front-end variable gain stage, a quadrature downconverter, an oscillator buffer, high-linearity I and Q baseband amplifiers, and offset correction amplifiers.

The front-end AGC dynamic range is over 50dB. Specifically, the AGC control can be adjusted so that a sine wave at RFIN ranging in power from -69dBm to -19dBm will produce a sine wave at IOUT and QOUT at 500mVp-p levels. The noise figure is lowest when the AGC is at its maximum gain setting (see *Typical Operating Characteristics*). The VSWR at RFIN is unaffected by the AGC setting.

The LO buffer accepts an external LO signal at LO, $\overline{LO}$, and internally limits the signals to provide a consistent on-chip LO level. The LO input drive level should be maintained within the specified limits (see *Applications Information* section).

The quadrature downconverter follows the front-end AGC. Two mixers are driven by the previous stage AGC amplifier output. The mixer LO ports are fed with the two LO signals, which are 90° apart in phase. These quadrature LO signals are generated on-chip using the LO signals from the LO buffer.

The resulting I/Q baseband signals are fed through separate I and Q channel baseband amplifiers. Robust output stages drive IOUT and QOUT. The outputs are capable of driving lowpass filters with 100Ω characteristic impedance (that is, the equivalent of an AC-coupled, 100Ω load). The baseband -3dB output bandwidth is over 90MHz.

Direct-Conversion Tuner IC for Digital DBS Applications

Applications Information

Front-End Tuner Circuitry for DBS Tuners

In a typical application, the signal path ahead of the MAX2102 will include a discrete LNA/buffer and a PIN-diode attenuator. Alternatively, a dual-gate GaAsFET can serve this function. This circuitry is usually required in order to meet system noise-figure requirements, may provide a buffered F-connector output, and may also be required to meet stringent LO leakage requirements. The PIN attenuator is typically controlled by the same voltage as the MAX2102 AGC control pin so that, overall, a single AGC line from the baseband processor can control the entire tuner.

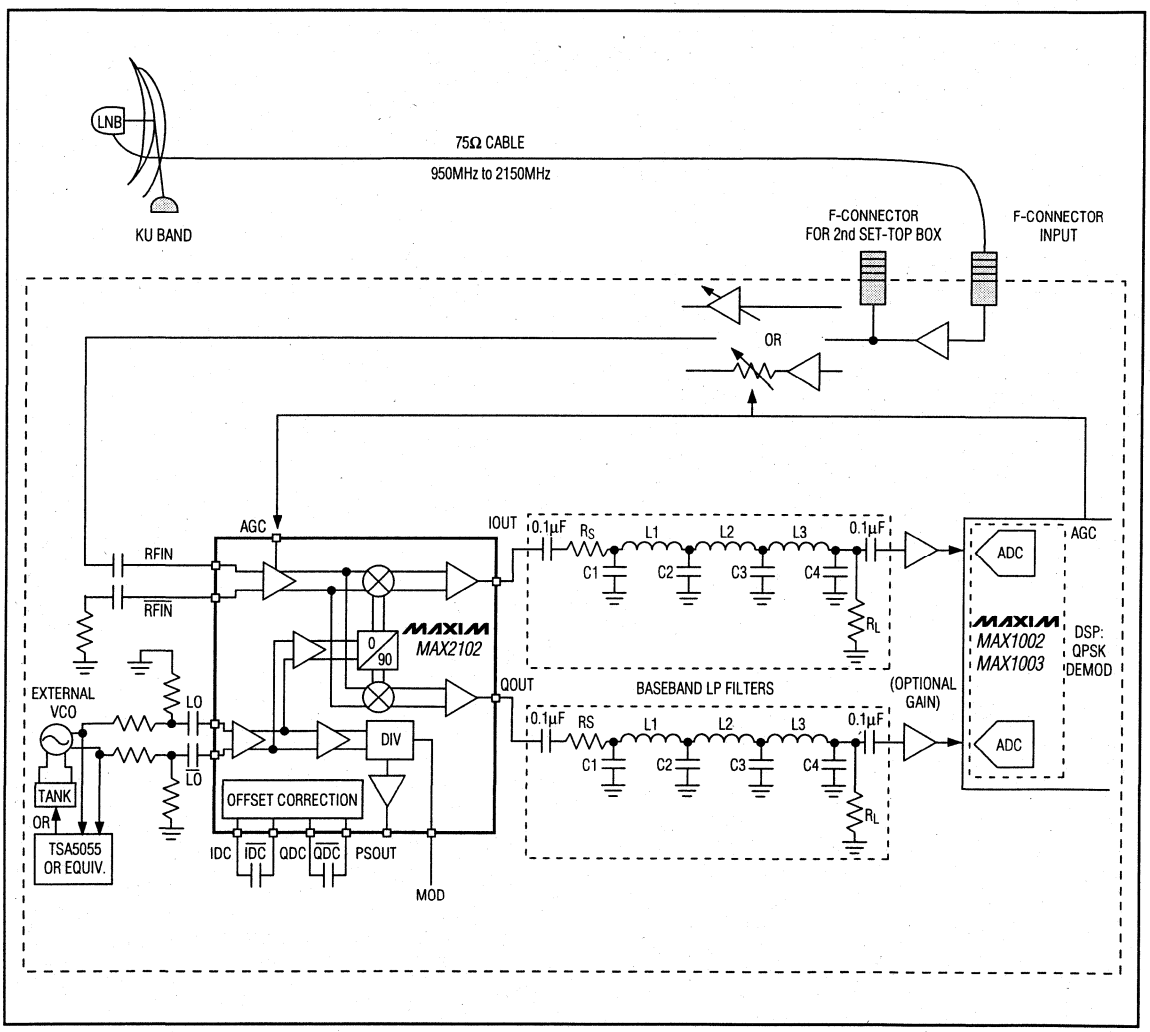


Figure 2. Typical Application

In some applications, a varactor-tuned preselection bandpass filter is added between the discrete LNA and the MAX2102. This is usually required only for very high-linearity tuners, such as those designed for SCPC (low-data-rate) applications. The filter provides a means of broadly filtering adjacent interferers, thus improving the intermodulation performance of the tuner. Additionally, the filter removes the RF interferer at twice the LO frequency, which would otherwise add to cochannel interference (the MAX2102 alone rejects this carrier to approximately 32.3dBc).

External Oscillator

Since the MAX2102 is a direct-conversion receiver, the external LO must tune to the same frequencies as the desired RF input signals.

The MAX2102 oscillator input port (LO, $\overline{LO}$) accepts either a single-ended or differential (balanced) LO signal. A differential LO offers reduced LO leakage to the RFIN port, as well as lower spurious downconversion levels of RF signals, which are at twice the LO frequency. Refer to Figure 3 for differential LO connections. For best performance, ensure that the LO and $\overline{LO}$ traces are symmetrical.

The LO drive levels should be maintained to within the specified limits. If the LO drive falls below the specified range, quadrature performance may be affected. Driving LO above the specified limits will cause a higher LO leakage level at RFIN; this may be acceptable in some applications. The MAX2102 offset-correction loop can withstand LO leakage levels corresponding to at least 0dBm of LO input power drive.

Prescaler

Typical stand-alone tuner applications will not use the MAX2102 prescaler function, but instead use a commercial synthesizer IC such as the Philips TSA5055, which has an internal prescaler. To disable the MAX2102 prescaler, disconnect the PSGND pin (leave open). The prescaler will cause an output spur in the baseband spectrum, to a level of about -20dBc (referred to 500mVp-p baseband output level), which may land within the desired signal bandwidth in some applications.

To use the MAX2102 prescaler, connect the PSGND pin to ground. In some applications, the prescaler may be toggled on and off using a MOSFET to switch PSGND to ground. PSGND should be forced to within

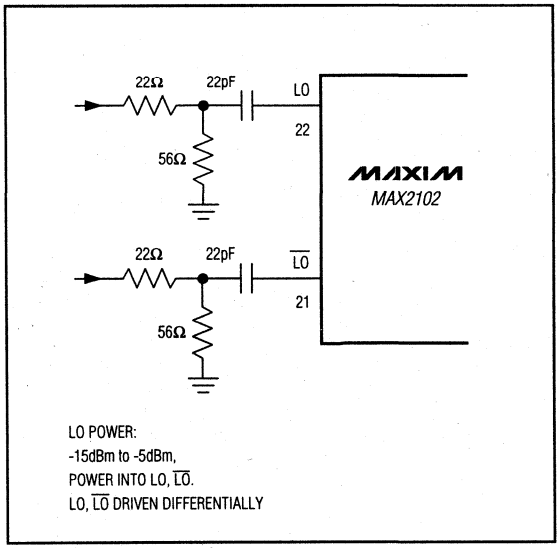


Figure 3. Differential LO Drive

100mV of ground, and the MOSFET must be capable of sinking 15mA. PSOUT is capable of driving a typical CMOS load of 10kΩ in parallel with 5pF. A 2kΩ pull-down resistor must be connected from PSOUT to GND.

The prescaler requires a stable level at the MOD pin 12ns before the falling edge of PREOUT to assert the desired modulus. The level at MOD must remain static until 3ns after this falling edge.

Baseband Amplifiers

The MAX2102 baseband amplifiers provide over 2Vp-p swing at IOUT and QOUT, and are capable of driving 100Ω. IOUT and QOUT must be AC-coupled to any lowpass filters. In a typical application, IOUT and QOUT drive a 5th- or 7th-order lowpass filter for ADC antialiasing purposes (see *Systems Considerations: Lowpass Filters in Direct-Conversion Tuners*). After the filters, in some cases, additional gain may be required. This can be accomplished with a pair of video-speed op amps, such as the MAX4216 dual video op amp. Alternatively, the MAX1002/MAX1003 dual ADC has built-in gain ahead of the ADCs, digitizing levels as low as 125mVp-p. Contact Maxim for more information about the MAX4216 or the MAX1002/MAX1003.

Direct-Conversion Tuner IC for Digital DBS Applications

Offset Correction

The internal offset-correction amplifiers remove the DC offsets present in the baseband amplifiers. The offset-correction loop effectively AC-couples the baseband signal path, yielding a -3dB highpass corner frequency according to the following:

$$f_{-3dB} = 100 / C_{DC}\ (\mu F)$$

where C_{DC} is the value of the capacitors, in microfarads, across QDC, $\overline{QDC}$ and IDC, $\overline{IDC}$.

For applications where the DC information must be maintained through the signal path, the offset correction can be disabled by connecting QDC, $\overline{QDC}$, IDC, and $\overline{IDC}$ directly to ground. Disabling the offset correction will effectively limit the input dynamic range of the MAX2102. Typical input dynamic range will be approximately -45dBm to -19dBm for single-ended LO drive, and -55dBm to -19dBm for differential LO drive.

Layout Considerations

Observe standard RF layout rules. A ground plane is essential; when connecting areas of ground plane between layers, use vias liberally. Remove the ground plane under the external VCO area to reduce parasitic capacitance. If a ground plane is used under the lowpass filters, note that the filter shape may be slightly offset due to parasitic capacitance.

In a direct-conversion receiver, LO leakage to the RF input connector is a major issue, since filtering of the LO is impossible (the LO operates at the same frequency as the RF input). The external VCO section should be housed in a separate shielded compartment, if possible. Use of a differential (balanced) LO will dramatically reduce LO leakage. Also, the use of coplanar waveguide transmission-line structures reduces LO leakage (used on the MAX2102 EV kit).

Observe the power-supply bypass capacitor connections in the *Pin Description* table, notably pins 1, 3, 4, 6, 9, 11, 12, 14, 19, 20, 23, and 24. Traces from these IC pins to the bypass capacitors must be kept to an absolute minimum. Where possible, make these connections on the top side of the board.

Minimize parasitic capacitance to ground around the offset-correction circuit (pins 15–18) by removing the ground plane beneath these pins and placing the offset-correction capacitors as close to the IC as possible.

The MAX2102 EV kit includes ferrite beads in series with power-supply leads. The beads may not be required for all applications.

Table 1. Suggested Component Values for Discrete Lowpass Filters (0.1dB Ripple Chebyshev Type)

ADC SAMPLING RATE (Msps)	FILTER TYPE	R_S (Ω)	C1 (pF)	L1 (nH)	C2 (pF)	L2 (nH)	C3 (pF)	L3 (nH)	C4 (pF)	R_L (kΩ)
40	0.1dB Chebyshev, f_C = 20MHz	100	39	910	120	1500	150	1500	120	10
60	0.1dB Chebyshev, f_C = 30MHz	100	22	620	82	910	100	1000	820	10
90	0.1dB Chebyshev, f_C = 45MHz	100	18	390	56	620	68	680	56	10

Note: Suggested types: inductors: Coilcraft 1008CS, tolerance = ±5%; capacitors: use tolerance = ±2%. Refer to Figure 2 for circuit diagram.

Power-Supply Sequencing

The MAX2102 has several +5V supply pins. The supply layout should be in a star format, with a bypass capacitor that dominates the rise time of the supply at the center of the star, to ensure that all pins see approximately the same voltage during power-up.

The prescaler V_{CC} (pin 28) must be connected to the same V_{CC} as the other V_{CC} pins, even if the prescaler is not used. Leaving PSGND open will disable the prescaler function and, in this state, the prescaler will not dissipate any power.

Systems Considerations: Lowpass Filters in Direct-Conversion Tuners

Typically, a 5th or 7th-order L-C lowpass filter is used for anti-aliasing the ADCs following the MAX2102. Figures 4 and 5 describe typical filtering requirements. Table 1 offers suggested component values for these lowpass filters.

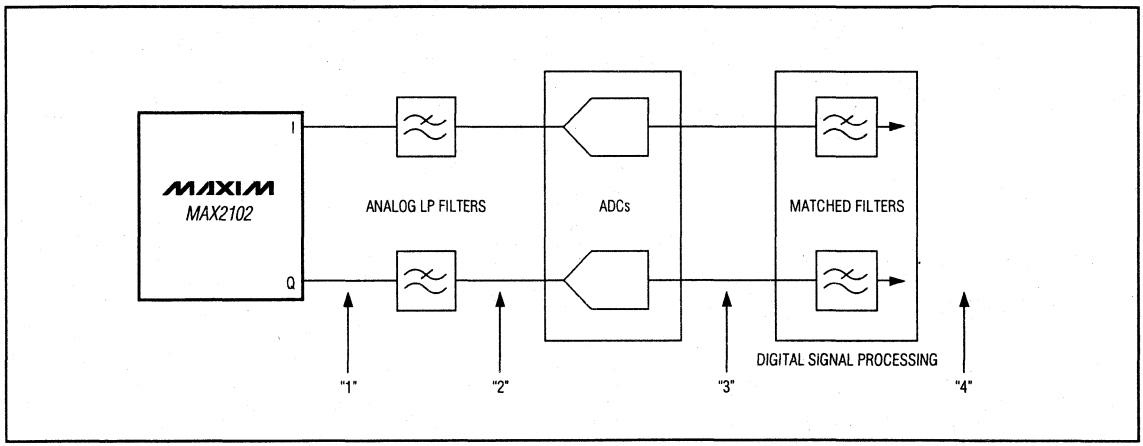


Figure 4. I, Q Signal Path

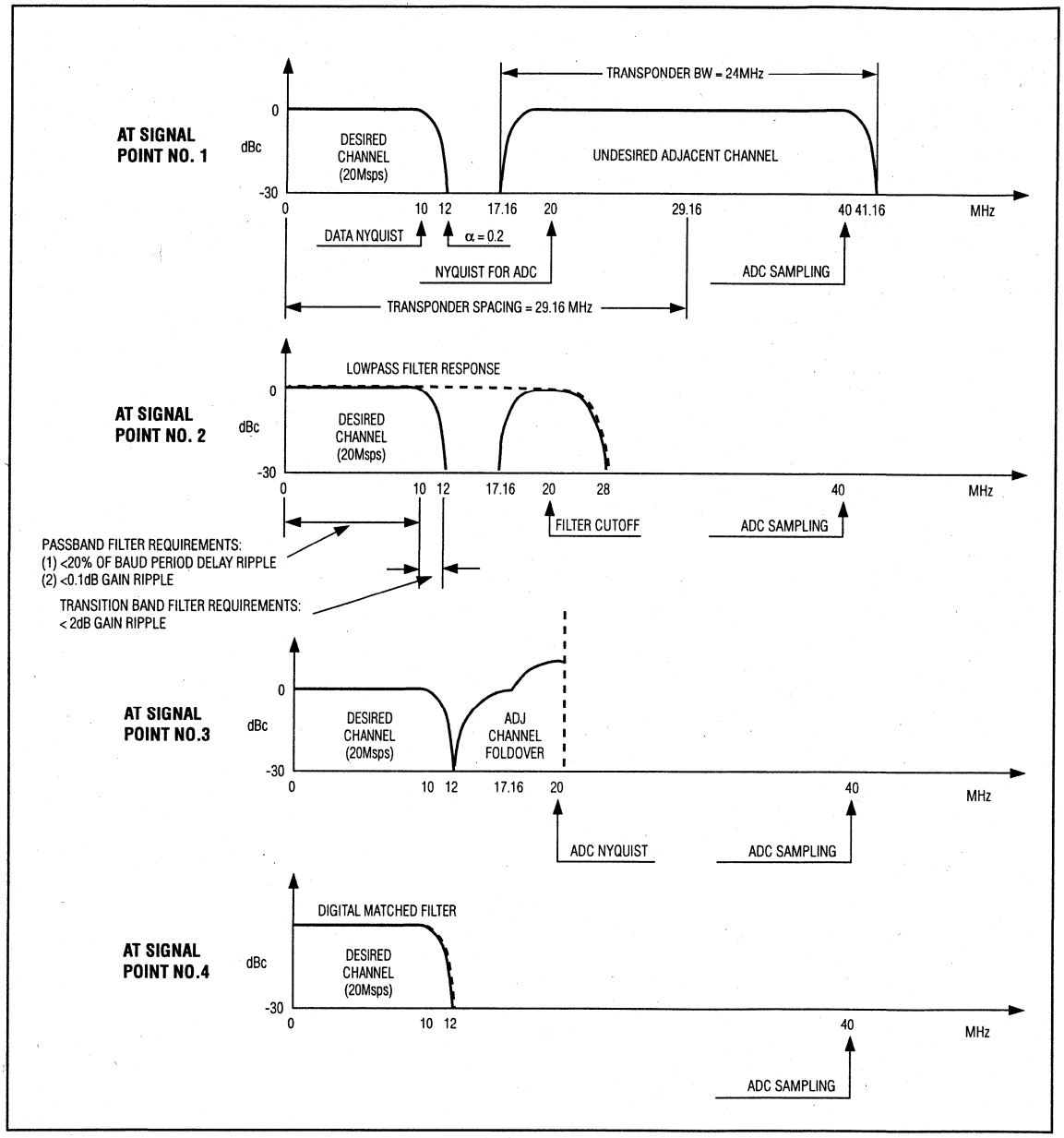


Figure 5. Lowpass Filtering Example Note: Data Rate = 40Mbps, Transponder BW = 24MHz, Transponder Spacing = 29.16MHz, Nyquist Filter: α = 0.2

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

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MAXIM

Low-Cost Downconverter with Low-Noise Amplifier

General Description

The MAX2406 is designed for use over a wide range of frequencies and is optimized for communication systems operating around 1.9GHz. Applications include PWT1900/DCT1900, DCS1800/PCS1900, PHS, and DECT. This device includes a low-noise amplifier, a downconverter mixer, and a local-oscillator buffer in a low-cost, plastic surface-mount package. The LNA has a 2.5dB noise figure and a -9.5dBm input IP3. The downconverter mixer has a low 9dB noise figure and a 4dBm input third-order intercept point. Image and local-oscillator filtering are implemented off-chip for maximum flexibility.

The MAX2406 has a differential IF output port, which can be used in a single-ended configuration by tying the unused side to V_{CC}. The LO buffer can also be driven differentially or in a single-ended configuration with only -10dBm of LO power. Power consumption is only 60mW in receive mode and drops to less than 3µW in shutdown mode.

For transceiver applications, the MAX2410 or MAX2411A both offer a transmitter along with a similar receiver.

Applications

PWT1900/DCT1900

DCS1800/PCS1900

PHS/PACS

DECT

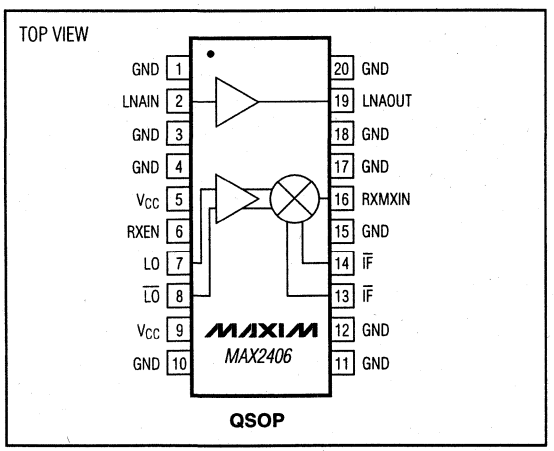
Features

- **+2.7V to +5.5V Single-Supply Operation**
- **Integrated LNA/Downconverter**
- **3.2dB Combined Receiver Noise Figure (2.5dB LNA, 9dB mixer)**
- **-12.3dBm Combined Receiver Input IP3 (-9.5dBm LNA, 4dBm mixer)**
- **LO Buffer**
- **60mW Power Consumption**
- **<3µW Shutdown Mode**

Ordering Information

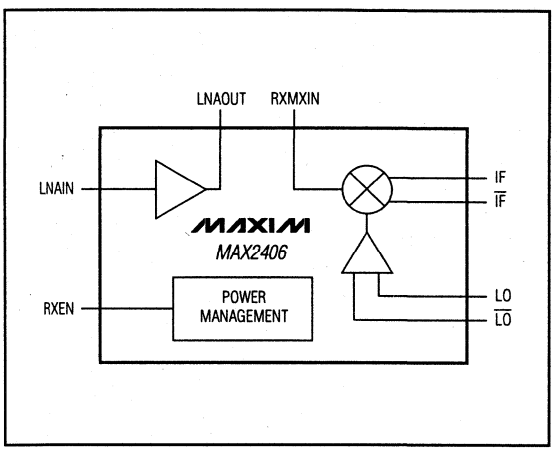
PART	TEMP. RANGE	PIN-PACKAGE
MAX2406EEP	-40°C to +85°C	20 QSOP

Pin Configuration



QSOP

Functional Diagram



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

MAXIM

Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver

General Description

The MAX2410 is designed for use over a wide range of frequencies and is optimized for TDD systems operating at 1.9GHz. Applications include PWT1900/DCT1900, DCS1800/PCS1900, PHS, and DECT. This device includes a low-noise amplifier, a downconverter mixer, a local-oscillator buffer, an upconverter mixer, and an output PA predriver amplifier in a low-cost, plastic surface-mount package.

The LNA has a 2.5dB (typ) noise figure and a -9.5dBm input IP3. The downconverter mixer has a low 9dB noise figure and 3dBm input third-order intercept point. Image and local oscillator filtering are implemented off-chip for maximum flexibility. The PA driver has 14.5dB gain, which can be reduced over a >20dB range. Power consumption is only 60mW in receive mode and 90mW in transmit mode while putting out 3dBm, and it drops to less than 3µW in shutdown mode (TXEN = RXEN = low).

For applications that use the same IF filter for both transmit and receive, refer to the MAX2411A, which offers one common differential IF port. For a receive-only version, consult the MAX2406 data sheet.

Applications

PWT1900/DCT1900
DCS1800/PCS1900
PHS/PACS
DECT

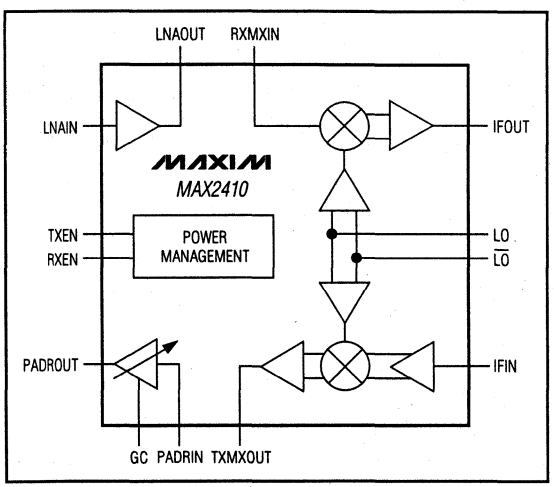
Features

- **+2.7V to +5.5V Single-Supply Operation**
- **Integrated Upconvert/Downconvert Function**
- **3.2dB Combined Receiver Noise Figure (2.5dB LNA, 9dB mixer)**
- **-12.5dBm Combined Receiver Input IP3 (-9.5dBm LNA, 3dBm mixer)**
- **3dBm Transmit Compression Power**
- **20dB Transmit Gain-Control Range**
- **LO Buffer**
- **Low Power Consumption:**
  60mW (receive mode)
  90mW (full-power transmit mode)
- **Low-Power Shutdown Mode**
- **Advanced System Power Management**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2410EEI	-40°C to +85°C	28 QSOP

Block Diagram



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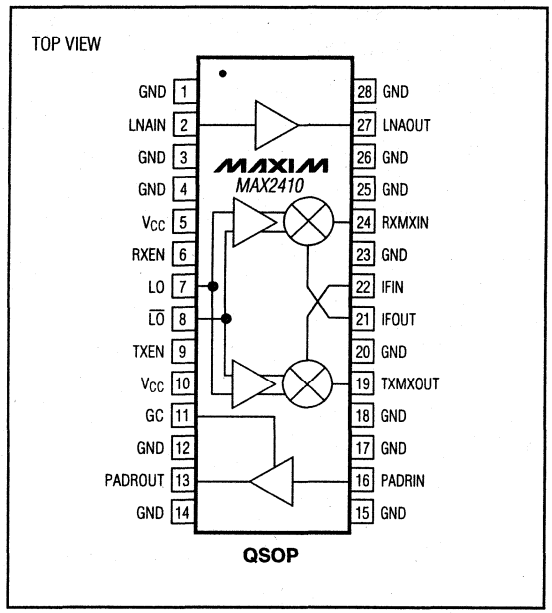
For small orders, phone 408-737-7600 ext. 3468.

Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver

Pin Configuration



ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver

General Description

The MAX2411A is designed for use over a wide range of frequencies and is optimized for TDD systems operating around 1.9GHz. Applications include PWT1900/DCT1900, DCS1800/PCS1900, PHS, and DECT. This device includes a low-noise amplifier, a downconverter mixer, a local-oscillator buffer, an upconverter mixer, and an output PA predriver amplifier in a low-cost, plastic surface-mount package. The LNA has a 2.5dB (typ) noise figure and a -9.5dBm input IP3. The downconverter mixer has a low 9dB noise figure and 3dBm input third-order intercept point. Image and local-oscillator filtering are implemented off-chip for maximum flexibility.

The MAX2411A has a common (shared) differential IF port. This bidirectional port eliminates the need for separate transmit and receive filters, at a significant cost savings. The PA driver has 14.5dB gain, which can be reduced over a >20dB range. Power consumption is only 60mW in receive mode and 90mW in transmit mode while putting out 3dBm, and it drops to less than 3µW in shutdown mode (TXEN = RXEN = low).

For applications where separate transmit and receive IF ports are required, consult the MAX2410 data sheet. The MAX2406 is a receive-only version of the MAX2411A.

Applications

PWT1900/DCT1900
DCS1800/PCS1900
PHS/PACS
DECT

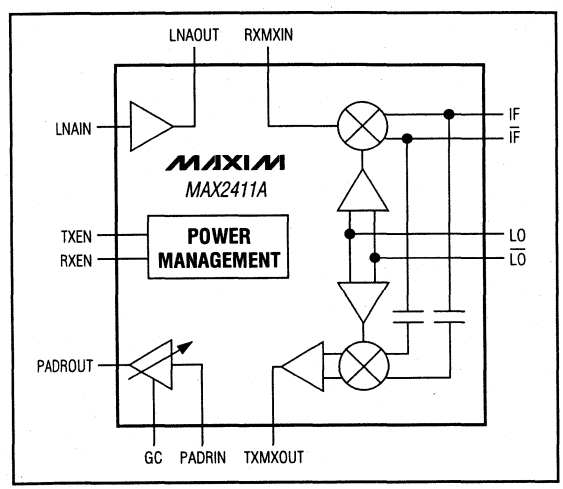
Features

- ♦ **+2.7V to +5.5V Single-Supply Operation**
- ♦ **Integrated Upconvert/Downconvert Function**
- ♦ **3.2dB Combined Receiver Noise Figure (2.5dB LNA, 9dB mixer)**
- ♦ **-12.5dBm Combined Receiver Input IP3 (-9.5dBm LNA, 3dBm mixer)**
- ♦ **3dBm Transmit Compression Power**
- ♦ **20dB Transmit Gain-Control Range**
- ♦ **LO Buffer**
- ♦ **Low Power Consumption:**
  60mW (receive mode)
  90mW (full-power transmit mode)
- ♦ **Low-Power Shutdown Mode**
- ♦ **Advanced System Power Management**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2411AEEI	-40°C to +85°C	28 QSOP

Block Diagram



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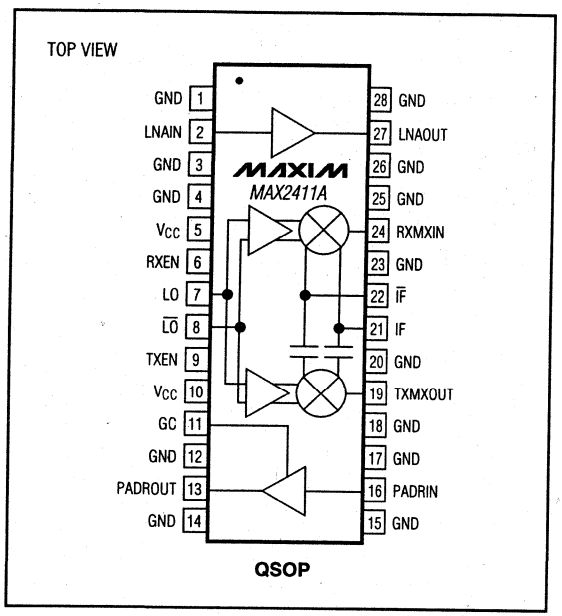
For small orders, phone 408-737-7600 ext. 3468.

Low-Cost RF Up/Downconverter with Low-Noise Amplifier and Power-Amplifier Driver

Pin Configuration



ADVANCE INFORMATION
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8/97

MAXIM

900MHz Image-Reject Transceivers

General Description

The MAX2420/MAX2421/MAX2422/MAX2460/MAX2463 are highly integrated front-end ICs that provide the lowest-cost solutions for cordless and ISM-band radios operating in the 900MHz band. All devices incorporate transmit and receive image-reject mixers to reduce filter cost. They operate from a +2.7V to +4.8V single supply, allowing direct connection to a 3-cell battery stack.

The receive path incorporates an adjustable-gain LNA and an image-reject downconverter with 35dB image suppression. These features yield excellent combined downconverter noise figure (4dB) and high linearity with an input third-order intercept point (IIP3) of up to 2dBm.

The transmitter consists of a variable-gain IF amplifier with more than 35dB control range, an image-reject upconverter with 35dB image rejection, and a power amplifier (PA) predriver that produces up to 2dBm (in some applications serving as the final power stage).

These devices include an on-chip local oscillator (LO), requiring only an external varactor-tuned LC tank for operation. The MAX2420/MAX2421/MAX2422 are optimized for IF frequencies of 10.7MHz, 46MHz, and 70MHz, respectively, and these parts use high-side LO injection ($f_{LO} > f_{RF}$). The MAX2460/MAX2463 are optimized for IF frequencies of 10.7MHz and 110MHz, respectively, with low-side LO injection ($f_{LO} < f_{RF}$).

The integrated divide-by-64/65 dual-modulus prescaler can also be set to a direct mode in which it acts as an LO buffer amplifier. Four separate power-down inputs can be used for advanced system power management, including a 0.5µA shutdown mode. These parts are compatible with commonly used modulation schemes such as FSK, BPSK, and QPSK, as well as frequency-hopping and direct-sequence spread-spectrum systems. For applications requiring direct BPSK modulation as well as receive image rejection, please consult the MAX2426 data sheet. The MAX2420/MAX2421/MAX2422/MAX2460/MAX2463 come in 28-pin SSOP packages.

Applications

Cordless Phones

Wireless Telemetry

Wireless Networks

Spread-Spectrum Communications

Two-Way Paging

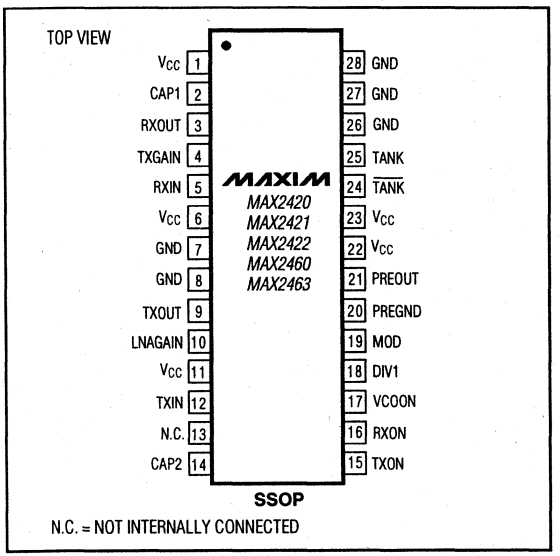
Features

- **Receive/Transmit Mixers with 35dB Image Suppression**
- **Adjustable-Gain LNA**
- **Up to +2dBm Combined Receiver Input IP3**
- **4dB Combined Receive Noise Figure**
- **> 35dB of Transmit Power Control Range**
- **Up to 2dBm PA Predriver**
- **Low Current Consumption: 23mA Receive**
  26mA Transmit
  9.5mA Oscillator
- **0.5µA Shutdown Mode**
- **Operate from a Single +2.7V to +4.8V Supply**

Ordering Information

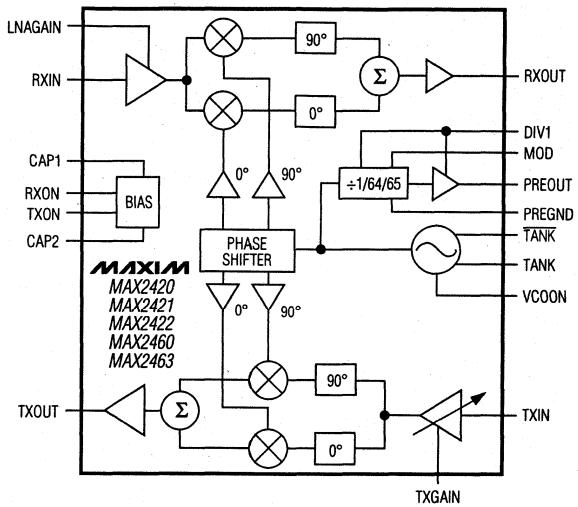
PART	TEMP. RANGE	PIN-PACKAGE
MAX2420EAI	-40°C to +85°C	28 SSOP
MAX2421EAI	-40°C to +85°C	28 SSOP
MAX2422EAI	-40°C to +85°C	28 SSOP
MAX2460EAI	-40°C to +85°C	28 SSOP
MAX2463EAI	-40°C to +85°C	28 SSOP

Pin Configuration



For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800
For small orders, phone 408-737-7600 ext. 3468.

Functional Diagram



*THE MAX2460/MAX2463 USE SWAPPED LO PHASE-SHIFTER CONNECTIONS, RESULTING IN LOW-SIDE INJECTION ($f_{RF} > f_{LO}$)

MAXIM

900MHz Image-Reject Receiver with Transmit Mixer

General Description

The MAX2426 is a highly integrated front-end IC that provides the lowest-cost solution for cordless and ISM-band radios operating in the 900MHz band. It incorporates a receive image-reject mixer (to reduce filter cost) and a versatile transmit mixer. The device operates from a +2.7V to +4.8V single supply, allowing direct connection to a 3-cell battery stack.

The receive path incorporates an adjustable-gain LNA and an image-reject downconverter with 35dB image suppression. These features yield excellent combined downconverter noise figure (4dB) and high linearity with an input third-order intercept point (IIP3) of up to 2dBm.

The transmitter consists of a balanced mixer and a power amplifier (PA) predriver that outputs 2dBm. It can be used in a variety of configurations, including BPSK modulation, direct VCO modulation, and transmitter upconversion. For devices featuring transmit as well as receive image rejection, refer to the MAX2420/MAX2421/MAX2422/MAX2460 data sheet.

The MAX2426 includes an on-chip local oscillator (LO), requiring only an external varactor-tuned LC tank for operation. The MAX2426 is optimized for a receive IF frequency of 70MHz and uses high-side LO injection ($f_{LO} > f_{RF}$). The integrated divide-by-64/65 dual-modulus prescaler can also be set to a direct mode in which it acts as an LO buffer amplifier.

Four separate power-down inputs can be used for advanced system power management, including a 0.5µA shutdown mode.

This device is compatible with commonly used modulation schemes such as FSK, BPSK, and QPSK, as well as frequency-hopping and direct-sequence spread-spectrum systems. The MAX2426 comes in a 28-pin SSOP package.

Applications

Cordless Phones

Wireless Telemetry

Wireless Networks

Spread Spectrum Communications

Two-Way Paging

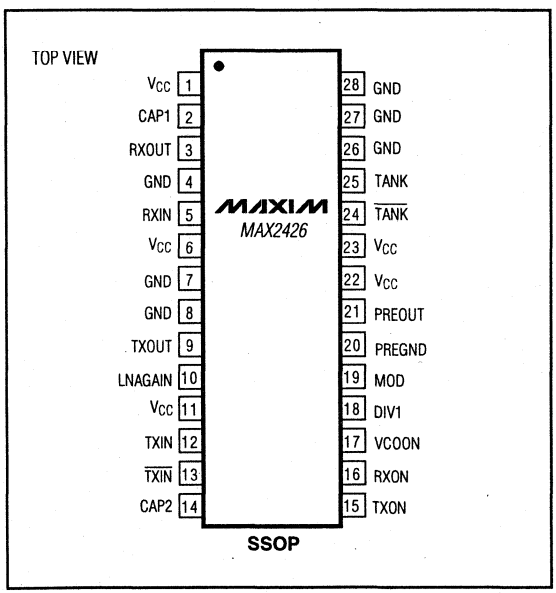
Features

- ♦ **35dB Receive Image Rejection**
- ♦ **Adjustable-Gain LNA**
- ♦ **Up to 2dBm Combined Receiver Input IP3**
- ♦ **4dB Combined Receive Noise Figure**
- ♦ **PA Predriver Provides up to 2dBm**
- ♦ **Low Current Consumption: 23mA Receive**
  15mA Transmit
  9.5mA Oscillator
- ♦ **0.5µA Shutdown Mode**
- ♦ **Operates from Single +2.7V to +4.8V Supply**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2426EAI	-40°C to +85°C	28 SSOP

Pin Configuration



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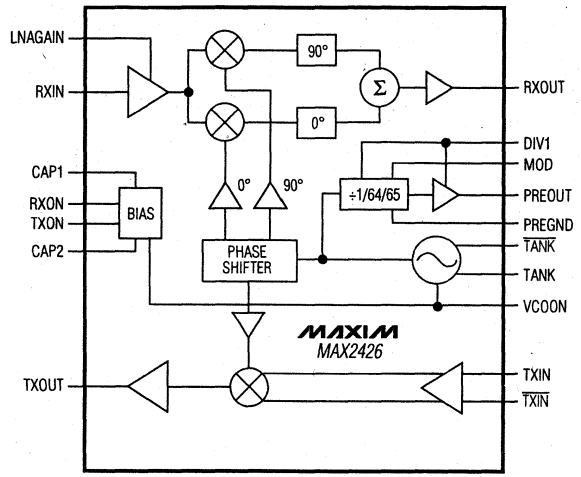
900MHz Image-Reject Receiver with Transmit Mixer

Functional Diagram



ADVANCE INFORMATION
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8/97

MAXIM

Low-Power IF Transceiver with Limiter/RSSI and Quadrature Modulator

General Description

The MAX2510 is a highly integrated IF transceiver for digital wireless applications employing a dual-conversion architecture. Alternatively, the MAX2510 can be used as a single-conversion transceiver if the RF operating frequency ranges from 200MHz to 500MHz.

In a typical application, the receiver downconverts a high IF/RF (typically 200MHz to 500MHz) to a low IF using a double-balanced downconverter. Additional functions included in the receiver section are an IF buffer that can drive an off-chip IF filter, an on-chip limiting amplifier offering 90dB of received-signal-strength indication (RSSI), and a robust limiter output driver. The transmitter section upconverts in-phase and quadrature baseband signals to an IF in the 200MHz to 500MHz range using a quadrature modulator. The transmit output is easily matched to drive a SAW filter with an adjustable output from 0dBm to -40dB with excellent linearity. To extend battery life, the amplifier's unique biasing scheme adjusts current draw to the minimum necessary for sustaining the desired level of output power.

The MAX2510 operates from a +2.7V to +5.5V supply voltage and features four operating modes for advanced system power management. Supply current is reduced to 0.5µA in shutdown mode.

The MAX2511 has features similar to those of the MAX2510, but upconverts a 10.7MHz IF with an image-reject mixer. The MAX2511 downconverter also offers image rejection with a limiter/RSSI stage similar to that of the MAX2510.

Applications

PWT1900 Wireless Handsets and Base Stations

PACS, PHS, DECT (and other PCS, Wireless Handsets, and Base Stations)

400MHz ISM Transceivers

IF Transceivers

Wireless Data Links

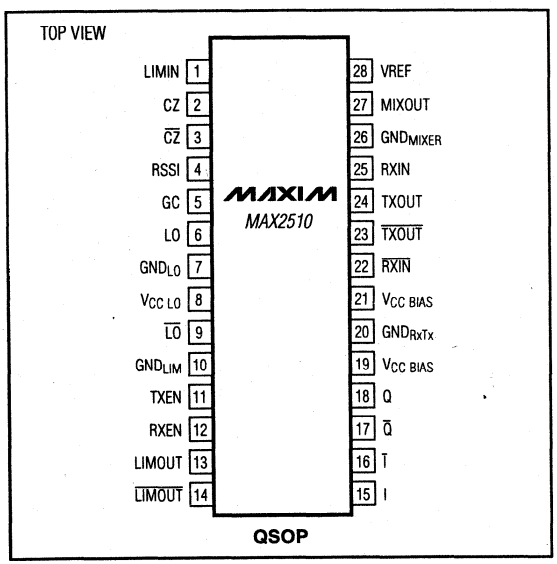
Features

- ♦ **+2.7V to +5.5V Single Supply**
- ♦ **Complete Receive Path:**
  200MHz to 500MHz 1st IF to a
  5MHz to 30MHz 2nd IF
- ♦ **Unique, Wide-Dynamic-Range Downconverter Mixer Offers -9dBm IIP3, 10.5dB NF**
- ♦ **RSSI Function with 90dB Monotonic Dynamic Range**
- ♦ **Limiter with Differential Outputs**
- ♦ **Up to 200MHz to 500MHz Transmit Quadrature Modulator**
- ♦ **40dB Sideband Suppression**
- ♦ **40dB Transmit Gain-Control Range; Up to 1dBm Output Power**
- ♦ **Advanced System Power Management (four modes)**
- ♦ **0.5µA Shutdown Supply Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2510EEI	-40°C to +85°C	28 QSOP

Pin Configuration



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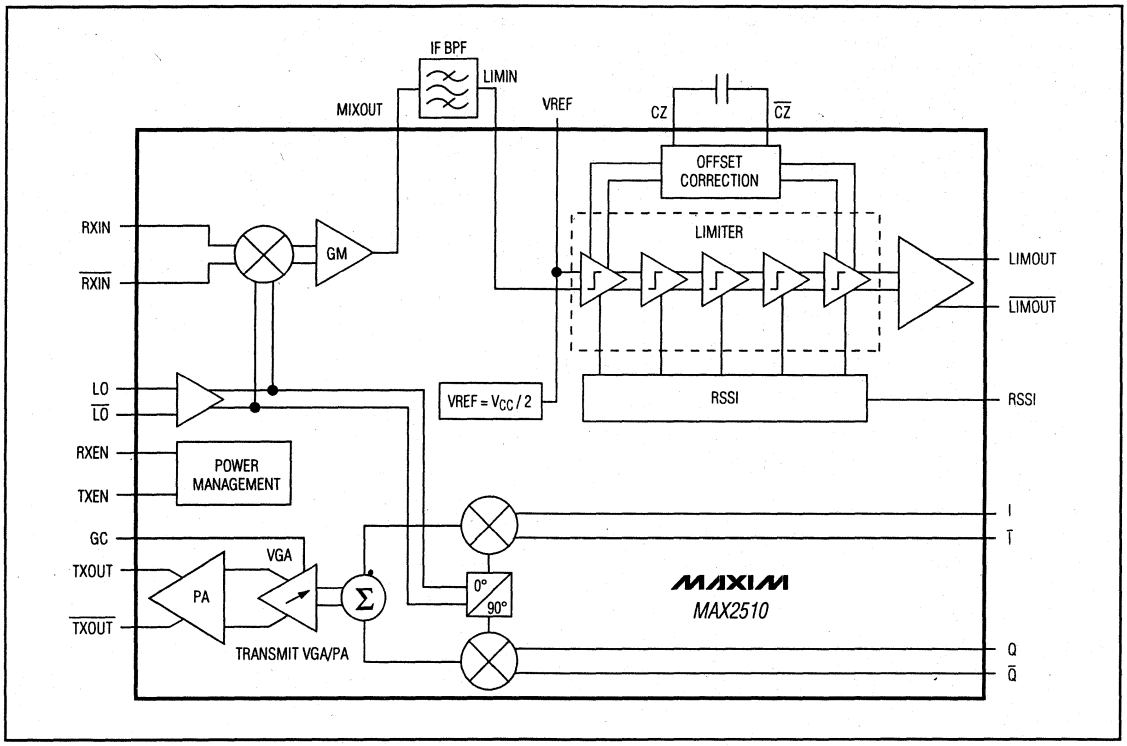
Low-Power IF Transceiver with Limiter/RSSI and Quadrature Modulator

Typical Application Circuit



19-1209; Rev 0; 10/97

EVALUATION KIT AVAILABLE

MAXIM

Low-Voltage IF Transceiver with Limiter and RSSI

General Description

The MAX2511 is a complete, highly integrated IF transceiver for applications employing a dual-conversion architecture. Alternatively, the MAX2511 can be used as a single-conversion transceiver if the RF operating frequency ranges from 200MHz to 440MHz.

In a typical application, the receiver downconverts a high IF/RF (200MHz to 440MHz) to a 10.7MHz low IF using an image-reject mixer. Functions include an image-reject downconverter with 34dB of image suppression followed by an IF buffer that can drive an off-chip IF filter; an on-chip limiting amplifier offering 90dB of monotonic received-signal-strength indication (RSSI); and a robust limiter output driver. The transmit image-reject mixer generates a clean output spectrum to minimize filter requirements. It is followed by a 40dB variable-gain amplifier that maintains IM3 levels below -35dBc. Maximum output power is 2dBm. A VCO and oscillator buffer for driving an external prescaler are also included.

The MAX2511 operates from a 2.7V to 5.5V supply and includes flexible power-management control. Supply current is reduced to 0.1µA in shutdown mode.

For applications using in-phase (I) and quadrature (Q) baseband architecture for the transmitter, Maxim offers a corresponding transceiver product: the MAX2510. The MAX2510 has features similar to those of the MAX2511, but upconverts I/Q baseband signals using a quadrature upconverter.

Applications

PWT1900 Wireless Handsets and Base Stations

PACS, PHS, DECT and Other PCS Wireless Handsets and Base Stations

400MHz ISM Transceivers

IF Transceivers

Wireless Data Links

Typical Operating Circuit appears at end of data sheet.

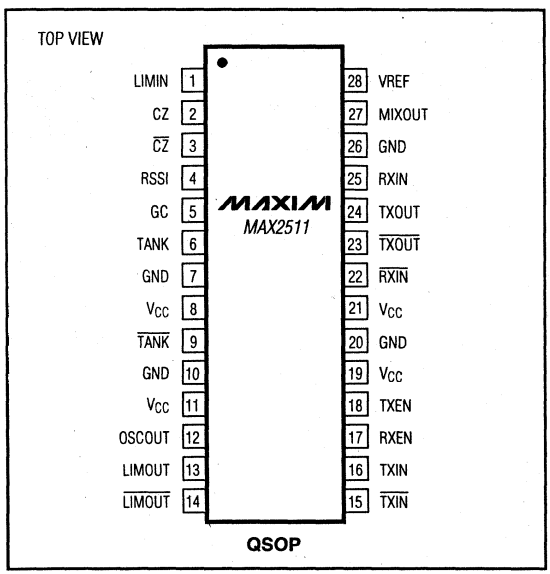
Features

- **Single +2.7V to +5.5V Supply**
- **Complete Receive Path:**
  200MHz to 440MHz (first IF) to
  8MHz to 13MHz (second IF)
- **Limiter with Differential Outputs (adjustable level)**
- **RSSI Function with 90dB Monotonic Dynamic Range**
- **Complete Transmit Path:**
  8MHz to 13MHz (second IF) to
  200MHz to 440MHz (first IF)
- **On-Chip Oscillator with Voltage Regulator and Buffer**
- **Advanced System Power Management (four modes)**
- **0.1µA Shutdown Supply Current**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2511EEI	-40°C to +85°C	28 QSOP

Pin Configuration



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Low-Voltage IF Transceiver with Limiter and RSSI

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to 8.0V
V_{CC} to Any Other V_{CC} .....±0.3V
TXIN, $\overline{TXIN}$ Input Voltage.....-0.3V to (V_{CC} + 0.3V)
TXIN to $\overline{TXIN}$ Differential Voltage .....±300mV
RXIN, $\overline{RXIN}$ Input Voltage .....-0.3V to 1.6V
TANK, $\overline{TANK}$ Voltage.....-0.3V to 2.0V
LIMIN Voltage .....(VREF - 1.3V) to (VREF + 1.3V)
LIMOUT, $\overline{LIMOUT}$ Voltage .....(V_{CC} - 1.6V) to (V_{CC} + 0.3V)
RXEN, TXEN, GC Voltage.....-0.3V to (V_{CC} + 0.3V)
RXEN, TXEN, GC Input Current 1mA
RSSI Voltage.....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
QSOP (derate 11mW/°C above 70°C) 909mW
Operating Temperature Range
MAX2511EEI.....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +5.5V, 0.01µF across CZ and $\overline{CZ}$; TANK = $\overline{TANK}$; MIXOUT tied to VREF through a 165Ω resistor; GC open, RXIN = $\overline{RXIN}$; TXOUT = $\overline{TXOUT}$ = V_{CC}; T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range			2.7	3.0	5.5	V
Digital Input Voltage High	RXEN, TXEN		2.0			V
Digital Input Voltage Low	RXEN, TXEN				0.4	V
Digital Input Current High				23	32	µA
Digital Input Current Low			-5	-1		µA
Typical Supply Current	V_{CC} = 3.0V, T_A = +25°C	Rx mode, RXEN = high, TXEN = low		24		mA
		Tx mode, RXEN = low, TXEN = high, V_{GC} = 0.5V		26		
		Standby mode, RXEN = high, TXEN = high		9.5		
		Shutdown mode, RXEN = low, TXEN = low		0.1		µA
Worst-Case Supply Current	V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C	Rx mode, RXEN = high, TXEN = low			38.5	mA
		Tx mode, RXEN = low, TXEN = high, V_{GC} = 0.5V			45	
		Standby mode, RXEN = high, TXEN = high			14.5	
		Shutdown mode, RXEN = low, TXEN = low			5	µA
VREF Voltage	(Note 1)		V_{CC} / 2 - 100mV	V_{CC} / 2	V_{CC} / 2 + 100mV	V
LIMOUT, $\overline{LIMOUT}$ Differential Output Impedance				2		kΩ
GC Input Resistance	Internally terminated to 1.35V		60	80	125	kΩ

AC ELECTRICAL CHARACTERISTICS

(MAX2511 test fixture, V_{CC} = +3.0V, RXEN = TXEN = low, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 330pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, $P_{RXIN, \overline{RXIN}}$ = -28dBm (200Ω system), $f_{RXIN, \overline{RXIN}}$ = 425MHz, f_{LO} = 435.7MHz, $f_{TXIN, \overline{TXIN}}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DOWNCONVERTER (RXEN = high)					
Downconverter Mixer Voltage Gain	T_A = +25°C	21.5	23.6	25.5	dB
	T_A = -40°C to +85°C (Note 1)	20		27	
Downconverter Mixer Noise Figure			14		dB
Downconverter Mixer Input 1dB Compression Level	(Note 2)		-16		dBm
Input Third-Order Intercept	Two tones at 424MHz and 425MHz, -30dBm per tone		-11		dBm
Image Rejection	$f_{IMAGE} = f_{LO} + f_{IF}$ = 446.4MHz	25	34		dB
MIXOUT Maximum Voltage Swing			2		Vp-p
Power-Up Time	Standby to RX or TX (Note 3)			5	µs
LIMITING AMPLIFIER AND RSSI (RXEN = high)					
Limiter Output Level	V_{GC} = 0.8V (Note 4)		120	160	mVp-p
	V_{GC} = open	475		625	
	V_{GC} = 2.0V (P_{LIMIN} = +5dBm)	950	1100		
Phase Variation	-75dBm to 5dBm from 50Ω		3.6		degrees
Minimum Linear RSSI Range	-75dBm to 5dBm from 50Ω		80		dB
Minimum Monotonic RSSI Range	-80dBm to 10dBm from 50Ω		90		dB
RSSI Slope	-75dBm to 5dBm from 50Ω		10.6		mV/dB
RSSI Maximum Intercept	(Note 5)		-82	-75	dBm
RSSI Relative Error	T_A = +25°C		±1	±2	dB
	T_A = -40°C to +85°C (Note 1)			±2.5	
RSSI Rise Time	Rise time to within 1dB accuracy; using a 100pF capacitor from RSSI to GND		6.4		µs
Minimum-Scale RSSI Voltage	At LIMIN input of -75dBm	50	90	135	mV
Maximum-Scale RSSI Voltage	At LIMIN input of 5dBm	850	940	1025	mV
OSCILLATOR (TXEN = RXEN = high)					
Frequency Range	(Note 7)	200		440	MHz
Phase Noise	At 10kHz offset		-88		dBc/Hz
Maximum LO Frequency Pulling	Standby mode to TX or RX mode		±36		kHz
LO Leakage	At RXIN port		-65		dBm
Oscillator Buffer Output Power	T_A = +25°C (Note 8)	-12	-9		dBm
	T_A = -40°C to +85°C (Notes 1 and 8)	-13			
Maximum Power-Up Time	Shutdown to standby mode (Note 9)		220		µs

Low-Voltage IF Transceiver with Limiter and RSSI

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2511 test fixture, V_{CC} = +3.0V, RXEN = TXEN = low, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 330pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, $P_{RXIN, \overline{RXIN}}$ = -28dBm (200Ω system), $f_{RXIN, \overline{RXIN}}$ = 425MHz, f_{LO} = 435.7MHz, $f_{TXIN, \overline{TXIN}}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (TXEN = high, V_{TXIN} and $V_{\overline{TXIN}}$ = 100mVp-p differential)					
Output Power	V_{GC} = 0.5V, T_A = +25°C		-44		dBm
	V_{GC} = open, T_A = +25°C		-19		
	V_{GC} = 2.0V, T_A = +25°C	-5	-2		
	V_{GC} = 2.0V, T_A = -40°C to +85°C (Note 1)	-6			
Image Rejection			34	25	dBc
LO Rejection			40	30	dBc
Output 1dB Compression Point	V_{GC} = 2.0V		2		dBm
Output IM3 Level	0.5V < V_{GC} < 1.87V -40dBm < P_{OUT} < -10dBm (Note 10)		-40		dBc
	V_{GC} = 2.0V		-35		

Note 1: Guaranteed by design and characterization.

Note 2: Driving RXIN or $\overline{RXIN}$ with a power level greater than the 1dB compression level forces the input stage out of its linear range, causing harmonic and intermodulation distortion. The RSSI output increases monotonically with increasing input levels beyond the mixer's 1dB compression level.

Note 3: Assuming the supply voltage has been applied, this includes settling of the limiter offset correction and the Rx or Tx bias stabilization time. Guaranteed by design.

Note 4: LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential. With no load, the output swing is approximately twice as large.

Note 5: The RSSI maximum intercept is the maximum input power (over a statistical sample of parts) at which the RSSI output is 0V. This point is extrapolated from the linear portion of the RSSI voltage versus limiter input power. This specification and the RSSI slope define the ideal behavior of the RSSI function (the slope and intercept of a straight line), while the RSSI relative error specification defines the deviations from this line. See the RSSI Output Voltage vs. Limiter Input Power graph in the *Typical Operating Characteristics*.

Note 6: The RSSI relative error is the deviation from the best-fitting straight line of RSSI output voltage versus limiter input power. A 0dB relative error is exactly on this line. The limiter input power range for this test is -75dBm to +5dBm from 50Ω. See the RSSI Relative Error graph in the *Typical Operating Characteristics* .

Note 7: Operation outside this frequency range is possible but has not been characterized. At lower frequencies, it might be necessary to overdrive the oscillator with an external signal source.

Note 8: If a larger output level is required, a higher value of load resistance (up to 100Ω) may be used.

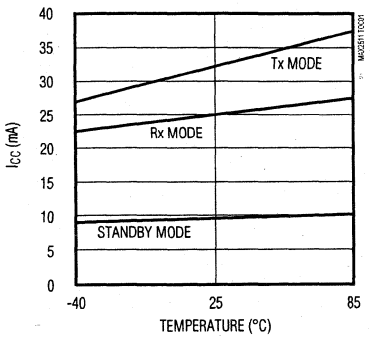
Note 9: This assumes that the supply voltage has been applied, and includes the settling time of V_{REF}, using the *Typical Operating Circuit*.

Note 10: Using two tones at 10.7MHz and 10.8MHz, 50mVp-p per tone at TXIN, $\overline{TXIN}$. See *Typical Operating Characteristics*.

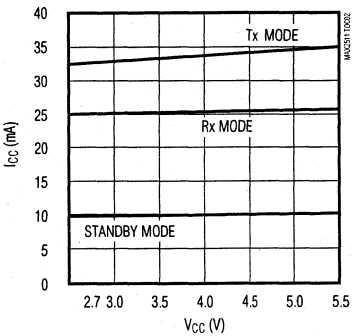
Typical Operating Characteristics

(MAX2511 test fixture, V_{CC} = +3.0V, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 100pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, P_{RXIN}, $\overline{RXIN}$ = -28dBm (200Ω system), f_{RXIN}, $\overline{RXIN}$ = 425MHz, f_{LO} = 435.7MHz, f_{TXIN}, $\overline{TXIN}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

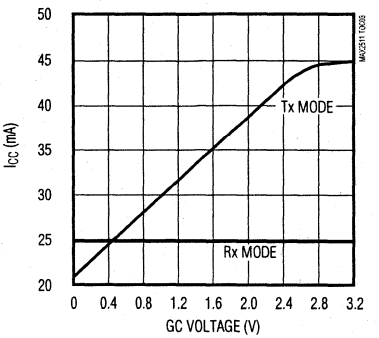
SUPPLY CURRENT vs. TEMPERATURE



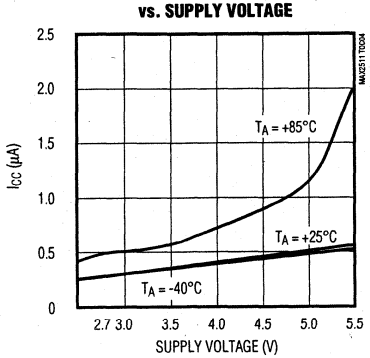
SUPPLY CURRENT vs. SUPPLY VOLTAGE



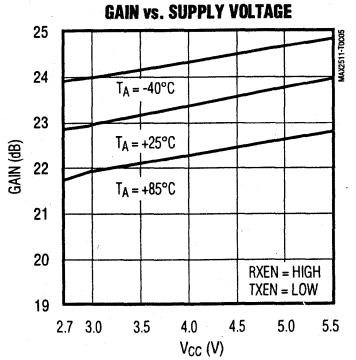
SUPPLY CURRENT vs. GC VOLTAGE



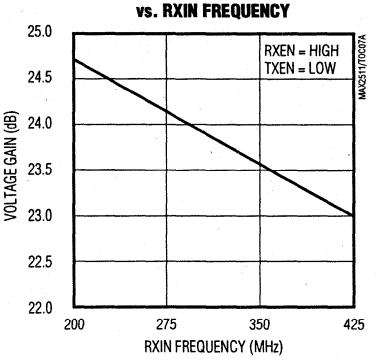
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



DOWNCONVERTER MIXER CONVERSION GAIN vs. SUPPLY VOLTAGE



DOWNCONVERTER GAIN vs. RXIN FREQUENCY



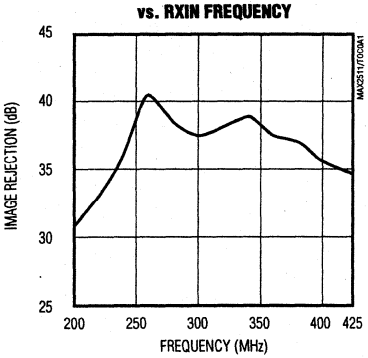
10

Low-Voltage IF Transceiver with Limiter and RSSI

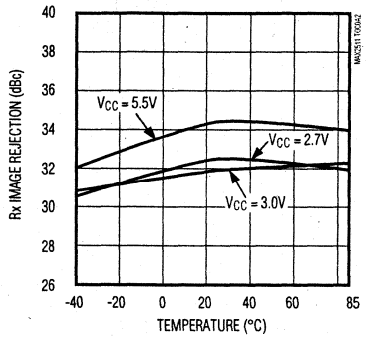
Typical Operating Characteristics (continued)

(MAX2511 test fixture, V_{CC} = +3.0V, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 100pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, $P_{RXIN, \overline{RXIN}}$ = -28dBm (200Ω system), $f_{RXIN, \overline{RXIN}}$ = 425MHz, f_{LO} = 435.7MHz, $f_{TXIN, \overline{TXIN}}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

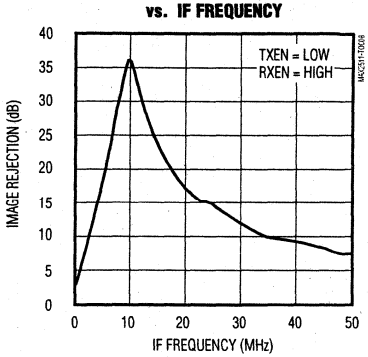
DOWNCONVERTER IMAGE REJECTION vs. RXIN FREQUENCY



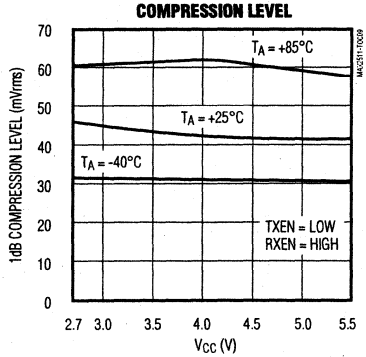
DOWNCONVERTER-MIXER IMAGE REJECTION vs. TEMPERATURE AND SUPPLY VOLTAGE



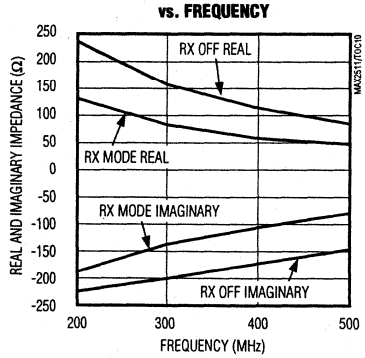
DOWNCONVERTER IMAGE REJECTION vs. IF FREQUENCY



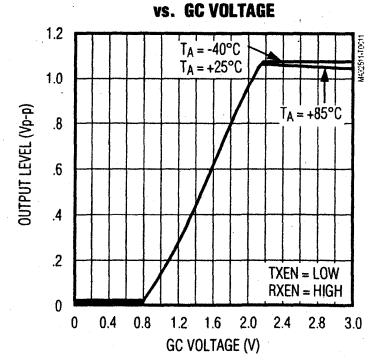
DOWNCONVERTER INPUT 1dB COMPRESSION LEVEL



RXIN DIFFERENTIAL INPUT IMPEDANCE vs. FREQUENCY



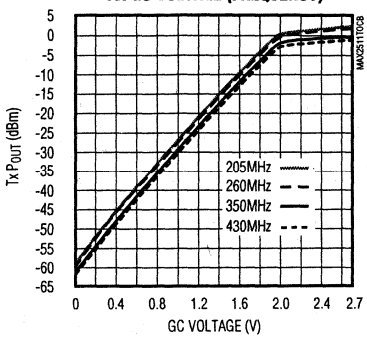
LIMITER OUTPUT LEVEL vs. GC VOLTAGE



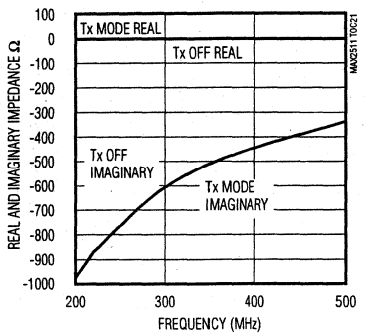
Typical Operating Characteristics (continued)

(MAX2511 test fixture, V_{CC} = +3.0V, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 100pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, $P_{RXIN, \overline{RXIN}}$ = -28dBm (200Ω system), $f_{RXIN, \overline{RXIN}}$ = 425MHz, f_{LO} = 435.7MHz, $f_{TXIN, \overline{TXIN}}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

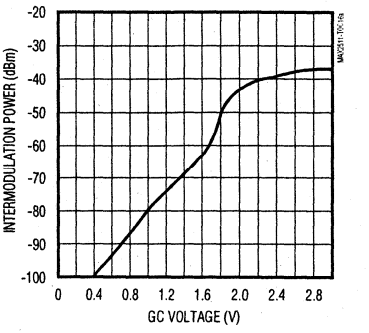
TRANSMITTER OUTPUT POWER vs. GC VOLTAGE (FREQUENCY)



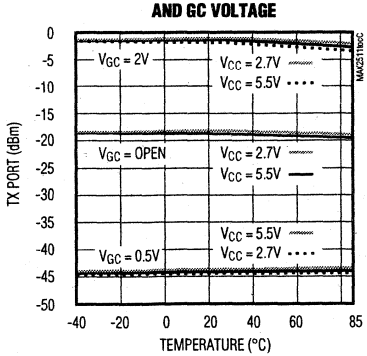
TRANSMITTER DIFFERENTIAL OUTPUT IMPEDANCE vs. FREQUENCY



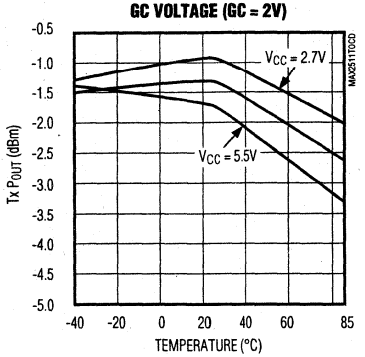
UPCONVERTER IM3 LEVELS vs. GC VOLTAGE (POWERS ARE PER TONE)



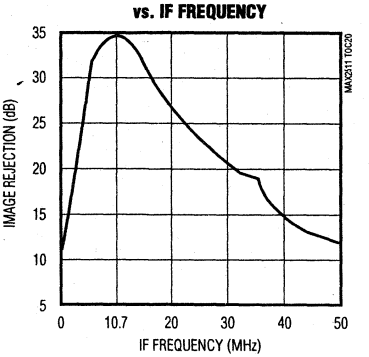
TRANSMITTER OUTPUT POWER vs. TEMPERATURE, SUPPLY, AND GC VOLTAGE



TRANSMITTER OUTPUT POWER vs. TEMPERATURE AND SUPPLY GC VOLTAGE (GC = 2V)



UPCONVERTER IMAGE REJECTION vs. IF FREQUENCY

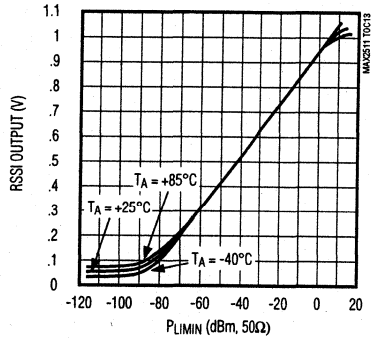


Low-Voltage IF Transceiver with Limiter and RSSI

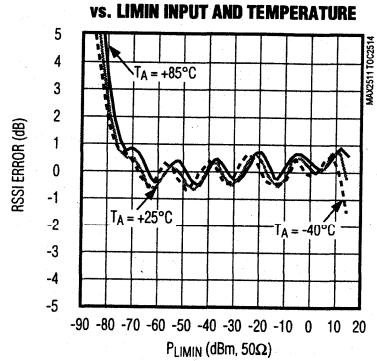
Typical Operating Characteristics (continued)

(MAX2511 test fixture, V_{CC} = +3.0V, 0.01µF across CZ and $\overline{CZ}$, MIXOUT tied to VREF through 165Ω resistor, TXIN, $\overline{TXIN}$ tied to VREF through 50Ω resistor, TXOUT and $\overline{TXOUT}$ loaded with 100Ω differential, GC open, LIMOUT, $\overline{LIMOUT}$ loaded with 2kΩ differential, TANK and $\overline{TANK}$ driven with -2.5dBm from a 100Ω source; OSCOUT AC-terminated with 50Ω, 100pF at RSSI pin, 0.1µF at VREF pin, Rx inputs and Tx outputs differentially coupled, $P_{RXIN, \overline{RXIN}}$ = -28dBm (200Ω system), $f_{RXIN, \overline{RXIN}}$ = 425MHz, f_{LO} = 435.7MHz, $f_{TXIN, \overline{TXIN}}$ = 10.7MHz, T_A = +25°C, unless otherwise noted.)

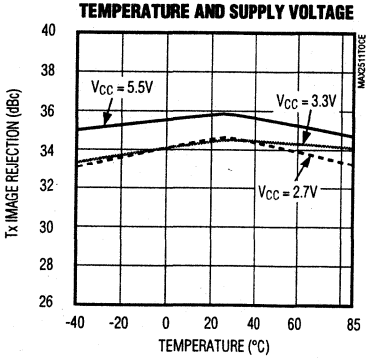
RSSI OUTPUT VOLTAGE vs. LIMIN INPUT POWER AND TEMPERATURE



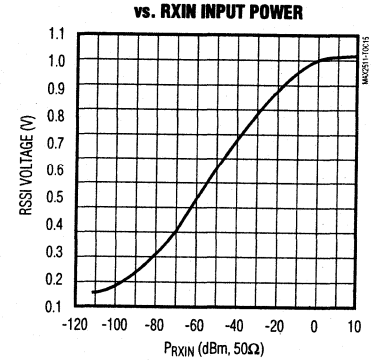
RSSI RELATIVE ERROR vs. LIMIN INPUT AND TEMPERATURE



TRANSMITTER IMAGE REJECTION vs. TEMPERATURE AND SUPPLY VOLTAGE



MIXER INPUT-REFERRED RSSI VOLTAGE vs. RXIN INPUT POWER



Pin Description

PIN	NAME	FUNCTION
1	LIMIN	Limiter Input. Connect a 330Ω (typ) resistor to VREF for DC bias, as shown in the *Typical Operating Circuit.*
2, 3	CZ, $\overline{CZ}$	Offset-Correction Capacitor pins. Connect a 0.01µF capacitor between CZ and $\overline{CZ}$.
4	RSSI	Receive-Signal-Strength-Indicator Output. The voltage on RSSI is proportional to the signal power at LIMIN. The RSSI output sources current pulses into an external capacitor (100pF typ). The output is internally terminated with 6kΩ, and this RC time constant sets the decay time.
5	GC	Gain-Control pin in transmit mode. Applying a DC voltage to GC between 0V and 2.0V adjusts the transmitter gain by 40dB. In receive mode, GC adjusts the limiter output level from 0Vp-p to about 1Vp-p. This pin's input impedance is typically 80kΩ terminated to 1.35V.
6, 9	TANK, $\overline{TANK}$	Tank pins. Connect the resonant tank across these pins, as shown in the *Typical Operating Circuit.*
7, 10	GND	Ground. Connect GND to the PC board ground plane with minimal inductance.
8, 11	V_{CC}	Supply Voltage. Bypass V_{CC} directly to GND. See the *Layout Issues* section.
12	OSCOUT	Oscillator-Buffer Output. OSCOUT provides a buffered oscillator signal (at the oscillator frequency) for driving an external prescaler. This pin is a current output and must be AC-coupled to a resistive load. The output power is typically -9dBm into a 50Ω load. If a larger output swing is required, a larger load resistance (up to 100Ω) can be used.
13, 14	LIMOUT, $\overline{LIMOUT}$	Differential Outputs of the Limiting Amplifier. LIMOUT and $\overline{LIMOUT}$ are open-collector outputs that are internally pulled up to V_{CC} through 1kΩ resistors.
15, 16	$\overline{TXIN}$, TXIN	Differential Inputs of the Image-Reject Upconverter Mixer. $\overline{TXIN}$ and TXIN are high impedance and must be pulled up to V_{CC} through two external resistors whose value is equal to the desired terminating impedance (50Ω to 50kΩ).
17	RXEN	Receiver-Enable pin. When high, RXEN enables the receiver if TXEN is low. If both RXEN and TXEN are high, the part is in standby mode; if both are low, the part is in shutdown. See the *Power Management* section for more details.
18	TXEN	Transmitter-Enable pin. When high, TXEN enables the transmitter, if RXEN is low. If both TXEN and RXEN are high, the part is in standby mode; if both are low, the part is in shutdown. See the *Power Management* section for more details.
19, 21	V_{CC}	Bias V_{CC} Supply pins. Decouple these pins to GND. See the *Layout Issues* section.
20	GND	Receiver/Transmitter Ground pin. Connect to the PC board ground plane with minimal inductance.
22, 25	$\overline{RXIN}$, RXIN	Differential Inputs of the Image-Reject Downconverter Mixer. In most applications, an impedance matching network is required. See the *Applications Information* section for more details.
23, 24	$\overline{TXOUT}$, TXOUT	Differential Outputs of the Image-Reject Upconverter. $\overline{TXOUT}$ and TXOUT must be pulled up to V_{CC} with two external inductors and AC coupled to the load.
26	GND	Receiver Front-End Ground. Connect GND to the PC board ground plane with minimal inductance.
27	MIXOUT	Single-Ended Output of the Image-Reject Downconverter. MIXOUT is high impedance and must be biased to the VREF pin through an external terminating resistor whose value depends on the interstage filter characteristics. See the *Applications Information* section for more details.
28	VREF	Reference Voltage pin. VREF is used to provide an external bias voltage for the MIXOUT and LIMIN pins. Bypass this pin with a 0.1µF capacitor to ground. VREF voltage is equal to V_{CC} / 2. See the *Typical Operating Circuit* for more information.

Low-Voltage IF Transceiver with Limiter and RSSI

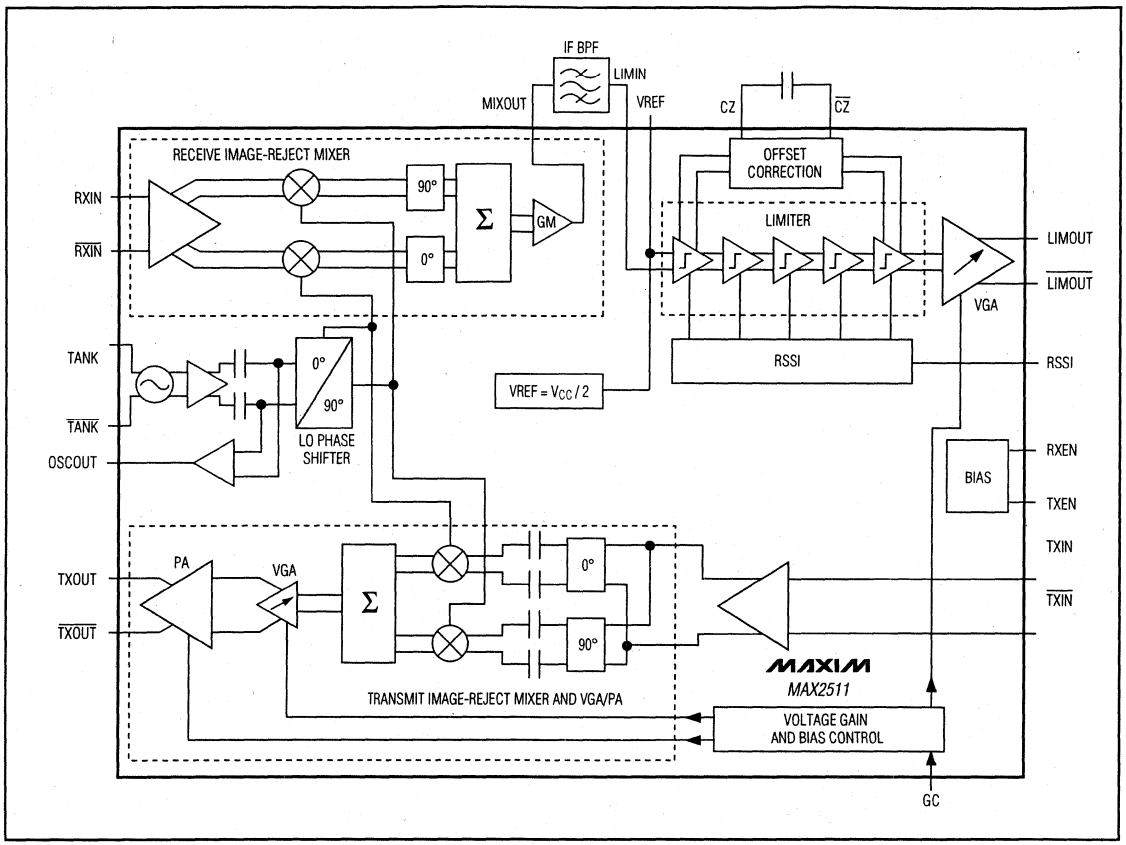


Figure 1. Functional Diagram

Detailed Description

The following sections describe each of the blocks shown in Figure 1.

Receiver

The receiver consists of two basic blocks: the image-reject downconverter mixer and the limiter/RSSI section.

The receiver inputs are the RXIN, $\overline{RXIN}$ pins, which should be AC coupled and may require a matching network, as shown in the *Typical Operating Circuit.* To design a matching network for a particular application, refer to the *Applications Information* section and the receiver input impedance plots in the *Typical Operating Characteristics.*

Image-Reject Mixer

The downconverter is implemented using an image-reject mixer consisting of an input buffer with dual outputs, each of which is fed to a double-balanced mixer. The LO signal is generated by an on-chip oscillator and an external tank circuit. The buffered oscillator signal drives a quadrature phase generator that provides two outputs with 90° of phase shift between them. This pair of LO signals is fed to the two receive mixers. The mixer's outputs are then passed through a pair of phase shifters, which provide 90° of phase shift across their outputs. The resulting two signals are then summed together. The final phase relationship is such that the desired signal is reinforced, and the image signal is largely canceled. The downconverter mixer's

output is buffered and converted to a single-ended current output at the MIXOUT pin, which can drive a shunt-terminated bandpass filter over a large dynamic range. MIXOUT can drive a shunt-terminated 330Ω filter (165Ω load) to more than 2Vp-p over the entire supply range.

Limiter

The signal passes through an external IF bandpass filter into the limiter input (LIMIN). LIMIN is a single-ended input that is centered around the VREF pin voltage. Open-circuit input impedance is typically greater than 10kΩ terminated to VREF. For proper operation, LIMIN must be tied to VREF through the filter terminating impedance (not more than 1kΩ). The limiter provides a constant output level, which is largely independent of the limiter input-signal level over an 80dB input range.

The adjustable output level allows easy interfacing of the limiter output to the downstream circuitry. The limiter's output drives a variable-gain amplifier that adjusts the limited output level from 0Vp-p to typically 1Vp-p as the GC pin voltage is adjusted from 0.5V to 2.0V. Using this feature allows the downstream circuitry, such as an analog-to-digital converter (ADC), to run at optimum performance by steering the limiter's output level to match the desired ADC input level. GC is also used for transmit (Tx) gain adjustment in Tx mode, so be sure to keep the voltage at an appropriate value for each mode.

Received-Signal-Strength Indicator

The RSSI output provides a linear indication of the received power level on the LIMIN input. The RSSI monotonic dynamic range exceeds 90dB while providing better than 80dB linear range. The RSSI output pulses current into an external filter capacitor (typically 100pF). The output is internally terminated with 6kΩ to GND, and this R-C time constant sets the decay time.

Transmitter

The image-reject upconverter mixer operates in a fashion similar to the downconverter mixer. The transmit mixer consists of an input buffer amplifier that drives on-chip IF phase shifters. The shifted signals are then input to a pair of double-balanced mixers, which are driven with the same quadrature (Q) LO source used by the receiver. The mixer outputs are summed together, largely canceling the image signal component. The image-canceled signal from the mixer outputs is fed through a variable-gain amplifier (VGA) with 40dB of gain-adjust range.

The VGA output is connected to a driver amplifier with an output 1dB compression point of 2dBm. The output power can be adjusted from approximately 2dBm to less than -40dBm by controlling the GC pin. For output levels between -10dBm and -40dBm, -40dBc IM3 levels are maintained. The resulting signal appears as a differential output on TXOUT and $\overline{\text{TXOUT}}$, which expect a 100Ω differential load impedance.

TXOUT and $\overline{\text{TXOUT}}$ are open-collector outputs and need external pull-up inductors to VCC for proper operation. They also need a DC block so the load does not affect DC biasing. A shunt resistor across TXOUT, $\overline{\text{TXOUT}}$ can be used to back-terminate an external filter, as shown in the *Typical Operating Circuit*. It is possible to use the receiver inputs RXIN and $\overline{\text{RXIN}}$ to provide this termination, as described in the *Filter Sharing* section. For single-ended operation, tie the unused input to VCC.

Local Oscillator and Oscillator Buffer

The on-chip LO requires only an external LC tank circuit for operation. The tank circuit is connected across TANK and $\overline{\text{TANK}}$. A dual varactor diode is typically used to adjust the frequency in a phase-locked loop (PLL). See the *Applications Information* section for the tank circuit design equations. Keep the resonator's Q as high

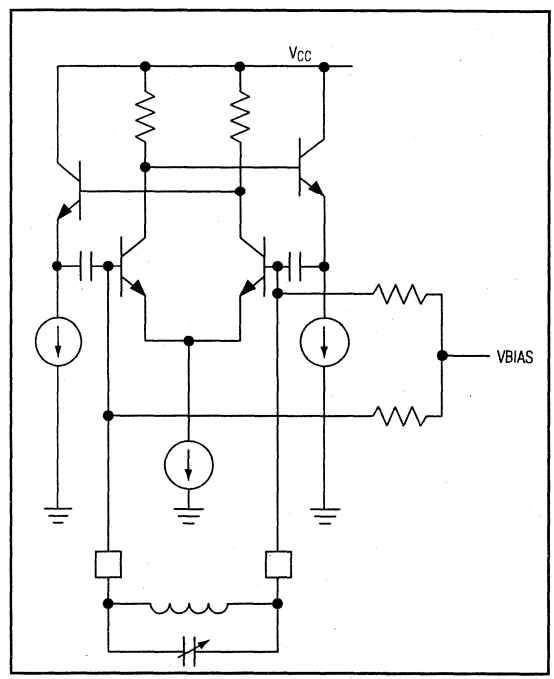


Figure 2. Simplified Oscillator Equivalent Circuit

Low-Voltage IF Transceiver with Limiter and RSSI

as possible for lowest phase noise. The tank's PC board layout is also critical to good performance (consult the *Layout Issues* section for more information).

The OSCOUT pin buffers the internal oscillator signal for driving an external PLL. This output should be AC coupled and terminated at the far end (typically the input to a prescaler) with a 50Ω load. If a larger output level is desired, you can use a resistive termination up to 100Ω. When a controlled-impedance PC board is used, this trace's impedance should match the termination impedance.

Power Management

The MAX2511 features four power-supply modes to preserve battery life. These modes are selected via the RXEN and TXEN pins, according to Table 1.

In shutdown mode, all part functions are off. In standby mode, the LO and the LO buffer are active. This allows a PLL (implemented externally to the MAX2511) to remain up and running, avoiding any delay resulting from PLL loop settling. Transmit (Tx) mode enables the LO circuitry, upconverter mixer, transmit VGA, and output driver amplifier. Receive (Rx) mode enables the LO circuitry, downconverter mixer, limiting amplifier, and adjustable output level amplifier.

Table 1. Power-Supply Mode Selection

RXEN STATE	TXEN STATE	MODE
Low	Low	Shutdown
Low	High	Transmit
High	Low	Receive
High	High	Standby

Applications Information

400MHz ISM Applications

The MAX2511 can be used in applications where the 200MHz to 440MHz signal is an RF (rather than an IF) signal, such as in 400MHz ISM applications. In this case, we recommend preceding the MAX2511 receiver section with a low-noise amplifier (LNA) that can operate over the same supply-voltage range. The MAX2630–MAX2633 family of amplifiers meets this requirement. But since these parts have single-ended inputs and outputs, it is necessary to AC terminate the unused MAX2511 input ($\overline{RXIN}$) to ground with 47nF.

Oscillator Tank

The on-chip oscillator circuit requires a parallel resonant tank circuit connected across TANK and $\overline{TANK}$. Figure 3 shows an example of an oscillator tank circuit. Inductor L1 is resonated with the effective total capacitance of C1 in parallel with the series combination of C2, C3, and (CD1) / 2. CD1 is the capacitance of one of the varactor diodes. Typically, C2 = C3 to maintain symmetry. The effective parasitic capacitance, C_P (including PCB parasitics), is approximately 3.5pF. The total capacitance is given by the following equation:

$$C_{EFF} = \frac{1}{\frac{2}{C2} + \frac{2}{C_{D1}}} + C1 + C_P$$

Using this value for the resonant tank circuit, the oscillation frequency is as follows:

$$F_{OSC} = \frac{1}{2\pi\sqrt{L_1 C_{EFF}}}$$

Starting with the inductor recommended in Table 2, choose the component values according to your application needs, such as phase noise, tuning range, and VCO gain. Keep the tank's Q as high as possible to reduce phase noise. For most of the MAX2511's applications (such as a first IF to second IF transceiver), the oscillator's tuning range can be quite small, since the IF frequencies are not tuned for channel selection. This allows a narrowband oscillator tank to be used, which typically provides better phase noise and stability performance than wideband tank circuits. Careful PC board layout of the oscillator tank is essential. See the *Layout Issues* section for more information.

To overdrive the oscillator from an external 50Ω source, see Figure 4.

Rx Input Impedance Matching

The RXIN, $\overline{RXIN}$ port typically needs an impedance-matching network for proper connection to external circuitry such as a filter. See the *Typical Operating Circuit* for an example circuit topology. A shunt resistor across RXIN, $\overline{RXIN}$ can be used to set terminating impedance, with a slight degradation of the Noise Figure.

The component values used in the matching network depend on the desired operating frequency as well as the filter impedance. Table 3 indicates the RXIN, $\overline{RXIN}$ differential input impedance in both series and parallel form. This data is also plotted in the *Typical Operating Characteristics.*

Filter Sharing

In half-duplex or TDD applications, the number of external filters can be minimized by combining transmit and receive filter paths (Figure 5).

The 10.7MHz filter that is usually connected to the TXIN, $\overline{TXIN}$ ports can be the same filter that is connected at LIMOUT and $\overline{LIMOUT}$. To use the same filter, connect TXIN to LIMOUT, and $\overline{TXIN}$ to $\overline{LIMOUT}$.

The 425MHz SAW filter needed at the RXIN, $\overline{RXIN}$ ports and the filter needed at TXOUT and $\overline{TXOUT}$ can be shared in a similar manner. The RXIN, $\overline{RXIN}$ ports must be DC blocked to prevent the bias voltage needed by the TXOUT and $\overline{TXOUT}$ pins from entering the receiver.

When sharing filters in this manner, the transmitter output port (TXOUT, $\overline{TXOUT}$) and receiver input port (RXIN, $\overline{RXIN}$) matching networks must be modified. The receiver port's input impedance must be the parallel combination of the receiver and transmitter ports in Rx mode. In this case, the receiver port is active, but the transmitter port adds an additional parasitic impedance. See the transmitter and receiver-port impedance graphs in the *Typical Operating Characteristics*.

When the part is in transmit mode, the RXIN and $\overline{RXIN}$ inputs provide back termination for the TXOUT and $\overline{TXOUT}$ outputs so that a single IF filter can be connected (Figure 5). With this technique, the matching network can be adjusted so the input VSWR is less than 1.5:1 in Rx mode, and the output VSWR is less than 2:1 in Tx mode.

Receive IF Filter

The interstage 10.7MHz filter, located between the MIXOUT pin and the LIMIN pin, is not shared. This filter prevents the limiter from acting on any undesired signals that are present at the mixer's output, such as LO feedthrough, out-of-band channel leakage, and other mixer products. This filter is also set up to pass DC bias voltage from the the V_{REF} pin into the LIMIN and MIXOUT pins through two filter-termination resistors (330Ω—see the *Typical Operating Circuit* for more information). If the filter can provide a DC shunt path, such as a transformer-capacitor based filter or some L-C filters, the two resistors can be combined into one parallel, equivalent resistor (165Ω) to reduce component count (Figure 5—inset).

Layout Issues

A well-designed PC board is an essential part of an RF circuit. For best performance, pay attention to power-supply issues, as well as the layout of the matching networks and tank circuit.

Power-Supply Layout

For minimizing coupling between different sections of the chip, the ideal power-supply layout is a star configuration, which has a heavily decoupled central V_{CC} node. The V_{CC} traces branch out from this node, each going to one V_{CC} node on the MAX2511. At the end of each of these traces is a bypass capacitor that is good at the RF frequency of interest. This arrangement provides local decoupling at each V_{CC} pin. At high frequency, any signal leaking from a supply pin sees a relatively high impedance (formed by the V_{CC} trace impedance) to the central V_{CC} node, and an even higher impedance to any other supply pin.

Place the VREF decoupling capacitor (0.1µF typ) as close to the MAX2511 as possible for best interstage filter performance. Use a high-quality, low-ESR capacitor for best results.

Matching Network Layout

The TXOUT, $\overline{TXOUT}$ port requires a bias network that consists of two inductors to V_{CC} (for differential drive) and optionally a back-termination resistor for matching to an external filter. The RXIN, $\overline{RXIN}$ port also needs an impedance-matching network. Both networks should be symmetrical and as close to the chip as possible. See the *Typical Operating Circuit* for more details. If you use a ground-plane PC board, cut out the ground plane under the matching network components to reduce parasitic capacitance.

Local-Oscillator Tank Layout

Oscillator-tank circuit layout is critical. Parasitic PC board capacitance, as well as trace inductance, can affect oscillation frequency. Keep the tank layout symmetrical, tightly packed, and as close to the device as possible. If a ground-plane PC board is used, the ground plane should be cut out under the oscillator components to reduce parasitic capacitance.

Low-Voltage IF Transceiver with Limiter and RSSI

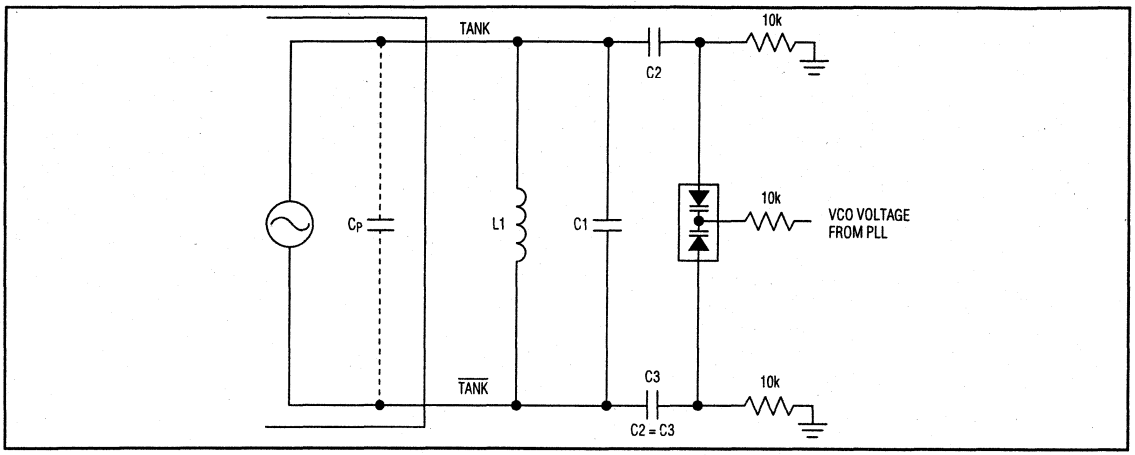


Figure 3. Oscillator Tank Schematic

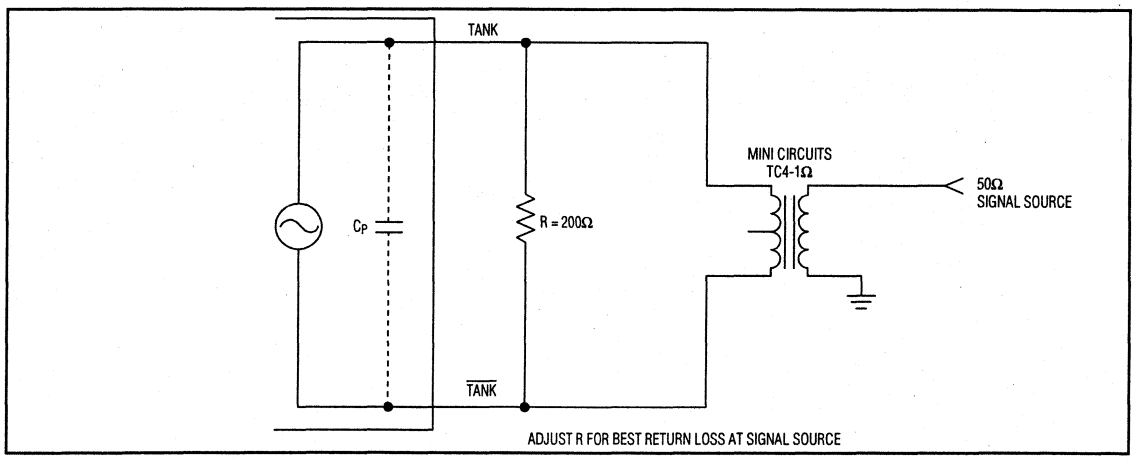


Figure 4. Overdriving the On-Chip Oscillator

Table 2. Recommended Values for L1

f_{LO} (MHz)	L1 (µH)
200 to 300	18
300 to 400	12
400 to 500	8.2

Table 3. Rx Input Impedance

FREQUENCY (MHz)	SERIES IMPEDANCE (Ω)	EQUIVALENT PARALLEL IMPEDANCE	
		R (Ω)	C (pF)
100	274-j226	460	2.85
200	131-j186	395	2.86
300	79-j138	320	2.9
400	58-j105	248	2.9
500	48-j82	188	2.9
600	43-j62	132	2.9

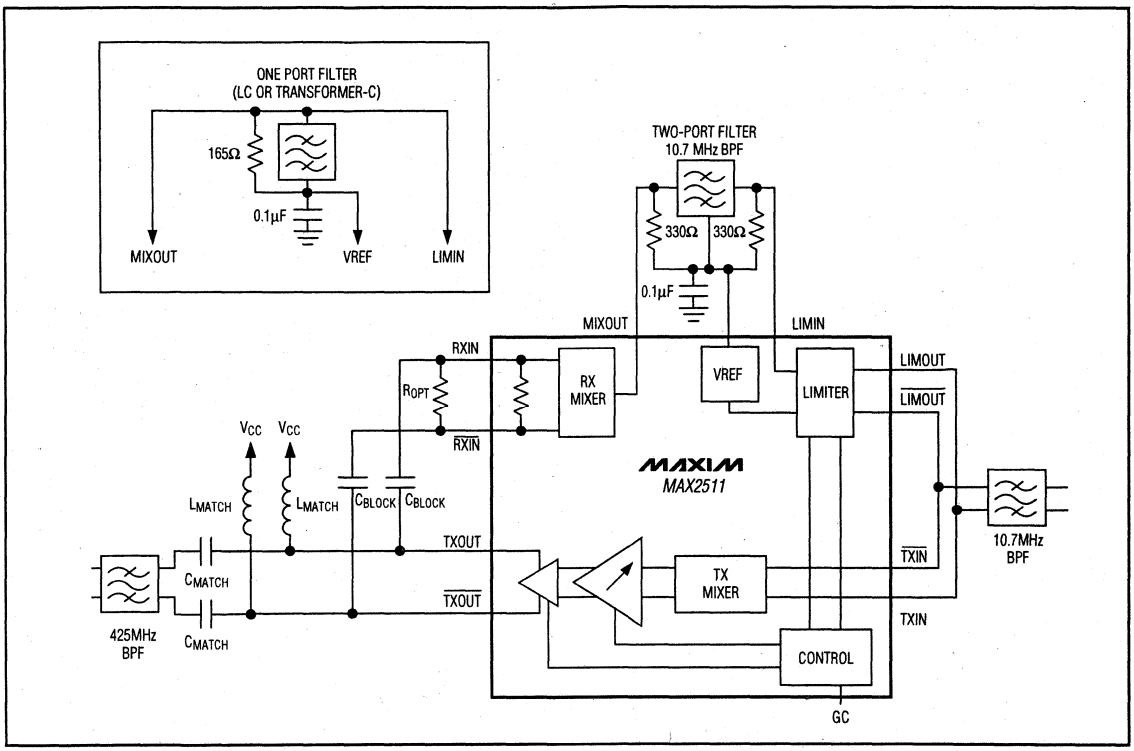
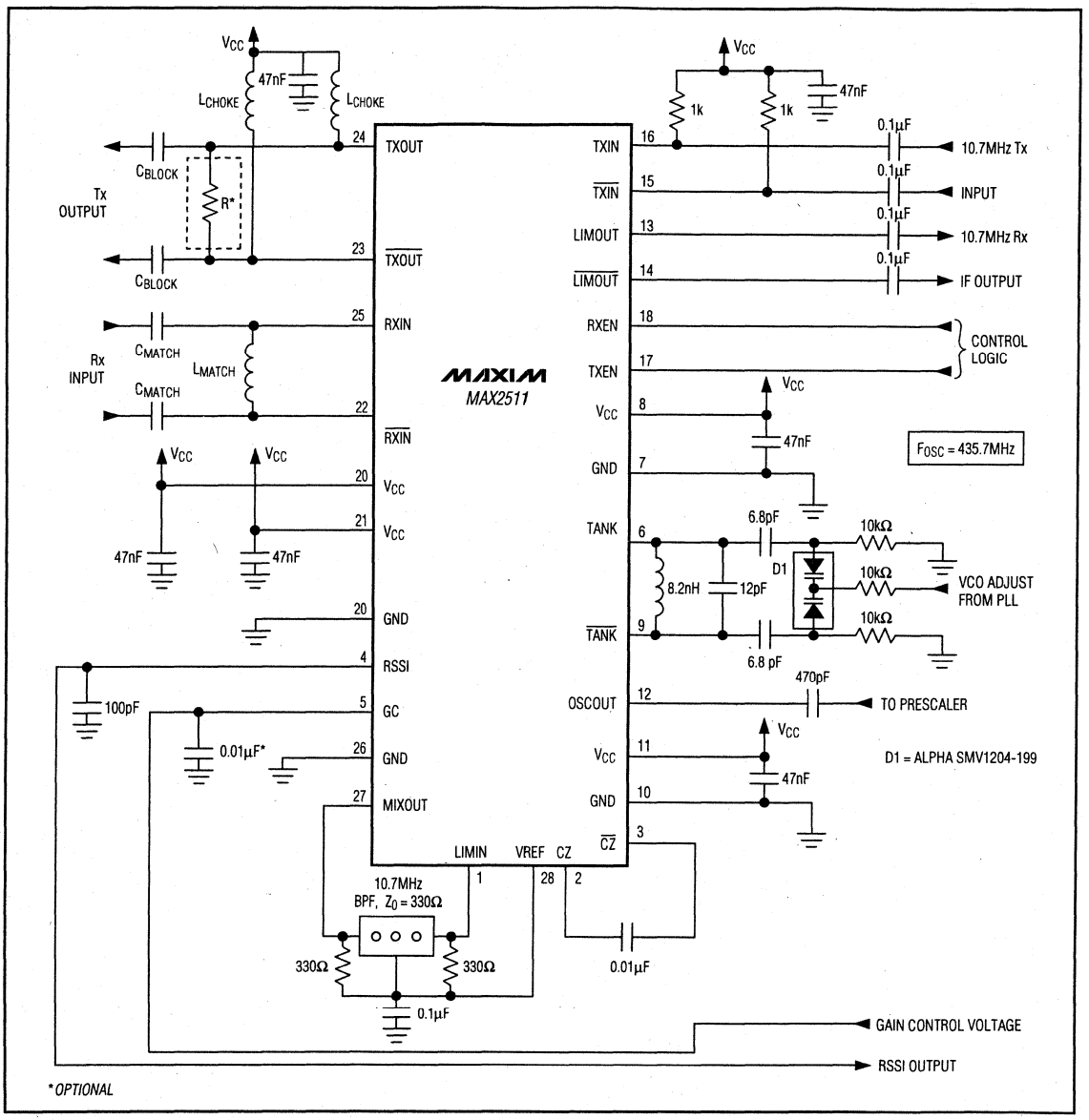


Figure 5. Filter Sharing

10

Low-Voltage IF Transceiver with Limiter and RSSI

Typical Operating Circuit



19-1185; Rev 2; 5/97

EVALUATION KIT AVAILABLE

3.6V, 1W RF Power Transistors for 900MHz Applications

General Description

The MAX2601/MAX2602 are RF power transistors optimized for use in portable cellular and wireless equipment that operates from three NiCd/NiMH cells or one Li-Ion cell. These transistors deliver 1W of RF power from a 3.6V supply with efficiency of 58% when biased for constant-envelope applications (e.g., FM or FSK). For NADC (IS-54) operation, they deliver 29dBm with -28dBc ACPR from a 4.8V supply.

The MAX2601 is a high-performance silicon bipolar RF power transistor. The MAX2602 includes a high-performance silicon bipolar RF power transistor, and a biasing diode that matches the thermal and process characteristics of the power transistor. This diode is used to create a bias network that accurately controls the power transistor's collector current as the temperature changes.

The MAX2601/MAX2602 can be used as the final stage in a discrete or module power amplifier. Silicon bipolar technology eliminates the need for voltage inverters and sequencing circuitry, as required by GaAsFET power amplifiers. Furthermore, a drain switch is not required to turn off the MAX2601/MAX2602. This increases operating time in two ways: it allows lower system end-of-life battery voltage, and it eliminates the wasted power from a drain-switch device.

The MAX2601/MAX2602 are available in thermally enhanced, 8-pin SO packages, which are screened to the extended temperature range (-40°C to +85°C). The MAX2602 is also available in die form.

Features

- **Low Voltage: Operates from 1 Li-Ion or 3 NiCd/NiMH Batteries**
- **DC-to-Microwave Operating Range**
- **1W Output Power at 900MHz**
- **On-Chip Diode for Accurate Biasing (MAX2602)**
- **Low-Cost Silicon Bipolar Technology**
- **Does Not Require Negative Bias or Supply Switch**
- **High Efficiency: 58%**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2601ESA	-40°C to +85°C	8 PSOPII
MAX2602ESA	-40°C to +85°C	8 PSOPII
MAX2602E/D	-40°C to +85°C	Dice*

**Dice are specified at T_A = +25°C, DC parameters only.*

Applications

Narrow-Band PCS (NPCS)

915MHz ISM Transmitters

Microcellular GSM (Power Class 5)

AMPS Cellular Phones

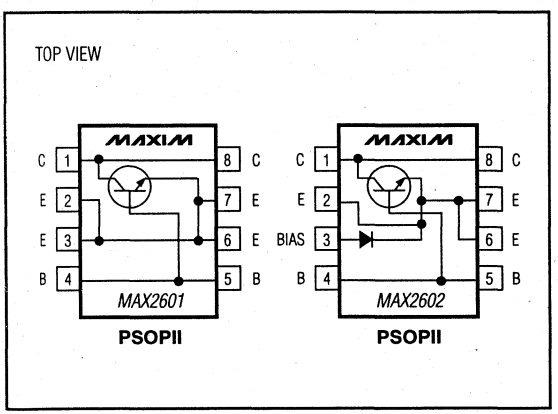
Digital Cellular Phones

Two-Way Paging

CDPD Modems

Land Mobile Radios

Pin Configurations



Typical Application Circuit appears at end of data sheet.

For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

3.6V, 1W RF Power Transistors for 900MHz Applications

ABSOLUTE MAXIMUM RATINGS

Collector-Emitter Voltage, Shorted Base (V_{CES}) 17V
Emitter Base Reverse Voltage (V_{EBO}).....2.3V
BIAS Diode Reverse Breakdown Voltage (MAX2602) 2.3V
Average Collector Current (I_C).....1200mA
Continuous Power Dissipation (T_A = +70°C)
PSOPII (derate 80mW/°C above +70°C) (Note 1) 6.4W

Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +165°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Backside slug must be properly soldered to ground plane (see *Slug Layout Techniques* section).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Collector-Emitter Breakdown Voltage	BV_{CEO}	I_C < 100µA	Open base	15			V
	BV_{CES}		Shorted base	15			
Collector-Emitter Sustaining Voltage	LV_{CEO}	I_C = 200mA		5.0			V
Collector-Base Breakdown Voltage	BV_{CBO}	I_C < 100µA, emitter open		15			V
DC Current Gain	h_{FE}	I_C = 250mA, V_{CE} = 3V		100			
Collector Cutoff Current	I_{CES}	V_{CE} = 6V, V_{BE} = 0V			0.05	1.5	µA
Output Capacitance	C_{OB}	V_{CB} = 3V, I_E = 0mA, f = 1MHz			9.6		pF

AC ELECTRICAL CHARACTERISTICS

(Test Circuit of Figure 1, V_{CC} = 3.6V, V_{BB} = 0.750V, Z_{LOAD} = Z_{SOURCE} = 50Ω, P_{OUT} = 30dBm, f = 836MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f	(Note 2)	DC		1	GHz
Base Current	I_B			4.2		mA
Harmonics	2fo, 3fo	V_{CC} = 3.6V, P_{OUT} = 30dBm		-43		dBc
		V_{CC} = 3.0V, P_{OUT} = 29dBm		-42		
Power Gain		P_{OUT} = 30dBm		11.6		dB
Collector Efficiency	η	No modulation		58		%
Stability under Continuous Load Mismatch Conditions	V_{SWR}	V_{CC} = 5.5V, all angles (Note 3)		8:1		
Two-Tone IMR	IM3	P_{OUT} = +30dBm total power, f1 = 835MHz, f2 = 836MHz		-16		dBc
	IM5			-25		
Noise Figure	NF	V_{BB} = 0.9V		3.3		dB

Note 2: Guaranteed by design.

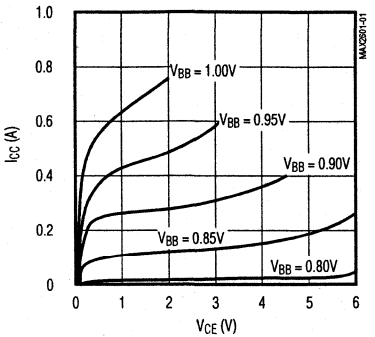
Note 3: Under these conditions: a) no spurious oscillations shall be observed at collector greater than -60dBc; b) no parametric degradation is observable when mismatch is removed; and c) no current draw in excess of the package dissipation capability is observed.

3.6V, 1W RF Power Transistors for 900MHz Applications

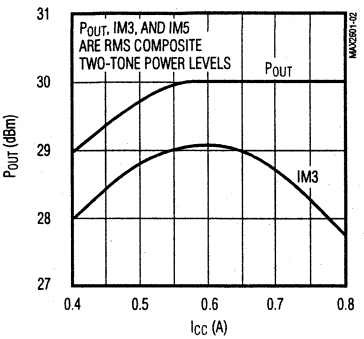
Typical Operating Characteristics

(Test Circuit of Figure 1, input/output matching networks optimized for specific measurement frequency, V_{CC} = 3.6V, V_{BB} = 0.750V, P_{OUT} = 30dBm, Z_{LOAD} = Z_{SOURCE} = 50Ω, f = 836MHz, T_A = +25°C, unless otherwise noted.)

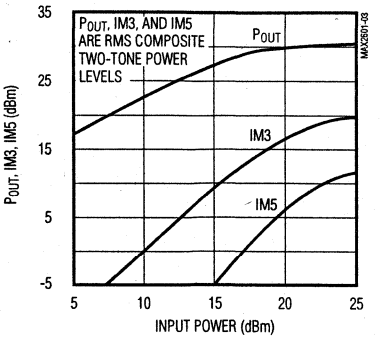
COLLECTOR CURRENT



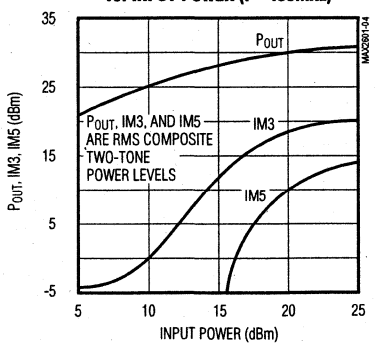
TWO-TONE OUTPUT POWER AND IM3 vs. COLLECTOR CURRENT



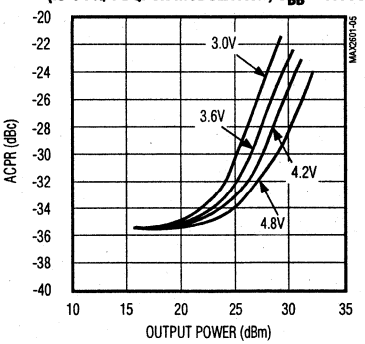
TWO-TONE OUTPUT POWER, IM3, IM5 vs. INPUT POWER



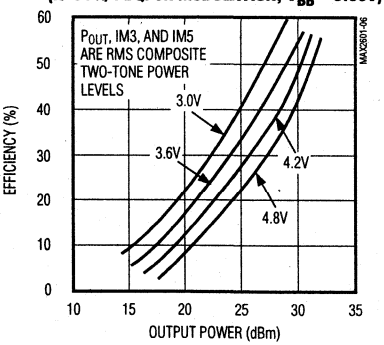
TWO-TONE OUTPUT POWER, IM3, IM5 vs. INPUT POWER (f = 433MHz)



ACPR vs. OUTPUT POWER (IS-54 π/4 DQPSK MODULATION, V_{BB} = 0.85V)



COLLECTOR EFFICIENCY vs. OUTPUT POWER (IS-54 π/4 DQPSK MODULATION, V_{BB} = 0.85V)



Pin Description

PIN		NAME	FUNCTION
MAX2601	MAX2602		
1, 8	1, 8	C	Transistor Collector
2, 3, 6, 7, Slug	2, 6, 7, Slug	E	Transistor Emitter
—	3	BIAS	Anode of the Biasing Diode that matches the thermal and process characteristics of the power transistor. Requires a high-RF-impedance, low-DC-impedance (e.g., inductor) connection to the transistor base (Pin 4). Current through the biasing diode (into Pin 3) is proportional to 1/15 the collector current in the transistor.
4, 5	4, 5	B	Transistor Base

3.6V, 1W RF Power Transistors for 900MHz Applications

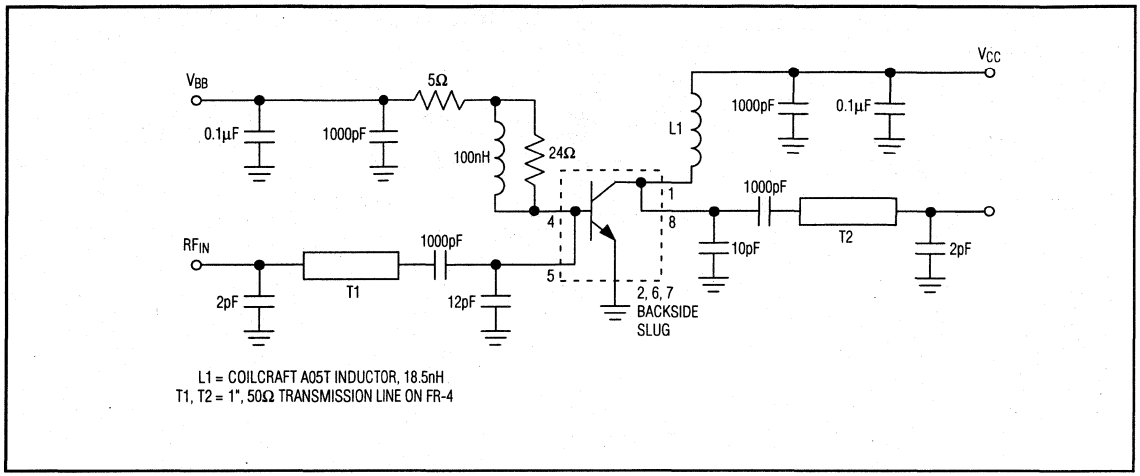


Figure 1. Test Circuit

Detailed Description

MAX2601/MAX2602

The MAX2601/MAX2602 are high-performance silicon bipolar transistors in power-enhanced, 8-pin SO packages. The base and collector connections use two pins each to reduce series inductance. The emitter connects to three (MAX2602) or four (MAX2601) pins in addition to a back-side heat slug, which solders directly to the PC board ground to reduce emitter inductance and improve thermal dissipation. The transistors are intended to be used in the common-emitter configuration for maximum power gain and power-added efficiency.

Current Mirror Bias (MAX2602 only)

The MAX2602 includes a high-performance silicon bipolar RF power transistor and a thermally matched biasing diode that matches the power transistor's thermal and process characteristics. This diode is used to create a bias network that accurately controls the power transistor's collector current as the temperature changes (Figure 2).

The biasing diode is a scaled version of the power transistor's base-emitter junction, in such a way that the current through the biasing diode is 1/15 the quiescent collector current of the RF power transistor. Supplying the biasing diode with a constant current source and connecting the diode's anode to the RF power transistor's base ensures that the RF power transistor's quiescent collector current remains constant through temperature variations. Simply tying the biasing diode to the supply through a resistor is adequate in most situations. If large supply variations are anticipated, connect the biasing diode to a reference voltage through a resistor, or use a stable current source. Connect the biasing diode to the base of the RF power transistor through a large RF impedance, such as an RF choke (inductor), and decouple to ground through a surface-mount chip capacitor larger than 1000pF.

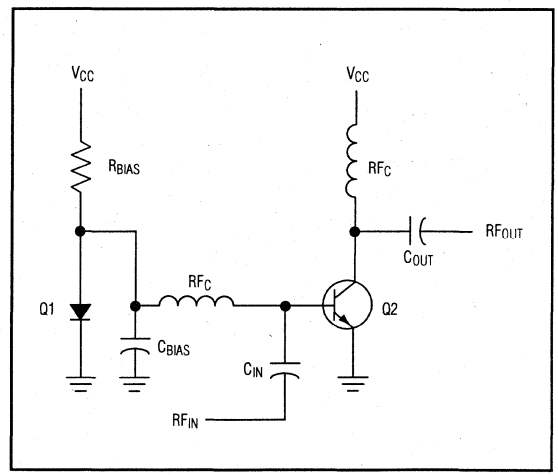


Figure 2. Bias Diode Application

3.6V, 1W RF Power Transistors for 900MHz Applications

Applications Information

Optimum Port Impedance

The source and load impedances presented to the MAX2601/MAX2602 have a direct impact upon its gain, output power, and linearity. Proper source- and load-terminating impedances (Z_S and Z_L) presented to the power transistor base and collector will ensure optimum performance.

For a power transistor, simply applying the conjugate of the transistor's input and output impedances calculated from small-signal S-parameters will yield less than optimum device performance.

For maximum efficiency at V_{BB} = 0.75V and V_{CC} = 3.6V, the optimum power-transistor source and load impedances (as defined in Figure 3) are:

At 836MHz: $Z_S = 5.5 + j2.0$
$Z_L = 6.5 + j1.5$

At 433MHz: $Z_S = 9.5 - j2.5$
$Z_L = 8.5 - j1.5$

Z_S and Z_L reflect the impedances that should be presented to the transistor's base and collector. The package parasitics are dominated by inductance (as shown in Figure 3), and need to be accounted for when calculating Z_S and Z_L.

The internal bond and package inductances shown in Figure 3 should be included as part of the end-application matching network, depending upon exact layout topology.

Slug Layout Techniques

The most important connection to make to the MAX2601/MAX2602 is the back side. It should connect directly to the PC board ground plane if it is on the top side, or through numerous plated through-holes if the ground plane is buried. For maximum gain, this connection should have very little self-inductance. Since it is also the thermal path for heat dissipation, it must have low thermal impedance, and the ground plane should be large.

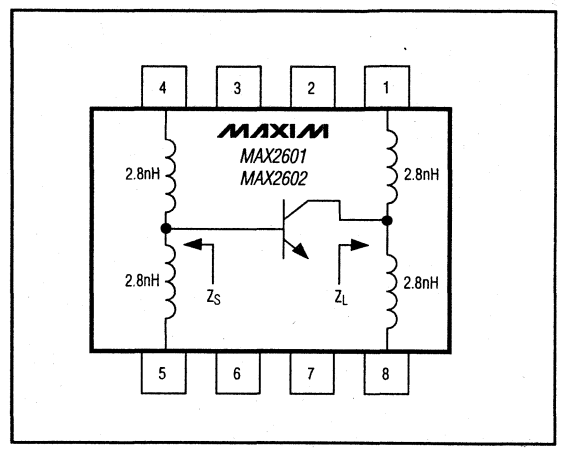


Figure 3. Optimum Port Impedance

10

19-1248; Rev 0; 7/97

EVALUATION KIT AVAILABLE

650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

General Description

The MAX2620 combines a low-noise oscillator with two output buffers in a low-cost, plastic surface-mount, ultra-small µMAX package. This device integrates functions typically achieved with discrete components. The oscillator exhibits low phase noise when properly mated with an external varactor-tuned resonant tank circuit. Two buffered outputs are provided for driving mixers or prescalers. The buffers provide load isolation to the oscillator and prevent frequency pulling due to load-impedance changes. Power consumption is typically just 27mW in operating mode (V_{CC} = 3.0V), and drops to less than 0.3µW in standby mode. The MAX2620 operates from a single +2.7V to +5.25V supply.

Applications

Analog Cellular Phones
Digital Cellular Phones
900MHz Cordless Phones
900MHz ISM-Band Applications
Land Mobile Radio
Narrowband PCS (NPCS)

Features

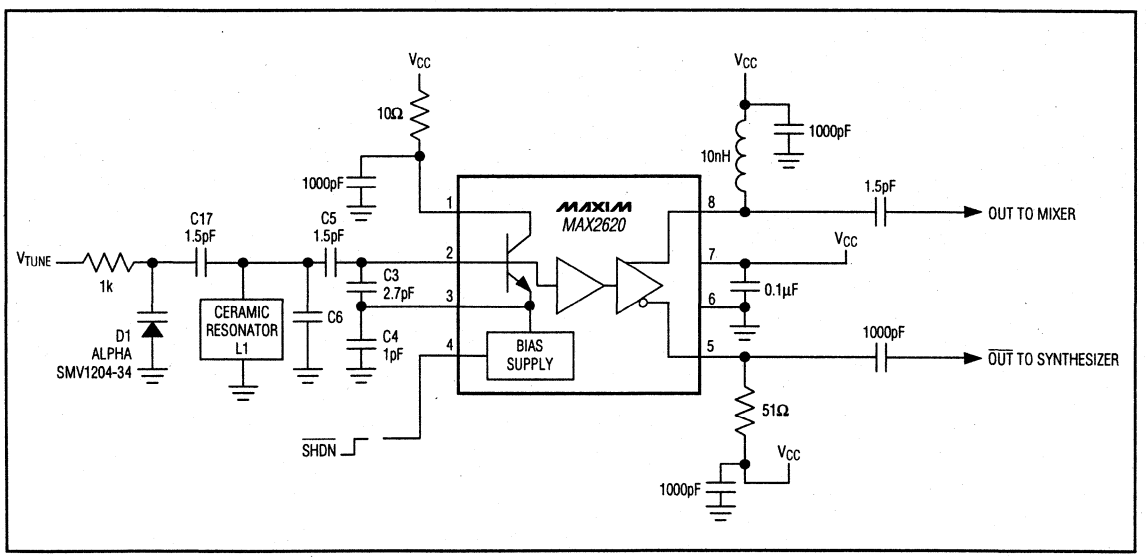
- **Low-Phase-Noise Oscillator: -110dBc/Hz (25kHz offset from carrier) Attainable**
- **Operates from Single +2.7V to +5.25V Supply**
- **Low-Cost Silicon Bipolar Design**
- **Two Output Buffers Provide Load Isolation**
- **Insensitive to Supply Variations**
- **Low, 27mW Power Consumption (V_{CC} = 3.0V)**
- **Low-Current Shutdown Mode: 0.1µA (typ)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2620EUA	-40°C to +85°C	8 µMAX

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

ABSOLUTE MAXIMUM RATINGS

$V_{CC}1$, $V_{CC}2$ to GND .....-0.3V to +6V
TANK, $\overline{SHDN}$, $\overline{OUT}$, OUT FDBK to GND ....-0.3V to (V_{CC} + 0.3V)
I_{FDBK}.....±20mA
Continuous Power Dissipation (T_A = +70°C)
μMAX (derate 5.7mW/°C above +70°C) 457mW
Operating Temperature Range
MAX2620EUA .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

($V_{CC}1$, $V_{CC}2$ = +2.7V to +5.25V, FDBK = open, TANK = open, OUT and $\overline{OUT}$ connected to V_{CC} through 50Ω, $\overline{SHDN}$ = 2V, T_A = -40°C to +85°C, unless otherwise noted. Typical values measured at $V_{CC}1$ = $V_{CC}2$ = 3.0V, T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current			9.0	12.5	mA
Shutdown Current	$\overline{SHDN}$ = 0.6V		0.1	2	μA
Shutdown Input Voltage High		2.0			V
Shutdown Input Voltage Low				0.6	V
Shutdown Bias Current High	$\overline{SHDN}$ = 2.0V		5.5	20	μA
Shutdown Bias Current Low	$\overline{SHDN}$ = 0.6V			0.5	μA

AC ELECTRICAL CHARACTERISTICS

(Per Test Circuit of Figure 1, V_{CC} = +3.0V, $\overline{SHDN}$ = V_{CC}, Z_{LOAD} = Z_{SOURCE} = 50Ω, P_{IN} = -20dBm (50Ω), f_{TEST} = 900MHz, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	T_A = -40°C to +85°C (Note 1)	650		1050	MHz
Reverse Isolation	OUT or $\overline{OUT}$ to TANK; OUT, $\overline{OUT}$ driven at P = -20dBm		50		dB
Output Isolation	OUT to $\overline{OUT}$		33		dB

Note 1: Over this frequency range, the magnitude of the negative real impedance measured at TANK is greater than one-tenth the magnitude of the reactive impedances at TANK. This implies proper oscillator start-up when using an external resonator tank circuit with Q > 10.

TYPICAL OPERATING CIRCUIT PERFORMANCE—CERAMIC-RESONATOR-BASED TANK

(Per Typical Operating Circuit, V_{CC} = +3.0V, V_{TUNE} = 1.5V, $\overline{SHDN}$ = V_{CC}, load at OUT = 50Ω, load at $\overline{OUT}$ = 50Ω, L1 = coaxial ceramic resonator: Trans-Tech SR8800LPQ1357BY, C6 = 1pF, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tuning Range	V_{TUNE} = 0.5V to 3.0V		±13		MHz
Phase Noise	SSB @ Δf = 25kHz		-110		dBc/Hz
	SSB @ Δf = 300kHz		-132		
Output Power (single-ended)	At OUT (Note 2)	-6	-2		dBm
	At OUT, per test circuit of Figure 1. T_A = -40°C to +85° (Note 2).	-11	-8		
	At $\overline{OUT}$ (Note 2)	-16	-12.5		
Noise Power	f_O ± >10MHz		-147		dBm/Hz
Average Tuning Gain			11		MHz/V
Second-Harmonic Output			-29		dBc
Load Pull	VSWR = 1.75:1, all phases		163		kHzp-p
Supply Pushing	V_{CC} stepped from 3V to 4V		71		kHz/V

Note 2: Guaranteed by design and characterization.

TYPICAL OPERATING CIRCUIT PERFORMANCE—INDUCTOR-BASED TANK

(Per Typical Operating Circuit, V_{CC} = +3.0V, V_{TUNE} = 1.5V, $\overline{SHDN}$ = V_{CC}, load at OUT = 50Ω, load at $\overline{OUT}$ = 50Ω, L1 = 5nH (Coilcraft A02T), C6 = 1.5pF, T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tuning Range	V_{TUNE} = 0.5V to 3.0V		±15		MHz
Phase Noise	SSB @ Δf = 25kHz		-107		dBc/Hz
	SSB @ Δf = 300kHz		-127		
Output Power (single-ended)	At OUT (Note 2)	-6	-2		dBm
	At OUT, per test circuit of Figure 1. T_A = -40°C to +85°C (Note 2).	-11	-8		
	At $\overline{OUT}$ (Note 2)	-16	-12.5		
Noise Power	f_O ± >10MHz		-147		dBm/Hz
Average Tuning Gain			13		MHz/V
Second-Harmonic Output			-29		dBc
Load Pull	VSWR = 1.75:1, all phase angles		340		kHzp-p
Supply Pushing	V_{CC} stepped from 3V to 4V		150		kHz/V

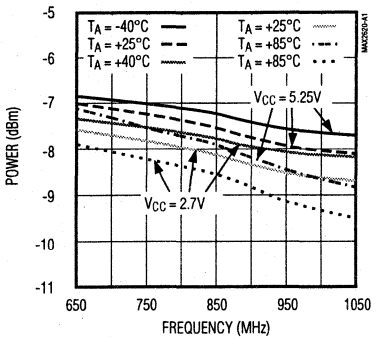
Note 2: Guaranteed by design and characterization.

650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

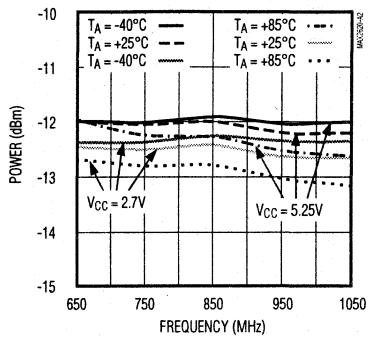
Typical Operating Characteristics

(Per test circuit of Figure 1, V_{CC} = +3.0V, $\overline{SHDN}$ = V_{CC}, Z_{LOAD} = Z_{SOURCE} = 50Ω, P_{IN} = -20dBm/50Ω, f_{TEST} = 900MHz, T_A = +25°C, unless otherwise noted.)

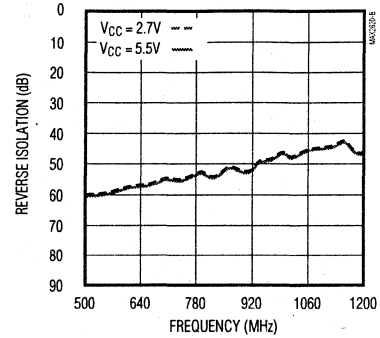
OUT OUTPUT POWER vs. FREQUENCY OVER V_{CC} AND TEMPERATURE



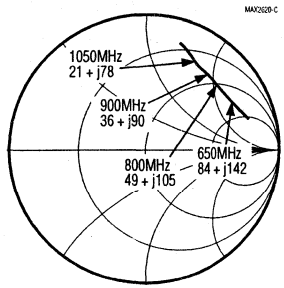
$\overline{OUT}$ OUTPUT POWER vs. FREQUENCY OVER V_{CC} AND TEMPERATURE



REVERSE ISOLATION vs. FREQUENCY



TYPICAL $1/S_{11}$ vs. FREQUENCY MEASURED AT TEST PORT



SUPPLY CURRENT vs. TEMPERATURE

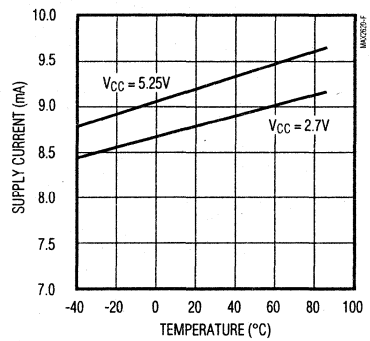


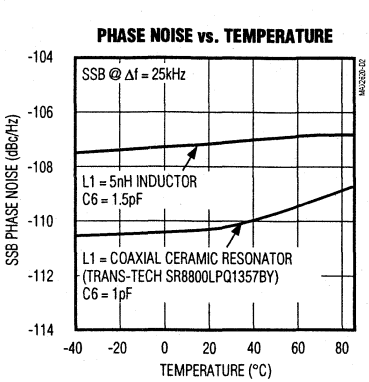
Table 1. Recommended Load Impedance at OUT or $\overline{OUT}$ for Optimum Power Transfer

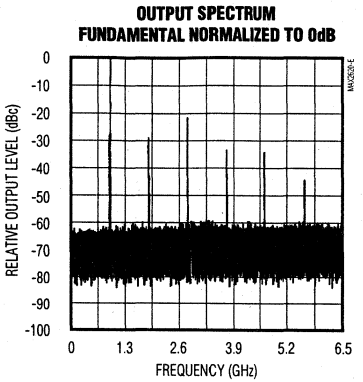
FREQUENCY (MHZ)	Real Component (R in Ω)	Imaginary Component (X in Ω)
650	17.5	62.3
750	17.2	50.6
850	10.9	33.1
950	7.3	26.3
1050	6.5	22.7

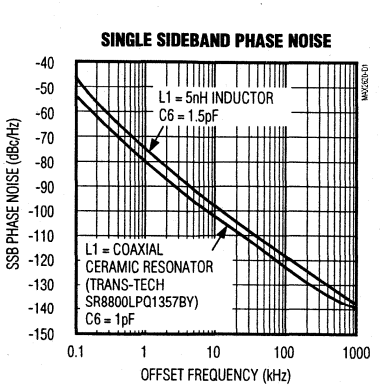
650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

Typical Operating Characteristics (continued)

(Per *Typical Operating Circuit*, V_{CC} = +3.0V, V_{TUNE} = 1.5V, $\overline{SHDN}$ = V_{CC}, load at OUT = 50Ω, load at $\overline{OUT}$ = 50Ω, L1 = coaxial ceramic resonator: Trans-Tech SR8800LPQ1357BY, C6 = 1pF, T_A = +25°C, unless otherwise noted.)







Pin Description

PIN	NAME	FUNCTION
1	$V_{CC}1$	Oscillator DC Supply Voltage. Decouple $V_{CC}1$ with 1000pF capacitor to ground. Use a capacitor with low series inductance (size 0805 or smaller). Further power-supply decoupling can be achieved by adding a 10Ω resistor in series from $V_{CC}1$ to the supply. Proper power-supply decoupling is critical to the low noise and spurious performance of any oscillator.
2	TANK	Oscillator Tank Circuit Connection. Refer to the *Applications Information* section.
3	FDBK	Oscillator Feedback Circuit Connection. Connecting capacitors of the appropriate value between FDBK and TANK and between FDBK and GND tunes the oscillator's reflection gain (negative resistance) to peak at the desired oscillation frequency. Refer to the *Applications Information* section.
4	$\overline{SHDN}$	Logic-Controlled Input. A low level turns off the entire circuitry such that the IC will draw only leakage current at its supply pins. This is a high-impedance input.
5	$\overline{OUT}$	Open-Collector Output Buffer (complement). Requires external pull-up to the voltage supply. Pull-up can be resistor, choke, or inductor (which is part of a matching network). The matching-circuit approach provides the highest-power output and greatest efficiency. Refer to Table 1 and the *Applications Information* section. $\overline{OUT}$ may be used with OUT in a differential output configuration.
6	GND	Ground Connection. Provide a low-inductance connection to the circuit ground plane.
7	$V_{CC}2$	Output Buffer DC Supply Voltage. Decouple $V_{CC}2$ with a 1000pF capacitor to ground. Use a capacitor with low series inductance (size 0805 or smaller).
8	OUT	Open-Collector Output Buffer. Requires external pull-up to the voltage supply. Pull-up can be resistor, choke, or inductor (which is part of a matching network). The matching-circuit approach provides the highest-power output and greatest efficiency. Refer to Table 1 and the *Applications Information* section. OUT may be used with $\overline{OUT}$ in a differential output configuration.

650MHz to 1050MHz Integrated Oscillator with Buffered Outputs

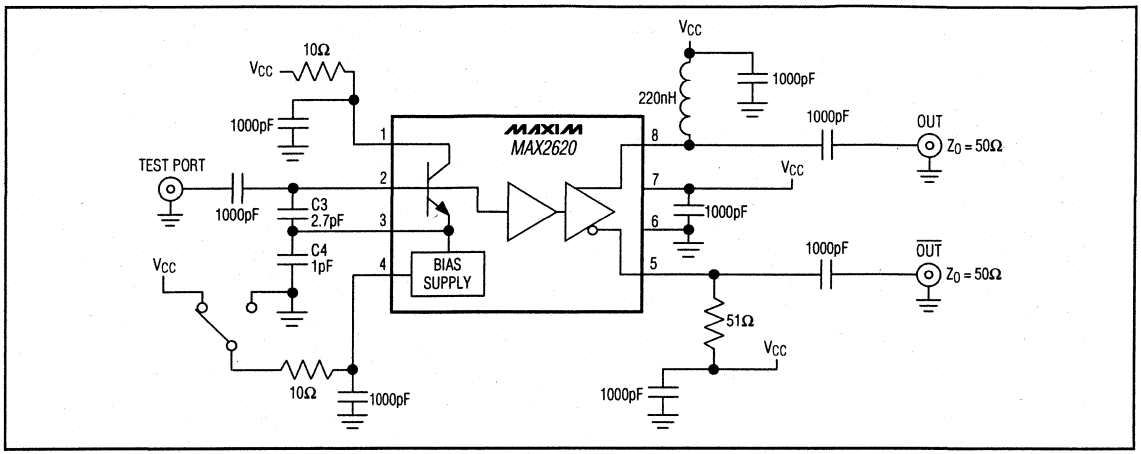


Figure 1. Test Circuit

Detailed Description

Oscillator

The oscillator is a common-collector, negative-resistance type that uses the IC's internal parasitic elements to create a negative resistance at the base-emitter port. The transistor oscillator has been optimized for low-noise operation. Base and emitter leads are provided as external connections for a feedback capacitor and resonator. A resonant circuit, tuned to the appropriate frequency and connected to the base lead, will cause oscillation. Varactor diodes may be used in the resonant circuit to create a voltage-controlled oscillator (VCO). The oscillator is internally biased to an optimal operating point, and the base and emitter leads need to be capacitively coupled due to the bias voltages present.

Output Buffers

The output buffers (OUT and $\overline{OUT}$) are an open-collector, differential-pair configuration and provide load isolation to the oscillator. The outputs can be used differentially to drive an integrated circuit mixer. Alternatively, isolation is provided between the buffer outputs when one output drives a mixer (either upconversion or downconversion) and the other output drives a prescaler. The isolation in this configuration prevents prescaler noise from corrupting the oscillator signal's spectral purity.

A logic-controlled $\overline{SHDN}$ pin turns off all bias to the IC when pulled low.

Applications Information

Tank Circuit Design

At the frequency of interest, the MAX2620 portion of Figure 2 shows the one-port circuit model for the TANK pin (test port in Figure 1).

For the circuit to oscillate at a desired frequency, the resonant tank circuit connected to TANK must present an impedance that is a complement to the network. This resonant tank circuit must have a positive real component that is one-third to one-half the magnitude of the negative real part of the oscillator device, as well as a reactive component that is opposite in sign to the reactive component of the oscillator device.

Keeping the resonant tank circuit's real component between one-third and one-half the magnitude of the negative real component ensures that oscillations will start. After start-up, the oscillator's negative resistance decreases, primarily due to gain compression, and reaches equilibrium with the real component (the circuit losses) in the resonant tank circuit. Making the resonant tank circuit reactance tunable (e.g., through use of a varactor diode) allows for tuneability of the oscillation frequency, as long as the oscillator exhibits negative resistance over the desired tuning range.

The MAX2620 provides an optimized negative-resistance device. The one-port characteristics of the device are given as a plot of 1/S11 in the *Typical Operating Characteristics*. 1/S11 is used because it maps inside the unit circle Smith chart when the device exhibits negative resistance (reflection gain).

Feedback Capacitors

To tune the negative-resistance characteristics, adjust the values of the feedback capacitors connected between TANK and FDBK (C3), and from FDBK to ground (C4). The capacitor valves to yield the desired TANK port impedance can be approximated as:

$$R_{TANK} = g_m X_{C3} X_{C4}$$

where g_m = 0.018mS, and X_{C3} and X_{C4} are the reactances of C3 and C4.

This tuning should be directly measured on a vector network analyzer performing a one-port measurement into TANK (test port in Figure 1). This measurement will establish more precisely what the tank characteristics need to be, such that the resonant tank network can be designed.

The MAX2620's oscillator is optimized for low-phase-noise operation. Achieving lowest phase-noise characteristics requires the use of high-Q (quality factor) components such as ceramic transmission-line type resonators or high-Q inductors. Also, keep C5 and C17 (see *Typical Operating Circuit*) as small a value as possible while still maintaining desired frequency and tuning range to maximize loaded Q.

There are many good references on the topic of oscillator design. An excellent reference is "The Oscillator as a Reflection Amplifier, an Intuitive Approach to Oscillator Design," by John W. Boyles, *Microwave Journal*, June 1986, pp. 83–98.

Output Matching Configuration

Both of the MAX2620's outputs (OUT and $\overline{OUT}$) are open collectors. They need to be pulled up to the supply by external components. An easy approach to this pull-up is a resistor. A 50Ω resistor value would inherently match the output to a 50Ω system. The *Typical Operating Circuit* shows $\overline{OUT}$ configured this way. Alternatively, a choke pull-up (Figure 1), yields greater output power (approximately -8dBm at 900MHz).

When maximum power is required, use an inductor as the supply pull-up, and match the inductor's output impedance to the desired system impedance. Table 1 in the *Typical Operating Characteristics* shows recommended load impedance presented to OUT and $\overline{OUT}$ for maximum power transfer. Using this data and standard matching-network synthesis techniques, a matching network can be constructed that will optimize power output into most load impedances. The value of the inductor used for pull-up should be used in the synthesis of the matching network.

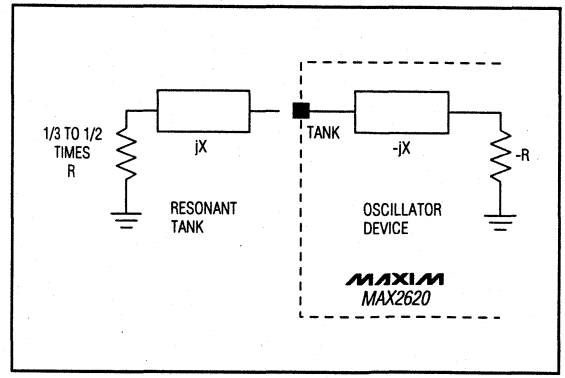
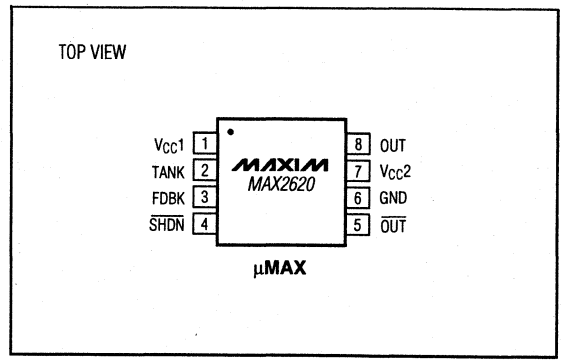


Figure 2. Oscillator Circuit Model

Pin Configuration



19-1181; Rev 1; 7/97

MAXIM

VHF-to-Microwave, +3V, General-Purpose Amplifiers

General Description

The MAX2630/MAX2631/MAX2632/MAX2633 are low-voltage, low-noise amplifiers for use from VHF to microwave frequencies. Operating from a single +2.7V to +5.5V supply, these devices have a flat gain response to 900MHz. Their low noise figure and low supply current make them ideal for receive, buffer, and transmit IF applications.

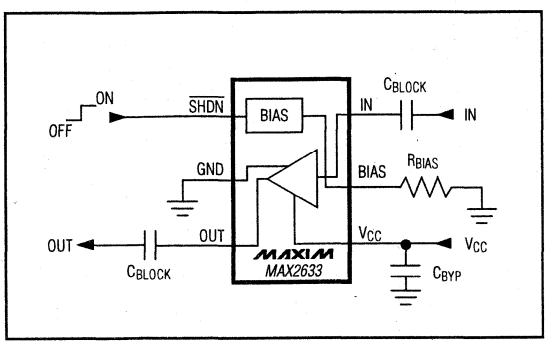
The MAX2630/MAX2631 are biased internally, eliminating the need for external bias resistors or inductors. The MAX2632/MAX2633 have a user-selectable supply current, which can be adjusted by adding a single external resistor. This allows customized output power and gain according to specific applications requirements. The MAX2631/MAX2633 feature a shutdown pin that allows them to be powered down to less than 1µA supply current. Aside from a single bias resistor required for the MAX2632/MAX2633, the only external components needed for this family of amplifiers are input and output blocking capacitors and a V_{CC} bypass capacitor.

The MAX2630 comes in a 4-pin SOT143 package, requiring minimal board space. The MAX2631/MAX2632 come in small 5-pin SOT23 packages. The MAX2633 comes in a 6-pin SOT23 package.

Applications

Personal Communicating Systems	Cordless Phones
Global Positioning Systems	Cellular Phones
Wireless Local Area Networks	ISM Radios
Wireless Local Loops	TV Tuners
Land Mobile Radios	Set-Top Boxes

Typical Operating Circuit



Features

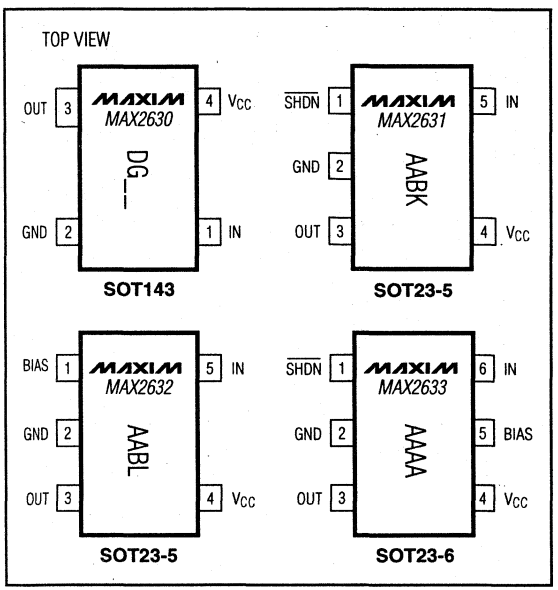
- ♦ **Single +2.7V to +5.5V Operation**
- ♦ **Internally Biased (MAX2630/MAX2631)**
- ♦ **Adjustable Bias (MAX2632/MAX2633)**
- ♦ **6.6mA Supply Current (insensitive to supply voltage)**
- ♦ **1µA Shutdown Current (MAX2631/MAX2633)**
- ♦ **3.7dB Noise Figure**
- ♦ **13.4dB Gain**
- ♦ **Ultra-Small SOT Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	SOT TOP MARK*
MAX2630EUS-T	-40°C to +85°C	4 SOT143	DG__
MAX2631EUK-T	-40°C to +85°C	5 SOT23-5	AABK
MAX2632EUK-T	-40°C to +85°C	5 SOT23-5	AABL
MAX2633EUT-T	-40°C to +85°C	6 SOT23-6	AAAA

**The first two letters in the SOT top mark identify the part, while the remaining two letters are the lot-tracking code.*

Pin Configurations



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VHF-to-Microwave, +3V, General-Purpose Amplifiers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to 6V
Input Power.....5dBm
OUT Current .....±12mA
IN to GND Voltage .....-1.2V to 1.2V
Bias to GND Voltage.....0.0V to 3V
Voltage at $\overline{SHDN}$ Input
(MAX2631/MAX2633).....-0.3V to (V_{CC} + 0.3V)
Current into $\overline{SHDN}$ Input (MAX2631/MAX2633).....100µA

Continuous Power Dissipation (T_A = +70°C)
SOT143 (derate 4mW/°C above +70°C).....320mW
SOT23-5 (derate 7.1mW/°C above +70°C).....571mW
SOT23-6 (derate 7.1mW/°C above +70°C).....571mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3V, Z_0 = 50Ω, f_{IN} = 900MHz, R_{BIAS} = 10kΩ (MAX2632/MAX2633), $V_{\overline{SHDN}}$ = V_{CC} (MAX2631/MAX2633), T_A = +25°C, unless otherwise noted.)

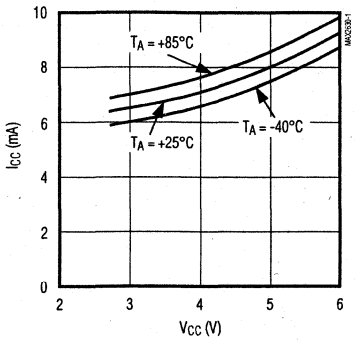
PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Temperature Range	(Note 1)		-40		85	degrees
Supply Voltage			2.7		5.5	V
Power Gain	T_A = +25°C		11	13.4	16.5	dB
	T_A = T_{MIN} to T_{MAX} (Note 1)		9.4		18.4	
Noise Figure				3.8		dB
Output 1dB Compression Point				-11		dBm
Output IP3				-1		dBm
Input Voltage Standing-Wave Ratio	f_{IN} = 800MHz to 1000MHz			1.3:1		
Output Voltage Standing-Wave Ratio	f_{IN} = 800MHz to 1000MHz			1.25:1		
Supply Current	R_{BIAS} = 40kΩ			1.3	1.5	mA
	R_{BIAS} = 10kΩ	V_{CC} = 3V, T_A = +25°C	5.5	6.5	8.0	
		V_{CC} = 3V, T_A = T_{MIN} to T_{MAX} (Note1)	4.2	6.5	9.2	
		V_{CC} = 2.7V to 5.5V, T_A = +25°C	5.2	6.5	11.0	
	R_{BIAS} = 500Ω		15	17		
Shutdown Supply Current	MAX2631/MAX2633			<0.1	1	µA
$\overline{SHDN}$ Input Low Voltage	MAX2631/MAX2633, V_{CC} = 2.7V to 5.5V				0.45	V
$\overline{SHDN}$ Input High Voltage	MAX2631/MAX2633, V_{CC} = 2.7V to 5.5V		2.0			V
$\overline{SHDN}$ Input Bias Current	MAX2631/ MAX2633	$V_{\overline{SHDN}}$ = V_{CC}			30	µA
		$V_{\overline{SHDN}}$ = GND			1	

Note 1: Guaranteed by design and characterization.

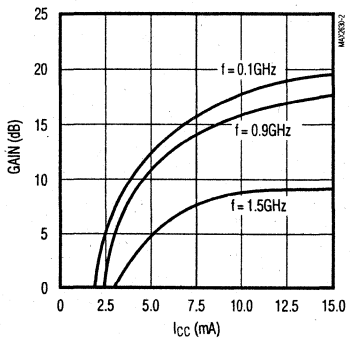
Typical Operating Characteristics

(V_{CC} = +3V, $V_{\overline{SHDN}}$ = V_{CC} (MAX2631/MAX2633), Z_0 = 50Ω, f_{IN} = 900MHz, R_{BIAS} = 10kΩ (MAX2632/MAX2633), T_A = +25°C, unless otherwise noted.)

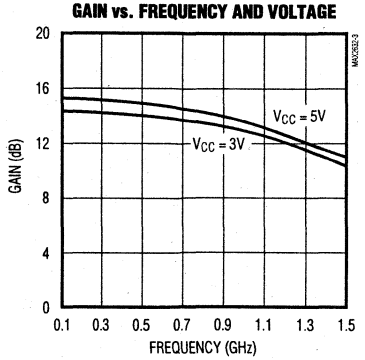
SUPPLY CURRENT vs. SUPPLY VOLTAGE



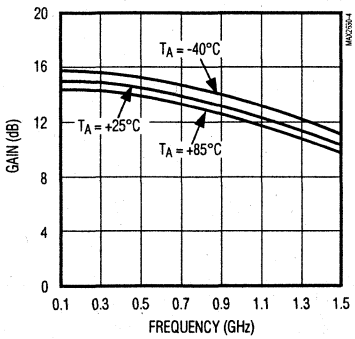
MAX2632/MAX2633 GAIN vs. SUPPLY CURRENT



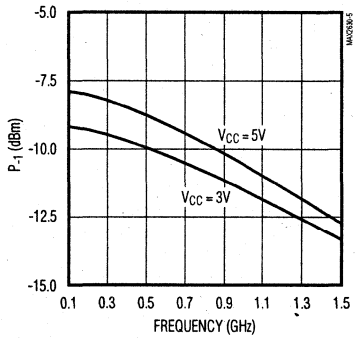
GAIN vs. FREQUENCY AND VOLTAGE



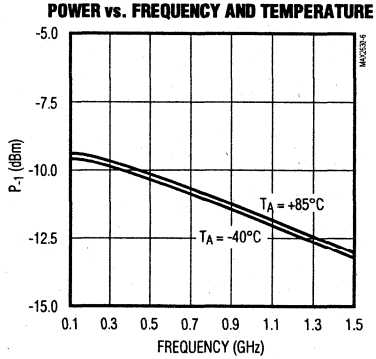
GAIN vs. FREQUENCY AND TEMPERATURE



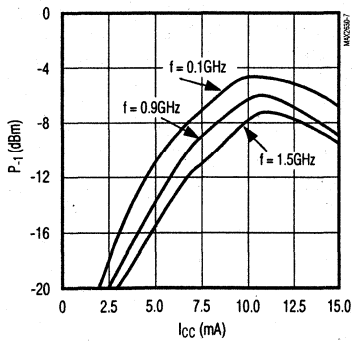
OUTPUT 1dB COMPRESSION POWER vs. FREQUENCY AND VOLTAGE



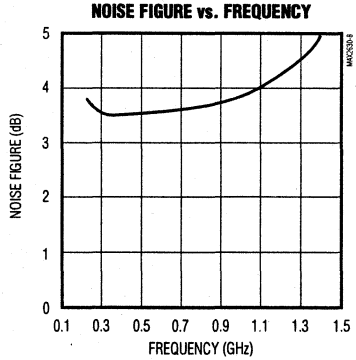
OUTPUT 1dB COMPRESSION POWER vs. FREQUENCY AND TEMPERATURE



MAX2632/MAX2633 OUTPUT 1dB COMPRESSION POWER vs. SUPPLY CURRENT



NOISE FIGURE vs. FREQUENCY



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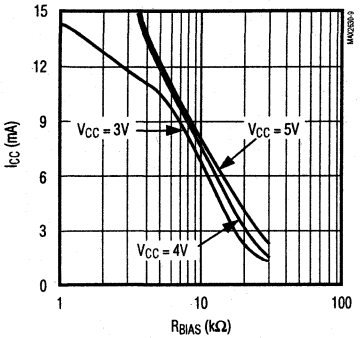
VHF-to-Microwave, +3V, General-Purpose Amplifiers

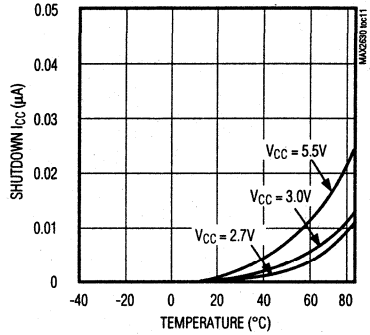
Typical Operating Characteristics (continued)

(V_{CC} = +3V, $V_{\overline{SHDN}}$ = V_{CC} (MAX2631/MAX2633), Z_O = 50Ω, f_{IN} = 900MHz, R_{BIAS} = 10kΩ (MAX2632/MAX2633), T_A = +25°C, unless otherwise noted.)

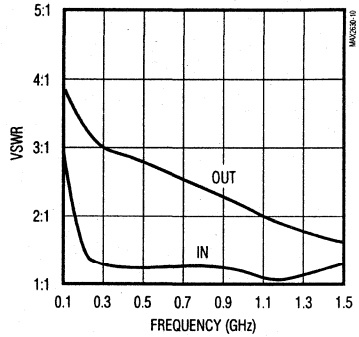
MAX2632/MAX2633 SUPPLY CURRENT vs. R_{BIAS}



MAX2631/MAX2633 SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



VOLTAGE STANDING-WAVE RATIO vs. FREQUENCY



Pin Description

PIN				NAME	FUNCTION
MAX2630	MAX2631	MAX2632	MAX2633		
1	5	5	6	IN	Amplifier Input. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency.
2	2	2	2	GND	Ground Connection. For optimum performance, provide a low-inductance connection to the ground plane.
3	3	3	3	OUT	Amplifier Output. Use a series blocking capacitor with less than 3Ω reactance at your lowest operating frequency.
4	4	4	4	V_{CC}	Supply Connection. Bypass directly at the supply pin. The value of the bypass capacitor is determined by the lowest operating frequency, and is typically the same as the blocking capacitor value. Additional bypassing may be necessary for long V_{CC} lines.
—	1	—	1	$\overline{SHDN}$	Shutdown Input. Driving $\overline{SHDN}$ with a logic low turns off the amplifier.
—	—	1	5	BIAS	Bias Resistor Connection. Connect a resistor to GND to set the bias current. See the Supply Current vs. R_{BIAS} graph in the *Typical Operating Characteristics*.

Table 1a. Typical Scattering Parameters

(V_{CC} = +3V, $V_{\overline{SHDN}}$ = V_{CC}, Z_0 = 50Ω, R_{BIAS} = 10kΩ, T_A = +25°C.)

FREQUENCY (GHz)	S11 (mag)	S11 (ang)	S21 (dB)	S21 (mag)	S21 (ang)	S12 (dB)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)	K
0.05	0.59	-50	12.9	4.39	46	-38.7	0.012	37	0.62	-19	4.30
0.10	0.37	-70	14.2	5.11	1	-36.7	0.015	12	0.57	-29	4.07
0.20	0.22	-86	14.5	5.32	-49	-35.8	0.016	-13	0.54	-49	3.93
0.30	0.17	-100	14.5	5.32	-89	-35.0	0.018	-32	0.53	-71	3.74
0.40	0.16	-109	14.5	5.28	-125	-34.4	0.019	-51	0.51	-94	3.61
0.50	0.15	-99	14.3	5.19	-138	-33.6	0.021	-70	0.50	-118	3.45
0.60	0.14	-86	14.1	5.05	-127	-33.0	0.022	-89	0.48	-109	3.38
0.70	0.14	-68	13.9	4.93	-116	-32.2	0.025	-107	0.46	-96	3.27
0.80	0.14	-49	13.5	4.75	-104	-31.3	0.027	-124	0.44	-82	3.16
0.90	0.13	-31	13.0	4.49	-93	-30.3	0.031	-142	0.42	-68	3.05
1.00	0.13	-10	12.6	4.25	-82	-29.0	0.035	-161	0.40	-53	2.87
1.20	0.06	19	10.8	3.48	-58	-25.8	0.051	153	0.33	-25	2.59
1.40	0.11	-60	7.9	2.48	-110	-23.7	0.065	113	0.26	-12	2.90
1.60	0.24	-31	5.6	1.91	-162	-23.6	0.066	122	0.26	-7	3.51
1.80	0.30	-26	4.8	1.73	144	-23.7	0.065	120	0.26	-34	3.76
2.00	0.31	-66	4.3	1.63	86	-23.3	0.069	117	0.25	-63	3.80
2.20	0.27	-98	3.6	1.51	27	-22.3	0.077	116	0.24	-83	3.80
2.40	0.24	-115	2.6	1.36	5	-21.3	0.086	116	0.25	-97	3.81
2.50	0.22	-120	2.2	1.29	12	-21.0	0.089	114	0.27	-106	3.86

VHF-to-Microwave, +3V, General-Purpose Amplifiers

Table 1b. MAX2633 Typical Scattering Parameters

(V_{CC} = +5V, $V_{\overline{SHDN}}$ = V_{CC}, Z_0 = 50Ω, R_{BIAS} = 10k, T_A = +25°C.)

FREQUENCY (GHz)	S11 (mag)	S11 (ang)	S21 (dB)	S21 (mag)	S21 (ang)	S12 (dB)	S12 (mag)	S12 (ang)	S22 (mag)	S22 (ang)	K
0.05	0.58	-53	13.6	4.80	45	-39.2	0.011	36	0.62	-22	4.26
0.10	0.35	-76	15.0	5.62	1	-36.9	0.014	13	0.57	-29	3.83
0.20	0.20	-97	15.4	5.87	-48	-36.1	0.016	-14	0.55	-49	3.75
0.30	0.14	-101	15.4	5.91	-87	-35.2	0.017	-31	0.53	-72	3.48
0.40	0.12	-94	15.4	5.91	-123	-34.7	0.018	-50	0.52	-95	3.35
0.50	0.11	-82	15.4	5.87	-141	-33.8	0.020	-68	0.51	-119	3.14
0.60	0.11	-66	15.2	5.78	-130	-33.1	0.022	-86	0.49	-108	3.02
0.70	0.11	-45	15.1	5.68	-119	-32.3	0.024	-104	0.48	-94	2.87
0.80	0.11	-22	14.9	5.54	-108	-31.3	0.027	-121	0.45	-79	2.73
0.90	0.12	-2	14.5	5.30	-96	-30.0	0.032	-139	0.43	-65	2.51
1.00	0.12	21	14.1	5.09	-85	-28.5	0.038	-158	0.42	-49	2.28
1.20	0.08	-54	12.5	4.22	-59	-25.2	0.055	153	0.34	-18	2.01
1.40	0.10	-103	9.3	2.93	-112	-23.1	0.070	114	0.24	-4	2.36
1.60	0.22	-44	6.7	2.16	-163	-23.3	0.068	125	0.24	-7	3.07
1.80	0.29	-20	5.8	1.96	145	-23.7	0.065	124	0.24	-37	3.41
2.00	0.30	-60	5.3	1.85	89	-23.3	0.069	120	0.23	-65	3.41
2.20	0.26	-92	4.9	1.75	29	-22.2	0.078	117	0.21	-83	3.31
2.40	0.24	-110	3.9	1.57	2	-21.7	0.082	116	0.23	-95	3.48
2.50	0.23	-113	3.5	1.50	10	-20.9	0.090	115	0.25	-100	3.35

Detailed Description

The MAX2630–MAX2633 are broadband amplifiers with 3dB bandwidth greater than 1GHz. Their small size and internal bias circuitry make them ideal for applications where board space is limited. The MAX2632/MAX2633 have a user-selectable bias current that allows the user to set both gain and output power for a particular application, and the MAX2631/MAX2633 incorporate shutdown capability.

Applications Information

External Components

The MAX2630–MAX2633 are easy to use, as shown in the *Typical Operating Circuit* and Figures 1, 2 and 3. Input and output series capacitors may be necessary to block DC bias voltages generated by the amplifiers from interacting with adjacent circuitry. These capacitors must be large enough to contribute negligible reactance in a 50Ω system at the minimum operating frequency. Use the following equation to calculate their minimum value:

$$C_{BLOCK} = \frac{53{,}000}{f} \text{ (pF)}$$

where f (in megahertz) is the minimum operating frequency.

The V_{CC} pin must be RF bypassed for correct operation. To accomplish this, connect a capacitor between the V_{CC} pin and ground, as close to the package as is practical. Use the same equation given above (for DC-blocking capacitor values) to calculate the minimum capacitor value. If the PC board has long V_{CC} lines, additional bypassing may be necessary. This can be done farther away from the package, if needed.

Proper grounding of the GND pin is essential. If the PC board uses a topside RF ground, connect it directly to the GND pin. For a board where the ground plane is not on the component side, the best technique is to connect the GND pin to it with a plated through-hole close to the package.

An on-chip buffer at the MAX2631/MAX2633's $\overline{SHDN}$ pin makes bypassing this pin unnecessary except in very noisy applications. When RF filtering is needed, use a bypass capacitor similar to the one used on V_{CC}. Since negligible current flows into this pin, additional RF filtering may be done with a series resistor.

To set the MAX2632/MAX2633's supply current, connect a resistor from the BIAS pin to ground. To estimate the value of this resistor, refer to the graph Supply Current vs. R_{BIAS} in the *Typical Operating Characteristics*.

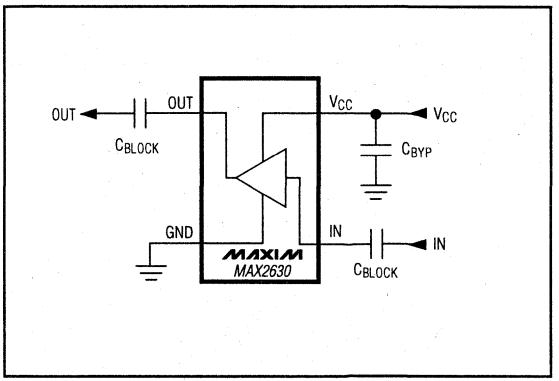


Figure 1. MAX2630 Typical Operating Circuit

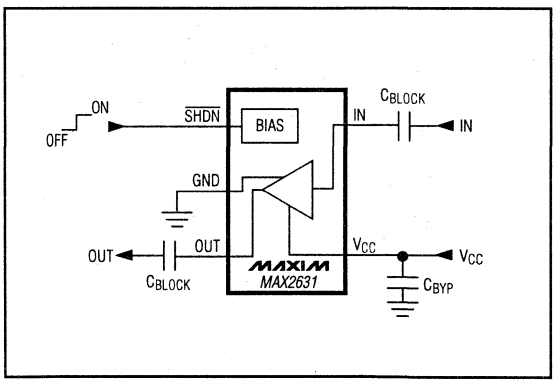


Figure 2. MAX2631 Typical Operating Circuit

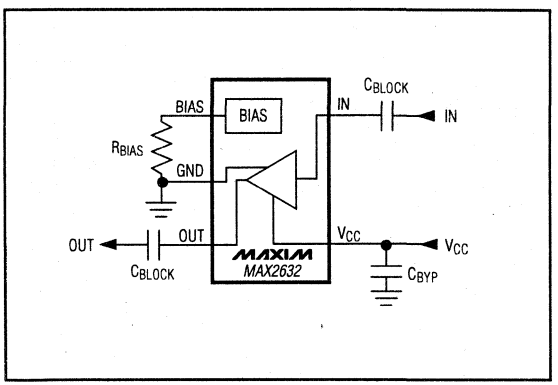


Figure 3. MAX2632 Typical Operating Circuit

VHF-to-Microwave, +3V, General-Purpose Amplifiers

PC Board Layout Example

Example PC board layouts are given in Figures 4 to 7. They use FR-4 with a 31mil layer thickness between the RF lines and the ground plane. The boards satisfy all of the above recommendations.

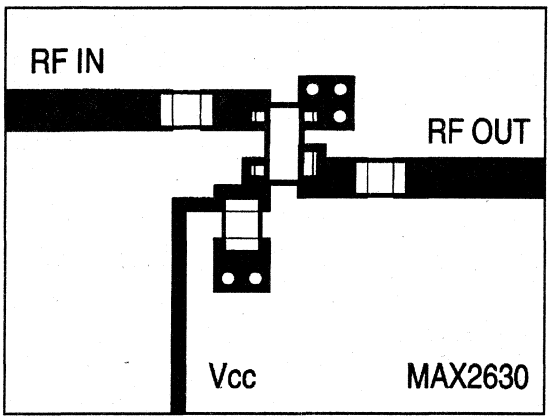


Figure 4. MAX2630 Example PC Board Layout

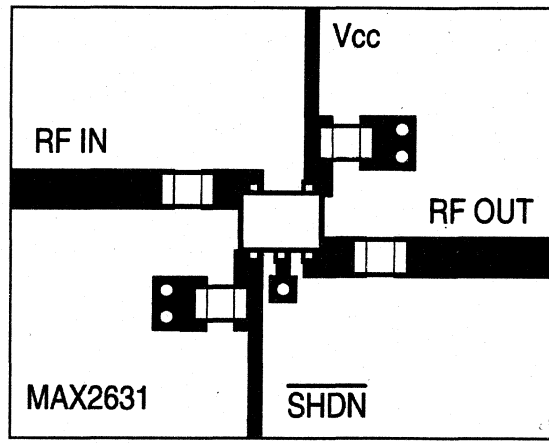


Figure 5. MAX2631 Example PC Board Layout

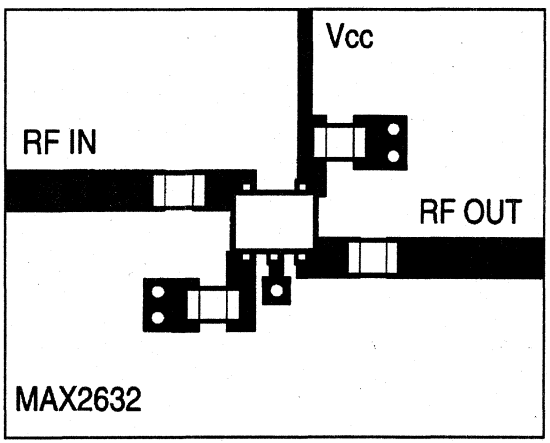


Figure 6. MAX2632 Example PC Board Layout

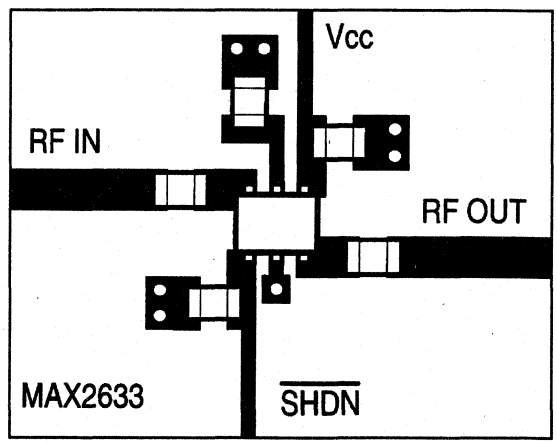
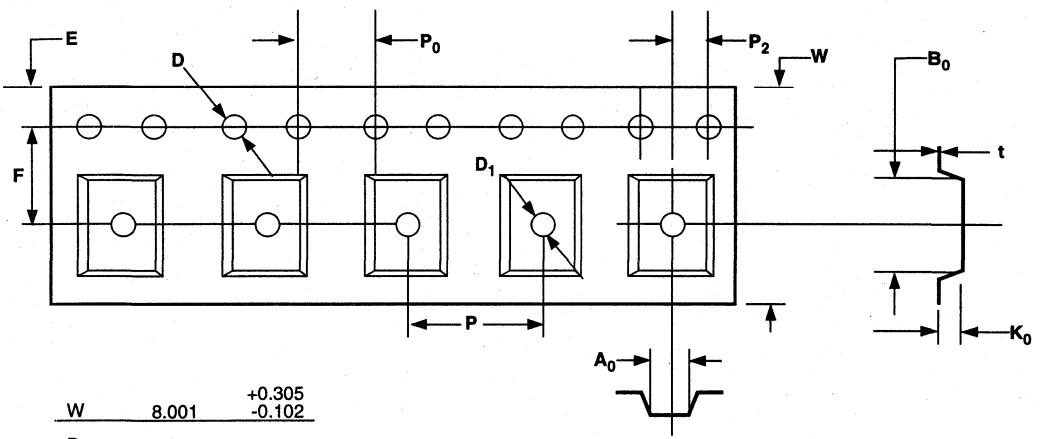


Figure 7. MAX2633 Example PC Board Layout

Chip Information

TRANSISTOR COUNT: 199

Tape-and-Reel Information



W	8.001	+0.305 -0.102
P	3.988	±0.102
E	1.753	±0.102
F	3.505	±0.051
D	1.499	+0.102 +0.000
D_1	0.991	+0.254 +0.000
P_0	3.988	±0.102
$P_0$10	40.005	±0.203
P_2	2.007	±0.051
A0	3.200	±0.102
B0	3.099	±0.102
K0	1.397	±0.102
t	0.254	±0.127

NOTE: DIMENSIONS ARE IN MM. AND FOLLOW EIA481-1 STANDARD.

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
8/97

MAXIM

Low-Noise, 2.5GHz Upconverter Mixer

General Description

The MAX2662 is a low-cost, low-noise upconverter designed for low-voltage operation. Ideal for battery-powered applications, this device operates with IF input frequencies between 10MHz and 500MHz, and upconverts to carrier frequencies as high as 2.5GHz.

A shutdown mode reduces the supply current to less than 1µA. The MAX2662 comes in a space-saving, 6-pin SOT23 package.

Features

- ♦ **Improved Performance over NEC8106/NEC8109**
- ♦ **Low Cost**
- ♦ **+2.7V to +5.5V Supply Voltage**
- ♦ **Wideband Operation**
- ♦ **Low Current Consumption**
- ♦ **High Output Intercept Point**
- ♦ **<1µA Shutdown Mode**
- ♦ **Ultra-Small, 6-Pin SOT23 Package**

Applications

2.4GHz Industrial Scientific Medical (ISM)

900MHz ISM

Hand-Held Radios

Wireless Local Area Network

Personal Communications Systems

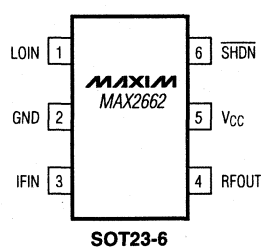
Cellular and Cordless Phones

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2662EUT-T	-40°C to +85°C	6 SOT23-6

Pin Configuration

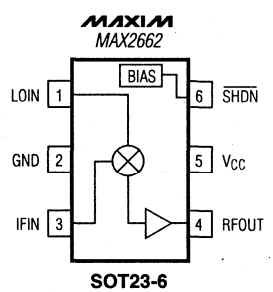
TOP VIEW



SOT23-6

Functional Diagram

TOP VIEW



SOT23-6

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For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800.
For small orders, phone 408-737-7600 ext. 3468.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

8/97

MAXIM

Low-Noise, 2.5GHz Downconverter Mixer

General Description

The MAX2690 is a miniature, low-noise, low-power downconverter mixer designed for use in portable consumer equipment. Signals at the RF input port are mixed with signals at the local-oscillator (LO) port using a double-balanced mixer. The RF port frequency range is 400MHz to 2500MHz. The LO port frequency range is 700MHz to 2500MHz. The IF frequency range is 10MHz to 500MHz, provided the LO and RF frequencies are chosen appropriately.

The IF port is differential, which provides good linearity and low LO emissions, and provides compatibility with applications using differential IF filters, such as CDMA cellular phones. The mixer noise figure is 10dB.

The MAX2690 draws 16mA at V_{CC} = 3V and operates from a +2.7V to +5.5V supply. A logic-controlled shutdown mode reduces the supply current to less than 1µA, making it ideal for battery-operated equipment. This device is offered in a miniature 10-pin µMAX package.

Features

- **7.6dBm Input Third-Order Intercept Point**
- **10dB Downconverter Mixer Noise Figure**
- **7.7dB Gain**
- **400MHz to 2500MHz Wideband Operation**
- **Low Cost**
- **+2.7V to +5.5V Single-Supply Operation**
- **1µA Shutdown Mode**
- **Ultra-Small 10-Pin µMAX Package**

Applications

2.45GHz Industrial-Scientific-Medical (ISM) Band Radios

Wireless Local Area Networks (WLANs)

Personal Communications Systems (PCS)

Code-Division Multiple Access (CDMA)

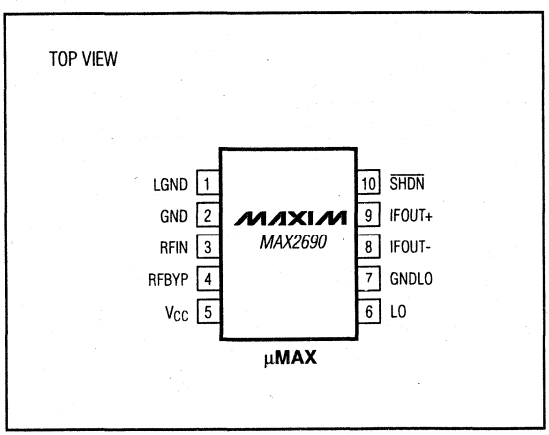
Cellular and Cordless Phones

Hand-Held Radios

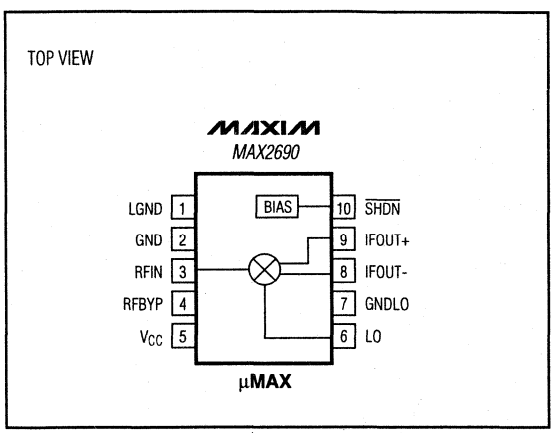
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX2690EUB	-40°C to +85°C	10 µMAX

Pin Configuration



Functional Diagram



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For free samples & the latest literature: http://www.maxim-ic.com, or phone 1-800-998-8800. For small orders, phone 408-737-7600 ext. 3468.

Fiber/Cable Products

Fiber/Cable Products, Product Table.....11-2

MAX3675 622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier.....11-5
MAX3680 +3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs 11-19
MAX3691 +3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs.....11-27

Regulated Telecommunications

Part Number	Supply Voltage (V)	Analog Bandwidth (MHz)	Transimpedance (kΩ)	Input Noise (nA)	Supply Current (mA)	Pins-Package	EV Kit	Features	Applications
TRANSIMPEDANCE PREAMPLIFIERS									
MAX3664	+3.0 to +3.6	590	6	55	25	8-SO, 8-µMAX 8-Die	Yes	Single 3.3V supply, low power, -40°C to +85°C operation	622Mbps SDH/SONET

Part Number	Supply Voltage (V)	Input Data Rate (Mbps)	Output Data Rate (Mbps)	Supply Current (mA)	Clock and Data Inputs	Data Outputs and Synchronization Inputs	EV Kit	Features	Applications
DESERIALIZERS									
MAX3680	+3.0 to +3.6	622	77	50	Differential PECL	TTL	Yes	1:8 deserializer, single 3.3V supply, low power, -40°C to +85°C operation	622Mbps SDH/SONET
MAX3681	+3.0 to +3.6	622	155	80	Differential PECL	LVDS	Yes	1:4 deserializer, single 3.3V supply, low power, LVDS outputs, -40°C to +85°C operation	622Mbps SDH/SONET

Part Number	Supply Voltage (V)	Input Data Rate (Mbps)	Output Data Rate (Mbps)	Supply Current (mA)	Clock and Data Inputs	Data Output	EV Kit	Features	Applications
SERIALIZERS									
MAX3691	+3.0 to +3.6	155	622	65	LVDS	Differential PECL	Yes	4:1 serializer, single 3.3V supply, low power, LVDS inputs, -40°C to +85°C operation	622Mbps SDH/SONET

Part Number	Supply Voltage (V)	Data Rate (Mbps)	I/O Levels	Bellcore Jitter Tolerance	Pins-Package	Features	Applications
CLOCK-RECOVERY AND DATA-RETIMING ICs							
MAX3270	+5 & -5	155 or 622	ECL	Surpasses specification	44-MQFP	Selectable data rate, fully integrated PLL, no external reference clock required	622Mbps SDH/SONET, 155Mbps SDH/SONET
MAX3675	+3.0 to +5.5	622	PECL	Surpasses specification	32-TQFP	Single +3.3V supply, includes limiting postamp, -40°C to +85°C	622Mbps SDH/SONET

Local-Area Network and Data Communications Products

Part Number	Supply Voltage (V)	Analog Bandwidth (GHz)	Trans-impedance (Ω)	Max Input (µA)	Input Noise (nA)	Pins-Package	Features	Applications
TRANSIMPEDANCE PREAMPLIFIERS								
MAX3260	+5	1.0	2000	900	240	Die only	Single supply, 25dB dynamic range, optimized for TO header	Fibre Channel, 622Mbps ATM/SDH/SONET

Part Number	Supply Voltage (V)	Input Sensitivity (mV)	Min LOS Sensitivity (mV)	Edge Speed (ps)	Pins-Package	EV Kit	Features	Applications
LIMITING POSTAMPLIFIERS								
MAX3262	+5	6	5	250	24-SSOP		900MHz bandwidth, programmable LOS threshold, single supply	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet
MAX3761	+5	4	3.2	250	20-QSOP	Yes	Chatter-free power detector, TTL LOS interface	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet
MAX3762	+5	4	3.2	250	20-QSOP	Yes	Chatter-free power detector, PECL LOS interface	Fibre Channel, 622Mbps ATM/SDH/SONET, 1Gbps Ethernet

Part Number	Supply Voltage (V)	Data Rate (Mbps)	Max Modulation Current (mA)	Max Bias Current (mA)	Pins-Package	EV Kit	Features	Applications
LASER DIODE DRIVERS								
MAX3261	+5	1250	30	60	32-TQFP	Yes	Automatic power control, single supply, temperature-compensated reference voltage	Fibre Channel, 622Mbps ATM/SDH/SONET
MAX3263	+5	155	25	60	24-SSOP		Automatic power control, single supply, temperature-compensated reference voltage	155Mbps ATM/SDH/SONET

19-1258; Rev 0a; 7/97

EVALUATION KIT AVAILABLE

MAXIM

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

General Description

The MAX3675 is a complete clock-recovery and data-retiming IC incorporating a limiting amplifier. It is intended for 622Mbps SDH/SONET applications and operates from a single +3.3V supply.

The MAX3675 has two differential input amplifiers: one accepts PECL levels, while the other accepts small-signal analog levels. The analog inputs access the limiting amplifier stage, which provides both a received-signal-strength indicator (RSSI) and a programmable-threshold loss-of-power (LOP) monitor. Selecting the PECL amplifier disables the limiting amplifier, conserving power. A loss-of-lock (LOL) monitor is also incorporated as part of the fully integrated PLL.

Features

- ♦ **Single +3.3V or +5.0V Power Supply**
- ♦ **Complies with ANSI, ITU, and Bellcore SDH/SONET Specifications**
- ♦ **Low Power: 215mW at +3.3V**
- ♦ **Selectable Data Inputs, Differential PECL or Analog**
- ♦ **Received-Signal-Strength Indicator (RSSI)**
- ♦ **Loss-of-Power and Loss-of-Lock Monitors**
- ♦ **Differential PECL Clock and Data Outputs**
- ♦ **No External Reference Clock Required**

Applications

SDH/SONET Transmission Systems

SDH/SONET Access Nodes

Add/Drop Multiplexers

ATM Switches

Digital Cross-Connects

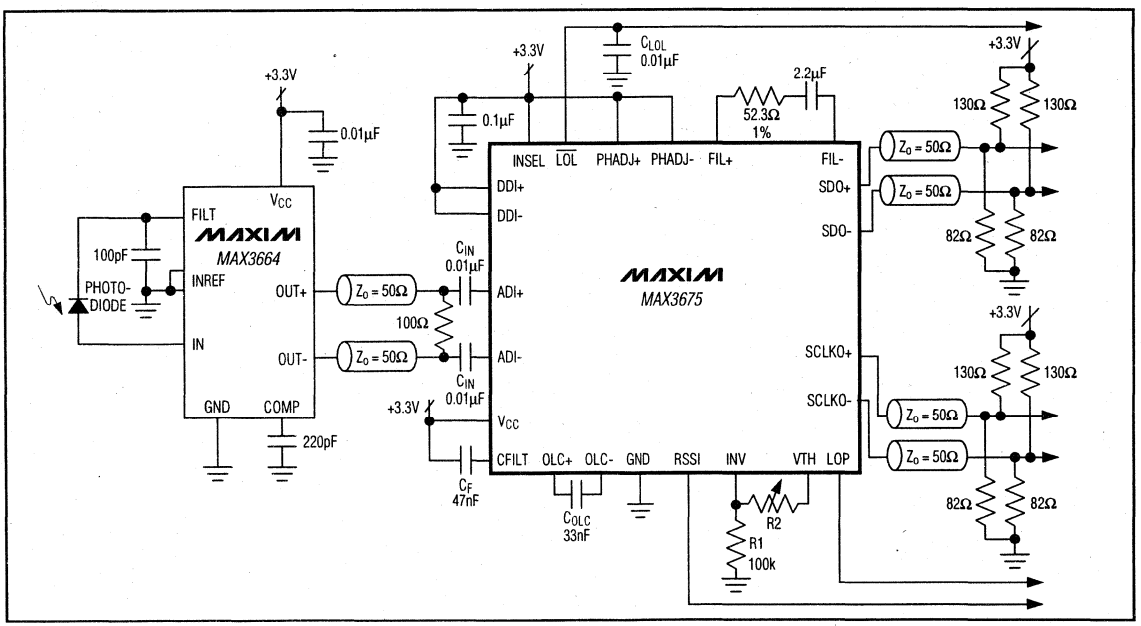
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3675ECJ	-40°C to +85°C	32 TQFP
MAX3675E/D	-40°C to +85°C	Dice*

*Contact factory for availability. Dice are designed to operate from -40°C to +85°C, but are tested and guaranteed only at T_j = +45°C.

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC} ..... -0.5V to 6.5V
Input Voltage Levels,
DDI+, DDI-, ADI+, ADI- ..... -0.5V to (V_{CC} + 0.5V)
Input Differential Voltage (ADI+) - (ADI-) ..... ±3V
PECL Output Currents, SDO+, SDO-, SCLKO+, SCLKO- ... 100mA
LOL, LOP, INSEL, PHADJ+, PHADJ- ..... -0.5V to (V_{CC} + 0.5V)
FIL+, FIL-, OLC+, OLC-, RSSI, VTH ..... -0.5V to (V_{CC} + 0.5V)
(OLC+) - (OLC-) ..... ±3V
(FIL+) - (FIL-) ..... ±700mV
CFILT ..... (V_{CC} - 2.5V) to (V_{CC} + 0.5V)
INV ..... -0.5V to 2.0V
Continuous Power Dissipation (T_A = +85°C)
TQFP (derate 11.1mW/°C above +85°C) 721mW
Operating Junction Temperature Range ..... -40°C to +150°C
Storage Temperature Range ..... -65°C to +160°C
Processing Temperature (die) ..... +400°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	MAX3675ECJ, PECL outputs unterminated	INSEL = V_{CC}		65	90	mA
			INSEL = GND		47	65	
PECL Input High Voltage	V_{IH}			V_{CC} - 1.16		V_{CC} - 0.88	V
PECL Input Low Voltage	V_{IL}			V_{CC} - 1.81		V_{CC} - 1.48	V
PECL Input High Current	I_{IH}			-10		10	µA
PECL Input Low Current	I_{IL}			-10		10	µA
PECL Output High Voltage	V_{OH}			V_{CC} - 1.03		V_{CC} - 0.88	V
PECL Output Low Voltage	V_{OL}			V_{CC} - 1.81		V_{CC} - 1.620	V
LOP, LOL High Voltage	V_{OH}			2.4			V
LOP Low Voltage	V_{OL}			0.1		0.4	V
LOL Low Voltage	V_{OL}	C_{LOL} = 0.01µF			0.44		V
ADI+, ADI- Input Bias Voltage				V_{CC} - 0.7	V_{CC} - 0.6	V_{CC} - 0.5	V
RSSI Output Voltage		ADI+, ADI- open			1.22		V
		(ADI+) - (ADI-) = 20mVp-p		2.00	2.12	2.30	
		(ADI+) - (ADI-) = 80mVp-p		2.38	2.51	2.70	
Op-Amp Input Bias Current		1MΩ between INV and VTH		-100		+100	nA
INV Input Bias Voltage		1MΩ between INV and VTH		1.10	1.18	1.30	V

Note 1: Dice are tested at T_j = +45°C, V_{CC} = +4.25V
Note 2: At T_A = -40°C, DC characteristics are guaranteed by design and characterization.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +5.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V and T_A = +25°C.) (Notes 3, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Input Voltage Range	V_{ID}	BER < 10^{-10}, ADI inputs (Note 5)		0.003		1.2000	Vp-p
Input Referred Noise	V_N	ADI inputs			100		µV
Power-Detect Hysteresis		$V_{RELEASE}$ = 3.6mVp-p (Note 6)		2	3	5	dB
Limiting Amplifier Small-Signal Bandwidth	BW	(Note 7)			800		MHz
RSSI Output Voltage		(ADI+) - (ADI-) = 2mVp-p			1.36		V
		(ADI+) - (ADI-) = 20mVp-p			1.93		
Threshold Voltage	V_{TH}	$V_{RELEASE}$ = 3.6mVp-p			1.40		V
RSSI Linearity		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p			±0.7		%
RSSI Slope		(ADI+) - (ADI-) = 2mVp-p to 50mVp-p (Note 8)			29		mV/dB
Loop Bandwidth		C_F = 2.2µF, R_F = 52.3Ω			350		kHz
		C_F = 0.022µF, R_F = 523Ω			3.5		MHz
Jitter Generation (Note 9)		C_F = 2.2µF, R_F = 52.3Ω			13		mUI
		C_F = 0.022µF, R_F = 523Ω			6		
Jitter-Transfer Peaking		R_F = 52.3Ω, C_F = 2.2µF				0.08	dB
Jitter Tolerance (Note 9)		R_F = 52.3Ω, C_F = 2.2µF	f = 10kHz		8		UI
			f = 25kHz	1.50	3.35		
			f = 250kHz	0.25	0.60		
			f = 1MHz	0.20	0.50		
Maximum Consecutive Input Run Length (1 or 0)					1000		Bits
Serial Clock-to-Q Delay	t_{CLK-Q}			195	275	370	ps
Serial Clock Frequency	f_{SCLK}				622.08		MHz

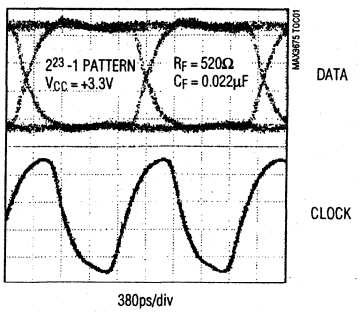
Note 3: AC parameters are guaranteed by design and characterization.
Note 4: The MAX3675 is characterized with a PRBS of 2^{23} - 1 maintaining a BER of ≤ 10^{-10} having a confidence level of 99.9%.
Note 5: A lower minimum input voltage of 2mVp-p is achievable; however, the LOP hysteresis is not guaranteed below 3.6mVp-p.
Note 6: Hysteresis = 20log($V_{RELEASE}$ / V_{ASSERT})
Note 7: Small-signal bandwidth cannot be measured directly.
Note 8: RSSI slope = [V_{RSSI2} - V_{RSSI1}] / [20log (V_{ID2} / V_{ID1})]
Note 9: 1UI = 1 unit interval = (622.08MHz)$^{-1}$ = 1.608ns

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

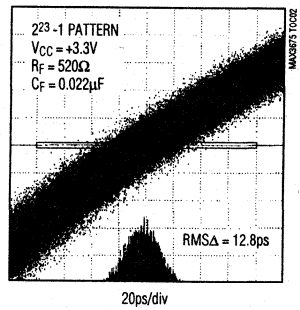
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

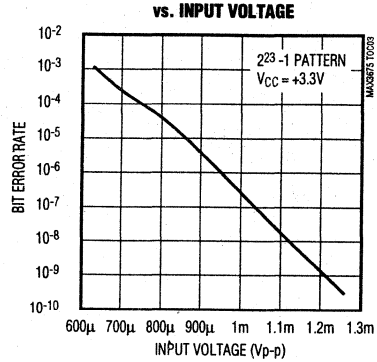
RECOVERED DATA AND CLOCK (SINGLE ENDED)



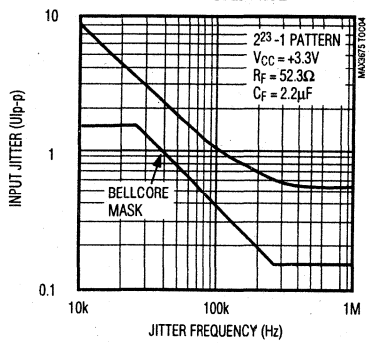
RECOVERED CLOCK JITTER



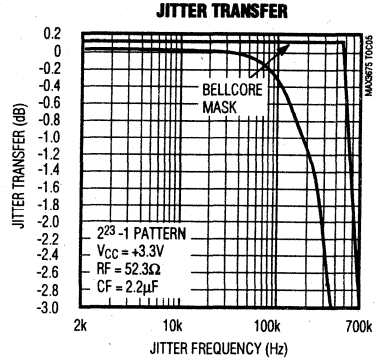
BIT ERROR RATE vs. INPUT VOLTAGE



JITTER TOLERANCE



JITTER TRANSFER

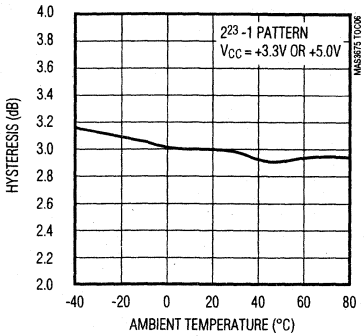


622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

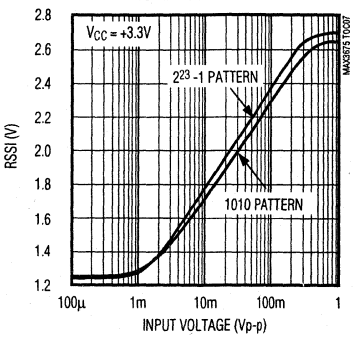
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

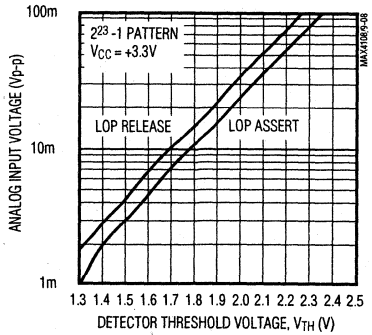
LOSS-OF-POWER HYSTERESIS vs. TEMPERATURE



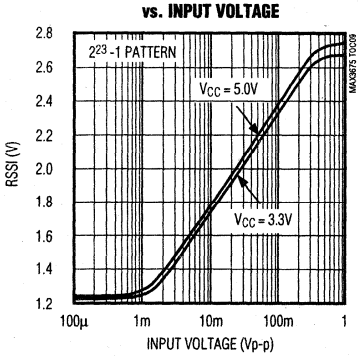
RECEIVED-SIGNAL-STRENTH INDICATOR vs. INPUT VOLTAGE



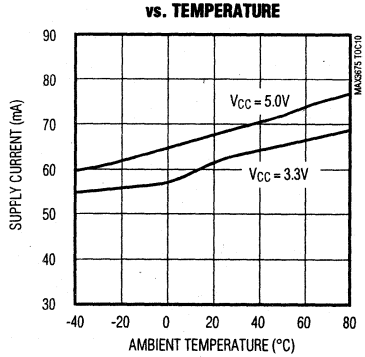
LOSS-OF-POWER ASSERT AND RELEASE LEVEL vs. THRESHOLD VOLTAGE



RECEIVED-SIGNAL-STRENGTH INDICATOR vs. INPUT VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



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622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Pin Description

PIN	NAME	FUNCTION
1	OLC+	Positive Offset-Correction Loop Capacitor Input
2	OLC-	Negative Offset-Correction Loop Capacitor Input
3	RSSI	Received-Signal-Strength Indicator Output
4, 8, 16, 24, 25	GND	Supply Ground
5	INV	Op-Amp Inverting Input. Attach to ground if op amp is not used.
6	VTH	Voltage Threshold Input. Threshold voltage for loss-of-power monitor. Attach to V_{CC} if LOP function is not used.
7	LOP	Loss-of-Power Output, TTL. Limiting amplifier loss-of-power monitor. Asserts high when input signal is below threshold set by VTH.
9, 12, 15, 18, 21, 31	V_{CC}	Positive Supply Voltage
10	SCLKO-	Negative Serial Clock Output, PECL, 622.08MHz. SDO- is clocked out on the falling edge of SCLKO-.
11	SCLKO+	Positive Serial Clock Output, PECL, 622.08MHz. SDO+ is clocked out on the rising edge of SCLKO+.
13	SDO-	Negative Serial Data Output, PECL, 622.08Mbps
14	SDO+	Positive Serial Data Output, PECL, 622.08Mbps
17	$\overline{LOL}$	Loss-of-Lock Output, TTL. PLL loss-of-lock monitor, active low (see *Design Procedure*).
19	PHADJ-	Negative Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
20	PHADJ+	Positive Phase-Adjust Input. Used to optimally align internal PLL phase. Attach to V_{CC} if not used.
22	FIL-	Negative Filter Input. PLL loop filter connection.
23	FIL+	Positive Filter Input. PLL loop filter connection.
26	DDI+	Positive Digital Data Input, PECL, 622.08Mbps serial-data stream
27	DDI-	Negative Digital Data Input, PECL, 622.08Mbps serial-data stream
28	INSEL	Input Select. Connect to GND to select digital data inputs or V_{CC} for analog data inputs.
29	ADI-	Negative Analog Data Input, 622.08Mbps serial-data stream
30	ADI+	Positive Analog Data Input, 622.08Mbps serial-data stream
32	CFILT	RSSI Filter Capacitor Input

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

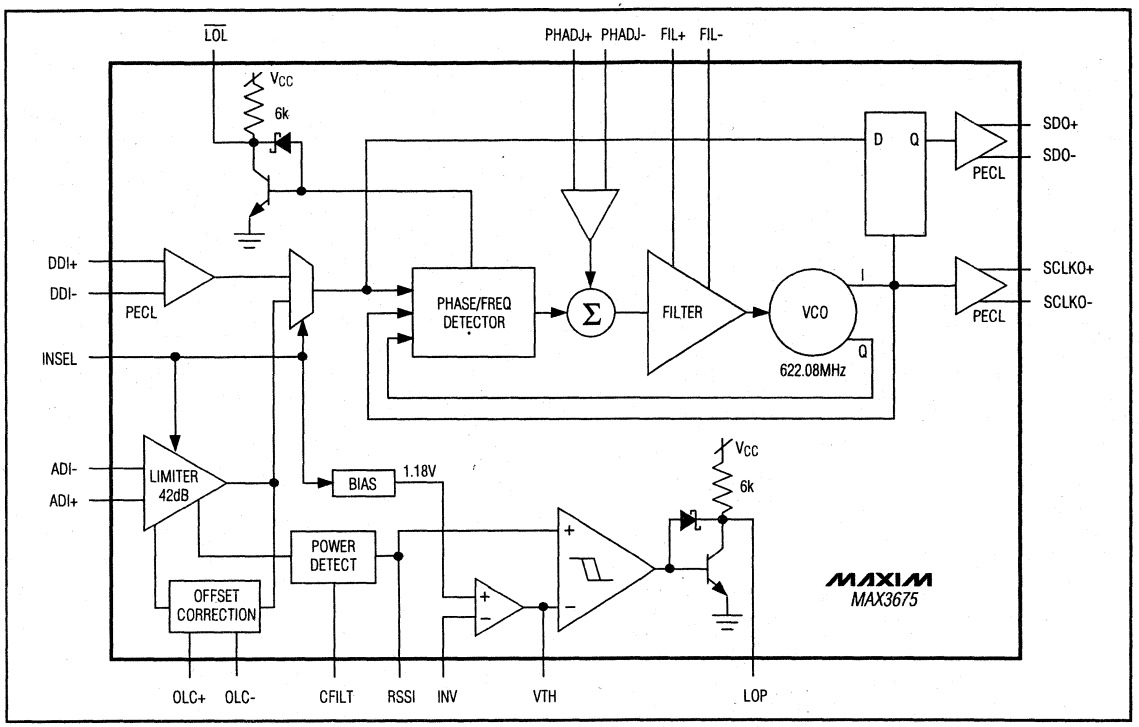


Figure 1. Functional Diagram

Detailed Description

The block diagram in Figure 1 shows the MAX3675's architecture. It consists of a limiting amplifier input stage followed by a fully integrated clock/data-recovery (CDR) block implemented with a phase-locked loop (PLL). The input stage is selectable between a limiting amplifier or a simple PECL input buffer. The limiting amplifier provides a loss-of-power (LOP) monitor and a received-signal-strength indicator (RSSI). The PLL consists of a phase/frequency detector (PFD), a loop filter amplifier, and a voltage-controlled oscillator (VCO).

Limiting Amplifier

The MAX3675's on-chip limiting amplifier accepts an input signal level from 3.0mVp-p to 1.2Vp-p. The amplifier consists of a cascade of gain stages that include full-wave logarithmic detectors. The combined small-signal gain is approximately 42dB, and the -3dB bandwidth is 800MHz. Input-referred noise is less than 100µVRMS, providing excellent sensitivity for small-amplitude data streams.

In addition to driving the CDR, the limiting amplifier provides both an RSSI output and an LOP monitor that allow the user to program the threshold voltage. The RSSI circuitry provides an output voltage that is linearly proportional to the input power (in decibels) detected between the ADI+ and ADI- input pins and is sensitive enough to reliably detect signals as small as 2mVp-p.

Input DC offset reduces the accuracy of the power detector; therefore, an integrated feedback loop is included that automatically nulls the input offset of the gain stage. The addition of this offset-correction loop requires that the input signal be AC coupled when using the ADI+ and ADI- inputs.

Finally, for applications that do not require the limiting amplifier, selecting the digital inputs conserves power by turning off the post-amplifier block.

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Phase Detector

The phase detector produces a voltage proportional to the phase difference between the incoming data and the internal clock. Because of its feedback nature, the PLL drives the error voltage to zero, aligning the recovered clock to the incoming data. The external phase adjustment pins (PHADJ+, PHADJ-) allow the user to vary the internal phase alignment.

Frequency Detector

A frequency detector incorporated into the PLL aids frequency acquisition during start-up conditions. The input data stream is sampled by quadrature components of the VCO clock, generating a difference frequency. Depending on the polarity of the difference frequency, the PFD drives the VCO so that the difference frequency is reduced to zero. Once frequency acquisition is obtained, the frequency detector returns to a neutral state.

Loop Filter and VCO

The VCO is fully integrated, while the loop filter requires an external R-C network. This filter network determines the bandwidth and peaking of the second-order PLL.

Design Procedure

Received-Signal-Strength Indicator (RSSI)

The RSSI output voltage is insensitive to temperature and supply fluctuations. The power detector functions as a broadband power meter that detects the total RMS power of all signals within the detector bandwidth (including input signal noise). The RSSI voltage varies linearly (in decibels) for inputs of 2mVp-p to 50mVp-p. The slope over this input range is approximately 29mV/dB.

The high-speed RSSI signal is filtered to an RMS level with one external capacitor tied from CFILT to V_{CC}. The impedance looking into CFILT is about 500Ω to V_{CC}. As a result, the lower -3dB cutoff frequency is set by the following simple relationship:

$$f_{FILT} = 1 / \left[2\pi(500)C_F\right]$$

For 622Mbps applications, Maxim recommends a cutoff frequency of 6.8kHz, which requires C_F = 47nF. The RSSI output is designed to drive a minimum load resistance of 10kΩ to ground and a maximum of 20pF. Loads greater than 20pF must be buffered by a series resistance of 10kΩ (i.e., voltmeter).

Input Offset Correction

The on-chip limiting amplifier provides more than 42dB of gain. A low-frequency feedback loop is integrated into the MAX3675 to remove the input offset. DC coupling to the ADI+ and ADI- inputs is not allowed, as this would prevent the proper functioning of the DC offset-correction circuitry.

The differential input impedance (Z_{IN}) is approximately 2.5kΩ. The impedance between OLC+ and OLC- (Z_{OLC}) is approximately 120kΩ. Take care when setting the combined low-frequency cutoff (f_{CUTOFF}), due to the input DC-blocking capacitor (C_{IN}) and the offset correction loop capacitor (C_{OLC}). Refer to Table 1 for selecting the values of C_{IN} and C_{OLC}.

These values ensure that the poles associated with C_{IN} and C_{OLC} work together to provide a flat response at the lower -3dB corner frequency (no gain peaking).

C_{IN} must be a low-TC, high-quality capacitor of type X7R or better in order to minimize f_{CUTOFF} deviations. C_{OLC} must be a capacitor of type Z5U or better.

Loss-of-Power (LOP) Monitor

A LOP monitor with a user-programmable threshold and a hysteresis comparator is also included with the limiting amplifier circuitry. Internally, one comparator input is tied to the RSSI output signal, and the other is tied to the threshold voltage (V_{TH}), which is set externally and provides a trip point for the LOP indication. A low-voltage, low-drift op amp, referenced to an internal bandgap voltage (1.18V), is supplied for programming a supply-independent threshold voltage. This op amp requires two external resistors to program the LOP trip point. V_{TH} is programmable from 1.18V to 2.4V using the equation:

$$V_{TH} = 1.18(1 + R2 / R1)$$

The op amp can source only 20µA of current. Therefore, an R1 value greater than or equal to 100kΩ is recommended for proper operation. The input bias

Table 1. Setting the Low-Frequency Cutoff

C_{IN}	C_{OLC}	COMBINED LOW f_{CUTOFF} (kHz)
0.022µF	0.047µF	3.0
0.010µF	0.033µF	6.8
6800pF	0.022µF	10
4700pF	0.010µF	13.5
2200pF	4700pF	29
1000pF	3300pF	68
470pF	1000pF	135
330pF	680pF	190
220pF	470pF	290

current of the op amp at the INV pin is guaranteed to be less than ±100nA. To set the threshold voltage externally (i.e., via a DAC control), completely disable the op amp by grounding the inverting terminal (INV). V_{TH} then becomes high impedance and must be driven externally.

The comparator is configured with an active-high LOP output. An on-chip, 6kΩ pull-up resistor is provided to reduce external part count.

Setting the Loop Filter

The loop filter within the PLL consists of a transconductance amplifier and external filter elements R_F and C_F (Figure 2). The closed-loop bandwidth of a PLL is approximated by:

$$K_D\ K_O\ Gm\ R_F$$

where K_D is the gain of the phase detector, K_O is the gain of the VCO, and Gm is the transconductance of the filter amplifier. For the MAX3675, an estimated value of $K_D K_O Gm$ is 7k.

Because the PLL is a second-order system, a zero in the open-loop gain is required for stability. This zero is set by the following equation:

$$\omega_Z = 1 / (R_F C_F)$$

where the recommended external value of C_F is 2.2µF.

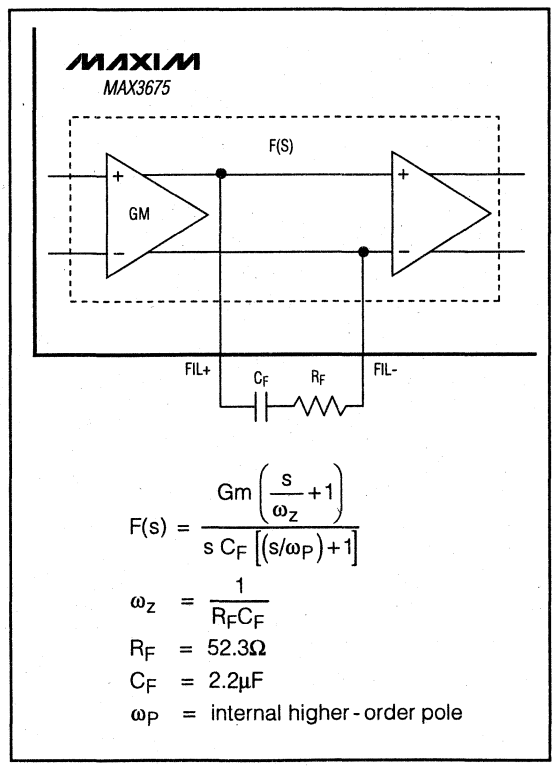
Increasing the value of R_F increases the PLL bandwidth (f_{LOOP}). Increasing this bandwidth improves jitter tolerance and jitter-generation performance, but also reduces jitter-transfer performance. (Decreasing the bandwidth has the opposite effect.)

This type of PLL is a classical second-order system. Therefore, as f_Z (the frequency of the zero) approaches f_{LOOP}, the jitter-transfer peaking increases. For an overdamped system (f_Z/f_{LOOP}) < 0.25, the jitter peaking of a second-order system can be approximated by:

$$Mp = 1 - (f_Z / f_{LOOP})$$

where Mp is the magnitude of the peaking. For (f_Z/f_{LOOP}) < 0.1, this equation holds to within 10%.

C_F can be made smaller if meeting the jitter-transfer specifications is not a requirement. For example, setting R_F to 300Ω and C_F to 3.3nF increases the loop bandwidth to approximately 2.2MHz (Figure 3). Loop stability is ensured by maintaining a separation of 10x between f_{LOOP} and f_Z. Be careful when changing the value of R_F. Lower values of R_F are limited by the internal resistance of the IC, and upper values are limited by the internal high-frequency pole.



$$F(s) = \frac{Gm\left(\frac{s}{\omega_Z}+1\right)}{s\,C_F\left[\left(s/\omega_P\right)+1\right]}$$

$$\omega_Z = \frac{1}{R_F C_F}$$

R_F = 52.3Ω

C_F = 2.2µF

ω_P = internal higher-order pole

Figure 2. Loop Filter

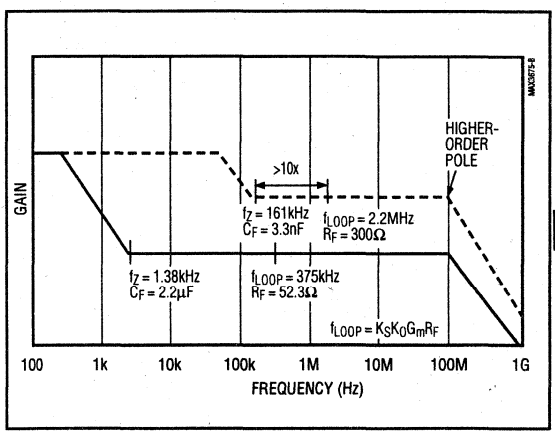


Figure 3. Loop-Filter Response

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

The MAX3675 is optimally designed to acquire lock and to provide a bit-error rate (BER) of less than 10^{-10} for long strings of consecutive zeros and ones. Using the recommended external component values of R_F = 52.3Ω ±1% and C_F = 2.2µF ±20%, measured results show that the MAX3675 can tolerate 1000 consecutive ones or zeros. It is important to select a type of capacitor for C_F that has a temperature stability of ±10% or better. This ensures performance over the -40°C to +85°C temperature range.

Lock Detect

The MAX3675's loss-of-lock (LOL) monitor indicates when the PLL is locked. Under normal operation, the loop is locked and the $\overline{LOL}$ output signal is high. When the MAX3675 loses lock, a fast negative-edge transition occurs on $\overline{LOL}$. The output level remains at a low level (held by C_{LOL}) until the loop reacquires lock (Figure 4).

Note that the LOL monitor is only valid when a data stream is present on the inputs to the MAX3675. As a result, LOL does not detect a loss-of-power condition resulting from a loss of the incoming signal. See the *Loss-of-Power (LOP) Monitor* section for this type of indicator.

Input and Output Terminations

The MAX3675 digital data and clock I/Os (DDI+, DDI-, SDO+, SDO-, SCLK+, and SCLK-) are designed to interface with PECL signal levels. It is important to bias these ports appropriately. A circuit that provides a Thevenin equivalent of 50Ω to V_{CC} - 2V should be used with fixed-impedance transmission lines for proper termination. Make sure that the differential outputs have balanced loads.

The digital data input signals (DDI+ and DDI-) are differential inputs to an emitter-coupled pair. As a result, the MAX3675 can accept differential input signals as low as 250mV. These inputs can also be driven single-ended by externally biasing DDI- to the center of the voltage swing.

The MAX3675's performance can be greatly affected by circuit board layout and design. Use good high-frequency design techniques, including minimizing ground inductance and using fixed-impedance transmission lines on the data and clock signals. Power-supply decoupling should be placed as close to V_{CC} as possible. Take care to isolate the input from the output signals to reduce feedthrough.

Applications Information

Driving the Limiting Amplifier Single-Ended

There are three important requirements for driving the limiting amplifier from a single-ended source (Figure 5):

1) There must be no DC coupling to the ADI+ and ADI- inputs. DC levels at these inputs disrupt the offset-correction loop.
2) The terminating resistor R_T (50Ω) must be referenced to the ADI- input to minimize common-mode coupling problems.
3) The low-frequency cutoff for the limiting amplifier is determined by either C_{IN} and the 2.5kΩ input impedance or $C_b/2$ together with R_T. With C_b = 0.22µF and R_T = 50Ω, the low-frequency cutoff is 29kHz.

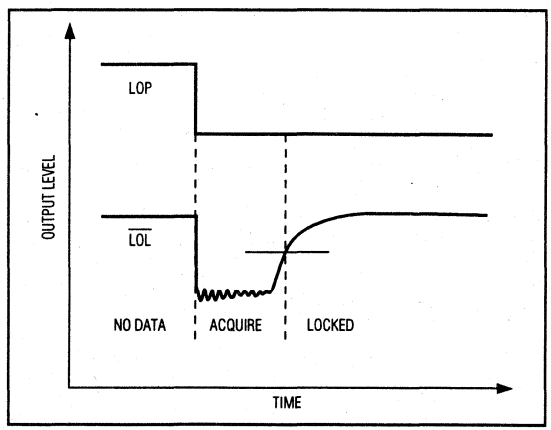


Figure 4. Loss-of-Lock Output

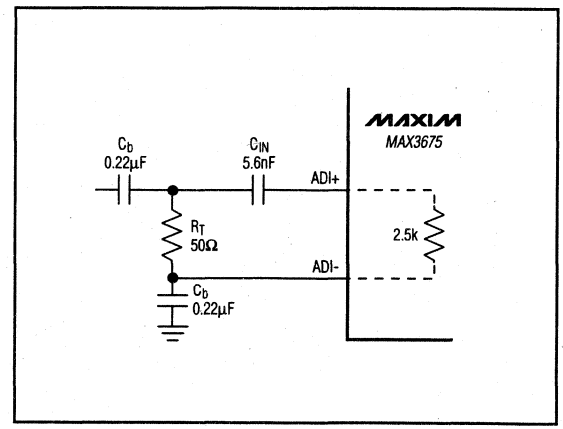


Figure 5. Single-Ended Input Termination

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Reduced Power Consumption Without the Limiting Amplifier

The limiting amplifier is biased independently from the clock recovery circuitry. Grounding INSEL turns off the limiting amplifier and selects the PECL DDI inputs.

Converting Average Optical Power to Signal Amplitude

Many of the MAX3675's specifications relate to input-signal amplitude. When working with fiber optic receivers, the input is usually expressed in terms of average optical power and extinction ratio. The relations given in Table 2 and Figure 6 are helpful for converting optical power to input signal when designing with the MAX3675.

In an optical receiver, the input voltage to the limiting amplifier can be found by multiplying the relationship in Table 2 by the photodiode responsivity and transimpedance amplifier gain.

Optical Hysteresis

Power and hysteresis are often expressed in decibels. By definition, decibels are always 10log (power). At the inputs to the MAX3675 limiting amplifier, the power is V_{IN}^2/R. If a receiver's optical input power (x) increases by a factor of two, and the preamplifier is linear, then the voltage at the input to the MAX3675 also increases by a factor of two.

The optical power increase is 10log(2x/x) = 10log(2) = +3dB.

At the MAX3675, the voltage increase is:

$$10\log\frac{(2V_{IN})^2/R}{V_{IN}^2/R} = 10\log(2^2) = 20\log(2) = +6dB$$

Table 2. Optical-Power Relations*

PARAMETER	SYMBOL	RELATION
Average Power	P_{AVE}	$P_{AVE} = (P0 + P1)/2$
Extinction Ratio	r_e	$r_e = P1 / P0$
Optical Power of a "1"	P1	$P1 = 2P_{AVE}\frac{r_e}{r_e+1}$
Optical Power of a "0"	P0	$P0 = 2P_{AVE}/(r_e+1)$
Signal Amplitude	P_{IN}	$P_{IN} = P1 - P0 = 2P_{AVE}\frac{(r_e-1)}{r_e+1}$

Assuming a 50% average input data duty cycle

In an optical receiver, the dB change at the MAX3675 always equals 2x the optical dB change.

The MAX3675's typical voltage hysteresis is 3.0dB. This provides an optical hysteresis of 1.5dB.

Jitter in Optical Receivers

Timing jitter, edge speeds, aberrations, optical dispersion, and attenuation all impact the performance of high-speed clock recovery for SDH/SONET receivers (Figure 7). These effects decrease the time available for error-free data recovery by reducing the received "eye opening" of non-return-to-zero (NRZ) transmitted signals.

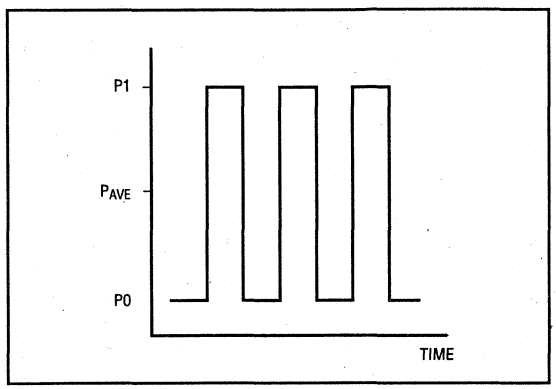


Figure 6. Optical Power Relations

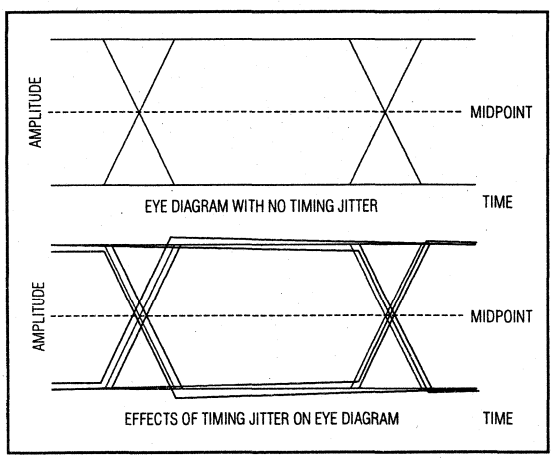


Figure 7. Eye Diagram With and Without Timing Jitter

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Optical receivers, incorporating transimpedance preamplifiers and limiting postamplifiers, can significantly clean up the effects of dispersion and attenuation. In addition, these amplifiers can provide fast transitions with minimal aberrations to the subsequent clock and data-recovery (CDR) blocks. However, these stages also add distortions to the midpoint crossing, contributing to timing jitter. Timing jitter is one of the most critical technical issues to consider when developing optical receivers and CDR circuits.

A better understanding of the different sources of jitter helps in the design and application of optical receiver modules and integrated CDR solutions. SDH/SONET specifications are well defined regarding the amount of jitter tolerance allowed at the inputs of optical receivers, as well as jitter peaking requirements, but they do little to define the different sources of jitter. The jitter that must be tolerated at an optical receiver input involves three significant sources, all of which are present in varying degrees in typical receiver systems:

1) Random jitter (RJ)
2) Pattern-dependent jitter (PDJ)
3) Pulse-width distortion (PWD)

Random Jitter (RJ)

RJ is caused by random noise present during edge transitions (Figure 8). This random noise results in random midpoint crossings. All electrical systems generate some random noise; however, the faster the speed of the transitions, the lower the effect of noise on random jitter. The following equation is a simple worst-case estimation of random jitter:

$$RJ\ (rms) = (rms\ noise) / (slew\ rate)$$

Pattern-Dependent Jitter (PDJ)

PDJ results from wide variations in the number of consecutive bits contained in NRZ data streams working against the bandwidth requirements of the receiver (Figure 9). The location of the lower -3dB cutoff frequency is important, and must be set to pass the low frequencies associated with long consecutive bit streams. AC coupling is common in optical receiver design.

When using a limiting preamplifier with a highpass frequency response, select the input AC-coupling capacitor, C_{IN}, to provide a low-frequency cutoff (f_C) one decade lower than the preamplifier low-frequency cutoff. As a result, the PDJ is dominated by the low-frequency cutoff of the preamplifier.

When using a preamplifier without a highpass response with the MAX3675, the following equation provides a good starting point for choosing C_{IN}:

$$C_{IN} \geq \frac{-t_L}{(1.25k\Omega)\ln\left[1-\frac{(PDJ)(BW)}{0.5}\right]}$$

where t_L = duration of the longest run of consecutive bits of the same value (seconds); PDJ = maximum

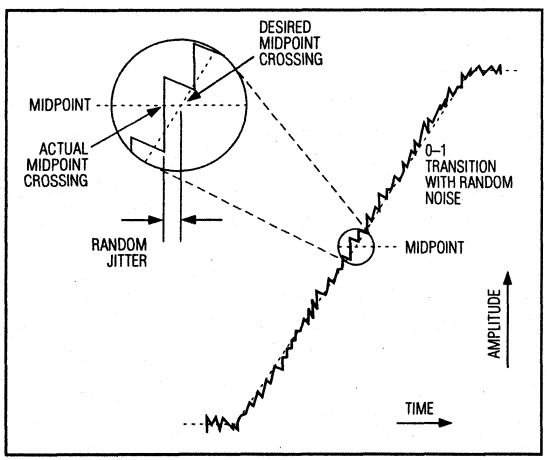


Figure 8. Random Jitter on Edge Transition

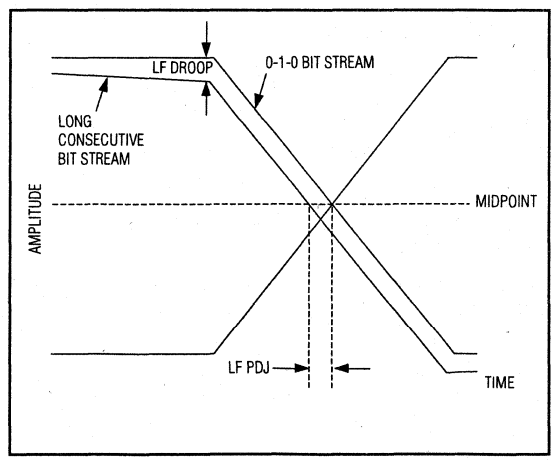


Figure 9. Pattern-Dependent Jitter Due to Low-Frequency Cutoff

allowable pattern-dependent jitter, peak-to-peak (seconds); and BW = typical system bandwidth, normally 0.6 to 1.0 times the data rate (Hertz). If the PDJ is still larger than desired, continue increasing the value of C_{IN}. Note that to maintain stability when using the MAX3675 analog inputs (ADI+, ADI-), it is important to keep the low-frequency cutoff associated with C_{OLC} below the corner frequency associated with C_{IN} (fc) (Table 1).

PDJ can also be present due to insufficient high-frequency bandwidth (Figure 10). If the amplifiers are not fast enough to allow for complete transitions during single-bit patterns, or if the amplifier does not allow adequate settling time, high-frequency PDJ can result.

Pulse-Width Distortion (PWD)

Finally, PWD occurs when the midpoint crossing of a 0–1 transition and a 1–0 transition do not occur at the same level (Figure 11). DC offsets and nonsymmetrical rising and falling edge speeds both contribute to PWD. For a 1–0 bit stream, calculate PWD as follows:

PWD = [(width of wider pulse) -
(width of narrower pulse)] / 2

Phase Adjust

The internal clock and data alignment in the MAX3675 is well maintained close to the center of the data eye. Although not required, this sampling point can be shifted using the PHADJ inputs to optimize BER performance. The PHADJ inputs operate with differential input signals to approximately ±1V. A simple resistor divider with a bypass capacitor is sufficient to set up these levels. When the PHADJ inputs are not used, they should be tied directly to V_{CC}.

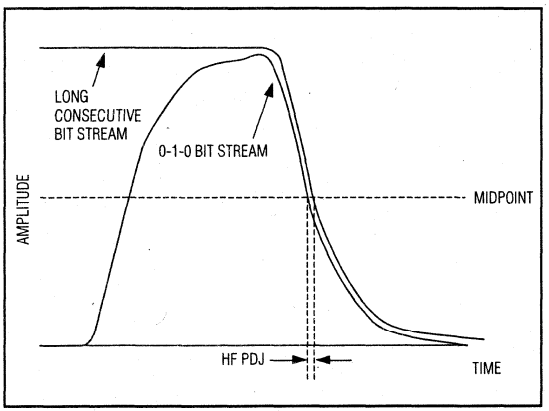


Figure 10. Pattern-Dependent Jitter Due to High-Frequency Roll-Off

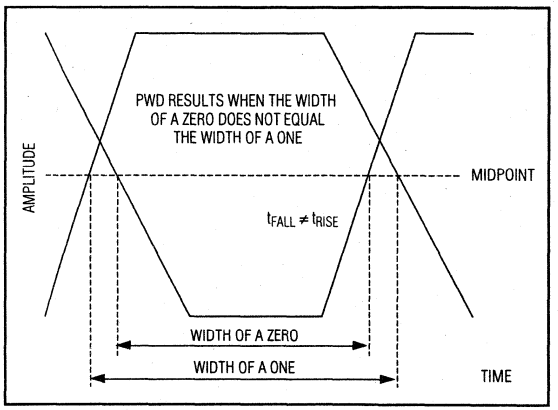
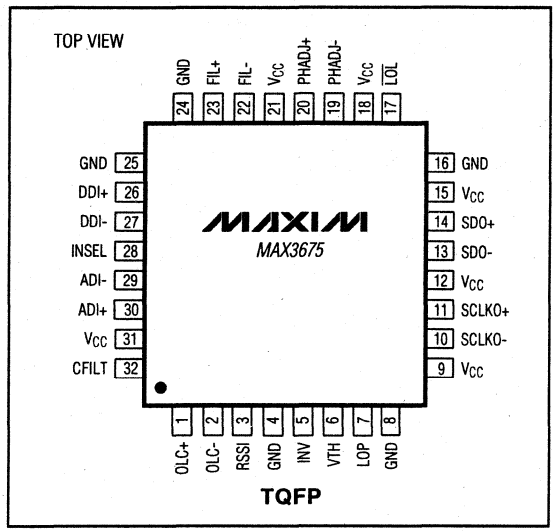


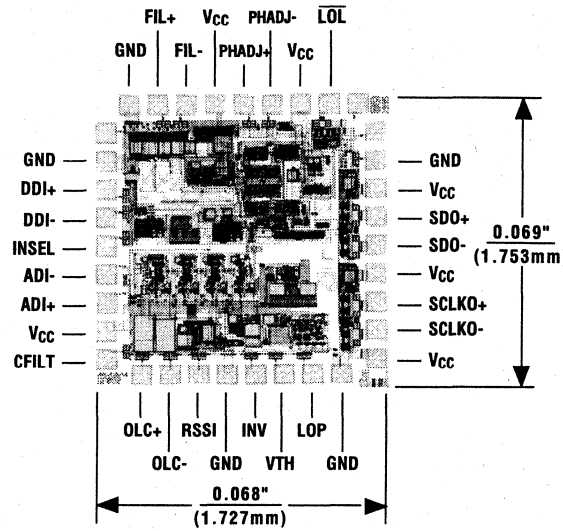
Figure 11. Pulse-Width Distortion

622Mbps, Low-Power, 3.3V Clock-Recovery and Data-Retiming IC with Limiting Amplifier

Pin Configuration



Chip Topography



19-1210; Rev 0; 3/97

EVALUATION KIT AVAILABLE

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

General Description

The MAX3680 deserializer is ideal for converting 622Mbps serial data to 8-bit-wide, 77Mbps parallel data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts PECL serial-clock and data inputs, and delivers TTL clock and data outputs. It also provides a TTL synchronization input that enables data realignment and reframing.

The MAX3680 is available in the extended-industrial temperature range (-40°C to +85°C), in a 28-pin SSOP package.

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

Digital Cross Connects

Features

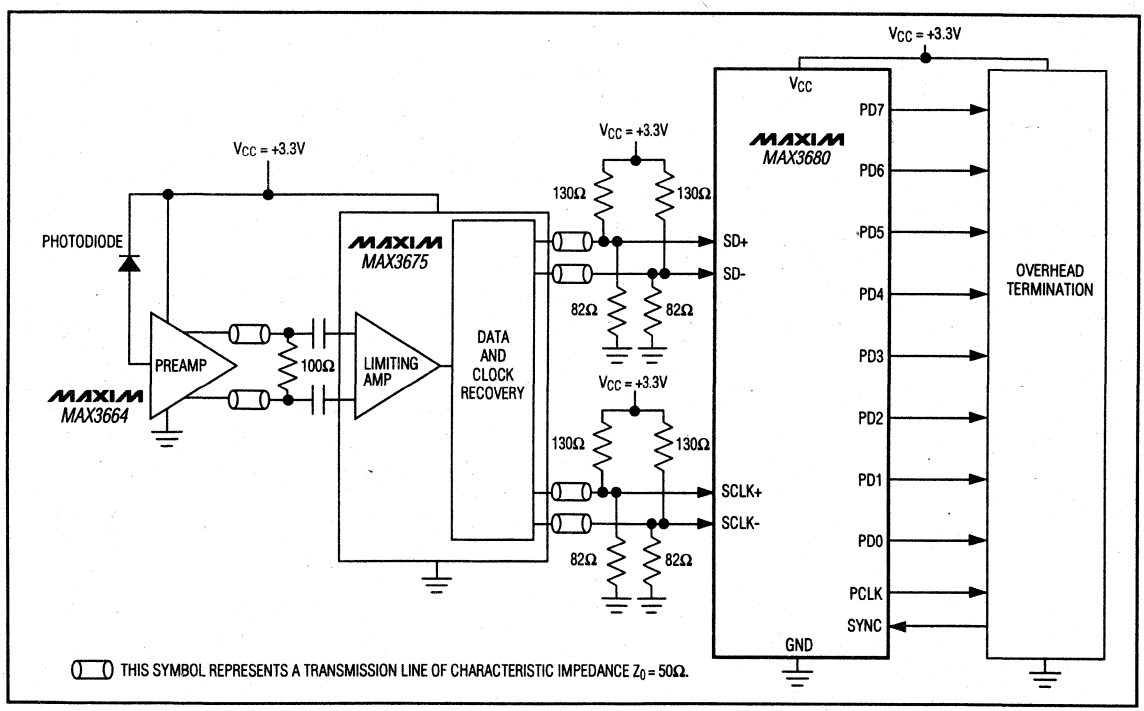
- **Single +3.3V Supply**
- **622Mbps Serial to 77Mbps Parallel Conversion**
- **165mW Power**
- **Synchronization Input for Data Realignment and Reframing**
- **Differential 3.3V PECL Clock and Data Inputs**
- **TTL Data Outputs and Synchronization Input**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3680EAI	-40°C to +85°C	28 SSOP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
V_{CC} .....-0.5V to 5V
PECL Inputs (SD+/-, SCLK+/-).....-0.5V to (V_{CC} + 0.5V)
TTL Input (SYNC) .....-0.5V to (V_{CC} + 0.5V)
TTL Outputs (PCLK, PD_).....-0.5V to (V_{CC} + 0.5V)

Continuous Power Dissipation (T_A = +85°C)
SSOP (derate 9.52mW/°C above +85°C) 619mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range.....-65°C to +160°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	TTL outputs = high	25	50	90	mA
PECL INPUTS (SD+/-, SCLK+/-)						
Input High Voltage	V_{IH}		V_{CC} - 1.16		V_{CC} - 0.88	V
Input Low Voltage	V_{IL}		V_{CC} - 1.81		V_{CC} - 1.48	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-10		10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MAX)}$	-10		10	µA
TTL INPUT AND OUTPUTS (SYNC, PCLK, PD_)						
Input High Voltage	V_{IH}		2.0			V
Input Low Voltage	V_{IL}				0.8	V
Input High Current	I_{IH}	$V_{IN} = V_{IH(MAX)}$	-10		10	µA
Input Low Current	I_{IL}	$V_{IN} = V_{IL(MAX)}$	-10		10	µA
Output High Voltage	V_{OH}	Output sourcing = 400µA	2.4		V_{CC}	V
Output Low Voltage	V_{OL}	Output sinking = 400µA	0		0.44	V

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, T_A = +25°C, unless otherwise noted.) (Note 1)

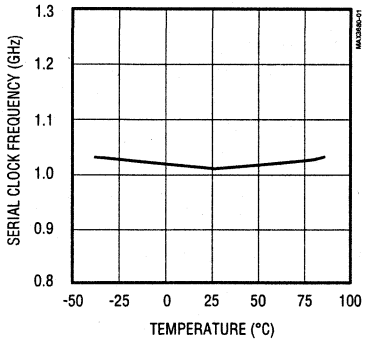
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Serial Clock Frequency	f_{SCLK}		622			MHz
Serial Data Setup Time	t_{SU}		800			ps
Serial Data Hold Time	t_H		50			ps
Parallel Clock to Data Output Delay	t_{CLK-Q}	V_{CC} = 3.3V, C_L = 18pF	-200	500	1300	ps

Note 1: AC characteristics guaranteed by design and characterization.

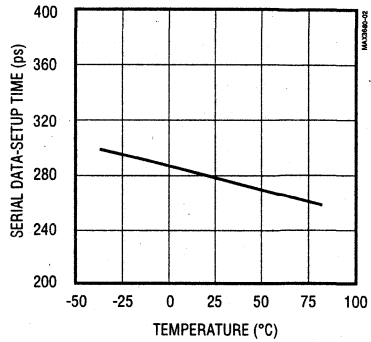
Typical Operating Characteristics

(V_{CC} = +3.0V to +3.6V, unless otherwise noted.)

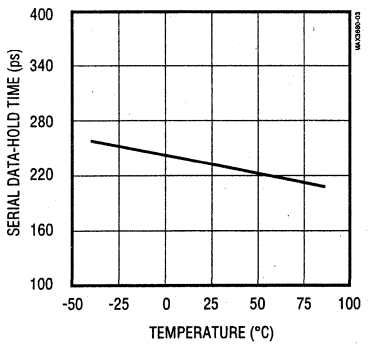
MAXIMUM SERIAL-CLOCK FREQUENCY vs. TEMPERATURE



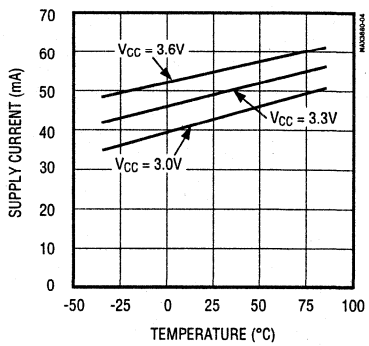
SERIAL DATA-SETUP TIME vs. TEMPERATURE



SERIAL DATA-HOLD TIME vs. TEMPERATURE



SUPPLY CURRENT vs. TEMPERATURE



+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

Pin Description

PIN	NAME	FUNCTION
1, 2, 5, 8, 14, 18, 25	V_{CC}	+3.3V Supply Voltage
3	SD+	Noninverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
4	SD-	Inverting PECL Serial Data Input. Data is clocked on the SCLK signal's positive transition.
6	SCLK+	Noninverting PECL Serial Clock Input
7	SCLK-	Inverting PECL Serial Clock Input
9, 11, 12, 16, 20, 23, 27	GND	Ground
10	SYNC	TTL Synchronization Pulse Input. Pulse high for at least two SCLK periods to shift the data alignment by dropping one bit in the serial input data stream.
13	PCLK	TTL Parallel Clock Output
15, 17, 19, 21, 22, 24, 26, 28	PD0–PD7	TTL Parallel Data Outputs. Data is updated on the falling edge of PCLK. See Figure 2 for the relationship between serial-data-bit position and output-data-bit assignment.

Detailed Description

The MAX3680 deserializer uses an 8-bit shift register, 8-bit parallel output register, 3-bit counter, PECL input buffers, and TTL input/output buffers to convert 622Mbps serial data to 8-bit-wide, 77Mbps parallel data (Figure 1).

The input shift register continuously clocks incoming data on the positive transition of the serial clock (SCLK) input signal. The 3-bit counter generates a parallel output clock (PCLK) by dividing down the serial clock frequency. The PCLK signal is used to clock the parallel output register. During normal operation, the counter divides the SCLK frequency by eight, causing the output register to latch every eight bits of incoming serial data.

The synchronization input (SYNC) is used for data realignment and reframing. When the SYNC signal is pulsed high for at least two SCLK cycles, PCLK is delayed by one SCLK cycle, causing the first incoming bit of the serial input data stream to be dropped. This realignment is guaranteed to occur within two PCLK cycles of the SYNC rising edge.

See Figure 2 for the functional timing diagrams and Figure 3 for the timing parameters diagram.

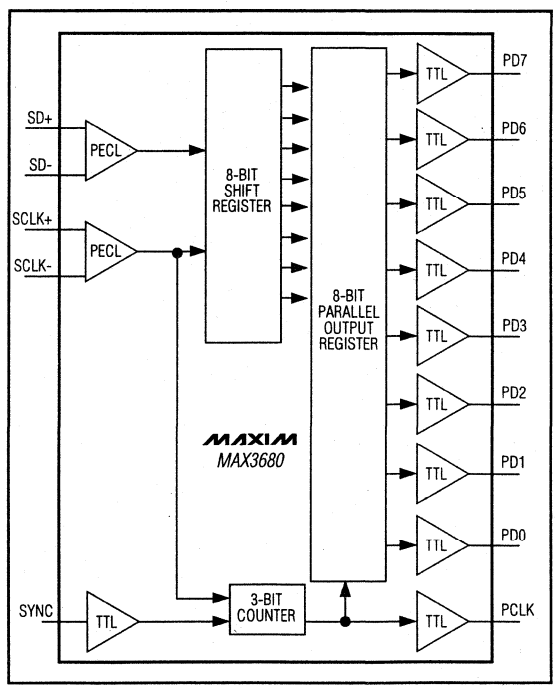


Figure 1. Functional Diagram

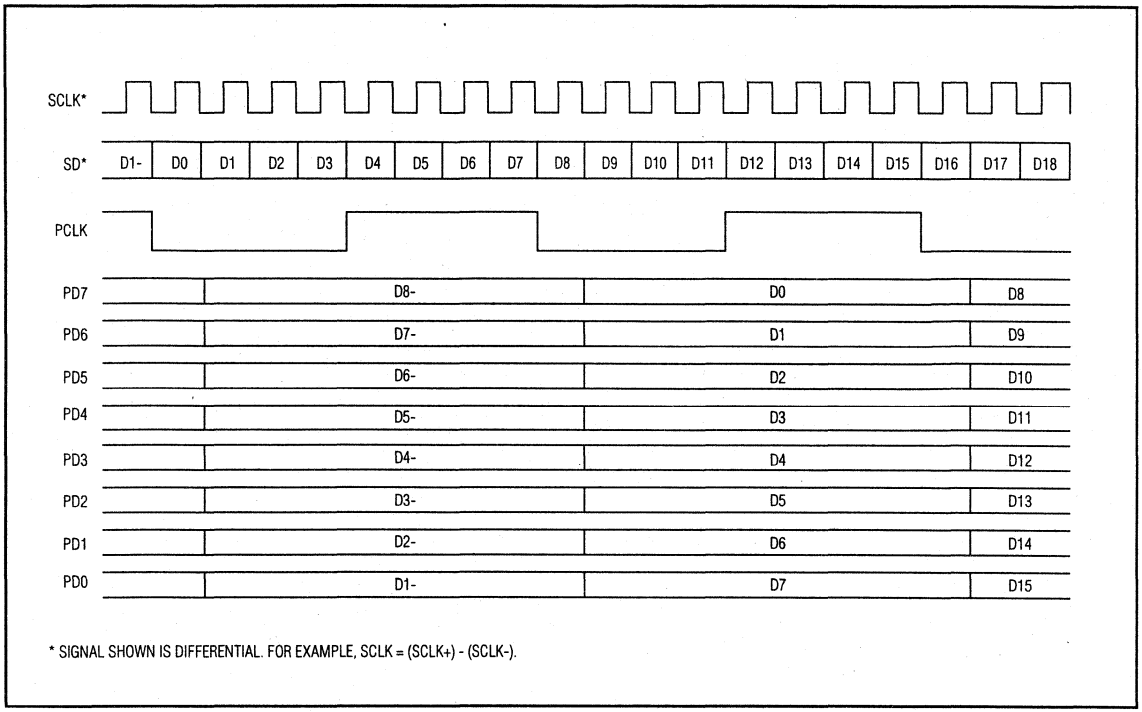


Figure 2a. Functional Timing Diagram—Normal Operation

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

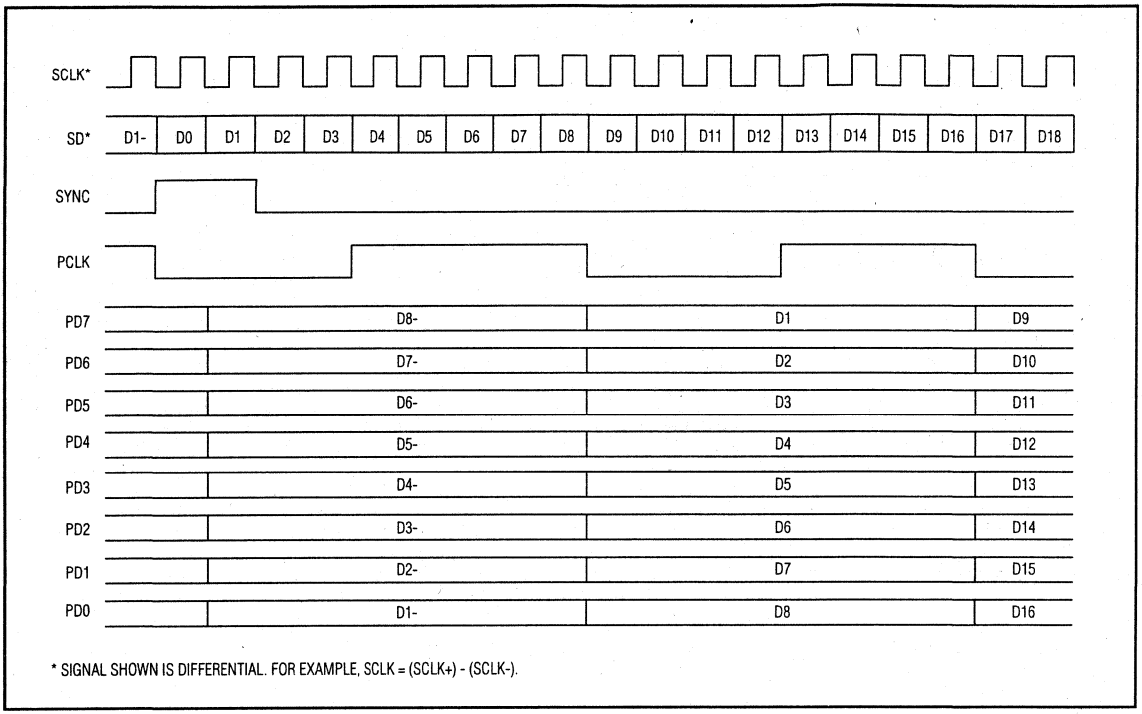


Figure 2b. Functional Timing Diagram—SYNC Operation

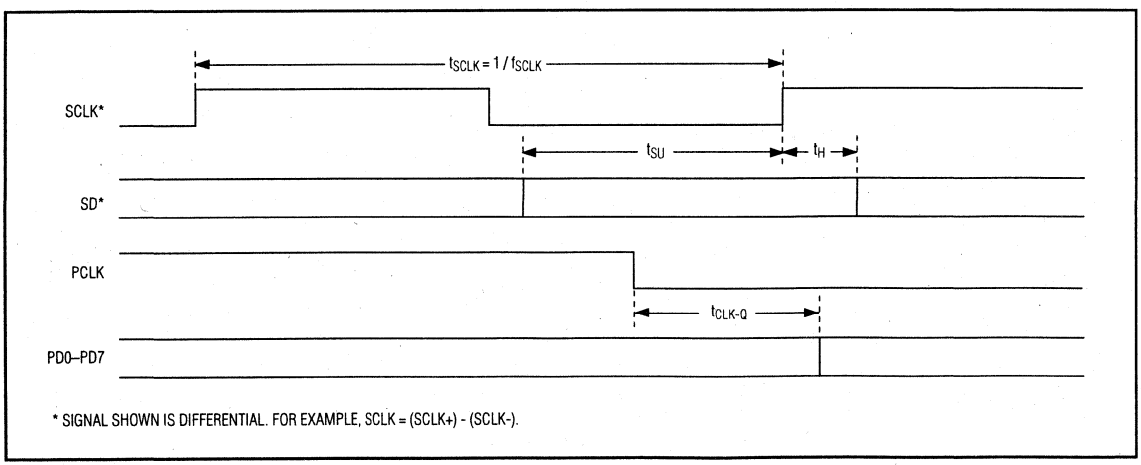


Figure 3. Timing Parameters

+3.3V, 622Mbps, SDH/SONET 1:8 Deserializer with TTL Outputs

PECL Inputs

The serial data and clock PECL inputs (SD+, SD-, SCLK+, SCLK-) require 50Ω termination to (VCC - 2V) when interfacing with a PECL source (see *Alternative PECL Input Termination*).

Applications Information

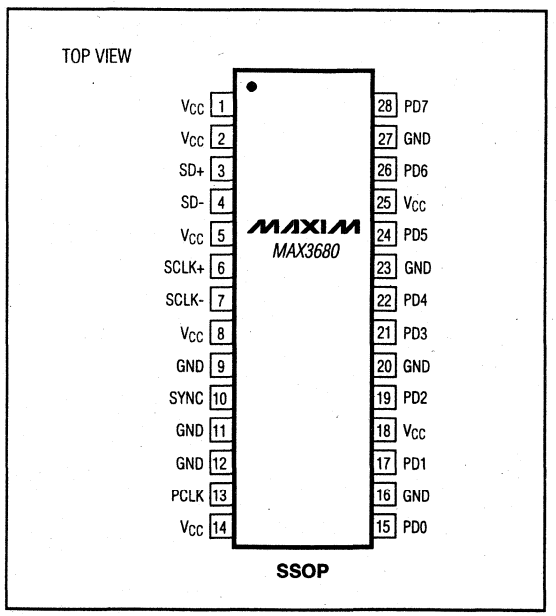
Alternative PECL Input Termination

Figure 4 shows alternative PECL input-termination methods. Use Thevenin-equivalent termination when a (VCC - 2V) termination voltage is not available. If AC coupling is necessary, such as when interfacing with an ECL-output device, use the ECL AC-coupling termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled impedance transmission lines to interface with the MAX3680 data inputs.

Pin Configuration



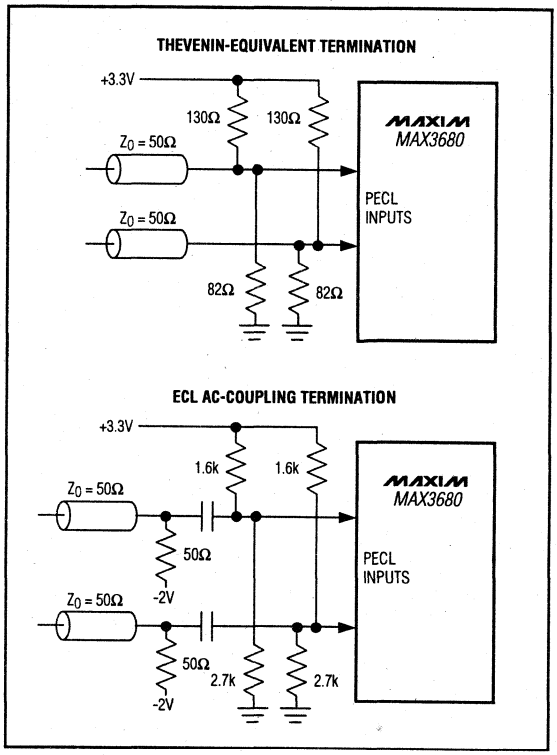


Figure 4. Alternative PECL Input Termination

Chip Information

TRANSISTOR COUNT: 1346

19-1207; Rev 0; 3/97

EVALUATION KIT AVAILABLE

MAXIM

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

General Description

The MAX3691 serializer is ideal for converting 4-bit-wide, 155Mbps parallel data to 622Mbps serial data in ATM and SDH/SONET applications. Operating from a single +3.3V supply, this device accepts low-voltage differential-signal (LVDS) clock and data inputs for interfacing with high-speed digital circuitry, and delivers a 3.3V PECL serial-data output. A fully integrated PLL synthesizes an internal 622Mbps serial clock from a 155.52MHz reference clock.

The MAX3691 is available in the extended-industrial temperature range (-40°C to +85°C), in a 32-pin TQFP package.

Features

- ♦ **Single +3.3V Supply**
- ♦ **155Mbps Parallel to 622Mbps Serial Conversion**
- ♦ **215mW Power**
- ♦ **LVDS Parallel Clock and Data Inputs**
- ♦ **Differential 3.3V PECL Serial-Data Output**

Applications

622Mbps SDH/SONET Transmission Systems

622Mbps ATM/SONET Access Nodes

Add/Drop Multiplexers

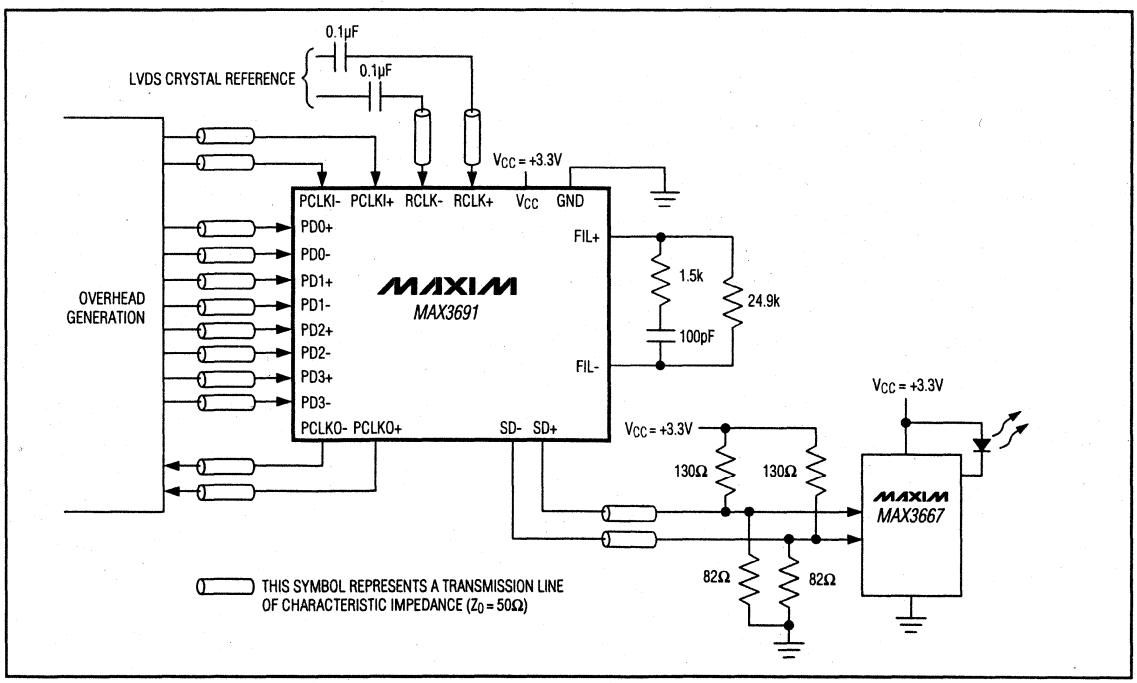
Digital Cross Connects

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX3691ECJ	-40°C to +85°C	32 TQFP

Pin Configuration appears at end of data sheet.

Typical Operating Circuit



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For small orders, phone 408-737-7600 ext. 3468.

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.5V to 5V
- All Inputs ..... -0.5V to (V_{CC} + 0.5V)

Output Current
- LVDS Outputs (PCLKO±) 10mA
- PECL Outputs (SD±) 50mA

Continuous Power Dissipation (T_A = +85°C)
- TQFP (derate 10.20mW/°C above +85°C) 663mW

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω ±1%, PECL loads = 50Ω ±1% to (V_{CC} - 2V), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	PECL outputs unterminated	38	65	100	mA
PECL OUTPUTS (SD±)						
Output High Voltage	V_{OH}	T_A = +25°C to +85°C	V_{CC} - 1.03		V_{CC} - 0.88	V
		T_A = -40°C	V_{CC} - 1.08		V_{CC} - 0.88	
Output Low Voltage	V_{OL}	T_A = +25°C to +85°C	V_{CC} - 1.81		V_{CC} - 1.62	V
		T_A = -40°C	V_{CC} - 1.95		V_{CC} - 1.62	
LVDS INPUTS AND OUTPUTS (PCLKI±, RCLK±, PCLKO±, PD_±)						
Input Voltage Range	V_I	Differential input voltage = 100mV	0		2.4	V
Differential Input Threshold	V_{IDTH}	Common-mode voltage = 50mV	-100		100	mV
Threshold Hysteresis	V_{HYST}			70		mV
Differential Input Resistance	R_{IN}		85	100	115	Ω
Output High Voltage	V_{OH}				1.475	V
Output Low Voltage	V_{OL}		0.925			V
Differential Output Voltage	V_{OD}		250		400	mV
Change in Magnitude of Differential Output Voltage for Complementary States	ΔV_{OD}				25	mV
Output Offset Voltage	V_{OS}	T_A = +25°C	1.125		1.275	V
Change in Magnitude of Output Offset Voltage for Complementary States	ΔV_{OS}				25	mV
Single-Ended Output Resistance	R_O		40	70	140	Ω
Change in Magnitude of Single-Ended Output Resistance for Complementary States	ΔR_O			±1	±10	%

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, differential LVDS load = 100Ω ±1%, PECL loads = 50Ω ±1% to (V_{CC} - 2V) T_A = +25°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V.) (Note 1)

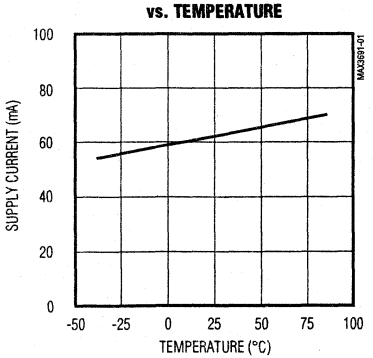
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial Clock Rate	f_{SCLK}			622.08		MHz
Parallel Data-Setup Time	t_{SU}		200			ps
Parallel Data-Hold Time	t_H		600			ps
PCLKO to PCLKI Skew	t_{SKEW}		-0.7		+3.3	ns
Output Jitter	Φ_O	T_A = -40°C to +85°C (Note 2)			13	ps_{RMS}
PECL Differential Output Rise/Fall Time	t_R, t_F			400		ps

Note 1: AC characteristics guaranteed by design and characterization.
Note 2: Assumes a 50% duty cycle ±5%.

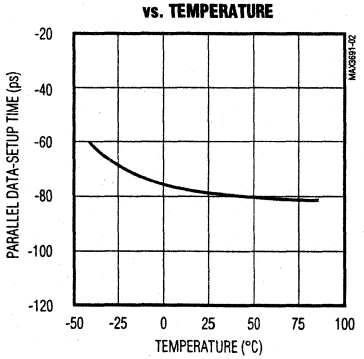
Typical Operating Characteristics

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω, unless otherwise noted.)

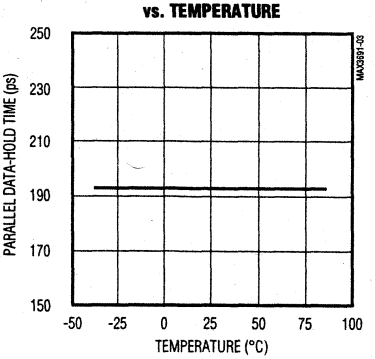
SUPPLY CURRENT vs. TEMPERATURE



PARALLEL DATA-SETUP TIME vs. TEMPERATURE



PARALLEL DATA-HOLD TIME vs. TEMPERATURE

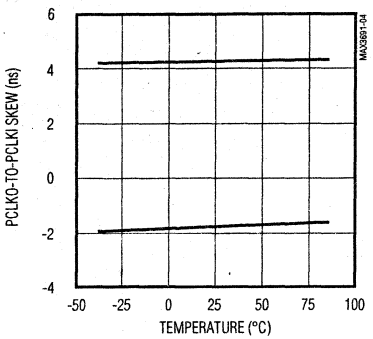


+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

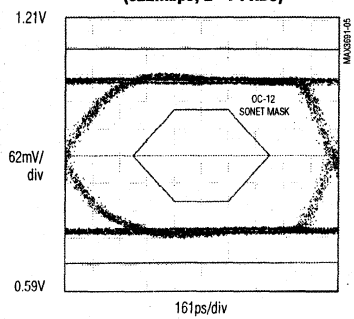
Typical Operating Characteristics (continued)

(V_{CC} = +3.0V to +3.6V, differential LVDS loads = 100Ω, unless otherwise noted.)

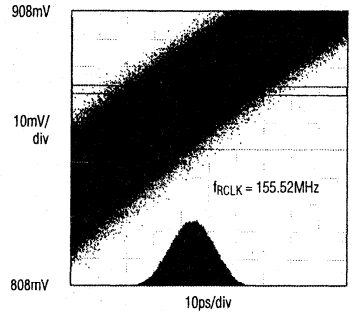
PCLKO-to-PCLKI SKEW vs. TEMPERATURE



SERIAL-DATA OUTPUT EYE DIAGRAM (622Mbps, 2^7-1 PRBS)



SERIAL-DATA OUTPUT JITTER



Mean	23.88ns	µ±1σ	68.774%
RMSΔ	8.418ps	µ±2σ	95.534%
PkPk	70.2ps	µ±3σ	99.738%

Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7	PD0+ to PD3+	Noninverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
2, 4, 6, 8	PD0- to PD3-	Inverting LVDS Parallel Data Inputs. Data is clocked in on the PCLKI signal's positive transition.
9, 17, 18, 19, 24, 25, 32	GND	Ground
10	PCLKO-	Inverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
11	PCLKO+	Noninverting LVDS Parallel-Clock Output. Use PCLKO to clock the overhead management circuit.
12, 13, 16, 20, 21, 28, 29	V_{CC}	+3.3V Supply Voltage
14	SD-	Inverting PECL Serial-Data Output
15	SD+	Noninverting PECL Serial-Data Output
22	FIL-	Filter Capacitor Input. See *Typical Operating Circuit* for external-component connections.
23	FIL+	Filter Capacitor Input. See *Typical Operating Circuit* for external-component connections.
26	RCLK+	Noninverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
27	RCLK-	Inverting LVDS Reference Clock Input. Connect (AC couple) a crystal reference clock (155.52MHz) to the RCLK inputs.
30	PCLKI+	Noninverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.
31	PCLKI-	Inverting LVDS Parallel Clock Input. Connect the incoming parallel-data-clock signal to the PCLKI inputs. Note that data is updated on the positive transition of the PCLKI signal.

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

Detailed Description

The MAX3691 serializer comprises a 4-bit parallel input register, a 4-bit shift register, control and timing logic, a PECL output buffer, LVDS input/output buffers, and a frequency-synthesizing PLL (consisting of a phase/frequency detector, loop filter/amplifier, and voltage-controlled oscillator). This device converts 4-bit-wide, 155Mbps data to 622Mbps serial data (Figure 1).

The PLL synthesizes an internal 622Mbps reference used to clock the output shift register. This clock is generated by locking onto the external 155.52MHz reference-clock signal (RCLK).

The incoming parallel data is clocked into the MAX3691 on the rising transition of the parallel-clock-input signal (PCLKI). The control and timing logic ensure proper operation if the parallel-input register is latched within a window of time that is defined with respect to the parallel-clock-output signal (PCLKO). PCLKO is the synthesized 622Mbps internal serial-clock signal divided by four. The allowable PCLKO-to-PCLKI skew is -0.7ns to +3.3ns. This defines a timing window at about the PCLKO rising edge, during which a PCLKI rising edge may occur. Figure 2 is the timing diagram.

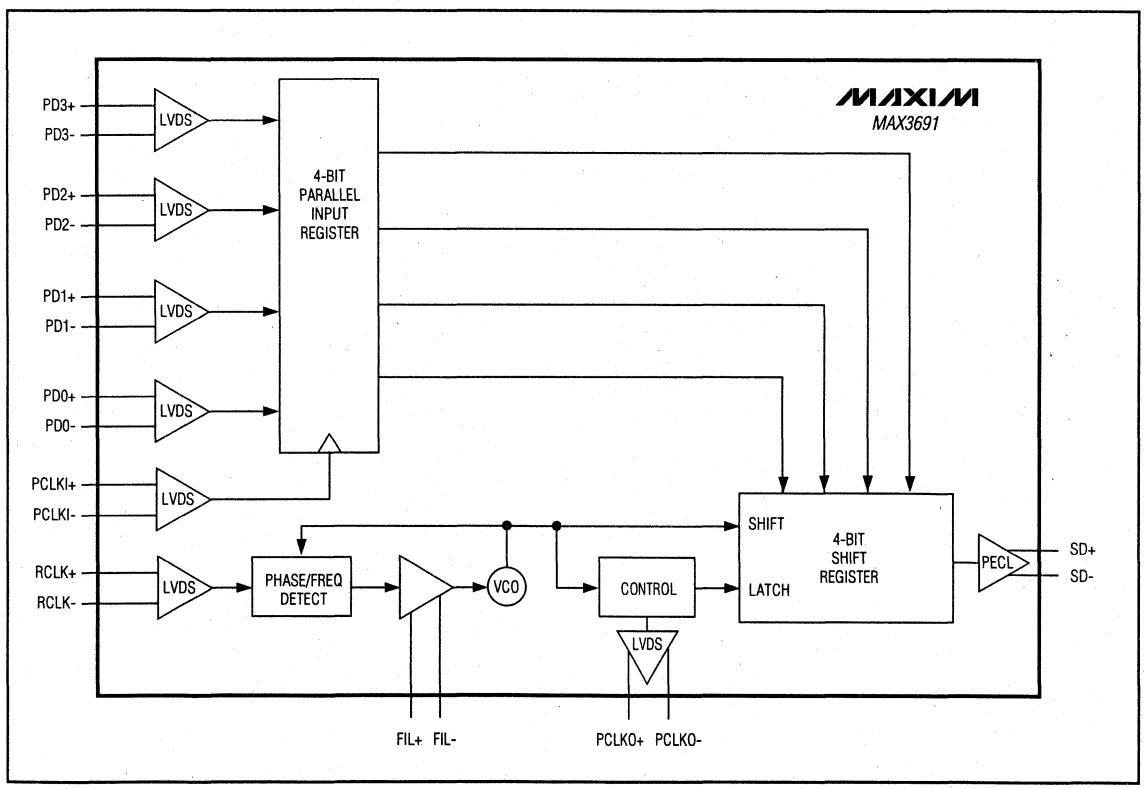


Figure 1. Functional Diagram

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

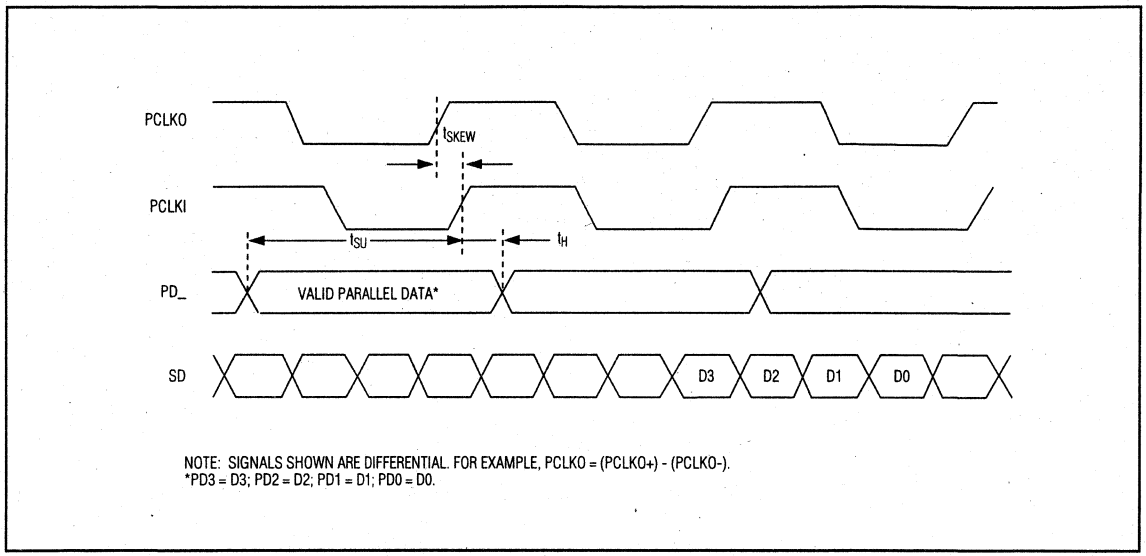


Figure 2. Timing Diagram

Low-Voltage Differential-Signal (LVDS) Inputs and Outputs

The MAX3691 features LVDS inputs and outputs for interfacing with high-speed digital circuitry. The LVDS standard is based on the IEEE 1596.3 LVDS specification. This technology uses 250mV–400mV differential low-voltage swings to achieve fast transition times, minimized power dissipation, and noise immunity.

For proper operation, the parallel-clock LVDS outputs (PCLKO+, PCLKO-) require 100Ω differential DC termination between the inverting and noninverting outputs. Do not terminate these outputs to ground.

The parallel data and parallel clock LVDS inputs (PD_+, PD_-, PCLKI+, PCLKI-) are internally terminated with 100Ω differential input resistance, and therefore do not require external termination.

PECL Outputs

The serial-data PECL outputs (SD+, SD-) require 50Ω DC termination to (V_{CC} - 2V). See the *Alternative PECL-Output Termination* section.

+3.3V, 622Mbps, SDH/SONET 4:1 Serializer with Clock Synthesis and LVDS Inputs

Applications Information

Alternative PECL-Output Termination

Figure 3 shows alternative PECL output-termination methods. Use Thevenin-equivalent termination when a (V_{CC} - 2V) termination voltage is not available. If AC coupling is necessary, be sure that the coupling capacitor is placed following the 50Ω or Thevenin-equivalent DC termination.

Layout Techniques

For best performance, use good high-frequency layout techniques. Filter voltage supplies and keep ground connections short. Use multiple vias where possible. Also, use controlled-impedance transmission lines to interface with the MAX3691 clock and data inputs and outputs.

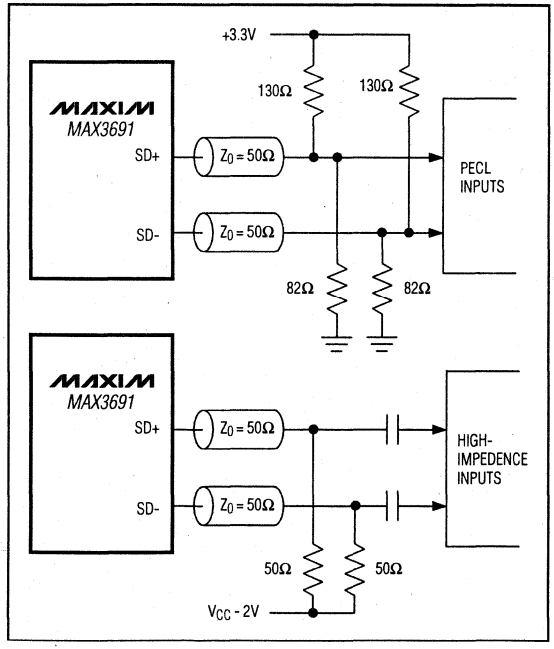
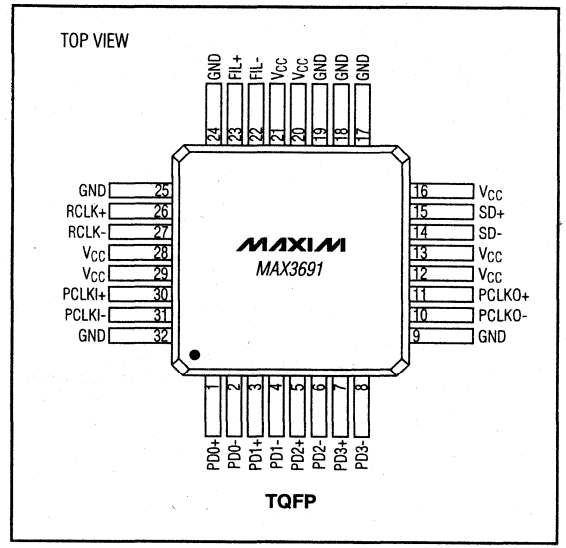


Figure 3. Alternative PECL-Output Termination

Pin Configuration



Chip Information

TRANSISTOR COUNT: 1633

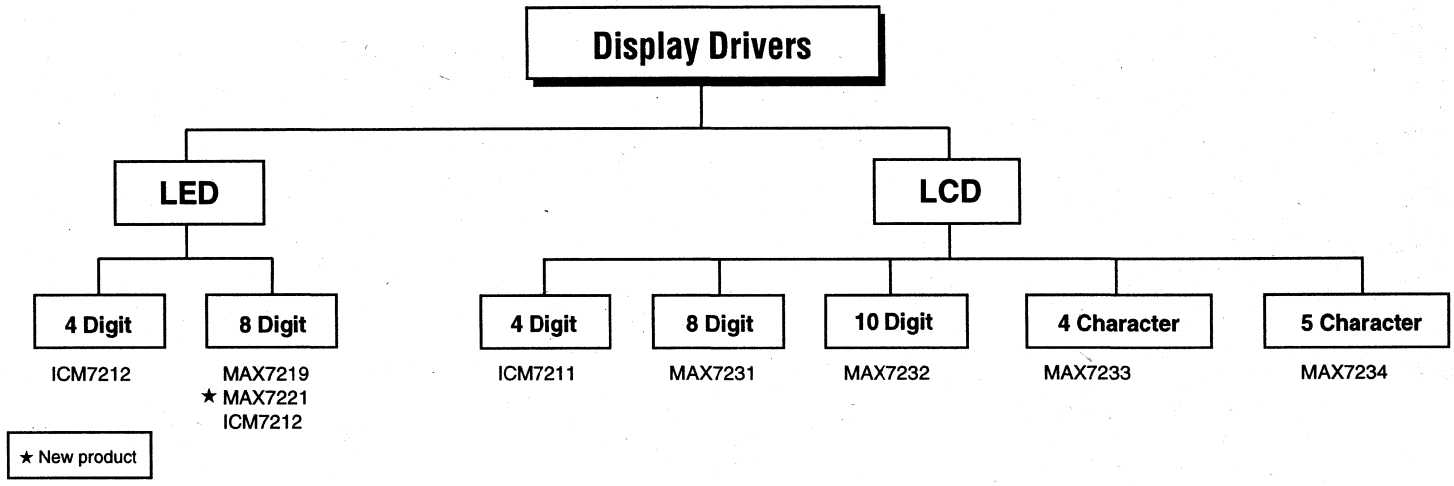
11

Display Drivers

Display Drivers, Product Tables and Trees 12-2

MAX7219 Serially Interfaced, 8-Digit, LED Display Driver 12-5

MAX7221 Serially Interfaced, 8-Digit, LED Display Driver with Slew-Rate-Limited Segment Drivers 12-5



Display Drivers

Part Number	Output	Display Format	Input Format	Input Formula	Number of Annunciators	LCD or LED	Features	Price† 1000-up ($)
ICM7211	4 digit	Hexadecimal or code B	Multiplexed or µP interface	4-bit data	No independent annunciators	LCD	Muxed version, 4-digit strobes; µP-interfaced version, 2-digit address	2.42
ICM7212	4 digit	Hexadecimal or code B	Multiplexed or µP interface	4-bit data	No independent annunciators	LED	Muxed version, 4-digit strobes; µP-interfaced version, 2-digit address	2.05
MAX7219	8 digit	7 segment, no decode, or code B	Serial entry	8-bit data, 8-bit address	1 decimal point per digit	LED	True 3-wire serial interface, easy to use, available in 24-pin SO	3.99
MAX7221	8 digit	7 segment, no decode, or code B	Serial entry	8-bit data, 8-bit address	1 decimal point per digit	LED	Slew-rate-limited MAX7219 with true SPI-compatible interface	3.99
MAX7231	8 digit	Hexadecimal or code B	Parallel entry	4-bit data, 2-bit annunciator, 3-bit address	16	LCD	"A" & "B" versions, both annunciators on COM3; "C" version, annunciators on COM1 & COM3	4.50
ICM7218	8 digit	Hexadecimal, no decode, or code B	Parallel and serial entry	6-bit data	1 decimal point per digit	LED	"A" version, serial format, drives common anode; "B" version, serial format, drives common cathode; "C" version, parallel format, drives common anode; "D" version, parallel format, drives common cathode	4.33
MAX7232	10 digit	Hexadecimal or code B	Serial entry	4-bit data, 2-bit annunciator, 4-bit address	20	LCD	"A" & "B" versions, both annunciators on COM3; "C" version, annunciators on COM1 & COM3	4.37
MAX7233	4 char.	64 character ASCII	Parallel entry	6-bit ASCII data, 2-bit address	No independent annunciators	LCD	"A" version, half-width numbers; "B" version, full-width numbers	4.06
MAX7234	5 char.	64 character	Serial entry	6-bit ASCII data,	No independent	LCD	"A" version, half-width numbers;	4.51

Counters and Timers

Part Number	Description	Maximum Count	Output[1]	Speed (MHz max)	Supply Voltage (V)	Supply Current (mA), max(typ)	Package Options[2]	Temp. Range[3]	Features	Price† 1000-up ($)
ICM7217	4-digit up/down	9999	C.A. LED & C.C. LED	2	4.5 to 5.5	(100-350)	DIP	I	Equals and zero outputs, counter presets and predetermining register set by thumb-wheel switches	4.67
ICM7224/7225	4-1/2 digit	19,999	LCD, C.A. LED	15	3 to 6	0.025	DIP, PLCC	I	Improved second source	4.86
ICM7240	8-bit binary	1-255	open drain	15	2 to 16	0.50	DIP	I	Improved second source, RC oscillator or ext. clock	2.04
ICM7242	Fixed 8-bit	128/256	CMOS	15	2 to 16	0.50	DIP	I,M	Programmable timeouts	1.97
ICM7250	2-digit BCD	1-99	open drain	15	2 to 16	0.50	DIP	I	RC oscillator or ext. clock	2.05
ICM7260	2-digit timer	1-59	open drain	15	2 to 16	0.50	DIP	I	RC oscillator or ext. clock	1.97
ICM7555/7556	CMOS 555/556 timer	—	CMOS	0.5	2 to 16.5	0.25-0.50	DIP, SO, Can	E,I,M	Improved second source	0.68

True RMS-to-DC Converters

Part Number	Conversion Accuracy (mV ±% read, max)	Full-Scale Range (V_{RMS})	Decibel Output (dB max)	Quiescent Current (mA max)	Features	Price† 1000-up ($)
MX536A	2 (±0.2) to 5 (±0.5)	7	0.3 to 0.6	2	General purpose	5.86
MX636	0.2 (±0.3) to 0.5 (±0.6)	0.2	0.2 to 0.5	1	Low power	4.94

Function Generator

Part Number	Operating Frequency (MHz)	Triangle, Sawtooth, Sine, Square, and Pulse Waveforms	Frequency Sweep Range	Sine Wave Distortion (%)	Output Impedance (Ω)	Duty Cycle Variance (%)	EV Kit
MAX038	20	Yes	350 to 1	0.75	0.1	15 to 85	Yes

[1] C.A. LED = Common Anode LED Display, C.C. LED = Common Cathode LED Display
[2] Package Options: DIP = Dual-In-Line Package; SO = Small Outline; PLCC = Plastic Leadless Chip Carrier (quad pack); FP = Flat Pack
[3] Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

19-4452; Rev 3; 7/97

MAXIM

Serially Interfaced, 8-Digit LED Display Drivers

General Description

The MAX7219/MAX7221 are compact, serial input/output common-cathode display drivers that interface microprocessors (µPs) to 7-segment numeric LED displays of up to 8 digits, bar-graph displays, or 64 individual LEDs. Included on-chip are a BCD code-B decoder, multiplex scan circuitry, segment and digit drivers, and an 8x8 static RAM that stores each digit. Only one external resistor is required to set the segment current for all LEDs. The MAX7221 is compatible with SPI™, QSPI™, and Microwire™, and has slew-rate-limited segment drivers to reduce EMI.

A convenient 3-wire serial interface connects to all common µPs. Individual digits may be addressed and updated without rewriting the entire display. The MAX7219/MAX7221 also allow the user to select code-B decoding or no-decode for each digit.

The devices include a 150µA low-power shutdown mode, analog and digital brightness control, a scan-limit register that allows the user to display from 1 to 8 digits, and a test mode that forces all LEDs on.

Applications

Bar-Graph Displays
7-Segment Displays
Industrial Controllers
Panel Meters
LED Matrix Displays

Features

- ♦ **10MHz Serial Interface**
- ♦ **Individual LED Segment Control**
- ♦ **Decode/No-Decode Digit Selection**
- ♦ **150µA Low-Power Shutdown (Data Retained)**
- ♦ **Digital and Analog Brightness Control**
- ♦ **Display Blanked on Power-Up**
- ♦ **Drive Common-Cathode LED Display**
- ♦ **Slew-Rate Limited Segment Drivers for Lower EMI (MAX7221)**
- ♦ **SPI, QSPI, Microwire Serial Interface (MAX7221)**
- ♦ **24-Pin DIP and SO Packages**

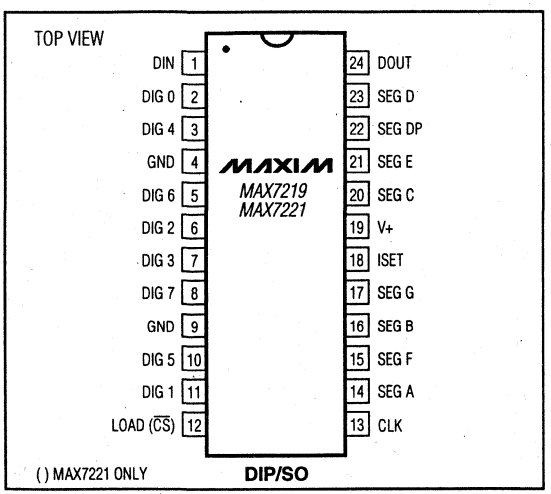
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX7219CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX7219CWG	0°C to +70°C	24 Wide SO
MAX7219C/D	0°C to +70°C	Dice*
MAX7219ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX7219EWG	-40°C to +85°C	24 Wide SO
MAX7219ERG	-40°C to +85°C	24 Narrow CERDIP

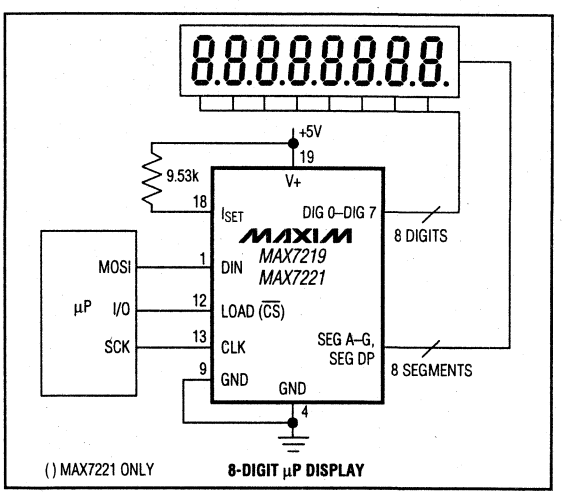
Ordering Information continued at end of data sheet.

**Dice are specified at T_A = +25°C.*

Pin Configuration



Typical Application Circuit



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ABSOLUTE MAXIMUM RATINGS

Voltage (with respect to GND)
- V+ ..... -0.3V to 6V
- DIN, CLK, LOAD, $\overline{CS}$ ..... -0.3V to 6V
- All Other Pins ..... -0.3V to (V+ + 0.3V)

Current
- DIG0–DIG7 Sink Current 500mA
- SEGA–G, DP Source Current 100mA

Continuous Power Dissipation (T_A = +85°C)
- Narrow Plastic DIP 0.87W
- Wide SO 0.76W
- Narrow CERDIP 1.1W

Operating Temperature Ranges
- MAX7219C_G/MAX7221C_G ..... 0°C to +70°C
- MAX7219E_G/MAX7221E_G ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V ±10%, R_{SET} = 9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V+		4.0		5.5	V
Shutdown Supply Current	I+	All digital inputs at V+ or GND, T_A = +25°C			150	µA
Operating Supply Current	I+	R_{SET} = open circuit			8	mA
		All segments and decimal point on, $I_{SEG_}$ = -40mA		330		
Display Scan Rate	f_{OSC}	8 digits scanned	500	800	1300	Hz
Digit Drive Sink Current	I_{DIGIT}	V+ = 5V, V_{OUT} = 0.65V	320			mA
Segment Drive Source Current	I_{SEG}	T_A = +25°C, V+ = 5V, V_{OUT} = (V+ - 1V)	-30	-40	-45	mA
Segment Current Slew Rate (MAX7221 only)	$\Delta I_{SEG}/\Delta t$	T_A = +25°C, V+ = 5V, V_{OUT} = (V+ - 1V)	10	20	50	mA/µs
Segment Drive Current Matching	ΔI_{SEG}			3.0		%
Digit Drive Leakage (MAX7221 only)	I_{DIGIT}	Digit off, V_{DIGIT} = V+			-10	µA
Segment Drive Leakage (MAX7221 only)	I_{SEG}	Segment off, V_{SEG} = 0V			1	µA
Digit Drive Source Current (MAX7219 only)	I_{DIGIT}	Digit off, V_{DIGIT} = (V+ - 0.3V)	-2			mA
Segment Drive Sink Current (MAX7219 only)	I_{SEG}	Segment off, V_{SEG} = 0.3V	5			mA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V ±10%, R_{SET} =9.53kΩ ±1%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

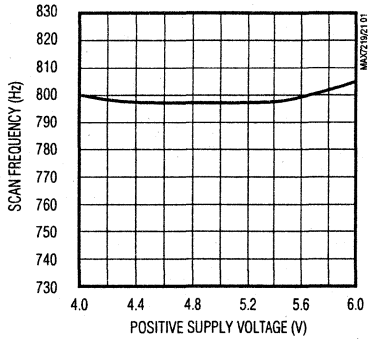
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS						
Input Current DIN, CLK, LOAD, $\overline{CS}$	I_{IH}, I_{IL}	V_{IN} = 0V or V+	-1		1	µA
Logic High Input Voltage	V_{IH}		3.5			V
Logic Low Input Voltage	V_{IL}				0.8	V
Output High Voltage	V_{OH}	DOUT, I_{SOURCE} = -1mA	V+ - 1			V
Output Low Voltage	V_{OL}	DOUT, I_{SINK} = 1.6mA			0.4	V
Hysteresis Voltage	ΔV_I	DIN, CLK, LOAD, $\overline{CS}$		1		V
TIMING CHARACTERISTICS						
CLK Clock Period	t_{CP}		100			ns
CLK Pulse Width High	t_{CH}		50			ns
CLK Pulse Width Low	t_{CL}		50			ns
$\overline{CS}$ Fall to SCLK Rise Setup Time (MAX7221 only)	t_{CSS}		25			ns
CLK Rise to $\overline{CS}$ or LOAD Rise Hold Time	t_{CSH}		0			ns
DIN Setup Time	t_{DS}		25			ns
DIN Hold Time	t_{DH}		0			ns
Output Data Propagation Delay	t_{DO}	C_{LOAD} = 50pF			25	ns
Load-Rising Edge to Next Clock Rising Edge (MAX7219 only)	t_{LDCK}		50			ns
Minimum $\overline{CS}$ or LOAD Pulse High	t_{CSW}		50			ns
Data-to-Segment Delay	t_{DSPD}				2.25	ms

Serially Interfaced, 8-Digit LED Display Drivers

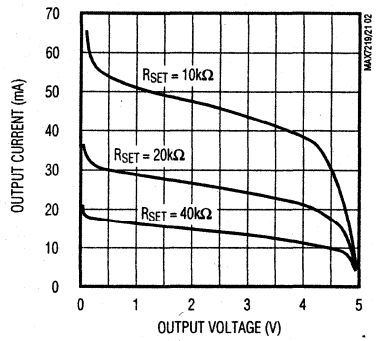
Typical Operating Characteristics

(V+ = +5V, T_A = +25°C, unless otherwise noted.)

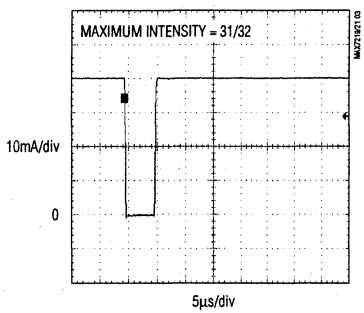
SCAN FREQUENCY vs. POSITIVE SUPPLY VOLTAGE



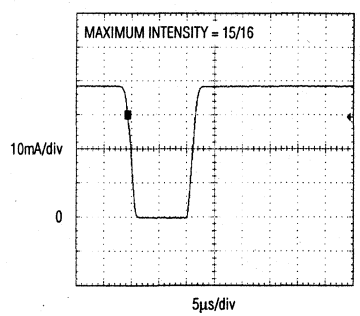
SEGMENT DRIVER OUTPUT CURRENT vs. OUTPUT VOLTAGE



MAX7219 SEGMENT OUTPUT CURRENT



MAX7221 SEGMENT OUTPUT CURRENT

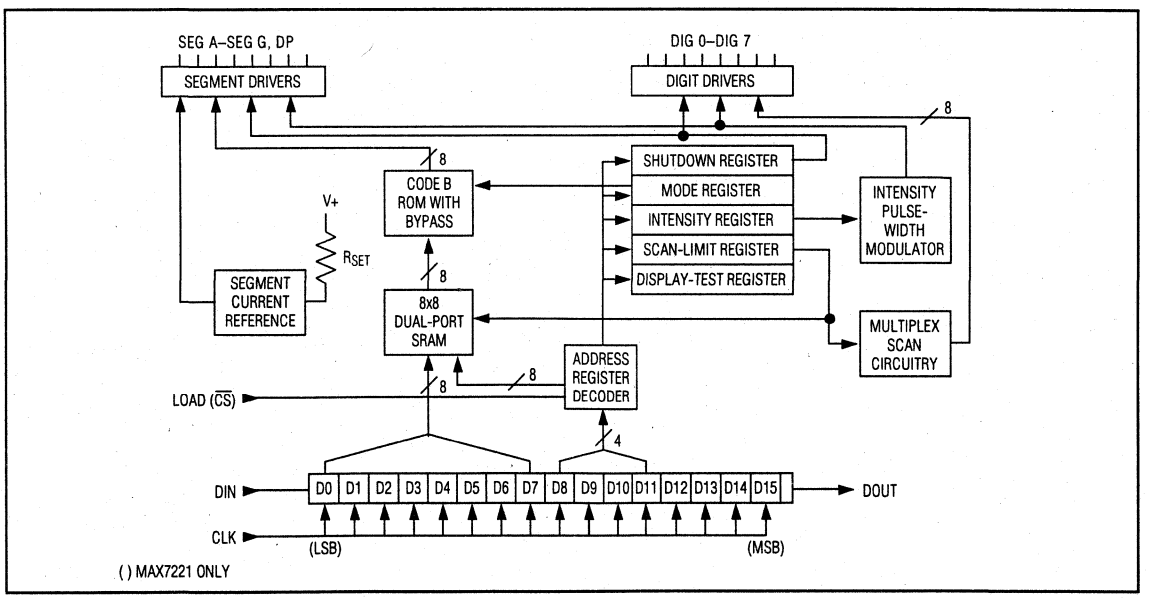


Serially Interfaced, 8-Digit LED Display Drivers

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial-Data Input. Data is loaded into the internal 16-bit shift register on CLK's rising edge.
2, 3, 5–8, 10, 11	DIG 0–DIG 7	Eight-Digit Drive Lines that sink current from the display common cathode. The MAX7219 pulls the digit outputs to V+ when turned off. The MAX7221's digit drivers are high-impedance when turned off.
4, 9	GND	Ground (both GND pins must be connected)
12	LOAD (MAX7219)	Load-Data Input. The last 16 bits of serial data are latched on LOAD's rising edge.
	$\overline{CS}$ (MAX7221)	Chip-Select Input. Serial data is loaded into the shift register while $\overline{CS}$ is low. The last 16 bits of serial data are latched on $\overline{CS}$'s rising edge.
13	CLK	Serial-Clock Input. 10MHz maximum rate. On CLK's rising edge, data is shifted into the internal shift register. On CLK's falling edge, data is clocked out of DOUT. On the MAX7221, the CLK input is active only while $\overline{CS}$ is low.
14–17, 20–23	SEG A–SEG G, DP	Seven Segment Drives and Decimal Point Drive that source current to the display. On the MAX7219, when a segment driver is turned off it is pulled to GND. The MAX7221 segment drivers are high-impedance when turned off.
18	ISET	Connect to V_{DD} through a resistor (R_{SET}) to set the peak segment current (Refer to *Selecting R_{SET} Resistor* section).
19	V+	Positive Supply Voltage. Connect to +5V.
24	DOUT	Serial-Data Output. The data into DIN is valid at DOUT 16.5 clock cycles later. This pin is used to daisy-chain several MAX7219/MAX7221's and is never high-impedance.

Functional Diagram



Serially Interfaced, 8-Digit LED Display Drivers

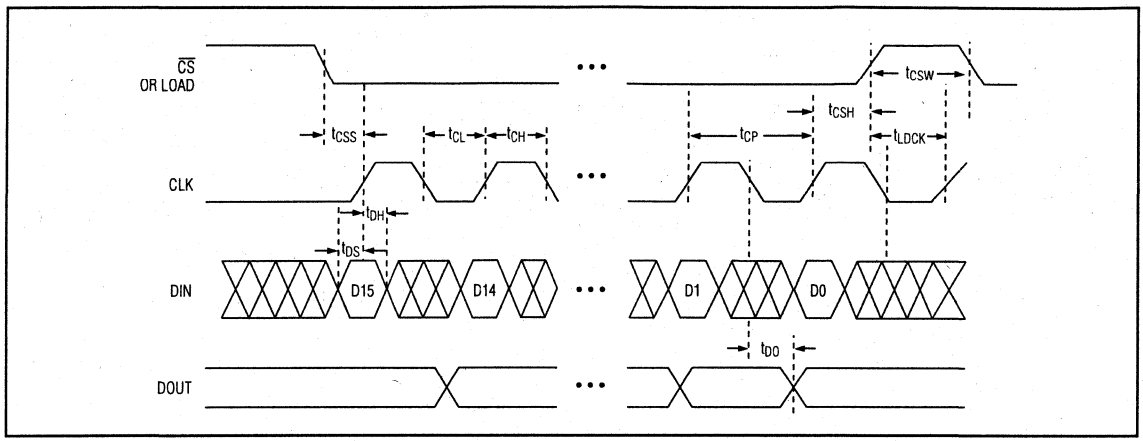


Figure 1. Timing Diagram

Table 1. Serial-Data Format (16 Bits)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	ADDRESS				MSB	DATA						LSB

Detailed Description

MAX7219/MAX7221 Differences

The MAX7219 and MAX7221 are identical except for two parameters: the MAX7221 segment drivers are slew-rate limited to reduce electromagnetic interference (EMI), and its serial interface is fully SPI compatible.

Serial-Addressing Modes

For the MAX7219, serial data at DIN, sent in 16-bit packets, is shifted into the internal 16-bit shift register with each rising edge of CLK regardless of the state of LOAD. For the MAX7221, $\overline{CS}$ must be low to clock data in or out. The data is then latched into either the digit or control registers on the rising edge of LOAD/$\overline{CS}$. LOAD/$\overline{CS}$ must go high concurrently with or after the 16th rising clock edge, but before the next rising clock edge or data will be lost. Data at DIN is propagated through the shift register and appears at DOUT 16.5 clock cycles later. Data is clocked out on the falling edge of CLK. Data bits are labeled D0–D15 (Table 1). D8–D11 contain the register address. D0–D7 contain the data, and D12–D15 are "don't care" bits. The first received is D15, the most significant bit (MSB).

Digit and Control Registers

Table 2 lists the 14 addressable digit and control registers. The digit registers are realized with an on-chip, 8x8 dual-port SRAM. They are addressed directly so that individual digits can be updated and retain data as long as V+ typically exceeds 2V. The control registers consist of decode mode, display intensity, scan limit (number of scanned digits), shutdown, and display test (all LEDs on).

Shutdown Mode

When the MAX7219 is in shutdown mode, the scan oscillator is halted, all segment current sources are pulled to ground, and all digit drivers are pulled to V+, thereby blanking the display. The MAX7221 is identical, except the drivers are high-impedance. Data in the digit and control registers remains unaltered. Shutdown can be used to save power or as an alarm to flash the display by successively entering and leaving shutdown mode. For minimum supply current in shutdown mode, logic inputs should be at ground or V+ (CMOS-logic levels).

Typically, it takes less than 250µs for the MAX7219/MAX7221 to leave shutdown mode. The display driver can be programmed while in shutdown mode, and shutdown mode can be overridden by the display-test function.

Table 2. Register Address Map

REGISTER	ADDRESS					HEX CODE
	D15–D12	D11	D10	D9	D8	
No-Op	X	0	0	0	0	X0
Digit 0	X	0	0	0	1	X1
Digit 1	X	0	0	1	0	X2
Digit 2	X	0	0	1	1	X3
Digit 3	X	0	1	0	0	X4
Digit 4	X	0	1	0	1	X5
Digit 5	X	0	1	1	0	X6
Digit 6	X	0	1	1	1	X7
Digit 7	X	1	0	0	0	X8
Decode Mode	X	1	0	0	1	X9
Intensity	X	1	0	1	0	XA
Scan Limit	X	1	0	1	1	XB
Shutdown	X	1	1	0	0	XC
Display Test	X	1	1	1	1	XF

Initial Power-Up

On initial power-up, all control registers are reset, the display is blanked, and the MAX7219/MAX7221 enter shutdown mode. Program the display driver prior to display use. Otherwise, it will initially be set to scan one digit, it will not decode data in the data registers, and the intensity register will be set to its minimum value.

Decode-Mode Register

The decode-mode register sets BCD code B (0-9, E, H, L, P, and -) or no-decode operation for each digit. Each bit in the register corresponds to one digit. A logic high selects code B decoding while logic low bypasses the decoder. Examples of the decode mode control-register format are shown in Table 4.

When the code B decode mode is used, the decoder looks only at the lower nibble of the data in the digit registers (D3–D0), disregarding bits D4–D6. D7, which sets the decimal point (SEG DP), is independent of the decoder and is positive logic (D7 = 1 turns the decimal point on). Table 5 lists the code B font.

When no-decode is selected, data bits D7–D0 correspond to the segment lines of the MAX7219/MAX7221. Table 6 shows the one-to-one pairing of each data bit to the appropriate segment line.

Table 3. Shutdown Register Format (Address (Hex) = XC)

MODE	ADDRESS CODE (HEX)	REGISTER DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
Shutdown Mode	XC	X	X	X	X	X	X	X	0
Normal Operation	XC	X	X	X	X	X	X	X	1

Table 4. Decode-Mode Register Examples (Address (Hex) = X9)

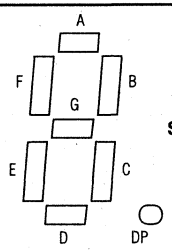
DECODE MODE	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
No decode for digits 7–0	0	0	0	0	0	0	0	0	00
Code B decode for digit 0 No decode for digits 7–1	0	0	0	0	0	0	0	1	01
Code B decode for digits 3–0 No decode for digits 7–4	0	0	0	0	1	1	1	1	0F
Code B decode for digits 7–0	1	1	1	1	1	1	1	1	FF

Table 5. Code B Font

7-SEGMENT CHARACTER	REGISTER DATA						ON SEGMENTS = 1							
	D7*	D6–D4	D3	D2	D1	D0	DP*	A	B	C	D	E	F	G
0		X	0	0	0	0		1	1	1	1	1	1	0
1		X	0	0	0	1		0	1	1	0	0	0	0
2		X	0	0	1	0		1	1	0	1	1	0	1
3		X	0	0	1	1		1	1	1	1	0	0	1
4		X	0	1	0	0		0	1	1	0	0	1	1
5		X	0	1	0	1		1	0	1	1	0	1	1
6		X	0	1	1	0		1	0	1	1	1	1	1
7		X	0	1	1	1		1	1	1	0	0	0	0
8		X	1	0	0	0		1	1	1	1	1	1	1
9		X	1	0	0	1		1	1	1	1	0	1	1
—		X	1	0	1	0		0	0	0	0	0	0	1
E		X	1	0	1	1		1	0	0	1	1	1	1
H		X	1	1	0	0		0	1	1	0	1	1	1
L		X	1	1	0	1		0	0	0	1	1	1	0
P		X	1	1	1	0		1	1	0	0	1	1	1
blank		X	1	1	1	1		0	0	0	0	0	0	0

*The decimal point is set by bit D7 = 1

Table 6. No-Decode Mode Data Bits and Corresponding Segment Lines



STANDARD 7-SEGMENT LED

	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Corresponding Segment Line	DP	A	B	C	D	E	F	G

Intensity Control and Interdigit Blanking

The MAX7219/MAX7221 allow display brightness to be controlled with an external resistor (R_{SET}) connected between V+ and ISET. The peak current sourced from the segment drivers is nominally 100 times the current entering ISET. This resistor can either be fixed or variable to allow brightness adjustment from the front panel. Its minimum value should be 9.53Ω, which typically sets the segment current at 40mA. Display brightness can also be controlled digitally by using the intensity register.

Digital control of display brightness is provided by an internal pulse-width modulator, which is controlled by the lower nibble of the intensity register. The modulator scales the average segment current in 16 steps from a maximum of 31/32 down to 1/32 of the peak current set by R_{SET} (15/16 to 1/16 on MAX7221). Table 7 lists the intensity register format. The minimum interdigit blanking time is set to 1/32 of a cycle.

Table 7. Intensity Register Format (Address (Hex) = XA)

DUTY CYCLE		D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
MAX7219	MAX7221									
1/32 (min on)	1/16 (min on)	X	X	X	X	0	0	0	0	X0
3/32	2/16	X	X	X	X	0	0	0	1	X1
5/32	3/16	X	X	X	X	0	0	1	0	X2
7/32	4/16	X	X	X	X	0	0	1	1	X3
9/32	5/16	X	X	X	X	0	1	0	0	X4
11/32	6/16	X	X	X	X	0	1	0	1	X5
13/32	7/16	X	X	X	X	0	1	1	0	X6
15/32	8/16	X	X	X	X	0	1	1	1	X7
17/32	9/16	X	X	X	X	1	0	0	0	X8
19/32	10/16	X	X	X	X	1	0	0	1	X9
21/32	11/16	X	X	X	X	1	0	1	0	XA
23/32	12/16	X	X	X	X	1	0	1	1	XB
25/32	13/16	X	X	X	X	1	1	0	0	XC
27/32	14/16	X	X	X	X	1	1	0	1	XD
29/32	15/16	X	X	X	X	1	1	1	0	XE
31/32	15/16 (max on)	X	X	X	X	1	1	1	1	XF

Table 8. Scan-Limit Register Format (Address (Hex) = XB)

SCAN LIMIT	REGISTER DATA								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
Display digit 0 only*	X	X	X	X	X	0	0	0	X0
Display digits 0 & 1*	X	X	X	X	X	0	0	1	X1
Display digits 0 1 2*	X	X	X	X	X	0	1	0	X2
Display digits 0 1 2 3	X	X	X	X	X	0	1	1	X3
Display digits 0 1 2 3 4	X	X	X	X	X	1	0	0	X4
Display digits 0 1 2 3 4 5	X	X	X	X	X	1	0	1	X5
Display digits 0 1 2 3 4 5 6	X	X	X	X	X	1	1	0	X6
Display digits 0 1 2 3 4 5 6 7	X	X	X	X	X	1	1	1	X7

*See *Scan-Limit Register* section for application.

Scan-Limit Register

The scan-limit register sets how many digits are displayed, from 1 to 8. They are displayed in a multiplexed manner with a typical display scan rate of 800Hz with 8 digits displayed. If fewer digits are displayed, the scan rate is $8f_{OSC}/N$, where N is the number of digits scanned. Since the number of scanned digits affects the display brightness, the scan-limit register should not be used to blank portions of the display (such as leading zero suppression). Table 8 lists the scan-limit register format.

If the scan-limit register is set for three digits or less, individual digit drivers will dissipate excessive amounts of power. Consequently, the value of the RSET resistor must be adjusted according to the number of digits displayed, to limit individual digit driver power dissipation. Table 9 lists the number of digits displayed and the corresponding maximum recommended segment current when the digit drivers are used.

Display-Test Register

The display-test register operates in two modes: normal and display test. Display-test mode turns all LEDs on by overriding, but not altering, all controls and digit registers (including the shutdown register). In display-test mode, 8 digits are scanned and the duty cycle is 31/32 (15/16 for MAX7221). Table 10 lists the display-test register format.

Table 9. Maximum Segment Current for 1-, 2-, or 3-Digit Displays

NUMBER OF DIGITS DISPLAYED	MAXIMUM SEGMENT CURRENT (mA)
1	10
2	20
3	30

Table 10. Display-Test Register Format (Address (Hex) = XF)

MODE	REGISTER DATA							
	D7	D6	D5	D4	D3	D2	D1	D0
Normal Operation	X	X	X	X	X	X	X	0
Display Test Mode	X	X	X	X	X	X	X	1

Note: The MAX7219/MAX7221 remain in display-test mode (all LEDs on) until the display-test register is reconfigured for normal operation.

No-Op Register

The no-op register is used when cascading MAX7219s or MAX7221s. Connect all devices' LOAD/$\overline{CS}$ inputs together and connect DOUT to DIN on adjacent devices. DOUT is a CMOS logic-level output that easily drives DIN of successively cascaded parts. (Refer to the *Serial Addressing Modes* section for detailed information on serial input/output timing.) For example, if four MAX7219s are cascaded, then to write to the fourth chip, sent the desired 16-bit word, followed by three no-op codes (hex XX0X, see Table 2). When LOAD/$\overline{CS}$ goes high, data is latched in all devices. The first three chips receive no-op commands, and the fourth receives the intended data.

Applications Information

Supply Bypassing and Wiring

To minimize power-supply ripple due to the peak digit driver currents, connect a 10µF electrolytic and a 0.1µF ceramic capacitor between V+ and GND as close to the device as possible. The MAX7219/MAX7221 should be placed in close proximity to the LED display, and connections should be kept as short as possible to minimize the effects of wiring inductance and electromagnetic interference. Also, both GND pins must be connected to ground.

Selecting RSET Resistor and Using External Drivers

The current per segment is approximately 100 times the current in ISET. To select RSET, see Table 11. The MAX7219/MAX7221's maximum recommended segment current is 40mA. For segment current levels above these levels, external digit drivers will be needed. In this application, the MAX7219/MAX7221 serve only as controllers for other high-current drivers or transistors. Therefore, to conserve power, use RSET = 47kΩ when using external current sources as segment drivers.

The example in Figure 2 uses the MAX7219/MAX7221's segment drivers, a MAX394 single-pole double-throw analog switch, and external transistors to drive 2.3" AND2307SLC common-cathode displays. The 5.6V zener diode has been added in series with the decimal point LED because the decimal point LED forward voltage is typically 4.2V. For all other segments the LED forward voltage is typically 8V. Since external transistors are used to sink current (DIG 0 and DIG 1 are used as logic switches), peak segment currents of 45mA are allowed even though only two digits are displayed. In applications where the MAX7219/MAX7221's digit drivers are used to sink current and fewer than four digits are displayed, Table 9 specifies the maximum allowable segment current. RSET must be selected accordingly (Table 11).

Refer to the Power Dissipation section of the Absolute Maximum Ratings to calculate acceptable limits for ambient temperature, segment current, and the LED forward-voltage drop.

Table 11. R_{SET} vs. Segment Current and LED Forward Voltage

I_{SEG} (mA)	V_{LED} (V)				
	1.5	2.0	2.5	3.0	3.5
40	12.2	11.8	11.0	10.6	9.69
30	17.8	17.1	15.8	15.0	14.0
20	29.8	28.0	25.9	24.5	22.6
10	66.7	63.7	59.3	55.4	51.2

Table 12. Package Thermal Resistance Data

PACKAGE	THERMAL RESISTANCE (θ_{JA})
24 Narrow DIP	+75°C/W
24 Wide SO	+85°C/W
24 CERDIP	+60°C/W
Maximum Junction Temperature (T_J) = +150°C	
Maximum Ambient Temperature (T_A) = +85°C	

Computing Power Dissipation

The upper limit for power dissipation (PD) for the MAX7219/MAX7221 is determined from the following equation:

$$PD = (V+ \times 8mA) + (V+ - V_{LED})(DUTY \times I_{SEG} \times N)$$

where:

V+ = supply voltage

DUTY = duty cycle set by intensity register

N = number of segments driven (worst case is 8)

V_{LED} = LED forward voltage

I_{SEG} = segment current set by R_{SET}

Dissipation Example:

I_{SEG} = 40mA, N = 8, DUTY = 31/32, V_{LED} = 1.8V at 40mA, V+ = 5.25V

$PD = 5.25V(8mA) + (5.25V - 1.8V)(31/32 \times 40mA \times 8) = 1.11W$

Thus, for a CERDIP package (θ_{JA} = +60°C/W from Table 12), the maximum allowed ambient temperature T_A is given by:

$$T_{J(MAX)} = T_A + PD \times \theta_{JA} + 150°C = T_A + 1.11W \times 60°C/W$$

where T_A = +83.4°C.

Cascading Drivers

The example in Figure 3 drives 16 digits using a 3-wire µP interface. If the number of digits is not a multiple of 8, set both drivers' scan limits registers to the same number so one display will not appear brighter than the other. For example, if 12 digits are need, use 6 digits per display with both scan-limit registers set for 6 digits so that both displays have a 1/6 duty cycle per digit. If 11 digits are needed, set both scan-limit registers for 6 digits and leave one digit driver unconnected. If one display for 6 digits and the other for 5 digits, the second display will appear brighter because its duty cycle per digit will be 1/5 while the first display's will be 1/6. Refer to the *No-Op Register* section for additional information.

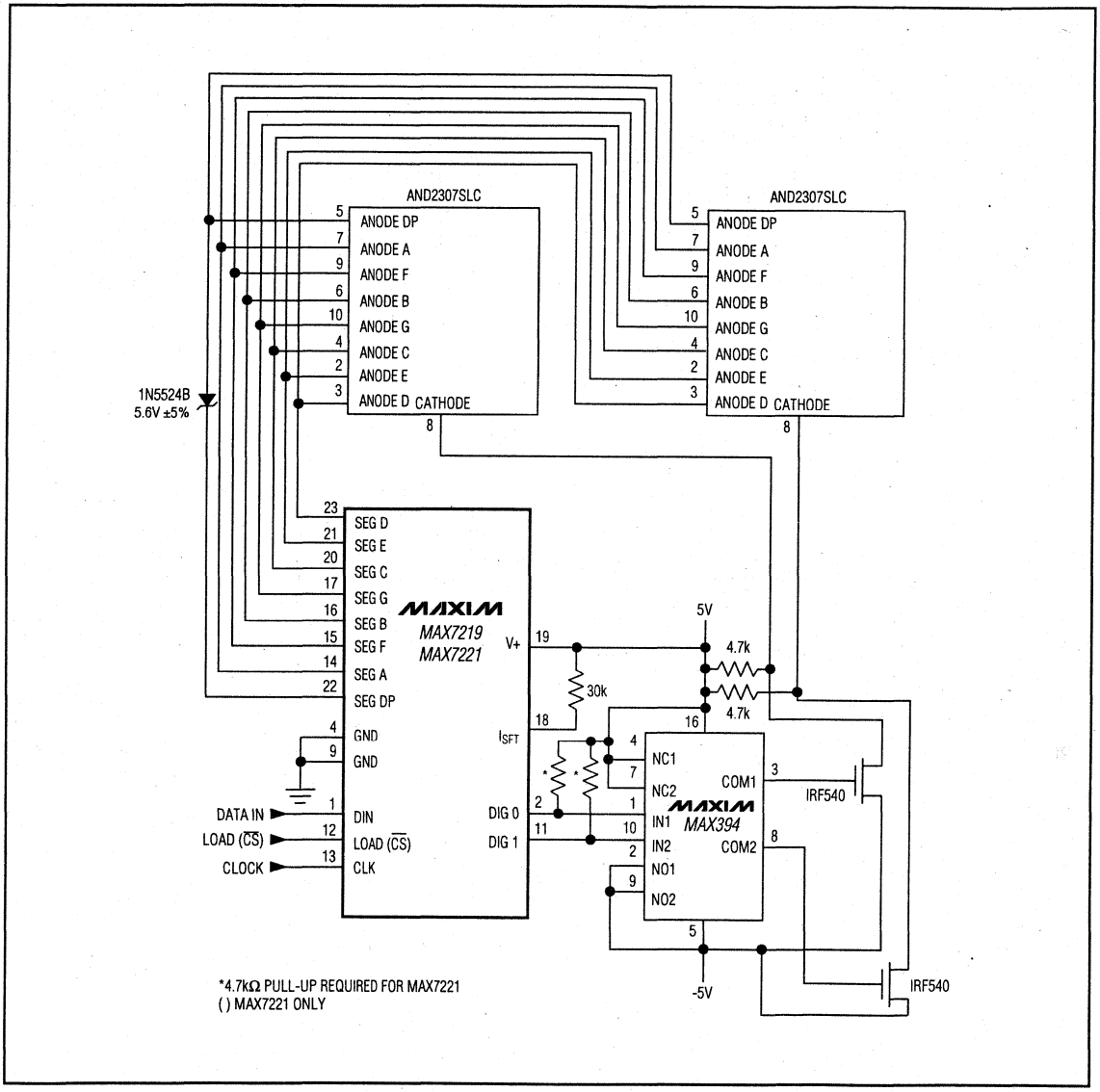


Figure 2. MAX7219/MAX7221 Driving 2.3-Inch Displays

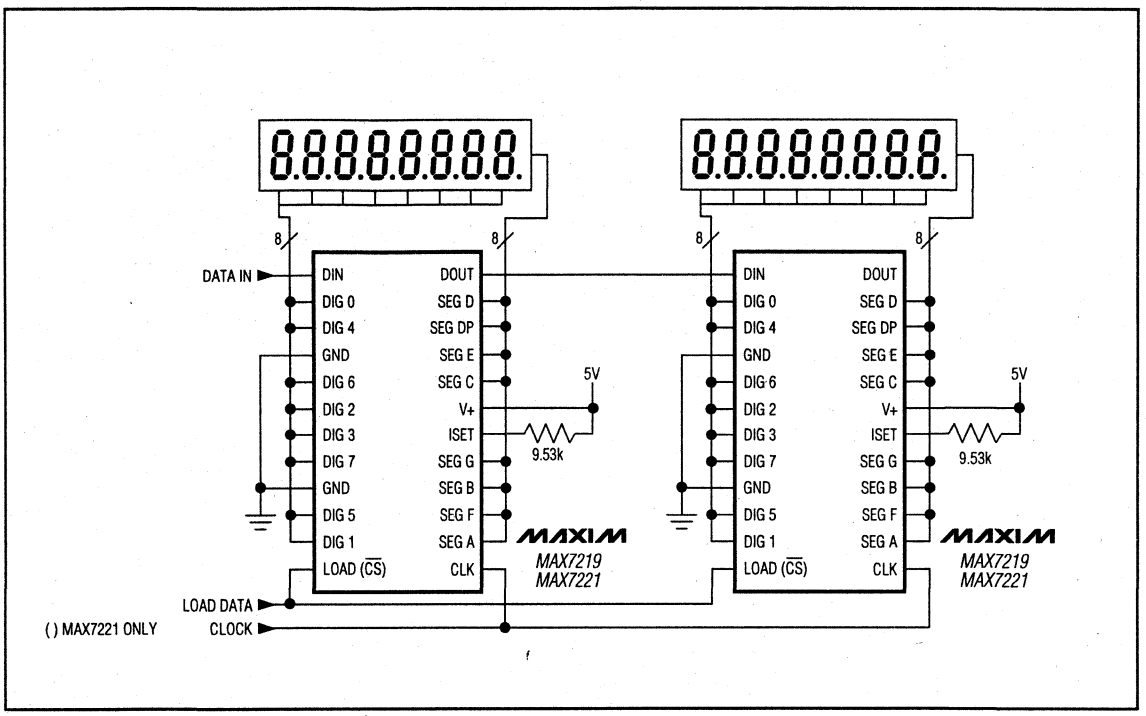


Figure 3. Cascading MAX7219/MAX7221s to Drive 16 7-Segment LED Digits

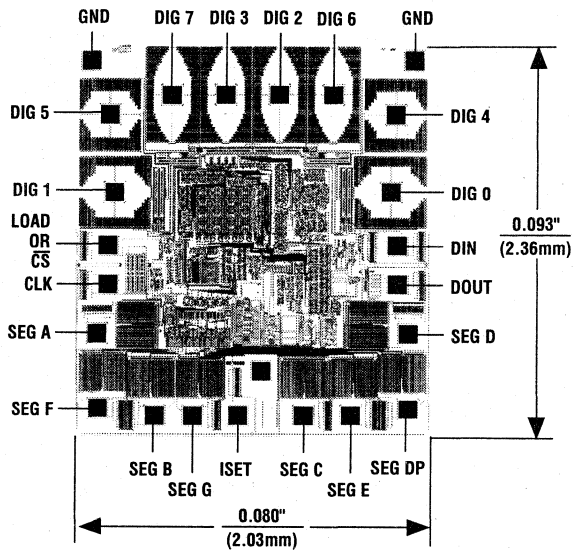
Serially Interfaced, 8-Digit LED Display Drivers

_Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX7221CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX7221CWG	0°C to +70°C	24 Wide SO
MAX7221C/D	0°C to +70°C	Dice*
MAX7221ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX7221EWG	-40°C to +85°C	24 Wide SO
MAX7221ERG	-40°C to +85°C	24 Narrow CERDIP

*Dice are specified at T_A = +25°C.

Chip Topography



TRANSISTOR COUNT: 5267

SUBSTRATE CONNECTED TO GND

Appendix

Evaluation Kits/Design Software Tables A-2
Packaged Products A-5
Surface-Mount Products A-6
Die and Wafer Products A-7
Maxim's /883B and High-Reliability Program A-9
Maxim's Military Program A-11
Product Numbering Systems A-12
Package Information A-13

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
A/D CONVERTERS (<1Msps)			
MAX110/MAX111	MAX110EVKIT-DIP	MAX111CPE	55.00
	MAX110EVC32-DIP**		150.00
MAX117/MAX118	MAX117EVKIT-DIP	MAX118CPI	48.00
MAX120/MAX122	MAX120EVKIT-DIP	MAX122BCNG	82.00
MAX121	MAX121EVKIT-DIP		85.00
MAX125	MAX125EVKIT-SSOP		††
	MAX125EVB16-SSOP**		††
MAX126	MAX126EVKIT-SSOP		††
	MAX126EVB16-SSOP**		††
MAX132	MAX132EVKIT-DIP**		95.00
MAX134	MAX134EVSYS1-DIP		†††
MAX146/MAX147	MAX147EVKIT-DIP	MAX146BCPP	55.00
	MAX147EVC32-DIP**		150.00
	MAX147EVC16-DIP**		150.00
MAX152/MAX153	MAX152EVKIT-DIP	MAX153CPP	65.00
MAX155	MAX155EVKIT-DIP**		95.00
MAX176	MAX176EVKIT-DIP		82.00
MAX180/MAX181	MAX180EVKIT-DIP**	MAX181CCPL	95.00
MAX186/MAX188	MAX186EVKIT-DIP	MAX188DCPP	55.00
	MAX186EVSYS-DIP**		150.00
MAX187/MAX189	MAX187EVKIT-DIP	MAX189BCPA	55.00
	MAX187EVC16-DIP**	MAX189BCPA	150.00
MAX190	MAX190EVKIT-DIP**		95.00
MAX191	MAX191EVKIT-DIP		55.00
	MAX191EVSYS-DIP**		150.00
MAX194	MAX194EVKIT-DIP		55.00
	MAX194EVC16-DIP**		150.00
MAX195	MAX195EVKIT-DIP		55.00
	MAX195EVC16-DIP**		150.00
MAX196/MAX198	MAX196EVKIT-DIP	MAX198BCNI	55.00
MAX197/MAX199	MAX197EVKIT-DIP	MAX199BCNI	55.00
	MAX197EVC16-DIP**		150.00
	MAX197EVC32-DIP**		150.00
MAX1110/MAX1112	MAX1110EVKIT-DIP	MAX1112CPP	36.00
	MAX1110EVL11-DIP**	MAX1112CPP	95.00
MAX1202/MAX1203	MAX1202EVKIT-DIP	MAX1203BCPP	39.00
	MAX1202EVL11-DIP**		95.00
MAX1240/MAX1241	MAX1241EVKIT-DIP	MAX1240BCPA	39.00
	MAX1241EVL11-DIP**		95.00
MAX1246	MAX1246EVKIT-QSOP		39.00
	MAX1246EVL11-QSOP**		95.00
MAX1247	MAX1247EVKIT-QSOP		39.00
	MAX1247EVL11-QSOP**		95.00

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
A/D CONVERTERS (>1Msps)			
MAX100	MAX100EVKIT		†††
MAX101A	MAX101AEVKIT		†††
MAX104	MAX104EVKIT		†††
MAX1002/MAX1003	MAX1002EVKIT	MAX1003CAX*	†††
MAX1114	MAX1114EVKIT		†††
MAX1125	MAX1125EVKIT		†††
MAX1150/MAX1151	MAX1150EVKIT		†††
MAX1160/MAX1161	MAX1160EVKIT		†††
MAX1170/1171/1172	MAX1170EVKIT		†††
D/A CONVERTERS			
MAX555	MAX555EVKIT		195.00
ANALOG FILTERS			
MAX274	MAX274EVKIT-DIP		20.00
FUNCTION GENERATOR			
MAX038	MAX038EVKIT-DIP		89.00
INTERFACE PRODUCTS			
MAX212	MAX212EVKIT-SO		38.00
OP AMPS/VIDEO PRODUCTS			
MAX458/MAX459	MAX459EVKIT-DIP	MAX458CQH	72.00
MAX464/MAX466	MAX466EVKIT-SO	MAX464CWI	67.00
MAX477	MAX477EVKIT-SO		31.25
MAX496/MAX497	MAX497EVKIT-SO	MAX496CSE	60.00
MAX498	MAX498EVKIT-SO		60.00
MAX4100/MAX4101	MAX4100EVKIT-SO	MAX4101ESA	31.25
MAX4102/MAX4103	MAX4103EVKIT-SO	MAX4102ESA	31.25
MAX4106/MAX4107	MAX4106EVKIT-SO	MAX4107ESA	31.25
MAX4108/MAX4109	MAX4108EVKIT-SO	MAX4109ESA	31.25
MAX4111/MAX4121	MAX4121EVKIT-SO	MAX4111CSA	31.25
MAX4112/MAX4113	MAX4112EVKIT-SO	MAX4113ESA	31.25
MAX4117/MAX4118	MAX4117EVKIT	MAX4118ESA	31.25
MAX4135–MAX4138	MAX4135EVKIT-SO	MAX4136/MAX4137/MAX4138EWG	31.25
MAX4141	MAX4141EVKIT-SO		31.25
MAX4144	MAX4144EVKIT-SO		31.25
MAX4146	MAX4146EVKIT-SO		††
MAX4147	MAX4147EVKIT-SO		31.25
MAX4159/MAX4259	MAX4159EVKIT-SO	MAX4259ESD	33.75
MAX4178/MAX4278	MAX4278EVKIT-SO	MAX4178ESA	31.25
MAX4180/MAX4181	MAX4180EVKIT-SO	MAX4181ESA	28.75
MAX4189	MAX4189EVKIT-SO		††
MAX4213	MAX4213EVKIT-SO		27.50
MAX4221	MAX4221EVKIT-SO		31.25
MAX4223/MAX4224	MAX4223EVKIT-SO	MAX4224ESA	28.75

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

** Includes microcontroller

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‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability.

††† *Contact factory for pricing.*

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
POWER SUPPLIES			
MAX606/MAX607	MAX606EVKIT-MM	MAX607EUA	60.00
MAX608	MAX608EVKIT-SO		35.00
MAX619	MAX619EVKIT-SO		25.00
MAX629	MAX629EVKIT		75.00
MAX639/MAX640/MAX653	MAX639EVKIT-DIP	MAX640/MAX653CPA	20.00
	MAX639EVKIT-SO	MAX640/MAX653CSA	20.00
MAX662A	MAX662EVKIT-SO	MAX662ACSA	20.00
MAX679	MAX679EVKIT		25.00
MAX682‡	MAX682EVKIT		††
MAX683‡/MAX684‡	MAX684EVKIT	MAX683EUA	††
MAX685	MAX685EVKIT		††
MAX686‡	MAX686EVKIT		††
MAX688/MAX689	MAX688EVKIT-SO	MAX689CSA	60.00
MAX710‡/MAX711‡	MAX710EVKIT	MAX711ESE	50.00
MAX712/MAX713	MAX712EVKIT-DIP	MAX713CPE	60.00
	MAX713SWEVKIT-SO	MAX712CSE	60.00
MAX717/MAX718/MAX719	MAX718EVKIT-SO	MAX717/MAX719CSE	30.00
MAX722/MAX723	MAX722EVKIT-SO	MAX723CSE	30.00
MAX730A/738A/744A/	MAX738EVKIT-DIP	MAX730/744/748/763ACPA	20.00
748A/763A	MAX738EVKIT-SO	MAX730/763ACSA, MAX744/748ACWE	20.00
MAX731	MAX731EVKIT-DIP		20.00
MAX732/MAX733/MAX752	MAX752EVKIT-DIP	MAX732/MAX733CPA	20.00
	MAX732EVKIT-SO		20.00
MAX734	MAX734EVKIT-SO		20.00
MAX736/737/739/759	MAX739EVKIT-DIP	MAX736/737/759CPD	20.00
MAX742	MAX742EVKIT-SO		50.00
MAX743	MAX743EVKIT-DIP		20.00
MAX745	MAX745EVKIT		120.00
MAX749	MAX749EVKIT-SO		20.00
MAX750A/MAX758A	MAX758EVKIT-DIP	MAX750ACPA	20.00
	MAX758EVKIT-SO	MAX750ACSA	20.00
MAX752	MAX752EVKIT-DIP		20.00
MAX756/MAX757	MAX756EVKIT-SO	MAX757CSA	25.00
MAX759	MAX759LCDKIT-SO		30.00
	MAX739EVKIT-DIP	MAX759CPD	20.00
MAX761/MAX762	MAX761EVKIT-SO	MAX762CSA	25.00
MAX764/MAX765/MAX766	MAX764EVKIT-SO	MAX765/MAX766CSA	35.00
MAX767	MAX767EVKIT-SO		60.00
MAX770/MAX771/MAX772	MAX770EVKIT-SO	MAX771/MAX772CSA	35.00
MAX774/MAX775/MAX776	MAX774EVKIT-SO	MAX775/MAX776CSA	35.00
MAX777L/MAX778L/MAX779L	MAX778LEVKIT-SO	MAX777/MAX779LCSA	25.00
MAX782	MAX782EVKIT-SO		95.00
MAX783	MAX783EVKIT-SO		95.00
MAX786	MAX786EVKIT-SO		95.00
MAX796/MAX799	MAX796EVKIT-SO	MAX799CSE	60.00
MAX797	MAX797EVKIT-SO		60.00
MAX830–MAX833	MAX831EVKIT-SO	MAX830/832/833CWE	60.00
MAX840/MAX843/MAX844	MAX840EVKIT-SO	MAX843/MAX844ISA	35.00
MAX845	MAX845EVKIT-MM		35.00
MAX846A	MAX846EVKIT		75.00
MAX848/MAX849	MAX848EVKIT	MAX349ESE	75.00
MAX850–MAX853	MAX850EVKIT-SO	MAX851/852/853ISA	35.00
MAX856–MAX859	MAX856EVKIT-MM	MAX857/858/859CUA	35.00
MAX863	MAX863EVKIT		50.00
MAX866/MAX867	MAX866EVKIT-MM	MAX867EUA	35.00
MAX881R	MAX881EVKIT		††
MAX887	MAX887EVKIT		75.00
MAX1610/MAX1611	MAX1611EVKIT-SO	MAX1610CSE	†††
MAX1624	MAX1624EVKIT		75.00
MAX1625	MAX1625EVKIT		75.00
MAX1626/MAX1627	MAX1626EVKIT-SO	MAX1627ESA	35.00
MAX1630/MAX1633	MAX1630EVKIT-SO	MAX1633CAI	†††
MAX1631/MAX1634	MAX1631EVKIT-SO	MAX1634CAI	†††
MAX1632/MAX1635	MAX1632EVKIT-SO	MAX1635CAI	†††
MAX1636‡	MAX1636EVKIT-SO		††
MAX1638‡	MAX1638EVKIT-SO		††
MAX1640/MAX1641	MAX1640EVKIT	MAX1641EEE	125.00
MAX1642/MAX1643	MAX1642EVKIT	MAX1643EUA	50.00
MAX1649/MAX1651	MAX1649EVKIT-SO	MAX1651CSA	35.00
MAX1652‡–MAX1655‡	MAX1653EVKIT	MAX1652/1654/1655EEE	††
MAX1672‡/MAX1673‡	MAX1672EVKIT	MAX1673ESA	††
MAX1700‡	MAX1700EVKIT		††
MAX1703‡	MAX1703EVKIT		††
MAX1705/MAX1706	MAX1705EVKIT	MAX1706EEE	60.00
MAX1771	MAX1771EVKIT-SO		35.00
MAX2003/MAX2003A	MAX2003AEVKIT-SO	MAX2003CSE	125.00
WIRELESS PRODUCTS (High Frequency)			
MAX2101	MAX2101EVKIT-SO		†††
MAX2102	MAX2102EVKIT-SO		250.00
MAX2402	MAX2402EVKIT-SO		†††
MAX2406‡	MAX2406EVKIT-SO		††
MAX2410‡	MAX2410EVKIT-SO		††
MAX2411A‡	MAX2411AEVKIT-SO		††
MAX2420	MAX2420EVKIT-SO		145.00
MAX2421‡	MAX2421EVKIT-SO		††
MAX2422‡	MAX2422EVKIT-SO		††
MAX2424‡	MAX2424EVKIT-SO		††
MAX2426‡	MAX2426EVKIT-SO		††
MAX2430ISE	MAX2430EVKIT-SO		99.00
MAX2430IEE‡	MAX2430EVKIT-QSOP		††
MAX2460‡	MAX2460EVKIT-SO		††
MAX2463‡	MAX2463EVKIT-SO		††

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

** Includes microcontroller

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‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability.

††† Contact factory for pricing.

Evaluation Kits/Design Software

Part Number	EV Kit	Order Free Sample*	EV Kit Price†($)
MAX2510‡	MAX2510EVKIT-SO		††
MAX2511	MAX2511EVKIT-SO		95.00
MAX2450/MAX2451/MAX2452	MAX2450EVKIT-SO	MAX2451/MAX2452CSE	†††
MAX2611	MAX2611PCB		††
MAX2620	MAX2620EVKIT-SO		95.00
MAX2630–MAX2633	MAX2633PCB	MAX2630EUS, 2633EUT, MAX2631/MAX2632EUK	50.00
MAX2650	MAX2650PCB		50.00
MAX2662‡	MAX2662EVKIT-SO		††
MAX2670‡	MAX2670EVKIT-SO		††
MAX2672‡	MAX2672EVKIT-SO		††
MAX2673‡	MAX2673EVKIT-SO		††
MAX2690‡	MAX2690EVKIT-SO		††
FIBER/CABLE COMMUNICATIONS PRODUCTS			
MAX3261	MAX3261EVKIT-SO		150.00
MAX3664	MAX3664EVKIT-SO		192.00
MAX3680	MAX3680EVKIT		†††
MAX3681	MAX3681EVKIT		192.00
MAX3691	MAX3691EVKIT		†††
MAX3761	MAX3761EVKIT-SO		192.00
MAX3762	MAX3762EVKIT-SO		192.00

Design Software

Part Number	Description	Price† ($)
MAX260SOFT	Filter design software for MAX260–MAX268	5.00
MAX274SOFT	Filter design software for MAX274/MAX275	5.00

Description	Price† ($)
Op-Amp/Comparator P-Spice Models	FREE

* Some kits are used to evaluate more than one device. In these cases, order the indicated EV kit and a free sample of the device you wish to evaluate.

** Includes microcontroller

‡ Future product—contact factory for pricing and availability.

†† Future EV kit—contact factory for pricing and availability

Wafer Inspection

All wafers are fabricated using standard processes with extremely tight control. Each wafer must pass numerous in-process checkpoints for oxide thickness, critical dimensions, pin-hole densities, and other requirements. And, each must comply with Maxim's demanding electrical and physical specifications.

Finished wafers are optically inspected for physical defects. They are then parametrically tested to ensure full conformity to Maxim's specifications. Our precision parametric measurement capability ensures reliability and reproducibility in analog circuits. We believe this quality-control technology to be the best in the industry, capable of resolving current levels below 1pA and capacitance less than 1pF. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface-state density, and other parameters that are crucial to predicting long-term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.

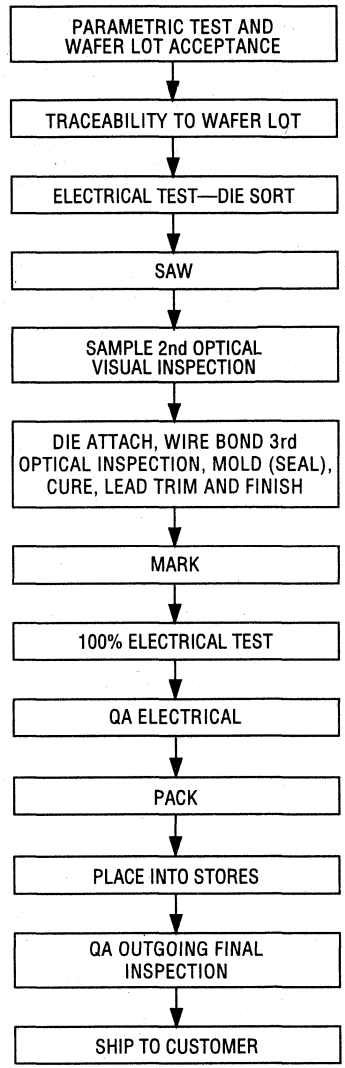
Testing

Sophisticated testing is an integral part of delivering the highest quality data-acquisition products. Maxim's analog test capability is a significant improvement in accuracy, noise performance, and speed compared to current industry standards. This provides our customers with assurance that they will receive the part they paid for every time, without fail.

Product Conditioning and Qualification

Maxim routinely monitors the products and processes through qualification testing, including Life Test, 85/85, Pressure Pot, Temperature Cycling, Long-Term Storage, and HAST testing. See Maxim's full *Product Reliability Report* (RR-1K) for more information.

Typical Packaged-Unit Process Flow



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Surface-Mount Products

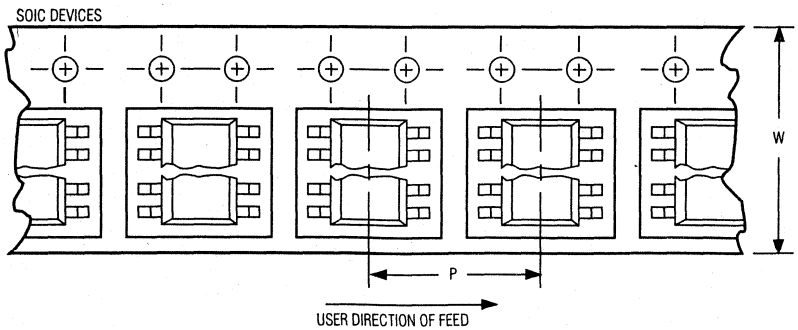
Maxim is committed to providing high-quality, high-reliability surface-mount products. Nearly every product is offered in a surface-mount package. Surface-mount products are tested through the same production flow as dual-in-line (DIP) plastic devices, and are tested to the same stringent electrical and visual AQL levels. Product qualification and reliability monitoring programs for DIP and surface-mount products are identical.

Surface-Mount Packages in Reeled Tape

Maxim surface-mount packages are shipped in antistatic plastic rails. For customers using automatic placement systems, parts also come mounted in pockets on embossed tape. The tape is wound and shipped on reels.

The table and diagram on this page indicate the tape sizes used for various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
Package	Pins		
SOIC	8	12	8
	14	16	8
	16	16	8
SOIC	16	16	12
	18	24	16
	20	24	12
	24	24	12
	28	24	12
PLCC	20	16	12
	28	24	16
	44	32	24
QFP	44	24	16
SOT	3	8	4
	4	8	4
SSOP	16	16	12
	20	16	12
	24	16	12
	28	16	12
	36	24	12
µMAX	8	12	8
	10	12	8
TQFP	32	16	12
	48	16	12
QSOP	16	12	8
SOT	3	8	4
	4	8	4
	5	8	4
	6	8	4



Die and Wafer Products

Many of Maxim's standard CMOS products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample that is assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow," the standard that ensures lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet's +25°C worst-case limits.

Generally, the parameters or parameter limits listed in the product data sheets are tested during electrical probe. However, some parameters are impossible to test, or to test with absolute accuracy on unassembled product. Information regarding any of these parameters or parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	VALUE	UNITS
Chip Thickness Backlapped Wafers	15 ±1	mils
Die Length/Width Tolerance	±1	mils
Bonding Pad Dimensions (minimum)	typical min = 3.5 x 3.5	mils
Bonding Pad and Interconnect Material Thickness	10 to 12	kÅ
Storage Temperature	-40 to +150	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B, with modifications reflecting CMOS requirements.

Each die surface is protected by a passivation layer, except for bonding pads and scribe lines. Surface passivation is removed from bonding-pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to the aluminum's surface roughness after the etching process.

Maxim guarantees die and wafer AQL levels as follows:

Visual.....1.0%
Functional Electrical Testing.....0.65%
Parametric DC Testing.....2.5%
Untested Parameters.....6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry environment—preferably an inert gas such as nitrogen. Extreme care should be taken when handling die. An unclean environment or mishandling may result in electrical and visual failure.

Die Attach

For eutectic die attach, we recommend using a 98% gold/2% silicon preform, at a die-attach temperature between 385°C and 435°C. To prevent oxidation, die attach should be done in a gaseous nitrogen ambient atmosphere. For epoxy die attach, the epoxy cure temperature should not exceed 150°C.

Bonding

When thermosonic or thermocompression gold ball bonding, use 1.0 or 1.3 mil diameter, 99.99% pure gold wire. When ultrasonic bonding, use 1.0 or 1.25 mil diameter, 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Figures 1 and 2 show how die and wafers are packaged for shipping.

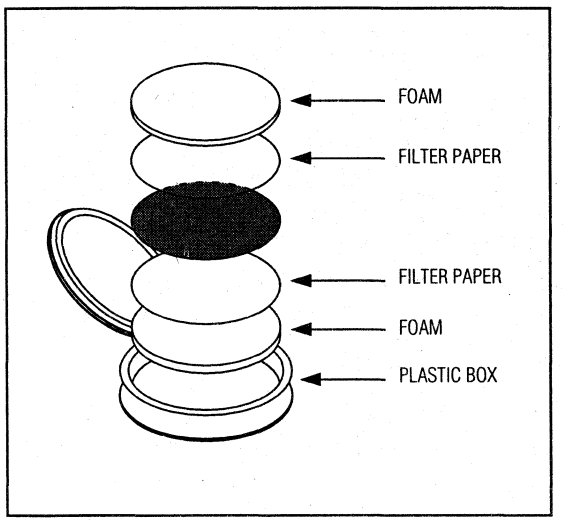


Figure 1. Wafer Carrier Package

A

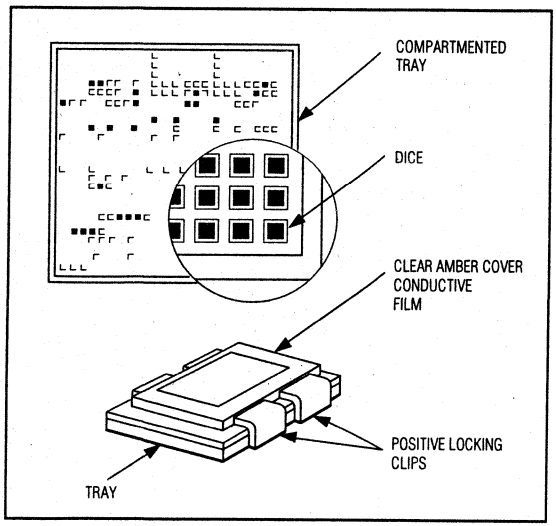


Figure 2. Die Carrier Package

Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. These improvements may result in slight changes in geometry, die electrical limits, pad layouts, or maximum die size. These changes are kept to a minimum, and we strive to notify customers whenever possible.

User Responsibility

Written notification of any nonconformance by Maxim or Maxim's dice specifications must be made within 60 days of the date the die is shipped to the user. Maxim assumes no responsibility for the die after 60 days or after further user processing such as, but not limited to, die attach or wire bonding.

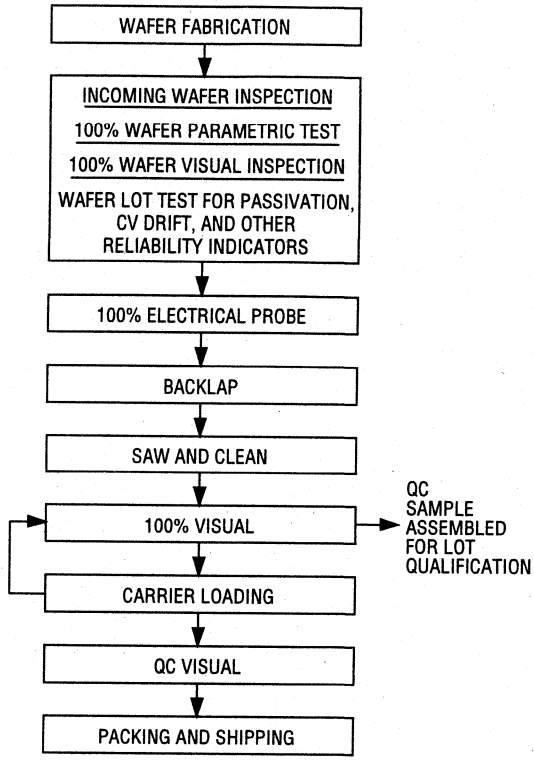
Ordering Information

Die orders are identified by a "/D" suffix. Example: ICL7109C/D.

When ordering dice as wafers, replace the "D" with a "W" in the part number. Example: MAX7231C/D die = MAX7231C/W wafer.

Contact the factory for availability.

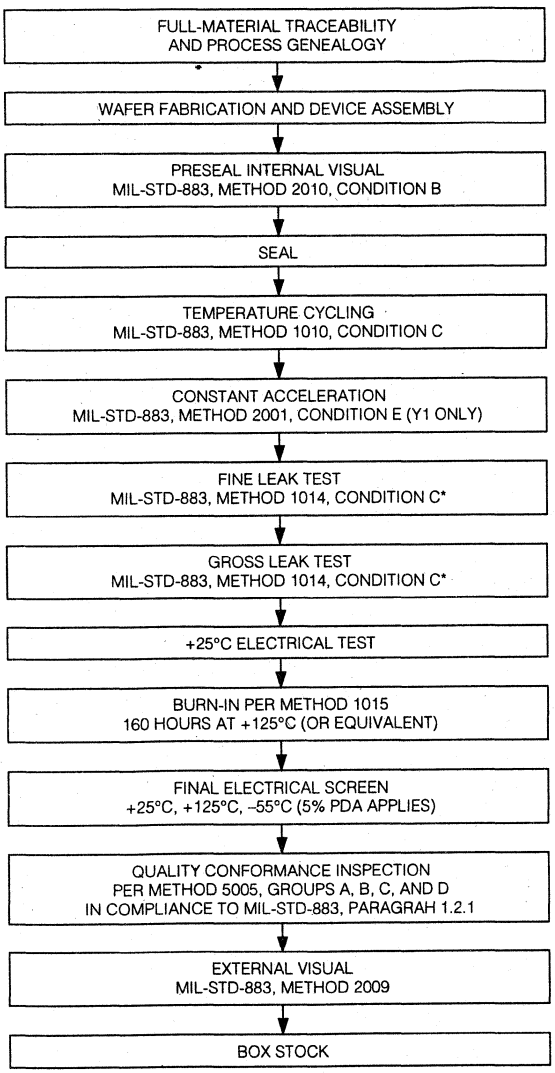
Die Process Flow



/883B Flow

Maxim's /883B flow is fully compliant to MIL-STD-883, paragraph 1.2.1. Environmental and electrical screening are performed per Method 5004, Class B of MIL-STD-883B. Quality conformance inspection is performed per method 5005 (Groups A, B, C, and D).

/883B Process Flow



**If seal perimeter is greater than 2.0 inches, Condition A applies.*

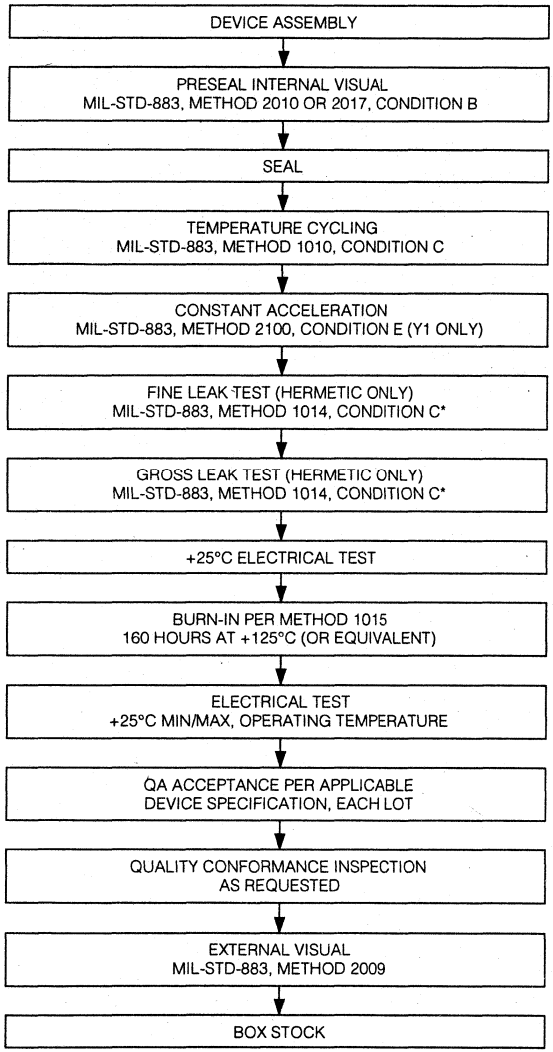
/HR Flow

Maxim's High Reliability (/HR) flow is offered for hybrid products as well as for products that have not yet been fully certified compliant to MIL-STD-883B, and are therefore noncompliant. The /HR flow will not be offered for parts certified to MIL-STD-883B.

As shown in the adjacent flow chart, the /HR process flow closely follows the steps and requirements of the MIL-STD-883B flow. Product processed to this flow is not documented in as much detail, nor does it have to adhere to the operating temperature range required by MIL-STD-883B. The /HR flow may also be used to screen product over the commercial (0°C to +70°C) and extended (–40°C to +85°C) temperature ranges. This flow applies to hermetic packaged product only.

It is Maxim's experience that this flow is desired by companies having older government projects or projects requiring an inherently higher reliability screening for critical application environments. Full QCI testing will be performed when requested. Only Group A will be performed per each inspection lot.

/HR Process Flow

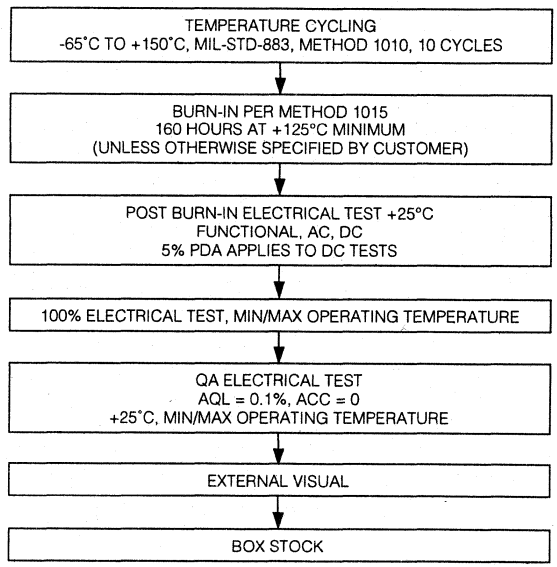


**If seal perimeter is greater than 2.0 inches, Condition A applies.*

Rugged Plastic Flow

In addition to the /883B and /HR screening flows, Maxim offers an extended rugged-plastic screening flow for plastic-encapsulated packages, including SOIC package types. Products screened to this flow can be used in high-reliability applications when hermetically sealed devices screened to MIL-STD-883 may not be justified. SOICs with full burn-in and screening not only offer excellent reliability, but also save valuable PC board space. Customers should contact the factory for availability of the specific device types currently offered.

Rugged-Plastic Process Flow



DESC Approved Devices to Standard Military Drawings (SMDs) Currently Available

MAXIM P/N	SMD NUMBER
MAX1044	5962-38707
MAX1232	5962-94514
MAX1259	5962-93264
MAX220/22/ 32A/42/43	5962-94565
MAX230/1/2/4/6-9	5962-89877
MAX280	5962-91595
MAX310/311	5962-94556
MAX333	5962-93180
MAX358	77052
MAX359	5962-85131
MAX4420/4429	5962-88770
MAX452-455	5962-94512
MAX500	5962-94527
MAX502	5962-88767
MAX532	5962-95667
MAX543	5962-92345
MAX630	5962-94540
MAX631/632/633	5962-92141
MAX634	5962-92124
MAX638	5962-92127
MAX641	5962-93254
MAX660	5962-94632
MAX663/4/6/7	5962-92126
MAX674	5962-94681
MAX680	5962-93120
MAX690/692/694	5962-90712
MAX691/693/695	5962-90711
MAX696/697	5962-93125
MAX705-708	5962-93267
MAX731/732/733	5962-94621
MAX738	5962-93121
MAX813L	5962-93267
MAX8211/8212	5962-90811
MX536A	5962-89805
MX574A	5962-85127
MX580	5962-86861
MX584	5962-38128
MX7226	5962-87802
MX7524	5962-87700
MX7528	5962-87701
MX7537	5962-87763
MX7541	5962-89481
MX7545	5962-87702
MX7547	5962-89657
MX7572	5962-87591
MX7574	5962-89616
MX7820	5962-88650
MX7824/7828	5962-88764
MXL1062	5962-91595
DG201A	77053
DG403	5962-89763
DG405	5962-89961
DG408/409	5962-92042
DG411/412/413	5962-90731
DG417/418/419	5962-90737
DG441/442	5962-92041
DG506A/7A/9A	5962-85131
DG508A	77052
DG528	5962-87689
HI-201	77053
ICL7660A	5962-38707
ICL7667	5962-87660
IH5040-5045	81006
IH5047	81006
IH5140-5145	81006
IH5148-5151	81006
REF01	5962-89581
REF02	85514
TSC426/427/428	5962-88503

Parts Currently /883B Compliant

MAX1044
MAX122
MAX1232
MAX1259
MAX154/158
MAX160/161
MAX170/172
MAX176
MAX180/181
MAX186/188
MAX220/222
MAX230/231/232
MAX232A
MAX234
MAX236-239
MAX242/243
MAX274
MAX280
MAX291
MAX310/311
MAX333
MAX358/359
MAX378/379
MAX4420/4426-9
MAX452-455
MAX481/483/485
MAX500
MAX502
MAX516
MAX526/527
MAX532
MAX543
MAX626/627/628
MAX630-634/638
MAX641
MAX660
MAX663/4/6/7
MAX674
MAX680
MAX690-697
MAX690A/692A
MAX691A/693A
MAX705-708
MAX730-733
MAX738
MAX805L
MAX813L
MAX8211/8212
MX536A
MX565
MX574A
MX580/581/584
MX674A
MX7225/7226
MX7501/2/3
MX7520/1/4/8
MX7533/7537
MX7541/2/3/5/7
MX7549
MX7572/7574
MX7628
MX7820/1/4/8
MXL1062
DG200A/201A/202
DG300A-309
DG381A/4A/7A
DG390A
DG401/403/405
DG406-409
DG411/412/413
DG417/418/419
DG441/442
DG506A-509A
DG528/529
HI-201/201HS
ICL7660A/7667
IH5040-5049
IH5050/5051
IH5140-5145
IH5147/5148/5151
IH5341/5352
OP07
REF01/02
TSC426/427/428

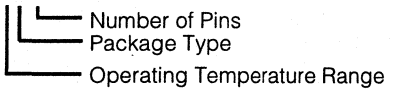
A

Proprietary Numbering System

Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped into categories, according to their functions. Maxim currently adds a "MAX" prefix to the part's unique number.

3-Letter Suffixes

EXAMPLE:
MAX358CPD



4-Letter Suffixes

When a part has a four-letter suffix, the first letter of the suffix denotes product grade. For example, the first "A" in MAX631ACPA indicates 5% output accuracy; the remaining three letters denote temperature range, package type, and number of pins. Therefore, the MAX631ACPA has 5% output accuracy, operates over the 0°C to +70°C range, comes in a plastic DIP package, and has eight pins.

Temperature Ranges

"C"	0°C to +70°C	"E"	-40°C to +85°C
"I"	-20°C to +85°C	"M"	-55°C to +125°C

Package Type

"A"	SSOP (Shrink Small-Outline Package)
"B"	CERQUAD
"C"	TO-220, TQFP (Thin Quad Flat Pack)
"D"	Ceramic Sidebraze
"E"	QSOP (Quarter Small-Outline Package)
"F"	Ceramic Flat Pack
"H"	Module, SBGA (Super Ball Grid Array)
"J"	CERDIP Dual-In-Line
"K"	TO-3, PPGA
"L"	LCC (Leadless Ceramic Chip Carrier)
"M"	MQFP (Metric Quad Flat Pack)
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	PLCC (Plastic Leaded Chip Carrier)
"R"	Narrow CERDIP (300 mil)
"S"	Small Outline (150 mil), TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-99, TO-100)
"U"	TSSOP, µMAX, SOT
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Y"	Narrow Sidebraze (300 mil)
"Z"	TO-92, MQUAD
"/D"	Dice
"/PR"	Rugged Plastic
"/W"	Wafer

Number of Pins

"A"	8	"N"	18
"B"	10, 64	"O"	42
"C"	12, 192	"P"	20
"D"	14	"Q"	2, 100
"E"	16	"R"	3, 84
"F"	22, 256	"S"	4, 80
"G"	24	"T"	6, 160
"H"	44	"U"	60
"I"	28	"V"	8 (0.200" pin circle, isolated case)
"J"	32	"W"	10 (0.230" pin circle, isolated case)
"K"	5, 68	"X"	36
"L"	40	"Y"	8 (0.200" pin circle, isolated case)
"M"	7, 48	"Z"	10 (0.230" pin circle, isolated case)

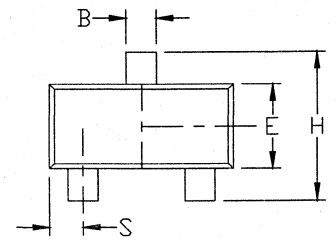
Second-Source Numbering System

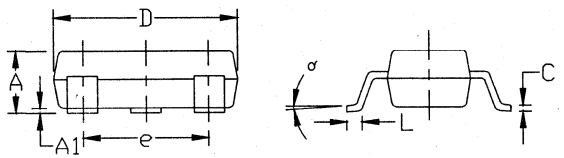
In most cases, Maxim's part number for a second-source product follows the industry's most widely accepted numbering system for that particular part, rather than our own convention. This includes the most commonly recognized prefix as well as the original designators for product grade, temperature range, package type, and number of pins.

Maxim frequently supplies second-source products in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, these devices are given a part number that follows the original numbering convention.

SOTPO3LEPS

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

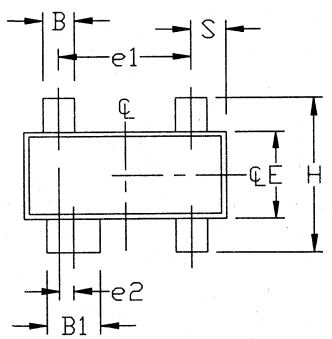




	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e	0.070	0.080	1.778	2.032
H	0.082	0.098	2.083	2.489
L	0.004	0.012	0.102	0.305
S	0.017	0.022	0.432	0.559
α	0°	8°	0°	8°

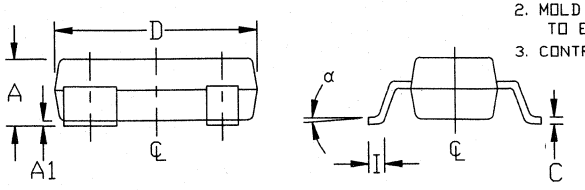
MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,SOT-23, 3L
APPROVAL | DOCUMENT CONTROL NO. 21-0051 | REV C | 1/1

SOT143EPS



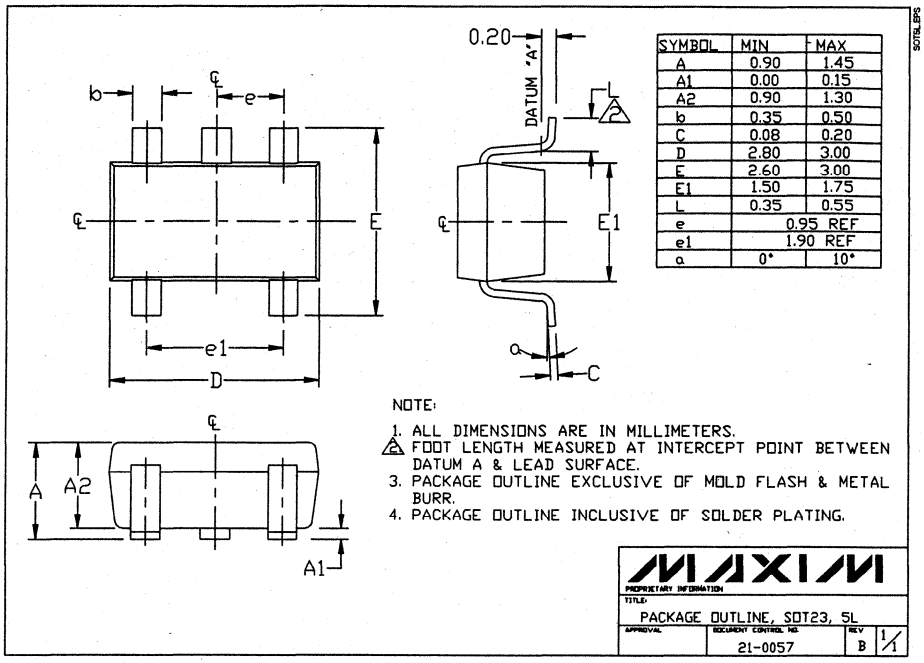
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.031	0.047	0.787	1.194
A1	0.001	0.005	0.025	0.127
B	0.014	0.022	0.356	0.559
B1	0.030	0.038	0.762	0.965
C	0.0034	0.006	0.086	0.152
D	0.105	0.120	2.667	3.048
E	0.047	0.055	1.194	1.397
e1	0.071	0.079	1.803	2.007
e2	0.008 BSC		0.200 BSC	
H	0.082	0.098	2.083	2.489
I	0.004	0.012	0.102	0.305
S	0.018	0.024	0.450	0.600
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

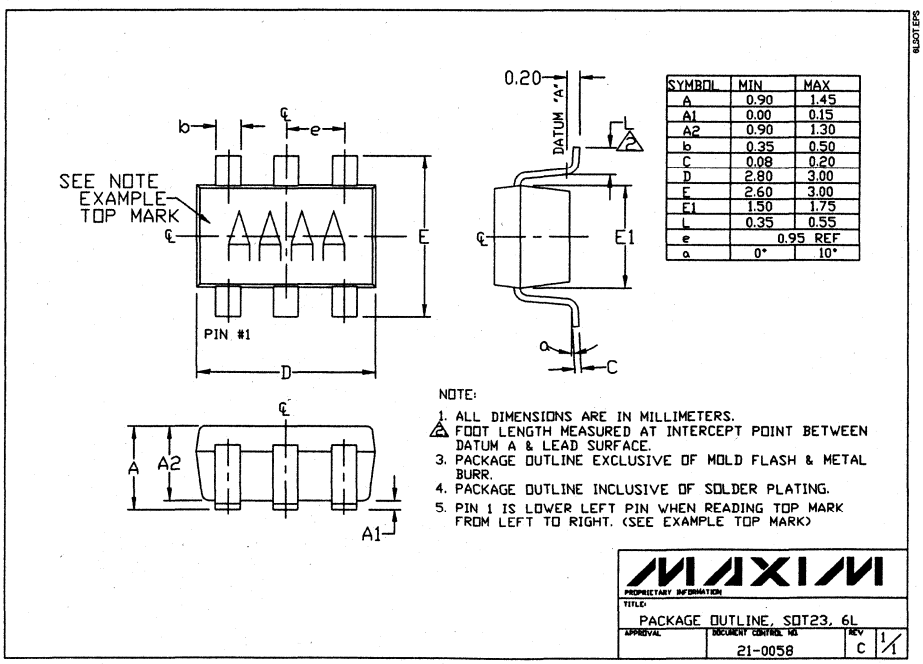


MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE,SOT-143, 4L
APPROVAL | DOCUMENT CONTROL NO. 21-0052 | REV C | 1/1

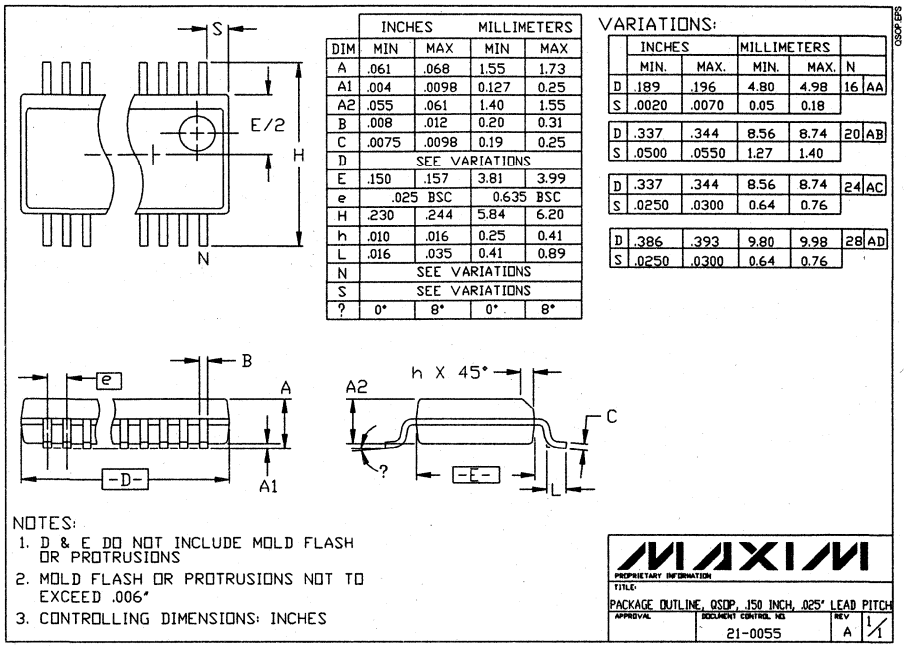
A



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
e1	1.90 REF	
α	0°	10°



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e	0.95 REF	
α	0°	10°



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.061	.068	1.55	1.73
A1	.004	.0098	0.127	0.25
A2	.055	.061	1.40	1.55
B	.008	.012	0.20	0.31
C	.0075	.0098	0.19	0.25
D	SEE VARIATIONS			
E	.150	.157	3.81	3.99
e	.025 BSC		0.635 BSC	
H	.230	.244	5.84	6.20
h	.010	.016	0.25	0.41
L	.016	.035	0.41	0.89
N	SEE VARIATIONS			
S	SEE VARIATIONS			
?	0°	8°	0°	8°

VARIATIONS:

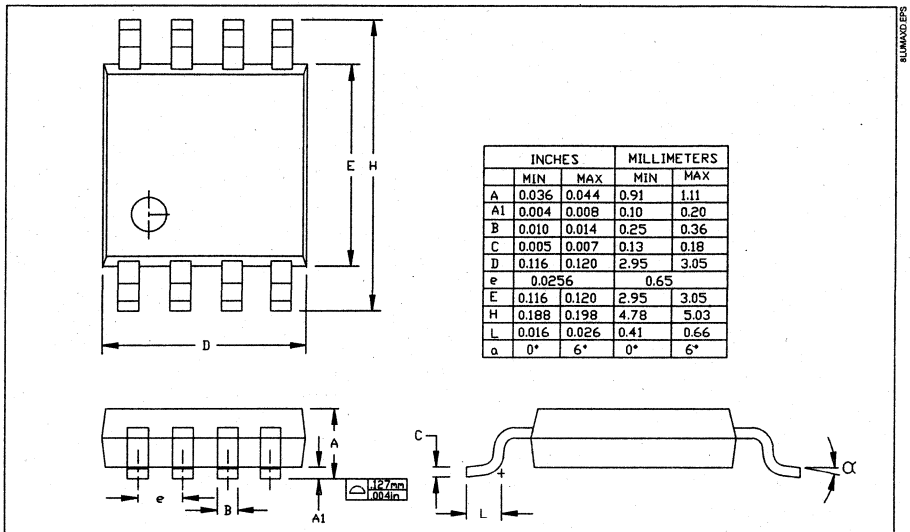
	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	N	
D	.189	.196	4.80	4.98	16	AA
S	.0020	.0070	0.05	0.18		
D	.337	.344	8.56	8.74	20	AB
S	.0500	.0550	1.27	1.40		
D	.337	.344	8.56	8.74	24	AC
S	.0250	.0300	0.64	0.76		
D	.386	.393	9.80	9.98	28	AD
S	.0250	.0300	0.64	0.76		

NOTES:
1. D & E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .006"
3. CONTROLLING DIMENSIONS: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, QSOP, .150 INCH, .025" LEAD PITCH
APPROVAL | DOCUMENT CONTROL NO. 21-0055 | REV. A | 1/1

QSOP.EPS

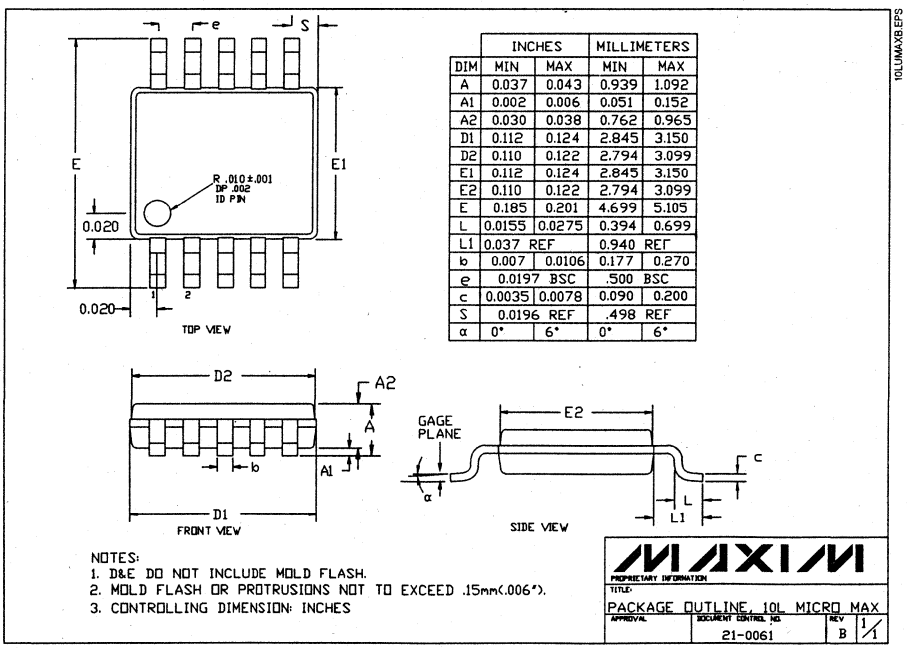
A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.036	0.044	0.91	1.11
A1	0.004	0.008	0.10	0.20
B	0.010	0.014	0.25	0.36
C	0.005	0.007	0.13	0.18
D	0.116	0.120	2.95	3.05
e	0.0256		0.65	
E	0.116	0.120	2.95	3.05
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

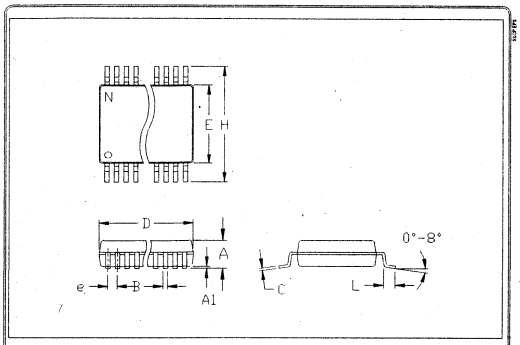
MAXIM
PROPRIETARY INFORMATION
TITLE:
8LD uMAX PACKAGE OUTLINE DWG.
APPROVAL | DOCUMENT CONTROL NO. 21-0036 | REV D | 1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.037	0.043	0.939	1.092
A1	0.002	0.006	0.051	0.152
A2	0.030	0.038	0.762	0.965
D1	0.112	0.124	2.845	3.150
D2	0.110	0.122	2.794	3.099
E1	0.112	0.124	2.845	3.150
E2	0.110	0.122	2.794	3.099
E	0.185	0.201	4.699	5.105
L	0.0155	0.0275	0.394	0.699
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		.498 REF	
α	0°	6°	0°	6°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, 10L MICRO MAX
APPROVAL | DOCUMENT CONTROL NO. 21-0061 | REV B | 1/1



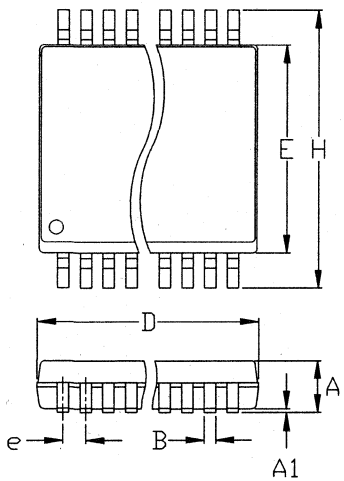
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
e	0.0256		0.65	
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.278	0.289	7.07	7.33	20
D	0.317	0.328	8.07	8.33	24
D	0.397	0.407	10.07	10.33	28

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SSOP .200" x .65mm | 1/1 | 21-0039 A

SSOP2.EPS



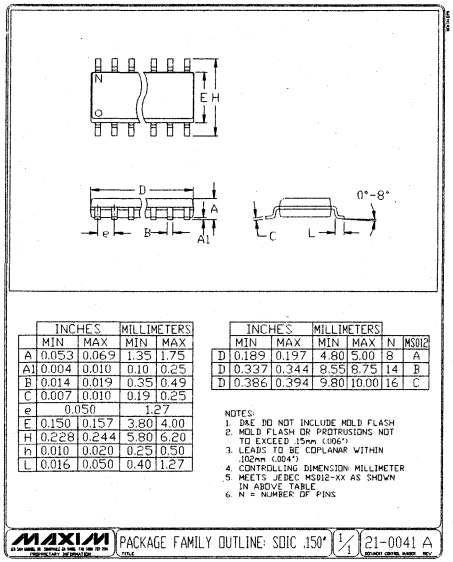
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.094	0.104	2.39	2.65
A1	0.004	0.011	0.10	0.28
B	0.011	0.017	0.30	0.44
C	0.009	0.012	0.23	0.32
e	0.0315		0.80	
E	0.292	0.298	7.42	7.57
H	0.398	0.416	10.10	10.57
L	0.020	0.035	0.51	0.89

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.604	0.610	15.34	15.49	36
D	0.702	0.708	17.83	17.98	44

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM
PROPRIETARY INFORMATION
TITLE:
PACKAGE OUTLINE, SSOP, 36/44L, .300X8mm
APPROVAL | DOCUMENT CONTROL NO. 21-0040 | REV A | 1/1

A

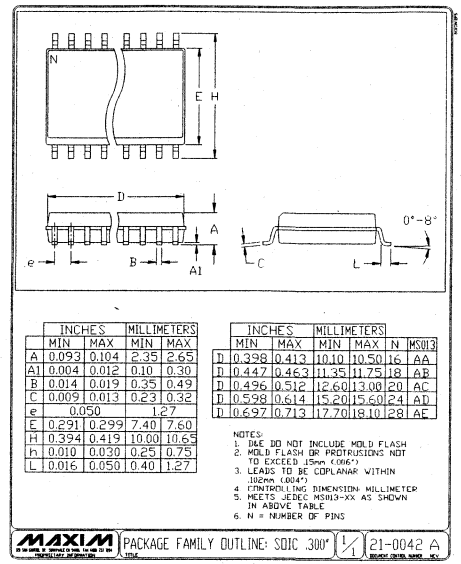


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

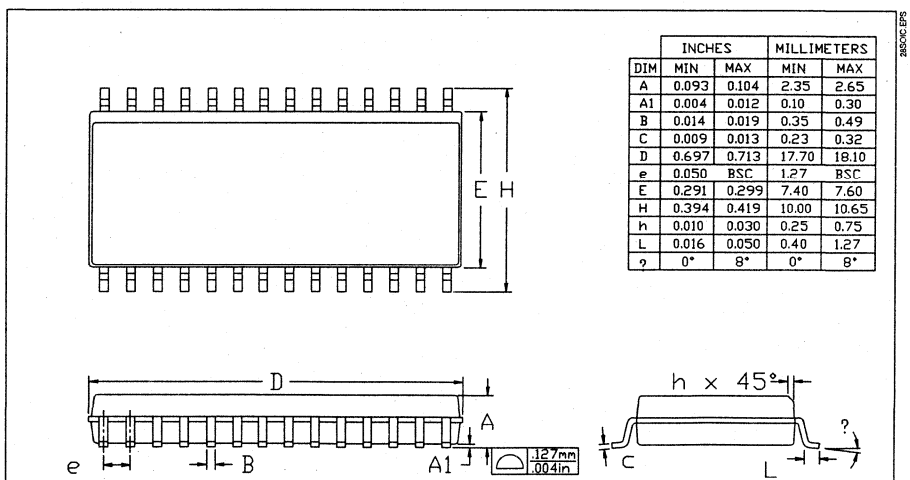


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

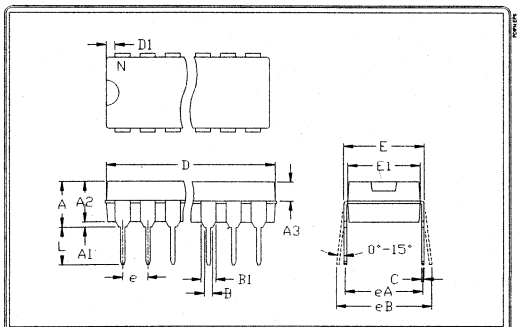
MAXIM | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
?	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AE

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 28L SOIC
APPROVAL | DWG 21-343 | REV B



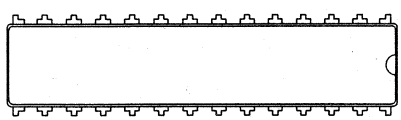
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

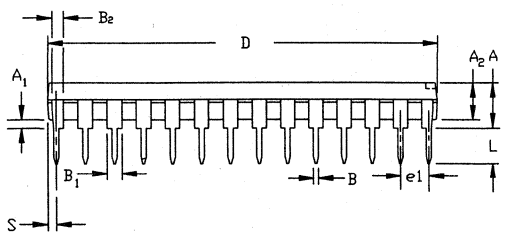
MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-095-AH.



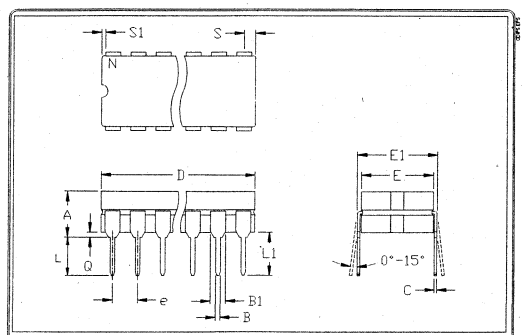
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.020	---	0.508	---
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	.100 BSC		2.540 BSC	
eA	.300 BSC		7.62 BSC	
L	0.115	0.150	2.921	3.810
α	0°	15°	0°	15°

28LNPDIP.EPS



MAXIM PROPRIETARY INFORMATION
TITLE: 28L(NAR) PDIP OUTLINE
APPROVAL | DOCUMENT CONTROL NO. 21-0400 | REV A | 1/1

A

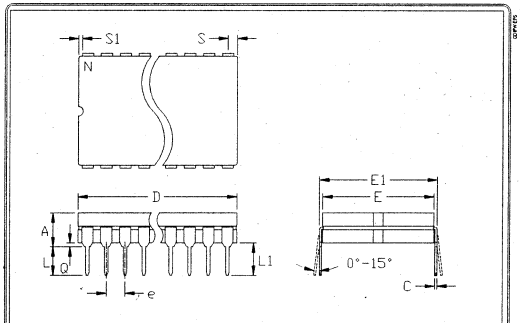


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P-D4
D	---	0.785	---	19.94	14	C-D1
D	---	0.840	---	21.34	16	E-D2
D	---	0.960	---	24.38	18	V-D6
D	---	1.060	---	26.92	20	R-D8
D	---	1.280	---	32.51	24	L-D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1935 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

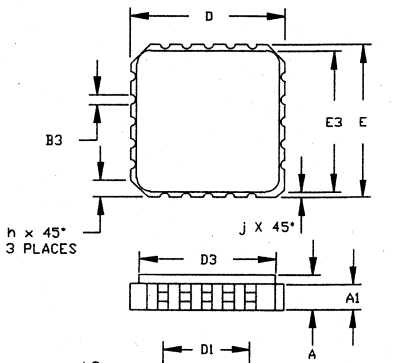


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.232	---	5.89
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.500	0.620	12.70	15.75
E1	0.590	0.630	14.99	16.00
e	0.100		2.54	
L	0.120	0.200	3.05	5.08
L1	0.150	---	3.81	---
Q	0.015	0.075	0.38	1.91
S	---	0.100	---	2.54
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	1.290	---	32.77	24	J-D3
D	---	1.490	---	37.85	28	D10
D	---	2.096	---	53.24	40	Q-D5

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1035 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .600" | 1/1 | 21-0046 A

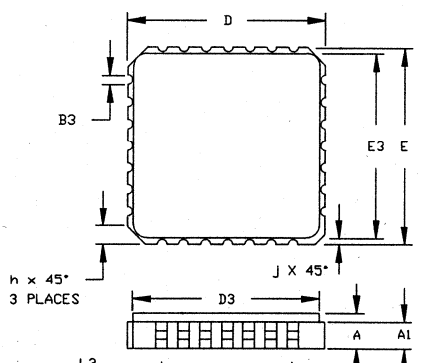


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	---	0.358	---	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 C-2

LCCPOLEPS1

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 20L LCC
APPROVAL | DWG: 21-0658 | REV: B | 1/1



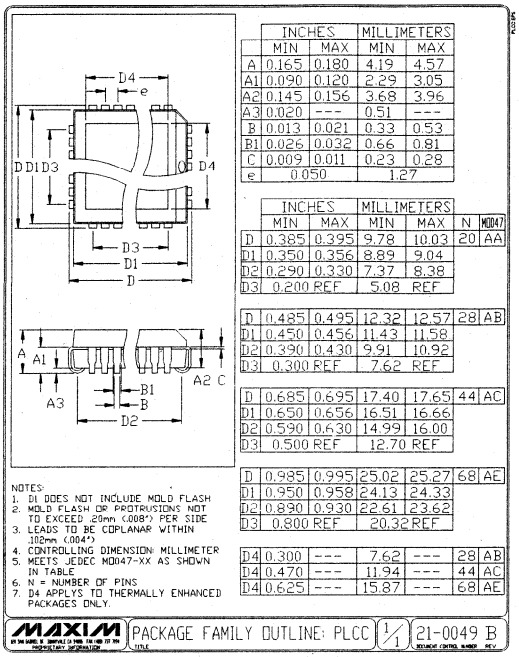
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300 BSC		7.62 BSC	
D2/E2	0.150 BSC		3.81 BSC	
D3/E3	---	0.460	---	11.68
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 C-4

LCCPOLEPS2

MAXIM
PROPRIETARY INFORMATION
TITLE: PACKAGE OUTLINE, 28L LCC
APPROVAL | DWG: 21-4497 | REV: A | 1/1

A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.145	0.156	3.68	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
e	0.050		1.27	

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MO047
D	0.385	0.395	9.78	10.03	20	AA
D1	0.350	0.356	8.89	9.04		
D2	0.290	0.330	7.37	8.38		
D3	0.200 REF		5.08 REF			

D	0.485	0.495	12.32	12.57	28	AB
D1	0.450	0.456	11.43	11.58		
D2	0.390	0.430	9.91	10.92		
D3	0.300 REF		7.62 REF			

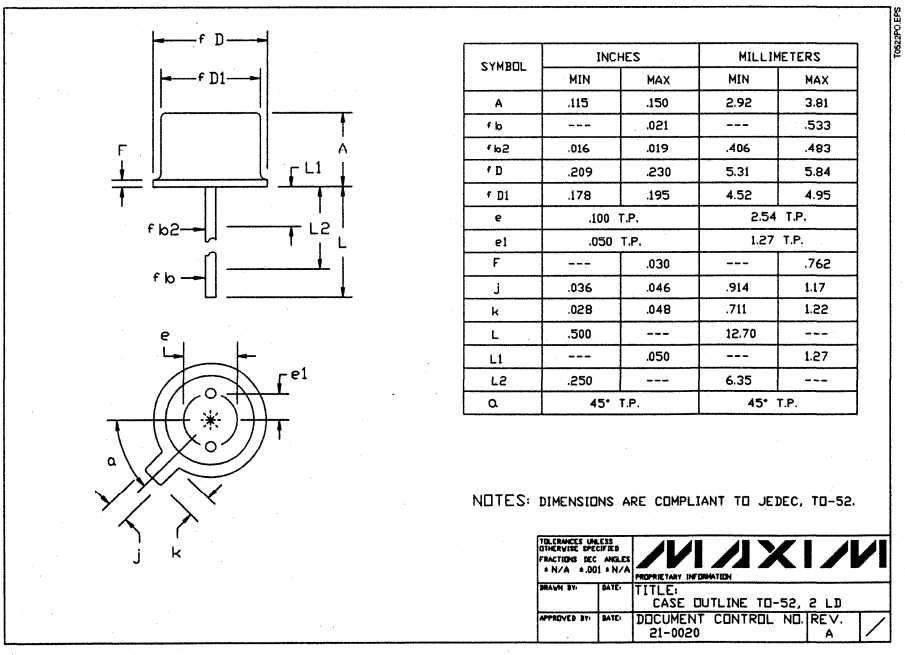
D	0.685	0.695	17.40	17.65	44	AC
D1	0.650	0.656	16.51	16.66		
D2	0.590	0.630	14.99	16.00		
D3	0.500 REF		12.70 REF			

D	0.985	0.995	25.02	25.27	68	AE
D1	0.950	0.958	24.13	24.33		
D2	0.890	0.930	22.61	23.62		
D3	0.800 REF		20.32 REF			

D4	0.300	---	7.62	---	28	AB
D4	0.470	---	11.94	---	44	AC
D4	0.625	---	15.87	---	68	AE

NOTES:
1. D1 DOES NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm (.008") PER SIDE
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MO047-XX AS SHOWN IN TABLE
6. N = NUMBER OF PINS
7. D4 APPLYS TO THERMALLY ENHANCED PACKAGES ONLY.

MAXIM	PACKAGE FAMILY OUTLINE: PLCC	1/1	21-0049 B
	TITLE	DOCUMENT CONTROL NUMBER	REV.

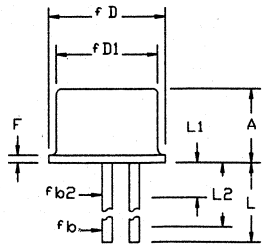


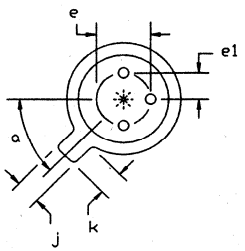
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.115	.150	2.92	3.81
f b	---	.021	---	.533
f b2	.016	.019	.406	.483
f D	.209	.230	5.31	5.84
f D1	.178	.195	4.52	4.95
e	.100 T.P.		2.54 T.P.	
e1	.050 T.P.		1.27 T.P.	
F	---	.030	---	.762
j	.036	.046	.914	1.17
k	.028	.048	.711	1.22
L	.500	---	12.70	---
L1	---	.050	---	1.27
L2	.250	---	6.35	---
Q	45° T.P.		45° T.P.	

NOTES: DIMENSIONS ARE COMPLIANT TO JEDEC, TO-52.

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ±.001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY:	DATE:	TITLE: CASE OUTLINE TO-52, 2 LD
APPROVED BY:	DATE:	DOCUMENT CONTROL NO. 21-0020 / REV. A

TM62PKO.EPS



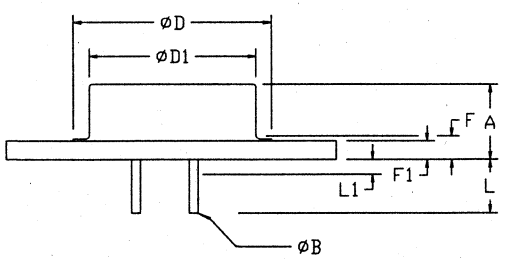


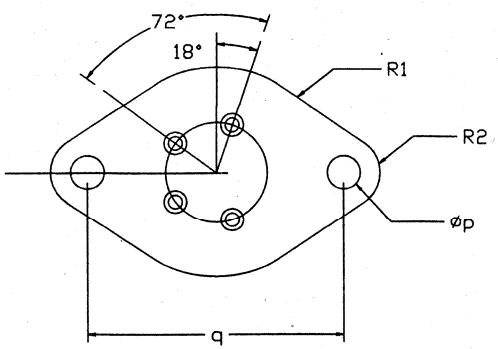
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.115	.150	2.92	3.81
ϕb	---	.021	---	.533
ϕb2	.016	.019	.406	.483
ϕD	.209	.230	5.31	5.84
ϕD1	.178	.195	4.52	4.95
e	.100 T.P.		2.54 T.P.	
e1	.050 T.P.		1.27 T.P.	
F	---	.030	---	.762
j	.036	.046	.914	1.17
k	.028	.048	.711	1.22
L	.500	---	12.70	---
L1	---	.050	---	1.27
L2	.250	---	6.35	---
α	45° T.P.		45° T.P.	

NOTES: DIMENSIONS ARE COMPLIANT TO JEDEC, TO-52.

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ±.001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY:	DATE:	TITLE: CASE OUTLINE TO-52, 3 LD
APPROVED BY:	DATE:	DOCUMENT CONTROL NO. 21-0019 / REV. A

TO3-4PO.EPS



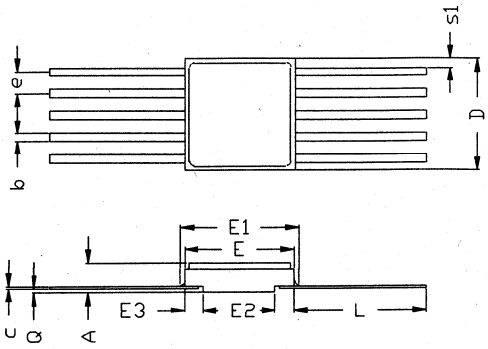


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
ϕa	.470 TP		11.94	
A	.315	.450	8.00	11.43
ϕB	.038	.041	0.96	1.04
ϕD	.850	.910	21.59	23.11
ϕD1	.765	.810	19.43	20.57
F	.067	.135	1.70	3.43
F1	.060	.100	1.52	2.54
L	.430	.470	10.9	11.94
L1	.000	.090	0.00	2.29
ϕp	.150	.160	3.81	4.06
q	1.177	1.197	29.90	30.40
R1	.445	.505	11.30	12.83
R2	.166	.188	4.22	4.78

TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC ANGLES ± N/A ±.001 ± N/A	MAXIM PROPRIETARY INFORMATION	
DRAWN BY:	DATE:	TITLE: TO-3, 4LD PKG OUTLINE
APPROVED BY:	DATE:	DOCUMENT CONTROL NO. 21-0031 / REV. A / 1/1

A

FPACKPO.EPS1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.29
b	0.010	0.022	0.25	0.56
c	0.004	0.009	0.10	0.23
D	---	0.290	---	7.11
E	0.240	0.260	6.10	6.60
E1	---	0.300	---	7.62
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	N/A	N/A	N/A	N/A
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

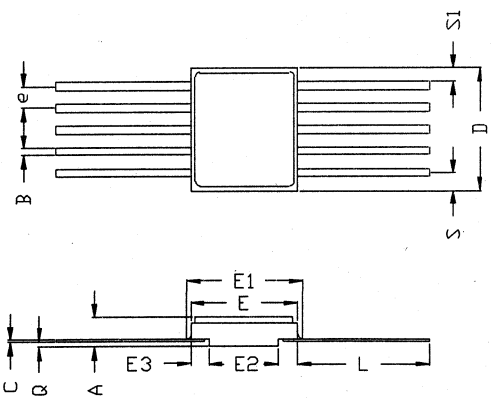
NOTES:
1. CONTROLLING DIMENSION: INCH
2. PACKAGE MEETS 1835 F4A CONFIG. B

MAXIM

10L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F10-2 | 21-0010 | C | 1/1

FPACKPO.EPS4



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.010	0.019	0.25	0.48
C	0.003	0.006	0.08	0.15
D	---	0.290	---	7.37
E	0.240	0.260	6.10	6.60
E1	---	0.280	---	7.11
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

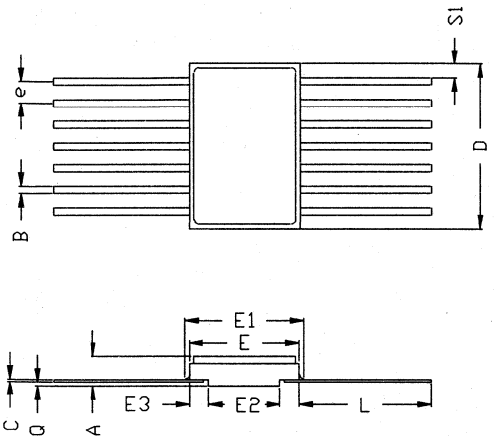
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-4A CONFIGURATION #2
   EXCEPT DIMENSION "Q" MIN

MAXIM

10L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F10-1 | 21-0014 | A | 1/1

FPACKPO.EPS/2



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

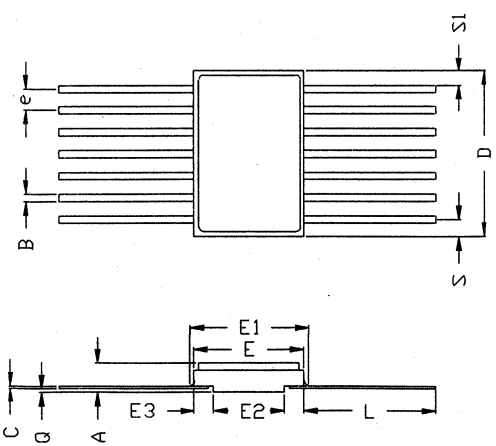
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-2A CONFIGURATION B

MAXIM

14L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F14-2 | 21-0011 | A | 1/1

FPACKPO.EPS/5



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.012	0.030	0.30	0.76
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

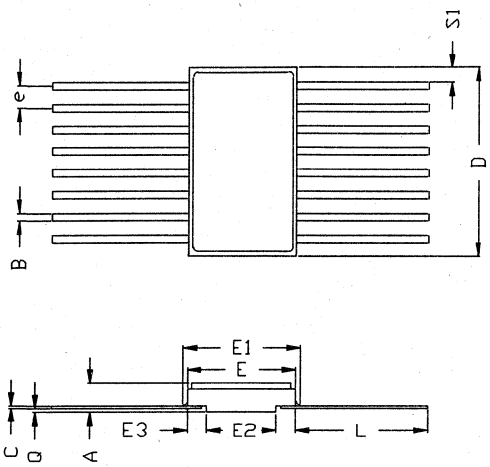
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-2A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

MAXIM

14L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F14-1 | 21-0012 | A | 1/1

A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

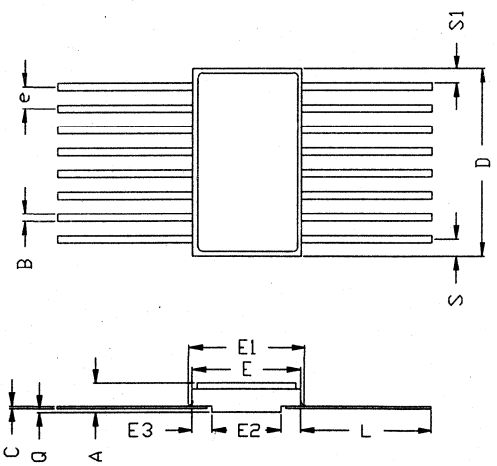
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-5A CONFIGURATION B

MAXIM

16L FLATPACK PACKAGE OUTLINE
MIL 1835 COMPLIANT

F16-2 | 21-0013 | A | 1/1

FRAGPKG EPS6



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

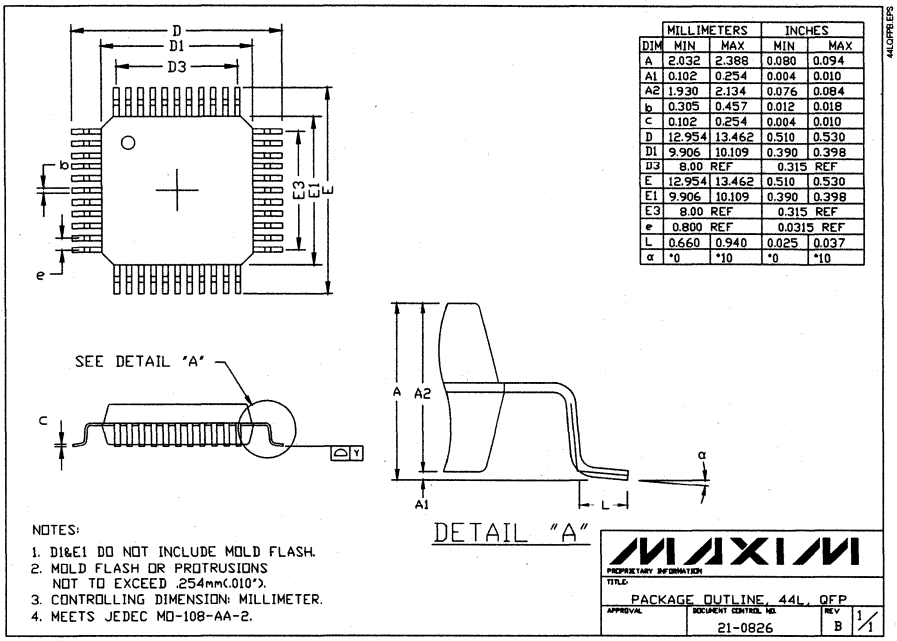
NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-5A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

MAXIM

16L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS

F16-1 | 21-828 | B | 1/1

FRAGPKG EPS6

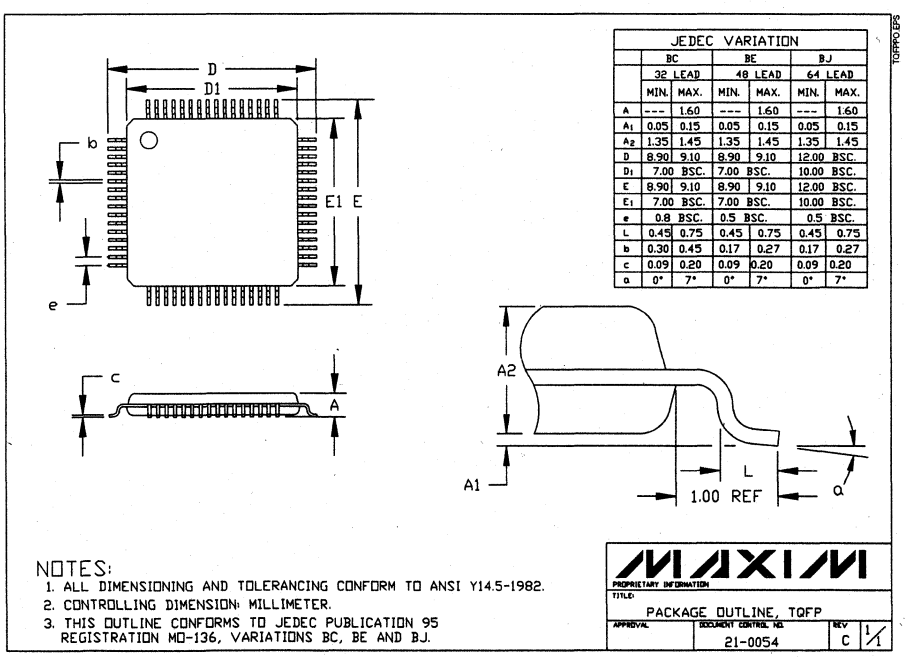


DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	2.032	2.388	0.080	0.094
A1	0.102	0.254	0.004	0.010
A2	1.930	2.134	0.076	0.084
b	0.305	0.457	0.012	0.018
c	0.102	0.254	0.004	0.010
D	12.954	13.462	0.510	0.530
D1	9.906	10.109	0.390	0.398
D3	8.00 REF		0.315 REF	
E	12.954	13.462	0.510	0.530
E1	9.906	10.109	0.390	0.398
E3	8.00 REF		0.315 REF	
e	0.800 REF		0.0315 REF	
L	0.660	0.940	0.025	0.037
α	*0	*10	*0	*10

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 44L, QFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0826	B	1/1



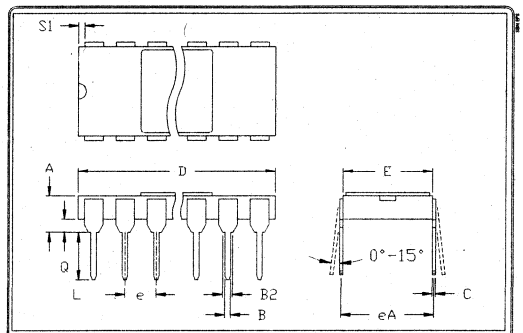
	BC 32 LEAD MIN.	BC 32 LEAD MAX.	BE 48 LEAD MIN.	BE 48 LEAD MAX.	BJ 64 LEAD MIN.	BJ 64 LEAD MAX.
A	---	1.60	---	1.60	---	1.60
A1	0.05	0.15	0.05	0.15	0.05	0.15
A2	1.35	1.45	1.35	1.45	1.35	1.45
D	8.90	9.10	8.90	9.10	12.00 BSC.	
D1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
E	8.90	9.10	8.90	9.10	12.00 BSC.	
E1	7.00 BSC.		7.00 BSC.		10.00 BSC.	
e	0.8 BSC.		0.5 BSC.		0.5 BSC.	
L	0.45	0.75	0.45	0.75	0.45	0.75
b	0.30	0.45	0.17	0.27	0.17	0.27
c	0.09	0.20	0.09	0.20	0.09	0.20
α	0°	7°	0°	7°	0°	7°

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TQFP

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0054	C	1/1

A

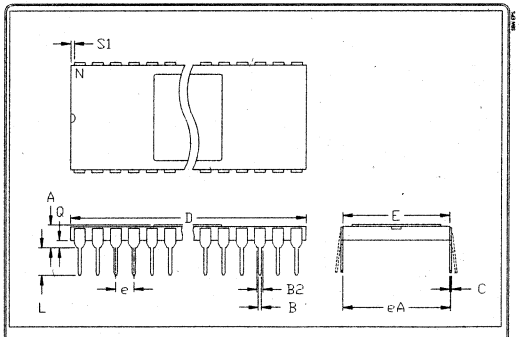


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---
S2	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.550	---	13.97	8	*3
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #3 AS SHOWN IN ABOVE TABLE
3. MEETS 1835 CASE 'P', D-4 CONFIGURATION #3 EXCEPT D AND S1 MAXIMUM DIMENSIONS
4. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SIDE BRAZE .300" | 1/1 | 21-0047 A

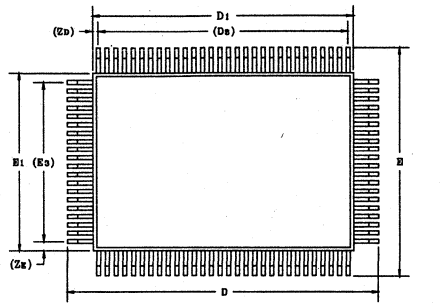


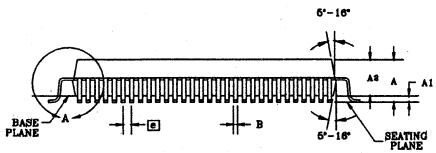
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.510	0.610	12.95	15.49
E1	0.590	0.620	14.99	15.75
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---
S2	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	1.29	---	32.77	24	J:D3
D	---	1.49	---	37.85	28	D10
D	---	2.096	---	53.24	40	Q:D5

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #3 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

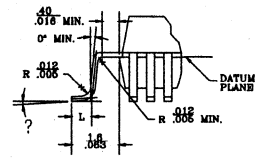
MAXIM | PACKAGE FAMILY OUTLINE: SIDE BRAZE .600" | 1/1 | 21-0048 A





	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.110	0.134	2.79	3.40
A1	0.010	---	0.25	---
A2	0.100	0.120	2.55	3.05
B	0.009	0.015	0.22	0.38
D	0.904	0.923	22.95	23.45
E	0.667	0.687	16.95	17.45
E1	0.547	0.555	13.90	14.10
E3	0.486	REF	12.35	REF
e	0.0256	BSC	0.65	BSC
D1	0.783	0.791	19.90	20.10
D3	0.742	REF	18.85	REF
L	0.026	0.037	0.65	0.95
ZD	0.023	REF	0.58	REF
ZE	0.033	REF	0.83	REF
?	0°	7°	0°	7°

DETAIL "A"



NOTES:

1. D1 & E1 DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .254mm(.010").
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC MO-108-CC-1.

MAXIM
PROPRIETARY INFORMATION

TITLE: 100L MQFP PACKAGE OUTLINE

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-7003	A	1/1

MQFP100.EPS

A